

## 8-Bit Parallel-Out Serial Shift Registers

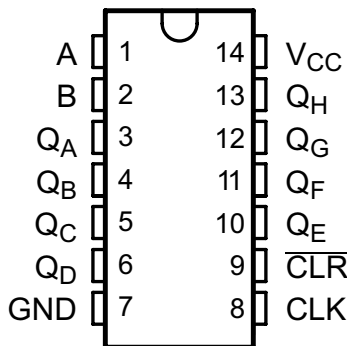
Check for Samples: [SN54HC164](#), [SN74HC164](#)

### FEATURES

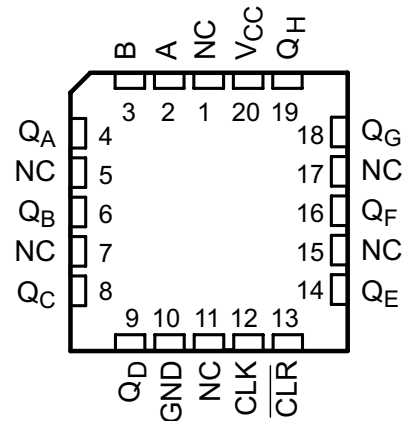
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd}$  = 20 ns
- $\pm 4$ -mA Output Drive at 5 V
- Low Input Current of 1- $\mu$ A Max
- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Direct Clear

### DESCRIPTION

These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear (CLR) input. The gated serial (A and B) inputs permit complete control over incoming data; a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock (CLK) pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs can be changed while CLK is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of CLK.



**SN54HC164...J OR W PACKAGE  
SN74HC164...D, N, NS, OR PW PACKAGE  
(TOP VIEW)**



NC – No internal connection

**SN54HC164...FK PACKAGE  
(TOP VIEW)**

**FUNCTION TABLE<sup>(1)(2)</sup>**

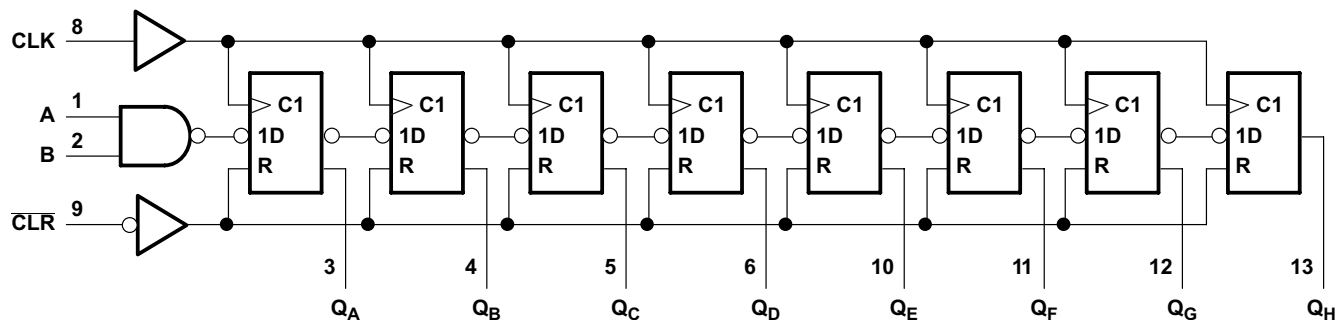
INPUTS				OUTPUTS			
CLR	CLK	A	B	QA	QB	...	QH
L	X	X	X	L	L	L	L
H	L	X	X	QA0	QB0		QH0
H	↑	H	H	H	QAn		QGn
H	↑	L	X	L	QAn		QGn
H	↑	X	L	L	QAn		QGn

- (1) QA0, QB0, QH0 = the level of QA, QB, or QH, respectively, before the indicated steady-state input conditions were established.
- (2) QAn, QGn = the level of QA or QG before the most recent ↑ transition of CLK: indicates a 1-bit shift.



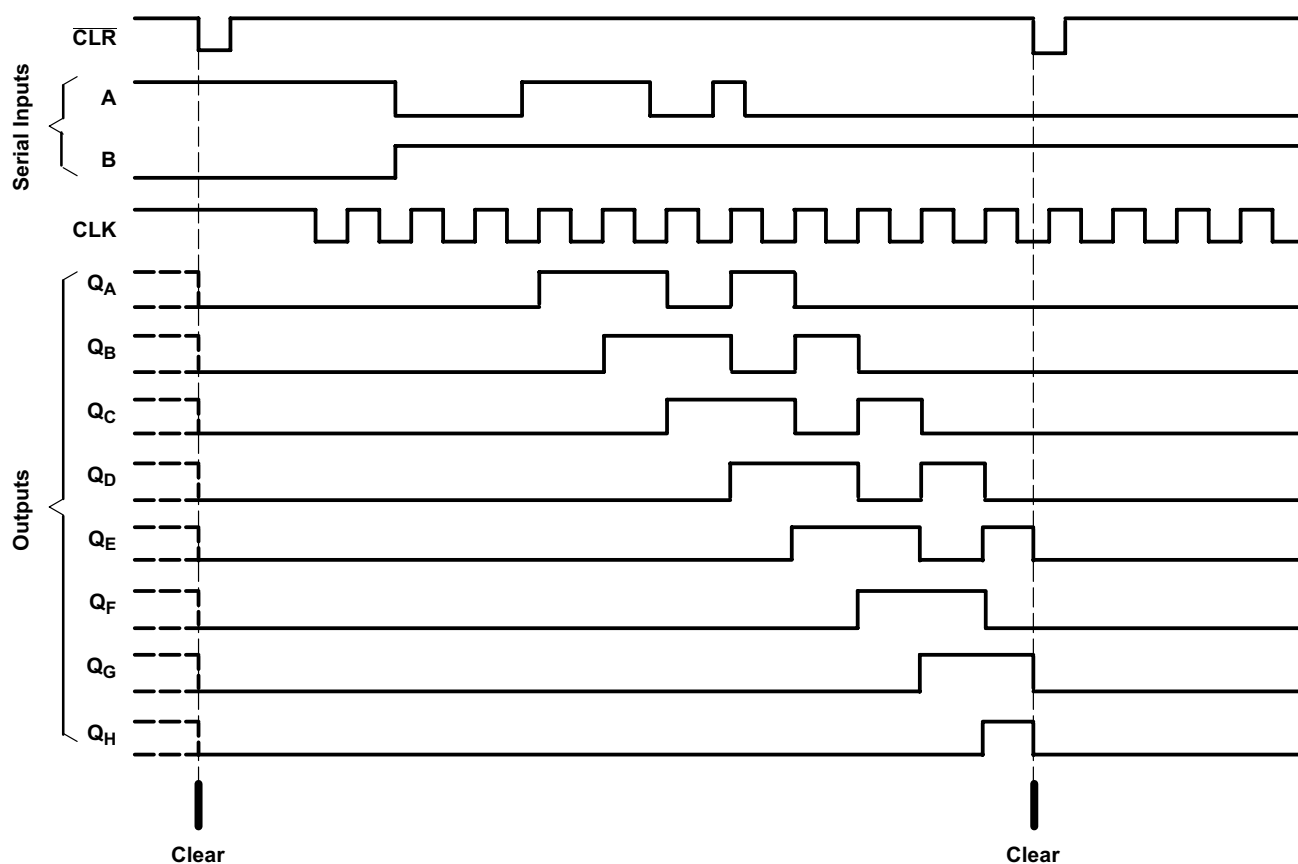
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### LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the D, J, N, NS, PW, and W packages.

### TYPICAL CLEAR, SHIFT, AND CLEAR SEQUENCE



## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNITS
$V_{CC}$	Supply voltage range		-0.5	7	V
$I_{IK}$	Input clamp current	$V_I < 0$ or $V_I > V_{CC}^{(2)}$		$\pm 20$	mA
$I_{OK}$	Output clamp current	$V_O < 0$ or $V_O > V_{CC}^{(2)}$		$\pm 20$	mA
$I_O$	Continuous output current	$V_O = 0$ to $V_{CC}$		$\pm 25$	mA
	Continuous current through $V_{CC}$ or GND			$\pm 50$	mA
$\theta_{JA}^{(3)}$	Package thermal impedance	D package		86	°C/W
		N package		80	
		NS package		76	
		PW package		113	
$T_{stg}$	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JEDEC 51-7.

## RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

		SN54HC164			SN74HC164			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	2	5	6	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5		1.5			V
		$V_{CC} = 4.5$ V	3.15		3.15			
		$V_{CC} = 6$ V	4.2		4.2			
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V		0.5			0.5	V
		$V_{CC} = 4.5$ V		1.35			1.35	
		$V_{CC} = 6$ V		1.8			1.8	
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$\Delta t/\Delta V^{(2)}$	Input transition rise/fall time	$V_{CC} = 2$ V		1000			1000	ns
		$V_{CC} = 4.5$ V		500			500	
		$V_{CC} = 6$ V		400			400	
$T_A$	Operating free-air temperature	-55		125	-40		125	°C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
- (2) If this device is used in the threshold region (from  $V_{IL\ max} = 0.5$  V to  $V_{IH\ min} = 1.5$  V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at  $t_i = 1000$  ns and  $V_{CC} = 2$  V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC164 –55°C to 125°C		SN74HC164 –55°C to 85°C		Recommended SN74HC164 –55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = –20 µA	2 V	1.9	1.998		1.9		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		5.9		
		I <sub>OH</sub> = –4 mA	4.5 V	3.98	4.3		3.7		3.84		3.7		
		I <sub>OH</sub> = –5.2 mA	6 V	5.48	5.8		5.2		5.34		5.2		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 µA	2 V		0.002	0.1		0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1		0.1	
		I <sub>OL</sub> = 4 mA	4.5 V		0.17	0.26		0.4		0.33		0.4	
		I <sub>OL</sub> = 5.2 mA	6 V		0.15	0.26		0.4		0.33		0.4	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		6 V		±0.1	±100		±1000		±1000		±1000	nA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0 I <sub>O</sub> = 0		6 V			8		160		80		160	µA
C <sub>i</sub>			2 V to 6 V		3	10		10		10		10	pF

## TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC164 –55°C to 125°C		SN74HC164 –55°C to 85°C		Recommended SN74HC164 –55°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	2 V		6		4.2		5		4.2	MHz
		4.5 V		31		21		25		21	
		6 V		36		25		28		25	
t <sub>w</sub>	Pulse duration	CL <sub>R</sub> low	2 V	100		150		125		125	ns
			4.5 V	20		30		25		25	
			6 V	17		25		21		21	
	CLK high or low		2 V	80		120		100		120	
			4.5 V	16		24		20		24	
			6 V	14		20		18		20	
t <sub>su</sub>	Setup time before CLK↑	Data	2 V	100		150		125		125	ns
			4.5 V	20		30		25		25	
			6 V	17		25		21		25	
	CL <sub>R</sub> inactive		2 V	100		150		125		125	
			4.5 V	20		30		25		25	
			6 V	17		25		21		25	
t <sub>h</sub>	Hold time, data after CLK↑		2 V	5		5		5		5	ns
			4.5 V	5		5		5		5	
			6 V	5		5		5		5	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see [Figure 1](#))

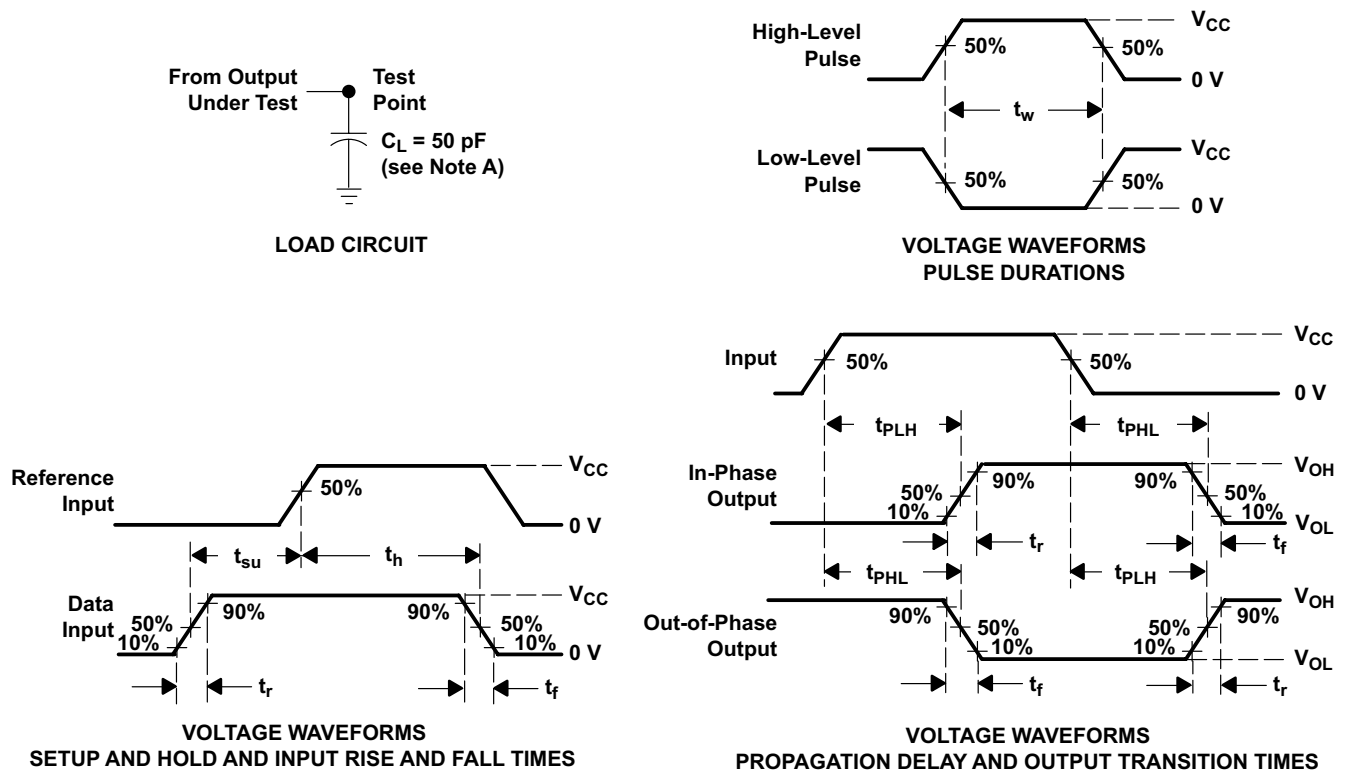
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC164 –55°C to 125°C		SN74HC164 –55°C to 85°C		Recommended SN74HC164 –55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			2 V	6	10		4.2		5		4..2		MHz
			4.5 V	31	54		21		25		21		
			6 V	36	62		25		28		25		
$t_{PHL}$	$\overline{CLR}$	Any Q	2 V		140	205		295		255		255	ns
			4.5 V		28	41		59		51		51	
			6 V		24	35		51		46		46	
$t_{pd}$	CLK	Any Q	2 V		115	175		265		220		220	
			4.5 V		23	35		53		44		44	
			6 V		20	30		45		38		38	
$t_t$			2 V		38	75		110		95		110	ns
			4.5 V		8	15		22		19		22	
			6 V		6	13		19		16		19	

## OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load	135	pF

## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
  - C. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

## REVISION HISTORY

Changes from Revision E (November 2010) to Revision F	Page
• Updated document to new TI data sheet format - no specification changes. ....	<a href="#">1</a>
• Removed ordering information. ....	<a href="#">1</a>
• Updated operating temperature range. ....	<a href="#">3</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8416201VCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8416201VC A SNV54HC164J	<a href="#">Samples</a>
5962-8416201VDA	ACTIVE	CFP	W	14	25	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8416201VD A SNV54HC164W	<a href="#">Samples</a>
84162012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84162012A SNJ54HC 164FK	<a href="#">Samples</a>
8416201CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8416201CA SNJ54HC164J	<a href="#">Samples</a>
SN54HC164J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54HC164J	<a href="#">Samples</a>
SN74HC164D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC164	<a href="#">Samples</a>
SN74HC164DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC164	<a href="#">Samples</a>
SN74HC164DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC164	<a href="#">Samples</a>
SN74HC164DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 125	HC164	<a href="#">Samples</a>
SN74HC164DRE4	ACTIVE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>
SN74HC164DRG3	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	HC164	<a href="#">Samples</a>
SN74HC164DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC164	<a href="#">Samples</a>
SN74HC164DT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC164	<a href="#">Samples</a>
SN74HC164DTE4	ACTIVE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>
SN74HC164DTG4	ACTIVE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>
SN74HC164N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU   CU SN	N / A for Pkg Type	-40 to 125	SN74HC164N	<a href="#">Samples</a>
SN74HC164N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	-40 to 125		



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC164NE3	PREVIEW	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SN74HC164N	
SN74HC164NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	SN74HC164N	<a href="#">Samples</a>
SN74HC164NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC164	<a href="#">Samples</a>
SN74HC164NSRE4	ACTIVE	SO	NS	14		TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>
SN74HC164NSRG4	ACTIVE	SO	NS	14		TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>
SN74HC164PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC164	<a href="#">Samples</a>
SN74HC164PWE4	ACTIVE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>
SN74HC164PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC164	<a href="#">Samples</a>
SN74HC164PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC164	<a href="#">Samples</a>
SN74HC164PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC164	<a href="#">Samples</a>
SN74HC164PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC164	<a href="#">Samples</a>
SN74HC164PWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC164	<a href="#">Samples</a>
SN74HC164PWTE4	ACTIVE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>
SN74HC164PWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC164	<a href="#">Samples</a>
SNJ54HC164FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84162012A SNJ54HC 164FK	<a href="#">Samples</a>
SNJ54HC164J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8416201CA SNJ54HC164J	<a href="#">Samples</a>
SNJ54HC164W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8416201DA SNJ54HC164W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54HC164, SN54HC164-SP, SN74HC164 :**

● Catalog: [SN74HC164](#), [SN54HC164](#)

● Military: [SN54HC164](#)

● Space: [SN54HC164-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC164DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC164DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC164DR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.3	8.0	16.0	Q1
SN74HC164DRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.3	8.0	16.0	Q1
SN74HC164DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC164DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC164DT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC164NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC164PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC164PWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC164DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74HC164DR	SOIC	D	14	2500	333.2	345.9	28.6
SN74HC164DR	SOIC	D	14	2500	364.0	364.0	27.0
SN74HC164DRG3	SOIC	D	14	2500	364.0	364.0	27.0
SN74HC164DRG4	SOIC	D	14	2500	333.2	345.9	28.6
SN74HC164DRG4	SOIC	D	14	2500	367.0	367.0	38.0
SN74HC164DT	SOIC	D	14	250	367.0	367.0	38.0
SN74HC164NSR	SO	NS	14	2000	367.0	367.0	38.0
SN74HC164PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74HC164PWT	TSSOP	PW	14	250	367.0	367.0	35.0

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004



N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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QQ        800077892  
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➤ Customer Service :

Email     service@ameya360.com

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