TPD12S016 HDMI Companion Chip with I²C Level Shifting Buffer, 12 Channel ESD Protection, and Current-Limit Load Switch

1 Features

- Conforms to HDMI Compliance Tests without any External Components
- IEC 61000-4-2 ESD Protection
  - ±8-kV Contact Discharge
- Supports HDMI 1.4 Data Rate
- Matches Class D and Class C Pin Mapping
- 8-Channel ESD Protection for Four Differential Pairs with Ultra-low Differential Capacitance Matching (0.05 pF)
- On-chip Load Switch with 55-mA Current Limit at the HDMI 5V_OUT Pin
- Auto-direction Sensing I²C Level Shifter with One-shot Circuit to Drive a Long HDMI Cable (750 pF Load)
- Back-drive Protection on HDMI Connector Side Ports
- Integrated Pull-up and Pull-down Resistors per HDMI Specification
- Space Saving 24-pin RKT Package and 24-TSSOP Package

2 Applications

- Cell Phones
- eBook
- Portable Media Players
- Set-top Box

3 Description

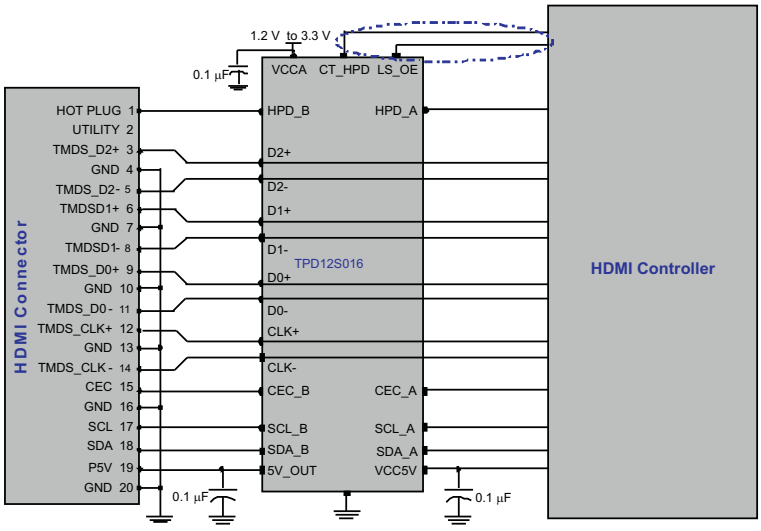
The TPD12S016 is a single-chip High Definition Multimedia Interface (HDMI) device with auto-direction sensing I²C voltage level shift buffers, a load switch, and integrated low capacitance high-speed electrostatic discharge (ESD) transient voltage suppression (TVS) protection diodes. A 55-mA current limited 5-V output (5V_OUT) sources the HDMI power line. The control of 5V_OUT and the hot plug detect (HPD) circuitry is independent of the LS_OE control signal, and is controlled by the CT_HPD pin, which enables the detection scheme (5V_OUT and HPD) to be active before enabling the HDMI link. The SDA, SCL, and CEC lines pull up to V_{CCA} on the A side. On the B side, the CEC_B pin pulls up to an internal 3.3 V supply rail, SCL_B and SDA_B each pull up to the 5-V rail (5V_OUT). The SCL and SDA pins meet the I²C specification and drive up to 750 pF capacitive loads, exceeding the HDMI 1.4 specifications. The HPD_B port has a glitch filter to avoid false detection due to plug bouncing during the HDMI connector insertion. TPD12S016 offers reverse current blocking at the 5V_OUT pin. SCL_B, SDA_B, CEC_B pins also feature reverse-current blocking when the system is powered off.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD12S016	QFN (24)	4.00 mm × 2.00 mm
	TSSOP (24)	7.80 mm × 6.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



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5 Revision History

Changes from Revision D (August 2013) to Revision E — **Page**

- Added Handling Rating table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ... 1

Changes from Original (January 2013) to Revision A — **Page**

- Added Eye Diagram Using EVM Without TPD12S016 for the TMDS Lines at 1080p, 340MHz Pixel Clock, 3.4Gbps ... 18
- Added Eye Diagram Using EVM with TPD12S016 for the TMDS Lines at 1080p, 340MHz Pixel Clock, 3.4Gbps ... 18

Changes from Revision A (February 2013) to Revision B — **Page**

- Added PW and RKT packages values for IO capacitance. ... 6
- Added LOAD SWITCH $I_{LEAKAGE\_REVERSE}$ vs V_{5V_OUT} graph. ... 11
- Updated Circuit Schematic Diagram. ... 13

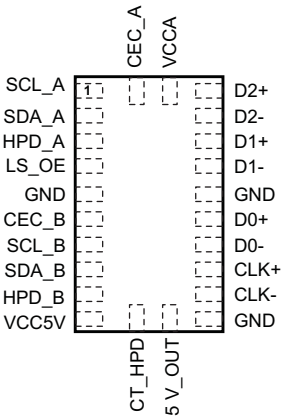
Changes from Revision B (February 2013) to Revision C — **Page**

- Updated table formatting. ... 6

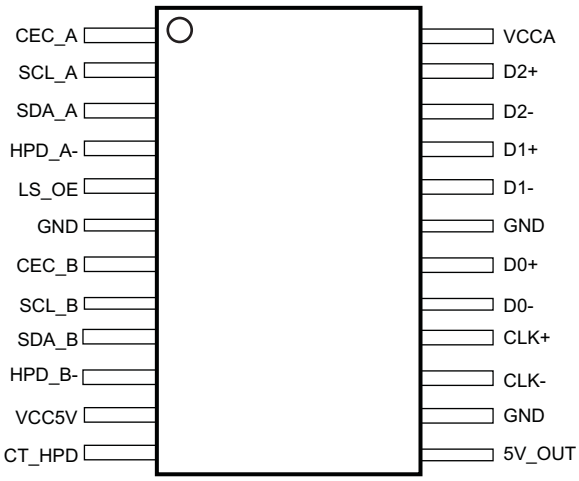
Changes from Revision C (August 2013) to Revision D — **Page**

- Updated power savings options table ... 16

6 Pin Configuration and Functions



24-RKT Package (Top View)
(4.0mm x 2.0mm x 0.5mm)



24-PW Package (Top View)
(7.8mm x 6.1mm x 1.2mm)

Pin Functions

NAME	PIN NO.		TYPE	DESCRIPTION
	RKT	PW		
D-, D+	16, 17, 19-22	17, 18, 20-23	IO	HDMI TMDS Data. Connect to HDMI Controller and HDMI Connector directly
CLK+, CLK-	14, 15	15, 16	IO	HDMI TMDS Clock. Connect to HDMI Controller and HDMI Connector directly
HPD_A	3	4	O	Hot plug detect Output referenced to V_{CCA}. Connect to HDMI controller Hot plug detect input pin
HPD_B	9	10	I	Hot plug detect Input. Connect directly to HDMI Connector Hot Plug Detect pin
CEC_A	24	1	IO	HDMI controller side CEC signal pin referenced to V_{CCA}. Connect to HDMI controller
CEC_B	6	7	IO	HDMI connector side CEC signal pin referenced to internal 3.3V supply. Connect to HDMI connector CEC pin
SCL_A	1	2	IO	HDMI controller side SCL signal pin referenced to V_{CCA}. Connect to HDMI controller
SCL_B	7	8	IO	HDMI connector side SCL signal pin referenced to 5V_OUT supply. Connect to HDMI connector SCL pin
SDA_A	2	3	IO	HDMI controller side SDA signal pin referenced to V_{CCA}. Connect to HDMI controller
SDA_B	8	9	IO	HDMI connector side SDA signal pin referenced to 5V_OUT supply. Connect to HDMI connector SDA pin
LS_OE	4	5	I	Disables the Level shifters when OE =L. The OE pin is referenced to V_{CCA}
CT_HPD	11	12	I	Disables the load switch and HPD_B when CT_HPD =L. The CT_HPD is referenced to V_{CCA}
V_{CC5V}	10	11	PWR	Internal 5V Supply (Input to the load siwtch)
V_{CCA}	23	24	PWR	Internal PCB Low Voltage Supply (Same as the HDMI Controller Chip Supply)
5V_OUT	12	13	O	External 5V Supply (Output of the load switch)
GND	5, 13, 18	6, 14, 19	GND	Connect to System Ground Plane

7 Specifications

7.1 Absolute Maximum Ratings[1][2]

over operating free-air temperature range (unless otherwise noted)

			VALUE		UNIT
			MIN	MAX	
V_{CCA}	Supply voltage range		–0.3	4.0	V
V_{CC5V}	Supply voltage range		–0.3	6.0	V
V_I	Input voltage range[2]	SCL_A, SDA_A, CEC_A	–0.3	4.0	V
		SCL_B, SDA_B, CEC_B	–0.3	6.0	
		CT_HPD, LS_OE	–0.3	4.0	
		D, CLK	–0.3	6.0	
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]	SCL_A, SDA_A, CEC_A, CT_HPD, LS_OE	–0.3	4.0	V
		SCL_B, SDA_B, CEC_B	–0.3	6.0	
V_O	Voltage range applied to any output in the high or low state[2][3]	SCL_A, SDA_A, CEC_A, CT_HPD, LS_OE	–0.3	V_{CCA} + 0.5	V
		SCL_B, SDA_B, CEC_B	–0.3	5V_OUT + 0.5	
I_{IK}	Input clamp current	VI < 0		–50	mA
I_{OK}	Output clamp current	VO < 0		–50	mA
	Continuous current through 5V_OUT, or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	LS_OE, CT_HPD, SCL_A, SDA_A, CEC_A, HPD_A, V_{CCA}	±2000	V
			Dx, CLKx, SCL_B, SDA_B, CEC_B, HPD_B , 5V_OUT	±15000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101		±1000	
		IEC 61000-4-2 Contact Discharge	Dx, CLKx, SCL_B, SDA_B, CEC_B, HPD_B , 5V_OUT	±8000	V

7.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)

				MIN	TYP	MAX	UNIT
V_{CCA}	Supply voltage			1.1		3.6	V
V_{CC5V}	Supply voltage			4.5		5.5	V
V_{IH}	High-level input voltage	SCL_A, SDA_A	V_{CCA} =1.1 V to 3.6 V	0.7 × V_{CCA}		V_{CCA}	V
		CEC_A	V_{CCA} =1.1 V to 3.6 V	0.7 × V_{CCA}		V_{CCA}	V
		CT__HPD, LS_OE	V_{CCA} =1.1 V to 3.6 V	1.0		V_{CCA}	V
		SCL_B, SDA_B	5V_OUT = 5.0 V	0.7 × 5V_OUT		5V_OUT	V
		CEC_B	5V_OUT = 5.0 V	0.7 × V_{3P3} (1)		V_{3P3}	
		HPD_B	5V_OUT = 5.0 V	2.0		5V_OUT	
V_{IL}	Low-level input voltage	SCL_A, SDA_A	V_{CCA} =1.1 V to 3.6 V	–0.5		0.082 × V_{CCA}	V
		CEC_A	V_{CCA} =1.1 V to 3.6 V	–0.5		0.082 × V_{CCA}	V
		CT_HPD, LS_OE	V_{CCA} =1.1 V to 3.6 V	–0.5		0.4	V
		SCL_B, SDA_B	5V_OUT = 5.0 V	–0.5		0.3 × 5V_OUT	V
		CEC_B	5V_OUT = 5.0 V	–0.5		0.3 × V_{3P3}	V
		HPD_B	5V_OUT = 5.0 V	0		0.8	V
V_{ILC}	(contention) Low-level input voltage	SCL_A, SDA_A, CEC_A	V_{CCA} =1.1 V to 3.6 V	–0.5		0.065 × V_{CCA}	V
V_{OL} - V_{ILC}	Delta between V_{OL} and V_{ILC}	SCL_A, SDA_A, CEC_A	V_{CCA} =1.1 V to 3.6 V	0.1 × V_{CCA}			mV
T_A	Operating free-air temperature			–40		85	°C

(1) The V_{3P3} is an internal 3.3V power supply node. The V_{3P3} is generated from the 5V supply pin through the on-chip LDO.

7.4 Thermal Information

THERMAL METRIC (1)		TPD12S016		UNIT
		RKT	PW	
		24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	77.9	88.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.0	26.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	29.3	43.5	
ψ_{JT}	Junction-to-top characterization parameter	0.5	1.1	
ψ_{JB}	Junction-to-board characterization parameter	29.3	43.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP	MAX	UNIT
HIGH SPEED ESD LINES: D_X, CLK_X									
I_{IO}	Current through ESD clamp ports		V_{CCA} = 3.3 V, V_{CC5V} = 5.0 V, V_{IO} = 3.3 V	D, CLK			0.01	0.5	µA
V_{DL}	Diode forward voltage		I_D = 8 mA	Lower clamp diode			0.8	1.0	V
R_{DYN}	Dynamic Resistance		I = 1 A	D, CLK			1		Ω
C_{IO}	IO capacitance	PW Package	V_{CC} = 5 V, V_{IO} = 2.5 V	D, CLK			1.0		pF
		RKT Package					1.2		
ΔC_{IO_TMDS}	Differential capacitance for the Dx+, Dx– lines		V_{CC} = 5 V, V_{IO} = 2.5 V	D, CLK			0.05		pF
V_{BR}	Break-down Voltage		I_{IO} = 1 mA			6.5		9	V
LOAD SWITCH V_{CC5V}, 5V_OUT									
I_{CC5V}	Supply current at V_{CC5V}		V_{CC5V} = 5 V, 5V OUT =Open, LS_OE = GND, CT_HPD = GND				1	45	µA
	Supply current at V_{CC5V}		V_{CC5V} = 5 V, 5V OUT =Open, LS_OE = GND, CT_HPD = 3.3 V				4	50	µA
I_{SC}	Short circuit current at 5V_OUT		V_{CC5V} = 5 V, 5V_OUT = GND			100	150	200	mA
V_{DROP}	5V_OUT output voltage drop		V_{CC5V} = 5 V, I_{5V_OUT} = 55 mA				35	50	mV
T_{ON}	Turn on Time, V_{CC5V} to 5V_OUT		C_{LOAD} = 0.1 µF, R_{LOAD} = 500 Ω				77		µs
T_{OFF}	Turn off Time, V_{CC5V} to 5V_OUT		C_{LOAD} = 0.1 µF, R_{LOAD} = 500 Ω				7.0		µs
T_{SHUT}	Thermal Shutdown		Shutdown threshold, TRIP(1)				140		°C
			HYST(2)				12		
VOLTAGE LEVEL SHIFTER – SCL, SDA LINES (x_A AND x_B PORTS)									
V_{OHA}			I_{OH} = –20 µA	$V_I = V_{IH}$	V_{CCA} = 1.1 V to 3.6 V	V_{CCA} × 0.80			V
V_{OLA}			I_{OL} = 20 µA	$V_I = V_{IL}$	V_{CCA} = 1.1 V to 3.6 V		V_{CCA} × 0.17		V
V_{OHB}			I_{OH} = –20 µA	$V_I = V_{IH}$		5VOUT × 0.90			V
V_{OLB}			I_{OL} = 3 mA	$V_I = V_{IL}$				0.4	V
ΔV_T	Hysteresis at the SDx_A ($V_{T+} – V_{T–}$)		V_{CCA} = 1.1 V to 3.6 V				40		mV
ΔV_T	Hysteresis at the SDx_B ($V_{T+} – V_{T–}$)		V_{CCA} = 1.1 V to 3.6 V				400		mV
R_{PU}	(Internal pull-up)		SCL_A, SDA_A	Pull-up connected to V_{CCA} rail			10		kΩ
			SCL_B, SDA_B	Pull-up connected to 5-V rail			1.75		
$I_{PULLUPAC}$	Transient boosted pull-up current (rise-time accelerator)		SCL_B, SDA_B	Pull-up connected to 5-V rail			15		mA
I_{off}	A port		V_{CCA} = 0 V, V_I or V_O = 0 to 3.6 V		V_{CCA} = 0 V			±5	µA
	B port		5VOUT = 0 V, V_I or V_O = 0 to 5.5 V		V_{CCA} = 0 V to 3.6 V			±5	
I_{OZ}	B port		$V_O = V_{CCO}$ or GND		V_{CCA} = 1.1 V to 3.6 V			±5	µA
	A port		$V_I = V_{CCI}$ or GND		V_{CCA} = 1.1 V to 3.6 V			±5	

(1) The TPD12S016 turns off after the device temperature reaches the TRIP temperature.
(2) Once the thermal shut-down circuit turns off the load switch, the switch turns on again after the device junction temperature cools down to a temperature equals to or less than TRIP-HYST.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
VOLTAGE LEVEL SHIFTER – CEC LINE (x_A AND x_B PORTS)								
V_{OHA}		I_{OH} = –20 µA	$V_I = V_{IH}$	V_{CCA} = 1.1 V to 3.6 V	V_{CCA} × 0.80			V
V_{OLA}		I_{OL} = 20 µA	$V_I = V_{IL}$	V_{CCA} = 1.1 V to 3.6 V		V_{CCA} × 0.17		V
V_{OHB}		I_{OH} = –20 µA	$V_I = V_{IH}$		V_{3P3} × 0.80			V
V_{OLB}		I_{OL} = 3 mA	$V_I = V_{IL}$				0.4	V
ΔV_T	Hysteresis at the Sxx_A ($V_{T+} – V_{T–}$)	V_{CCA} = 1.1 V to 3.6 V				40		mV
ΔV_T	Hysteresis at the Sxx_B ($V_{T+} – V_{T–}$)	V_{CCA} = 1.1 V to 3.6 V				300		mV
R_{PU}	(Internal pull-up)	CEC_A	Pull-up connected to V_{CCA} rail			10		kΩ
		CEC_B	Pull-up connected to 3.3 V rail		22	26	30	
I_{off}	A port	V_{CCA} = 0 V, V_I or V_O = 0 to 3.6 V		V_{CCA} = 0 V			±5	µA
	B port	5VOUT = 0 V, V_I or V_O = 0 to 5.5 V		V_{CCA} = 0 V to 3.6 V			±1.8	
I_{OZ}	B port	$V_O = V_{CCO}$ or GND		V_{CCA} = 1.1 V to 3.6 V			±5	µA
	A port	$V_I = V_{CCI}$ or GND		V_{CCA} = 1.1 V to 3.6 V			±5	
VOLTAGE LEVEL SHIFTER – HPD LINE (x_A AND x_B PORTS)								
V_{OHA}		I_{OH} = –3 mA	$V_I = V_{IH}$	V_{CCA} = 1.1 V to 3.6 V	V_{CCA} ×0.07			V
V_{OLA}		I_{OL} = 3 mA	$V_I = V_{IL}$	V_{CCA} = 1.1 V to 3.6 V			0.4	V
ΔV_T	Hysteresis ($V_{T+} – V_{T–}$)	V_{CCA} = 1.1 V to 3.6 V				400		mV
R_{PD}	(Internal pull-down resistor)	HPD_B	Pull-down connected to GND			11		kΩ
I_{off}	A port	$V_O = V_{CCO}$ or GND	V_{CCA} = 0 V				±5	µA
I_{OZ}	A port	$V_I = V_{CCO}$ or GND	V_{CCA} = 3.6 V				±5	µA
LS_OE, CT_CP_HPD								
I_I		$V_I = V_{CCA}$ or GND	V_{CCA} = 1.1 V to 3.6 V				±12	µA
I/O CAPACITANCES								
C_I	Control inputs	V_I = 1.89 V or GND	V_{CCA} = 1.1 V to 3.6 V			7.1		pF
C_{io}	A port	V_O = 1.89 V or GND	V_{CCA} = 1.1 V to 3.6 V			8.3		pF
	B port	V_O = 5.0 V or GND	V_{5VOUT} = 5.0 V			15		pF

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_L	Bus Load Capacitance (B Side)					750	pF
	Bus Load Capacitance (A Side)					15	
VOLTAGE LEVEL SHIFTER – SCL, SDA LINES (x_A And x_B PORTS) V_{CCA} = 1.2 V							
t_{PHL}	Propagation delay	A to B	SCL/SDA Channels Enabled		310		nS
		B to A			420		
t_{PLH}	Propagation delay	A to B			510		nS
		B to A			427		
t_{FALL}	A Port fall time	A-Port			334		nS
	B Port fall time	B-Port			225		
t_{RISE}	A Port rise time	A-Port			315		nS
	B Port rise time	B-Port			415		
$F_{(MAX)}$	Maximum switching frequency			400			kHz
VOLTAGE LEVEL SHIFTER – CEC LINES (x_A AND x_B PORTS) V_{CCA} = 1.2 V							
t_{PHL}	Propagation delay	A to B	CEC Channel Enabled		385		nS
		B to A			526		
t_{PLH}	Propagation delay	A to B			13.8		µS
		B to A			16.6		nS
t_{FALL}	A Port fall time	A-Port			334		nS
	B Port fall time	B-Port			170		
t_{RISE}	A Port rise time	A-Port			315		nS
	B Port rise time	B-Port			28		µS
VOLTAGE LEVEL SHIFTER – HPD LINES (x_A AND x_B PORTS) V_{CCA} = 1.2 V							
t_{PHL}	Propagation delay	B to A	HPD Channel Enabled		14.4		µS
t_{PLH}	Propagation delay	B to A			9.2		µS
t_{FALL}	A Port fall time	A-Port			2.1		nS
t_{RISE}	A Port rise time	A-Port			2.1		nS
VOLTAGE LEVEL SHIFTER – SCL, SDA LINES (x_A AND x_B PORTS) V_{CCA} = 1.5 V							
t_{PHL}	Propagation delay	A to B	SCL/SDA Channels Enabled		310		nS
		B to A			420		nS
t_{PLH}	Propagation delay	A to B			410		nS
		B to A			425		nS
t_{FALL}	A Port fall time	A-Port			250		nS
	B Port fall time	B-Port			225		nS
t_{RISE}	A Port rise time	A-Port			315		nS
	B Port fall time	B-Port			415		nS
$F_{(MAX)}$	Maximum switching frequency			400			kHz
VOLTAGE LEVEL SHIFTER – CEC LINES (x_A AND x_B PORTS) V_{CCA} = 1.5 V							
t_{PHL}	Propagation delay	A to B	CEC Channel Enabled		380		nS
		B to A			420		
t_{PLH}	Propagation delay	A to B			13.8		µS
		B to A			16.6		nS
t_{FALL}	A Port fall time	A-Port			250		nS
	B Port fall time	B-Port			170		
t_{RISE}	A Port rise time	A-Port			315		nS
	B Port rise time	B-Port			28		µS

Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE LEVEL SHIFTER – HPD LINES (x_A AND x_B PORTS) V_{CCA} = 1.5 V							
t_{PHL}	Propagation delay	B to A	HPD Channel Enabled		14.4		µS
t_{PLH}	Propagation delay	B to A			9.2		µS
t_{FALL}	A Port fall time	A-Port			1.8		nS
t_{RISE}	A Port rise time	A-Port			1.8		nS
VOLTAGE LEVEL SHIFTER – SCL, SDA LINES (x_A AND x_B PORTS) V_{CCA} = 1.8 V							
t_{PHL}	Propagation delay	A to B	SCL/SDA Channels Enabled		300		nS
		B to A			350		nS
t_{PLH}	Propagation delay	A to B			400		nS
		B to A			420		nS
t_{FALL}	A Port fall time	A-Port			210		nS
	B Port fall time	B-Port			225		nS
t_{RISE}	A Port rise time	A-Port			315		nS
	B Port fall time	B-Port			415		nS
$F_{(MAX)}$	Maximum switching frequency			400			kHz
VOLTAGE LEVEL SHIFTER – CEC LINES (x_A AND x_B PORTS) V_{CCA} = 1.8 V							
t_{PHL}	Propagation delay	A to B	CEC Channel Enabled		375		nS
		B to A			366		
t_{PLH}	Propagation delay	A to B			13.8		µS
		B to A			16.6		nS
t_{FALL}	A Port fall time	A-Port			210		nS
	B Port fall time	B-Port			170		
t_{RISE}	A Port rise time	A-Port			315		nS
	B Port rise time	B-Port			28		µS
VOLTAGE LEVEL SHIFTER – HPD LINES (x_A AND x_B PORTS) V_{CCA} = 1.8 V							
t_{PHL}	Propagation delay	B to A	HPD ChannelsEnabled		14.2		µS
t_{PLH}	Propagation delay	B to A			9.2		µS
t_{FALL}	A Port fall time	A-Port			1.5		nS
t_{RISE}	A Port rise time	A-Port			1.5		nS
VOLTAGE LEVEL SHIFTER – SCL, SDA LINES (x_A And x_B PORTS) V_{CCA} = 2.5 V							
t_{PHL}	Propagation delay	A to B	SCL/SDA Channels Enabled		300		nS
		B to A			400		
t_{PLH}	Propagation delay	A to B			290		nS
		B to A			420		
t_{FALL}	A Port fall time	A-Port			170		kHz
	B Port fall time	B-Port			225		
t_{RISE}	A Port rise time	A-Port			315		nS
	B Port fall time	B-Port			415		
$F_{(MAX)}$	Maximum switching frequency			400			kHz

Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE LEVEL SHIFTER – CEC LINES (x_A AND x_B PORTS) V_{CCA} = 2.5 V							
t_{PHL}	Propagation delay	A to B	CEC Channel Enabled		375		nS
		B to A			305		
t_{PLH}	Propagation delay	A to B			13.8		µS
		B to A			16.6		nS
t_{FALL}	A Port fall time	A-Port			170		nS
	B Port fall time	B-Port			170		
t_{RISE}	A Port rise time	A-Port			315		nS
	B Port rise time	B-Port			28		µS
VOLTAGE LEVEL SHIFTER – HPD LINES (x_A AND x_B PORTS) V_{CCA} = 2.5 V							
t_{PHL}	Propagation delay	B to A	HPD Channel Enabled		14.2		µS
t_{PLH}	Propagation delay	B to A			9.2		µS
t_{FALL}	A Port fall time	A-Port			1.2		nS
t_{RISE}	A Port rise time	A-Port			1.2		nS
VOLTAGE LEVEL SHIFTER – SCL, SDA LINES (x_A And x_B PORTS) V_{CCA} = 3.3 V							
t_{PHL}	Propagation delay	A to B	SCL/SDA Channels Enabled		300		nS
		B to A			400		
t_{PLH}	Propagation delay	A to B			260		nS
		B to A			415		
t_{FALL}	A Port fall time	A-Port			160		nS
	B Port fall time	B-Port			225		
t_{RISE}	A Port rise time	A-Port			305		nS
	B Port fall time	B-Port			415		
$F_{(MAX)}$	Maximum switching frequency			400			kHz
VOLTAGE LEVEL SHIFTER – CEC LINES (x_A AND x_B PORTS) V_{CCA} = 3.3V							
t_{PHL}	Propagation delay	A to B	CEC Channel Enabled		375		nS
		B to A			305		
t_{PLH}	Propagation delay	A to B			13.8		µS
		B to A			16.6		nS
t_{FALL}	A Port fall time	A-Port			160		nS
	B Port fall time	B-Port			170		
t_{RISE}	A Port rise time	A-Port			305		nS
	B Port rise time	B-Port			28		µS
VOLTAGE LEVEL SHIFTER – HPD LINES (x_A AND x_B PORTS) V_{CCA} = 3.3 V							
t_{PHL}	Propagation delay	B to A	HPD Channel Enabled		14.2		µS
t_{PLH}	Propagation delay	B to A			9.2		µS
t_{FALL}	A Port fall time	A-Port			1.1		nS
t_{RISE}	A Port rise time	A-Port			1.1		nS

7.7 Typical Characteristics

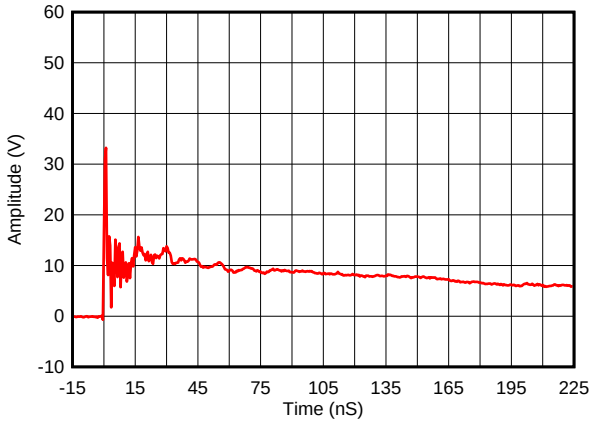


Figure 1. IEC Clamping Waveform +8kv Contact

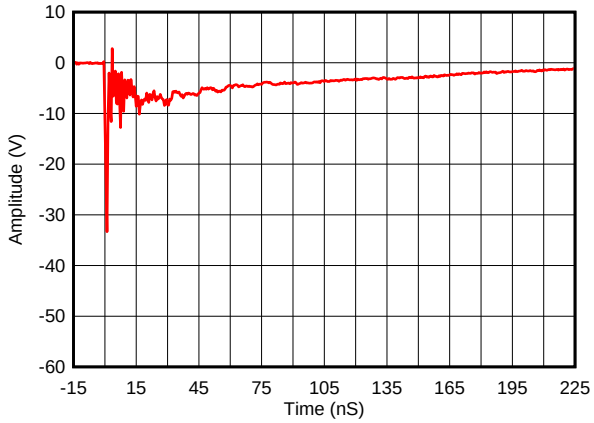


Figure 2. IEC Clamping Waveform –8kv Contact

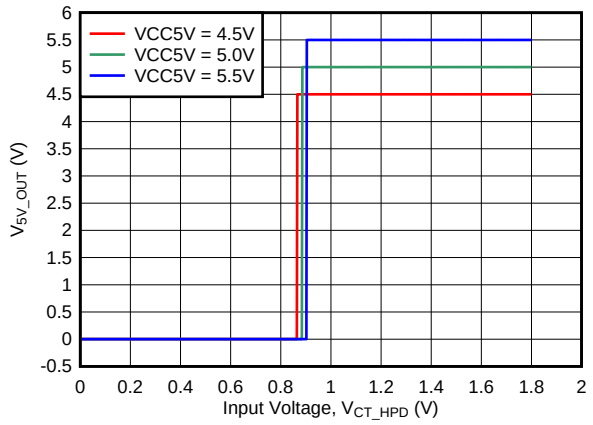


Figure 3. CT_HPD V_{IH}

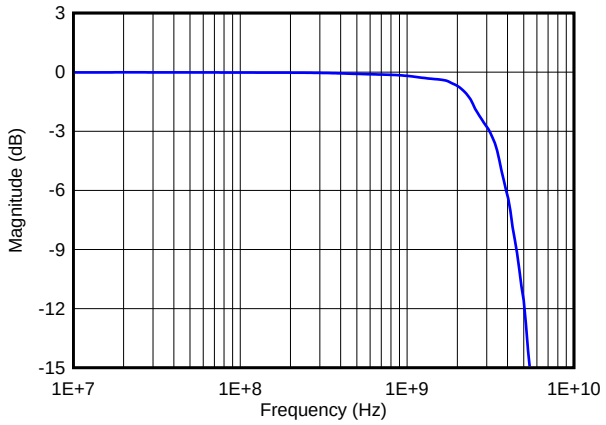


Figure 4. Insertion Loss, Data Line to GND

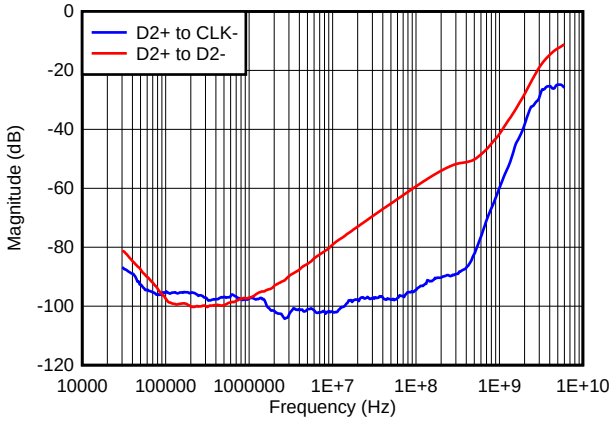


Figure 5. Channel-to-Channel Crosstalk

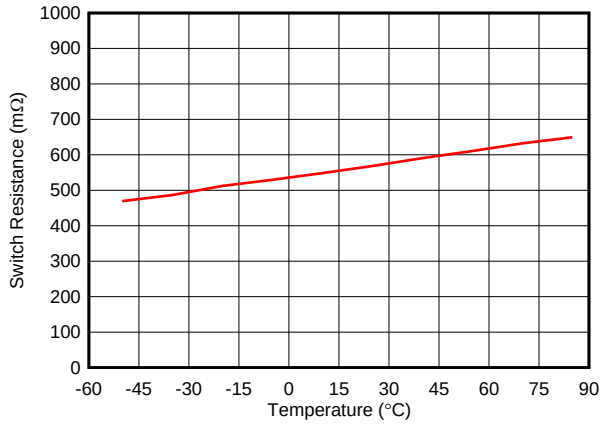


Figure 6. Switch Resistance vs Temperature, I_{switch} at Approximately 55 mA

Typical Characteristics (continued)

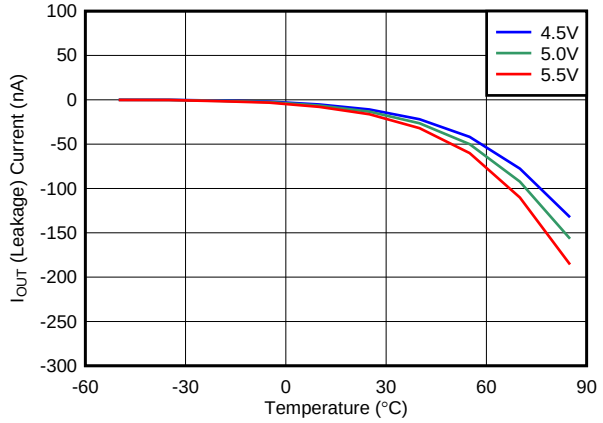


Figure 7. Load Switch $I_{leakage}$ vs Temperature

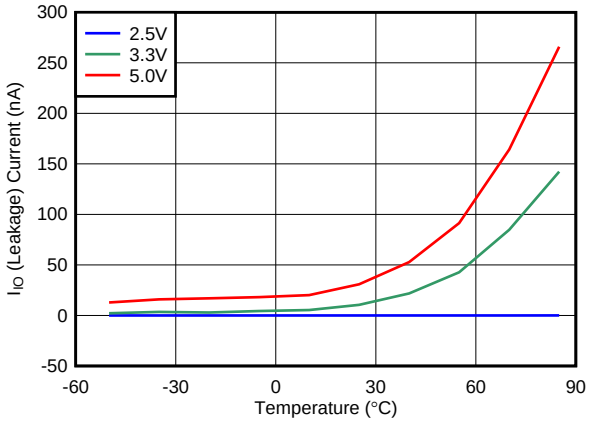


Figure 8. TMDS Line I_{IO} vs Temperature

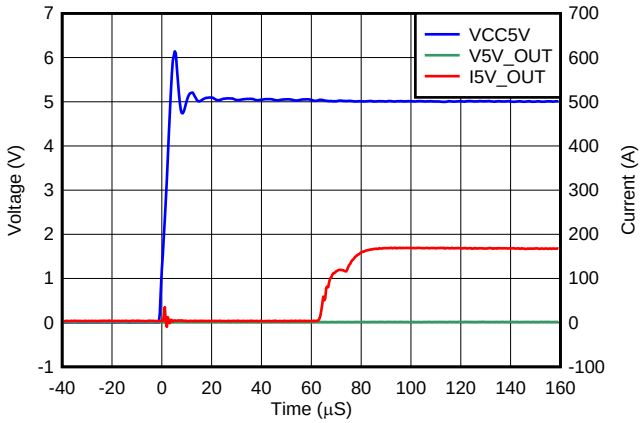


Figure 9. Short-Circuit Response Time (Powered-Up to Short)

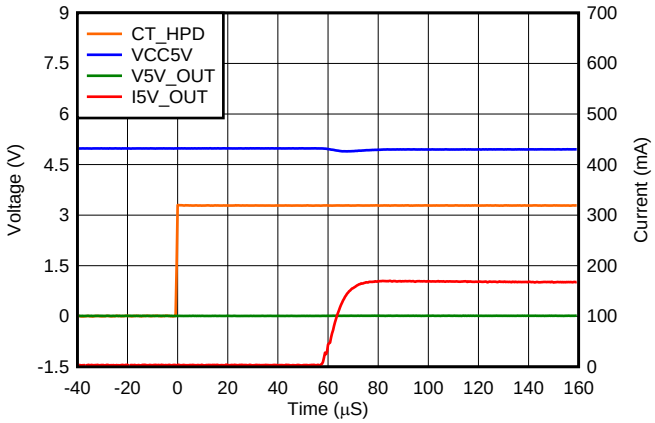


Figure 10. Current Limit Response Time (Switch Enabled to Short)

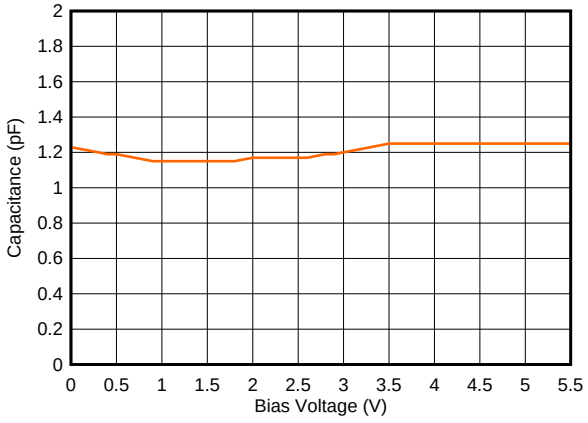


Figure 11. Capacitance vs Bias Voltage

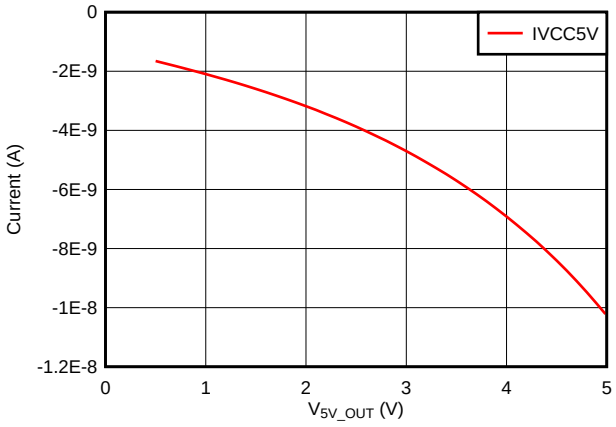


Figure 12. Load Switch $I_{LEAKAGE\_REVERSE}$ vs V_{5V_OUT}

8 Detailed Description

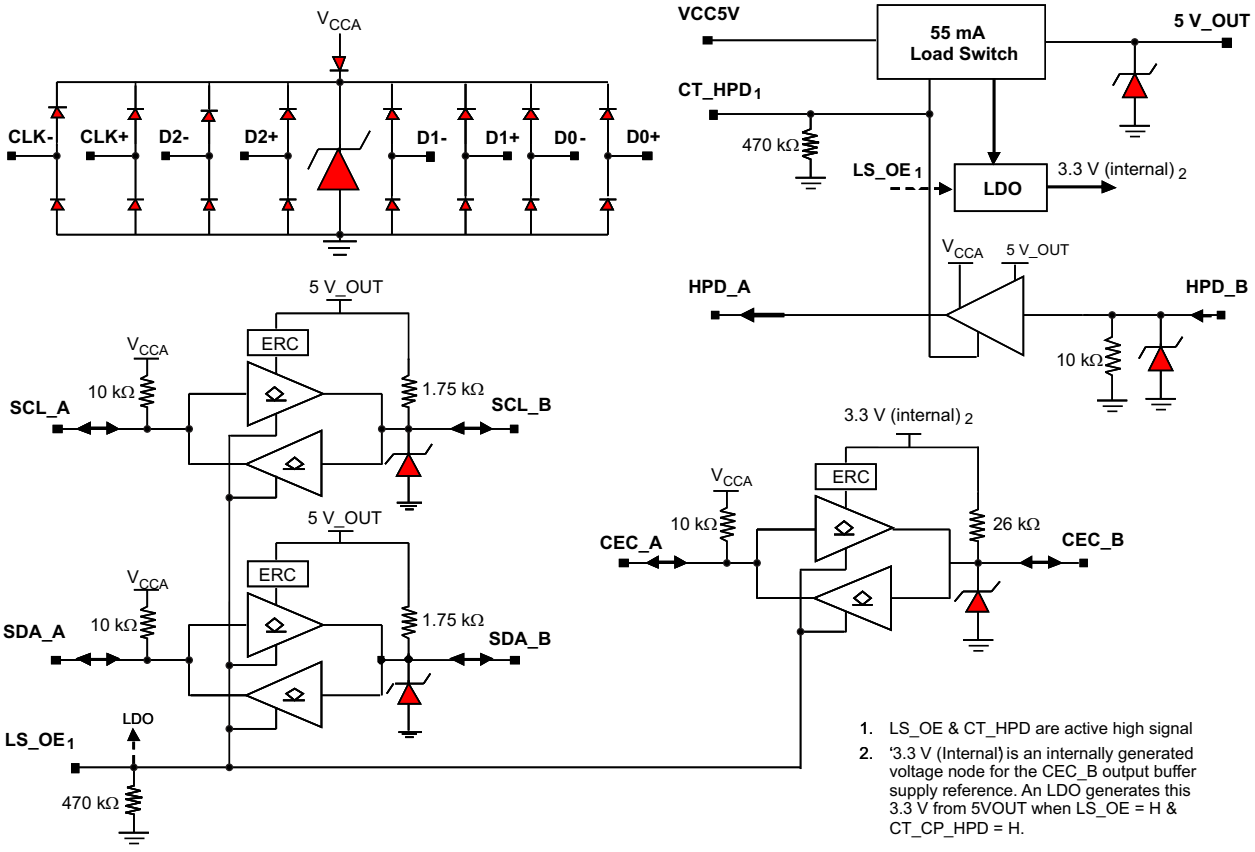
8.1 Overview

The TPD12S016 is a single-chip HDMI interface device with auto-direction sensing I^2C voltage level shifting buffers, a load switch, and integrated high-speed ESD protection clamps. The device pin mapping matches the HDMI connector with four differential pairs and control lines. This device offers eight low-capacitance ESD clamps, allowing HDMI 1.4 data rates. The integrated ESD circuits provides matching between each differential signal pair, which allows an advantage over discrete ESD solutions where variations between ESD protection clamps degrade the differential signal quality. The TPD12S016 provides a current limited 5-V output (5V_OUT) for sourcing the HDMI power line. The current limited 5-V output supplies up to 55 mA to the HDMI receiver. The control of 5V_OUT and the hot plug detect (HPD) circuitry is independent of the LS_OE control signal, and is controlled by the CT_HPD pin. This independent CT_HPD control enables the detection scheme (5V_OUT and HPD) to be active before enabling the HDMI link. An internal 3.3 V node powers the CEC pin eliminating the need for a 3.3 V supply on board.

The TPD12S016 integrates all the external termination resistors at the HPD, CEC, SCL, and SDA lines. There are three non-inverting bi-directional voltage level translation (VLT) circuits for the SDA, SCL, and CEC lines. Each have a common power rail (V_{CCA}) on the A side from 1.1 V to 3.6V. On the B side, the SCL_B and SDA_B each have an internal 1.75 kΩ pull up connected to the 5-V rail (5V_OUT). The SCL and SDA pins meet the I^2C specification and drive up to 750-pF capacitive loads exceeding the HDMI 1.4 specifications. The CEC_B pin has an internal 27-kΩ pull up resistor to the internal 3.3-V supply rail. The HPD_B port has a glitch filter to avoid false detection due to plug bouncing during the HDMI connector insertion.

The TPD12S016 offers a reverse current blocking feature at the 5V_OUT pin. In the fault conditions, such as when two HDMI transmitters connect to the same HDMI cable, the TPD12S016 ensures that the system is safe from powering up through an external HDMI transmitter. The SCL_B, SDA_B, CEC_B pins also feature reverse-current blocking when the system is powered off.

8.2 Functional Block Diagram



1. LS_OE & CT_HPD are active high signal
2. '3.3 V (Internal) is an internally generated voltage node for the CEC_B output buffer supply reference. An LDO generates this 3.3 V from 5VOUT when LS_OE = H & CT_CP_HPD = H.

8.3 Feature Description

8.3.1 Conforms to HDMI Compliance Tests without any External Components

The TPD12S016 has integrated pull-up or pull-down resistors on the DDC, CEC and HPD lines that conform to the HDMI 7.13 and 7.15 Compliance Tests without the designer needing to use any external components to TPD12S016.

8.3.2 IEC 61000-4-2 ESD Protection

In many cases, the core ICs, such as the scalar chipset, may not have robust ESD cells to sustain system-level ESD strikes. In these cases, the TPD12S016 provides the desired system-level ESD protection, such as the IEC 61000-4-2 Level 4 ESD protection of ±8-kV Contact rating by absorbing the energy associated with the ESD strike.

8.3.3 Supports HDMI 1.4 Data Rate

The high-speed TMDS pins of the TPD12S016 add only 1.0-pF (for PW package) or 1.2-pF (for RKT package) of capacitance to the TMDS lines. An Insertion Loss –3 dB point that is greater than 3 GHz provides enough bandwidth to pass HDMI 1.4 TMDS data rates.

8.3.4 Matches Class D and Class C Pin Mapping

The PW and RKT packages offer seamless layout routing options to eliminate the routing glitch for the differential signal pairs. The pin mapping follows the same order as the HDMI connector pin mapping.

8.3.5 8-Channel ESD Lines for Four Differential Pairs with Ultra-low Differential Capacitance Matching (0.05pF)

Excellent intra-pair capacitance matching of 0.05 pF provides ultra low intra-pair skew, which allows an advantage over discrete ESD solutions where variations between ESD protection clamps can degrade the differential signal quality.

8.3.6 On-chip Load Switch with 55mA Current Limit Feature at the HDMI 5V_OUT Pin

The TPD12S016 provides a current limited 5-V output (5V_OUT) for sourcing the HDMI power line. The current limited 5-V output supplies up to 55 mA to the HDMI receiver. The control of 5V_OUT and the HPD circuitry is independent of the LS_OE control signal, and is controlled by the CT_HPD pin. This independent CT_HPD control enables the detection scheme (5V_OUT and HPD) to be active before enabling the HDMI link.

8.3.7 Auto-direction Sensing I^2C Level Shifter with One-shot Circuit to Drive a Long HDMI Cable (750pF Load)

The TPD12S016 contains three bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage, V_{CCA} side DDC-bus and the 5-V DDC-bus or 3.3-V CEC line. The HDMI cable side of the DDC lines incorporates rise-time accelerators to support a high capacitive load on the HDMI cable side. The rise time accelerators boost the cable side DDC signal independent of which side of the bus is releasing the signal.

8.3.8 Back-drive Protection on HDMI Connector Side Ports

The TPD12S016 offers a reverse current blocking feature at the 5V_OUT pin. In fault conditions, such as when two HDMI transmitters connect to the same HDMI cable, the TPD12S016 ensures that the system is safe from powering up through an external HDMI transmitter. The SCL_B, SDA_B, CEC_B pins also feature reverse-current blocking when the system is powered off.

8.3.9 Integrated Pull-up and Pull-down Resistors per HDMI Specification

The system is designed to work properly according to the HDMI 1.4 specification with no external pull-up resistors on the DDC, CEC, and HPD lines.

Feature Description (continued)

8.3.10 Space Saving 24-pin RKT Package and 24-TSSOP Package

When compared to discrete ESD solutions, the fully integrated port protection offered by TPD12S016 reduces the overall area required to fully protect an HDMI transmitter port.

8.3.11 DDC/CEC LEVEL SHIFT Circuit Operation

The TPD12S016 enables DDC translation from V_{CCA} (system side) voltage levels to 5-V (HDMI cable side) voltage levels without degradation of system performance. The TPD12S016 contains two bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage, V_{CCA} side DDC-bus and the 5-V DDC-bus. The port B I/Os are over-voltage tolerant to 5.5 V, even when the device is un-powered. After power-up and with the LS_OE and CT_HPD pins HIGH, a LOW level on port A (below approximately V_{ILC} = 0.08 × V_{CCA} V) turns the corresponding port B driver (either SDA or SCL) on and drives port B down to V_{OLB} V. When port A rises above approximately 0.10 × V_{CCA} V, the port B pull-down driver is turned off and the internal pull-up resistor pulls the pin HIGH. When port B falls first and goes below 0.3 × 5 VOUT V, a CMOS hysteresis input buffer detects the falling edge, turns on the port A driver, and pulls port A down to approximately VOLA = 0.16 × V_{CCA} V. The port B pull-down is not enabled unless the port A voltage goes below V_{ILC}. If the port A low voltage goes below V_{ILC}, the port B pull-down driver is enabled until port A rises above (V_{ILC} + $\Delta V_{T\text{-}HYSTA}$), then port B, if not externally driven LOW, will continue to rise being pulled up by the internal pull-up resistor.

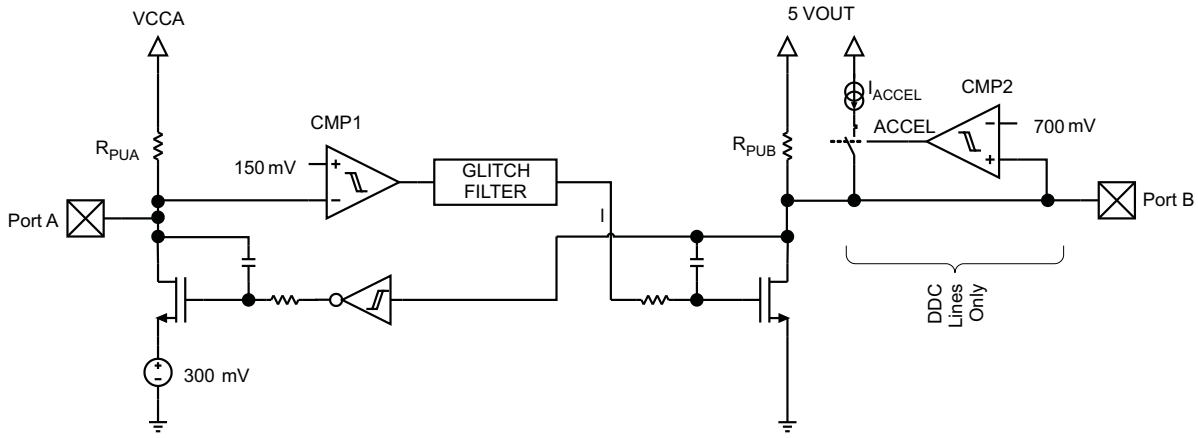


Figure 13. DDC/CEC Level Shifter Block Diagram

8.3.12 DDC/CEC Level Shifter Operational Notes For V_{CCA} = 1.8 V

- The threshold of CMP1 (see Figure 13) is approximately 150 mV ± the 40 mV of total hysteresis.
- The comparator will trip for a falling waveform at approximately 130 mV.
- The comparator will trip for a rising waveform at approximately 170 mV.
- To be recognized as a zero, the level at Port A must first go below 130 mV (V_{ILC} in spec) and then stay below 170 mV (V_{ILA} in spec).
- To be recognized as a one, the level at A must first go above 170 mV and then stay above 130 mV.
- V_{ILC} is set to 117 mV in Electrical Characteristics Table to give some margin to the 130 mV.
- V_{ILA} is set to 148 mV in the *Electrical Characteristics* table to give some margin to the 170 mV.
- V_{IHA} is set to 70% of V_{CCA} to be consistent with standard CMOS levels.

Feature Description (continued)

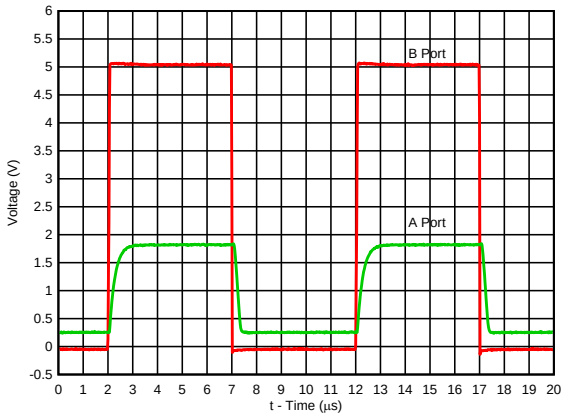


Figure 14. DDC Level Shifter Operation (B To A Direction)

8.3.13 Rise-Time Accelerators

The HDMI cable side of the DDC lines incorporates rise-time accelerators to support high capacitive load (up to 750 pF) on the HDMI cable side. The rise time accelerators boost the cable side DDC signal independent of which side of the bus is releasing the signal.

8.3.14 Noise Considerations

Ground offset between the TPD12S016 ground and the ground of devices on port A of the TPD12S016 must be avoided. The reason for this cautionary remark is that a CMOS/NMOS open-drain capable of sinking 3 mA of current at 0.4 V will have an output resistance of 133 Ω or less (R = E / I). Such a driver will share enough current with the port A output pull-down of the TPD12S016 to be seen as a LOW as long as the ground offset is zero. If the ground offset is greater than 0 V, then the driver resistance must be less. Since V_{ILC} can be as low as 90 mV at cold temperatures and the low end of the current distribution, the maximum ground offset should not exceed 50 mV. Bus repeaters that use an output offset are not interoperable with the port A of the TPD12S016 as their output LOW levels will not be recognized by the TPD12S016 as a LOW. If the TPD12S016 is placed in an application where the V_{IL} of port A of the TPD12S016 does not go below its V_{ILC} it will pull port B LOW initially when port A input transitions LOW but the port B will return HIGH, so it will not reproduce the port A input on port B. Such applications should be avoided. Port B is interoperable with all I^2C-bus slaves, masters and repeaters.

8.3.15 Resistor Pull-Up Value Selection

The system is designed to work properly with no external pull-up resistors on the DDC, CEC, and HPD lines.

8.4 Device Functional Modes

The LS_OE and CT_HPD are active-high enable pins. They control the TPD12S016 power saving options according to the following table:

Table 1. Power Saving Options(1)

LS_OE	CT_HPD	V_{CCA}	V_{CC5V}	A-side Pull-ups	DDC, B-Side Pull-ups	CEC_B Pull-ups	CEC LDO	Load SW and HPD	DDC/ CEC VLTs	ICCA Typ	ICC5V Typ	Comments
L	L	1.8V	5.0V	Off	Off	Off	Off	Off	Off	1µA	1 µA	Fully Disabled
L	H	1.8V	5.0V	On	On	Off	Off	On	Off	1 µA	30 µA	Load Switch on
H	L	1.8V	5.0V	Off	Off	Off	Off	Off	Off	1 µA	1 µA	Not a Valid State
H	H	1.8V	5.0V	On	On	On	On	On	On	13 µA	200 µA	Fully On
X	X	0V	0V	High-Z	High-Z	High-Z	Off	Off	Off	0	0	Power Down
X	X	1.8V	0V	High-Z	High-Z	High-Z	Off	Off	Off	0	0	Power Down
X	X	0V	5.0V	High-Z	High-Z	High-Z	Off	Off	Off	0	0	Power Down

(1) X = Don't Care, H = Signal High, and L = Signal Low

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

TPD12S016 provides IEC 61000-4-2 Level 4 Contact ESD rating to the HDMI 1.4 transmitter port. Buffered VLT's translate DDC and CEC channels bi-directionally. The system is designed to work properly with no external pull-up resistors on the DDC, CEC, and HPD lines. The CEC line has an integrated 3.3-V rail, eliminating the need for a 3.3-V supply on board.

9.2 Typical Application

The TPD12S016 is placed as close as possible to the HDMI connector to provide voltage level translation, 5V_OUT current limiting and overall ESD protection for the HDMI Controller.

9.2.1 Example 1: HDMI Controller Using One Control Line

In the example shown below, the HDMI Driver Chip is controlling the TPD12S016 via only one control line, CT_HPD. In this mode the HPD_A to LS_OE pin are connected as shown in the oval dotted line of Figure 15. To fully enable TPD12S016, set CT_HPD above V_{IH}. To fully disable TPD12S016, set CT_HPD below V_{IL}.

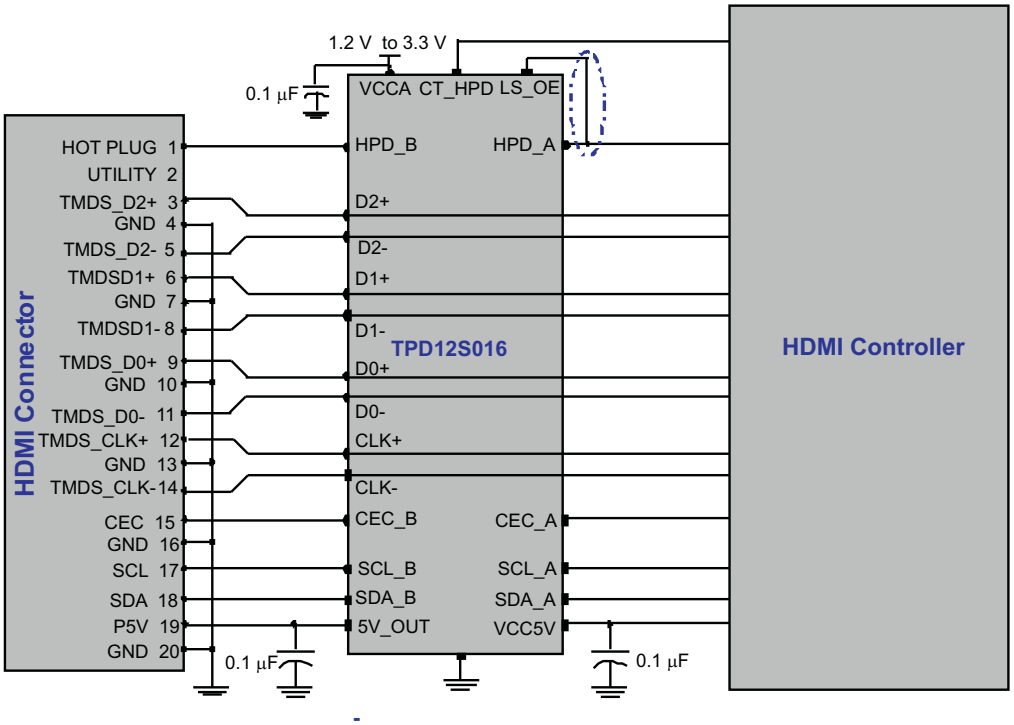


Figure 15. TPD12S016 with an HDMI Controller Using One GPIO for HDMI Interface Control

Typical Application (continued)

9.2.1.1 Design Requirements

For this example, use the following table as input parameters:

Table 2. HDMI Controller Using One Control Line Design Parameters

Design Parameters			Example Value
Voltage on V_{CCA}			1.8 V
Voltage on V_{CC5V}			5.0 V
Drive CT_HPD low (disabled)			-0.5 V – 0.4 V
Drive CT_HPD high (enabled)			1.0 V – 1.8 V
Drive a logical "1"	A to B	SCL and SDA	1.26 V – 1.8 V
		CEC	
	B to A	SCL and SDA	3.5 V – 5.0 V
		CEC	2.31 V – 3.3 V
Drive a logical "0"	A to B	SCL and SDA	-0.5 V – 0.117 V
		CEC	
	B to A	SCL and SDA	-0.5 V – 1.5 V
		CEC	-0.5 V – 0.99 V

9.2.1.2 Detailed Design Procedure

To begin the design process the designer needs to know the V_{CC5V} voltage range and the logic level, V_{CCA}, voltage range.

9.2.1.3 Application Curves

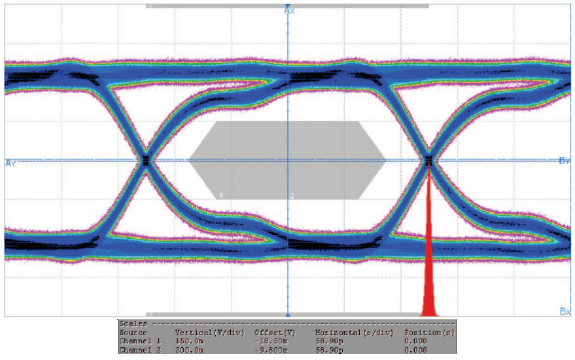


Figure 16. Eye Diagram Using EVM Without TPD12S016 for the TMDS Lines at 1080p, 340 MHz Pixel Clock, 3.4 Gbps

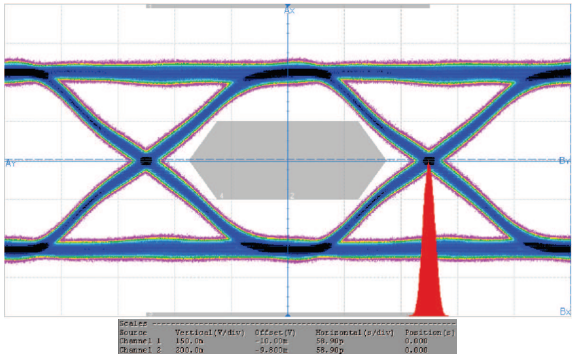


Figure 17. Eye Diagram Using EVM With TPD12S016 for the TMDS Lines at 1080p, 340 MHz Pixel Clock, 3.4 Gbps

9.2.2 Example 2: HDMI Controller Using CT_HPD and LS_OE

Some HDMI driver chips may have two GPIOs to control the HDMI interface chip. In this case a flexible power saving mode can be implemented. The load switch can be activated by CT_HPD while the level shifters are inactive, using LS_OE. This results in TPD12S016 drawing only approximately 30 µA, a reduction of 170 µA from being fully on. After a hot plug is detected, the HDMI controller can enable the rest of the HDMI interface chip using LS_OE.

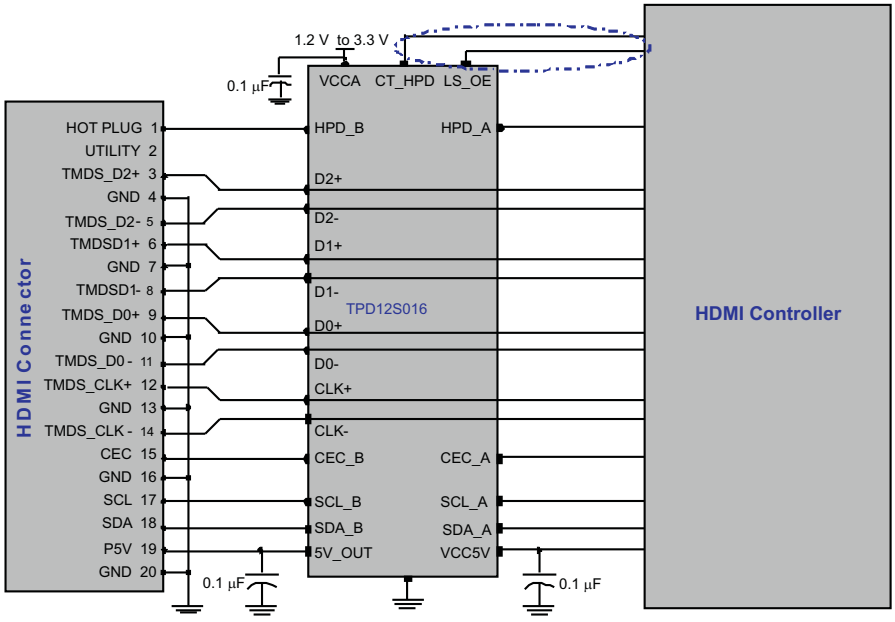


Figure 18. TPD12S016 with an HDMI Controller Using Two GPIOs For HDMI Interface Control

9.2.2.1 Design Requirements

For this example, use the following table as input parameters:

Table 3. HDMI Controller Using CT_HPD and LS_OE Design Parameters

Design Parameters			Example Value
Voltage on V_{CCA}			3.3 V
Voltage on V_{CC5V}			5.0 V
Drive CT_HPD low (disabled)			-0.5 V – 0.4 V
Drive LS_OE low (disabled)			
Drive CT_HPD high (enabled)			1.0 V – 3.3 V
Drive LS_OE high (enabled)			
Drive a logical "1"	A to B	SCL and SDA	2.31 V – 3.3 V
		CEC	
	B to A	SCL and SDA	3.5 V – 5.0 V
		CEC	2.31 V – 3.3 V
Drive a logical "0"	A to B	SCL and SDA	-0.5 V – 0.214 V
		CEC	
	B to A	SCL and SDA	-0.5 V – 1.5 V
		CEC	-0.5 V – 0.99 V

9.2.2.2 Detailed Design Procedure

To begin the design process the designer needs to know the V_{CC5V} voltage range and the logic level, V_{CCA}, voltage range.

9.2.2.3 Application Curves

Refer to *Application Curves* for related application curves.

10 Power Supply Requirements

TPD12S016 has two power input pins: V_{CC5V} and V_{CCA}. It can operate normally with V_{CC5V} between 4.5 V and 5.5 V; and V_{CCA} between 1.1 V and 3.6 V. Thus, the power supply (with a ripple of V_{RIPPLE}) requirement for TPD12S016 for V_{CC5V} is between 4.5 V + V_{RIPPLE} and 5.5 V – V_{RIPPLE}; and for V_{CCA} it is between 1.1 V + V_{RIPPLE} and 3.6 V – V_{RIPPLE}.

11 Layout

11.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures. Therefore, the PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Avoid using VIAs between the connecter and an I/O protection pin on TPD12S016.
- Avoid 90º turns in traces.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- Minimize impedance on the path to GND for maximum ESD dissipation.
- The capacitors on V_{BUS} and V_{OTG_IN} should be placed close to their respective pins on TPD12S016.

11.2 Layout Example

11.2.1 TPD12S016RKT

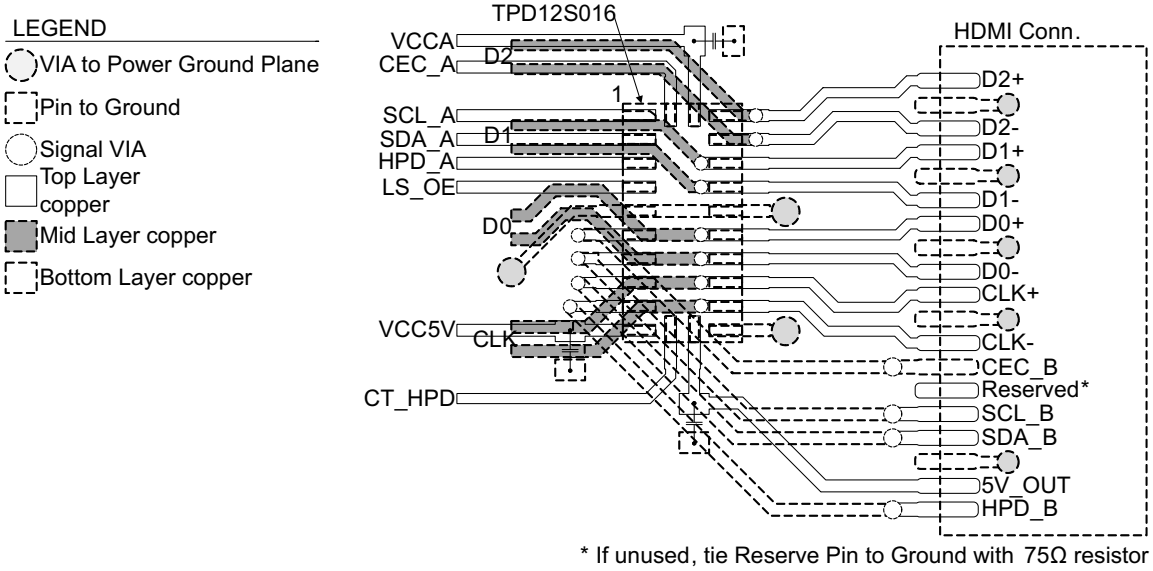
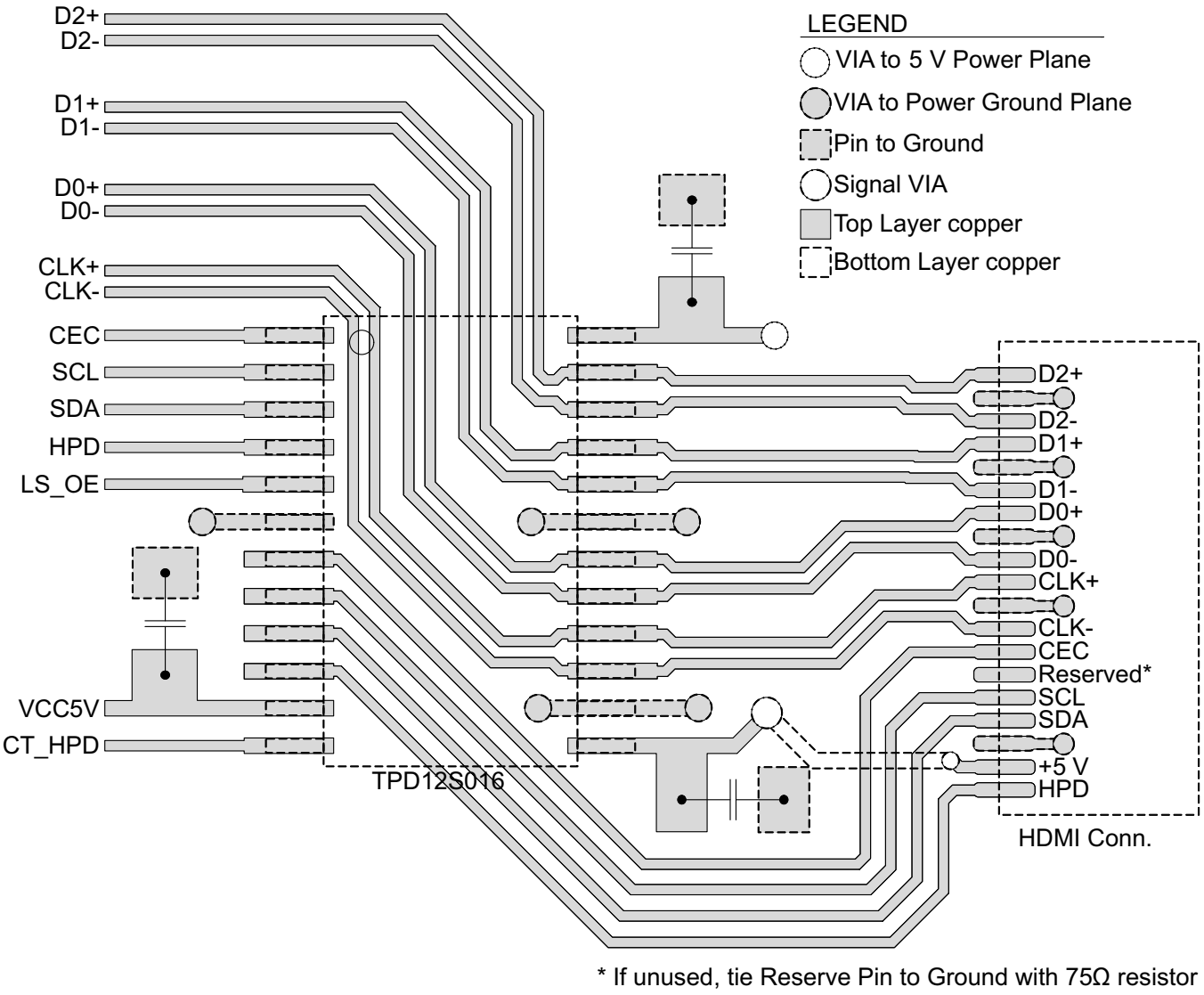


Figure 19. TPD12S016RKT Layout Example

Layout Example (continued)

Routing with TPD12S016RKT requires three layers. VIAs are an integral part of layout for such a design. Proper placement of VIAs can eliminate exposing the system unnecessarily to an ESD event. The example shown above routes the TMDS lines directly from the connector to the protection pins *before* using VIAs to an internal layer. This helps promote ESD energy dissipation at the TPD12S016 protection pins. Note that while there is a VIA between the connector and the DDC/CEC/HPD lines, the traces terminate at the protection pins, leaving no other path for ESD energy to dissipate except at the TPD12S016 protection pins. All ground pins should have a large VIA near them connecting to as many internal and external ground planes as possible to reduce any impedance between TPD12S016 and ground. Tenting of VIAs near to SMD pads should be done to eliminate any solder-wicking during PCB assembly.

11.2.2 TPD12S016PW



* If unused, tie Reserve Pin to Ground with 75Ω resistor

Figure 20. TPD12S016PW Layout Example

The TPD12S016PW can be routed on a single layer. HDMI connector pin matching has been arranged to allow for a flow through routing style. All ground pins should have a large VIA near them connecting to as many internal and external ground planes as possible to reduce any impedance between TPD12S016 and ground. Tenting of VIAs near to SMD pads should be done to eliminate any solder-wicking during PCB assembly.

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD12S016PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PN016	Samples
TPD12S016RKTR	ACTIVE	UQFN	RKT	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PN016	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

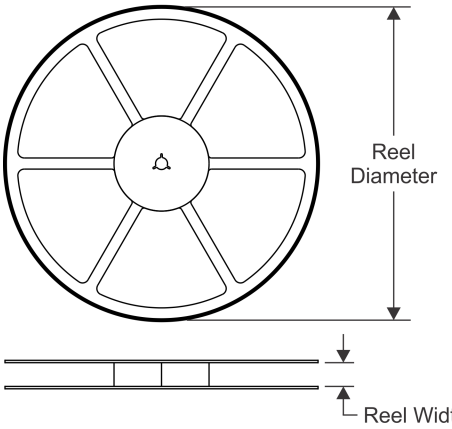
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

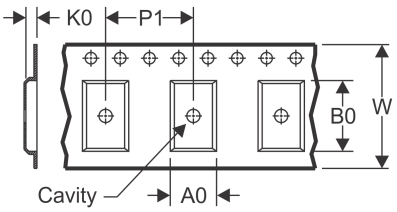
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

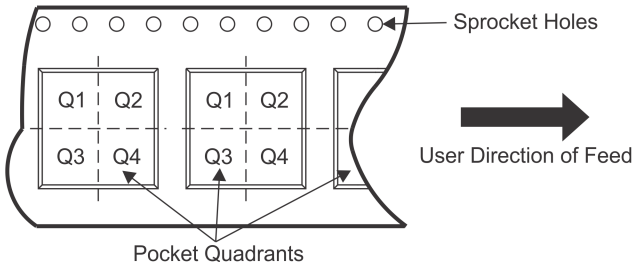


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

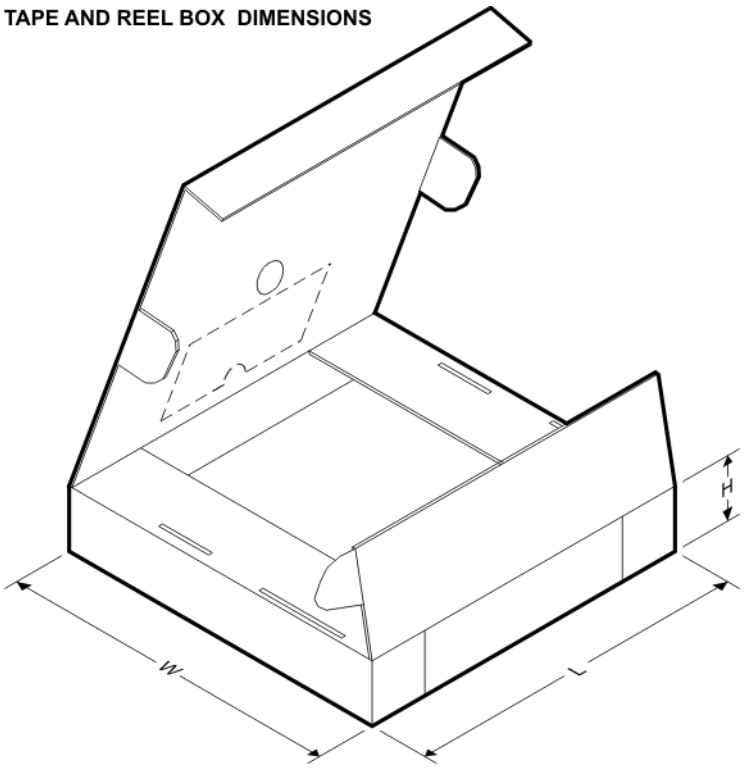
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD12S016PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TPD12S016RKTR	UQFN	RKT	24	3000	177.8	12.4	2.21	4.22	0.81	4.0	12.0	Q1

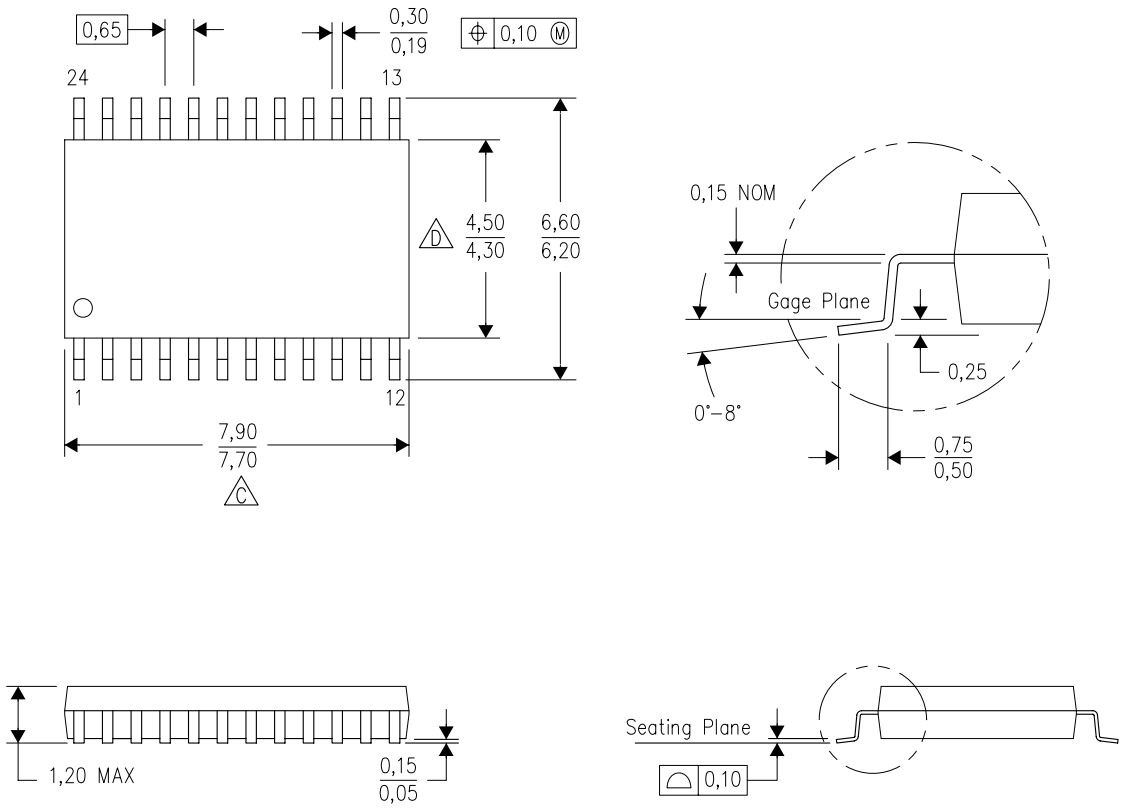
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD12S016PWR	TSSOP	PW	24	2000	367.0	367.0	38.0
TPD12S016RKTR	UQFN	RKT	24	3000	202.0	201.0	28.0

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



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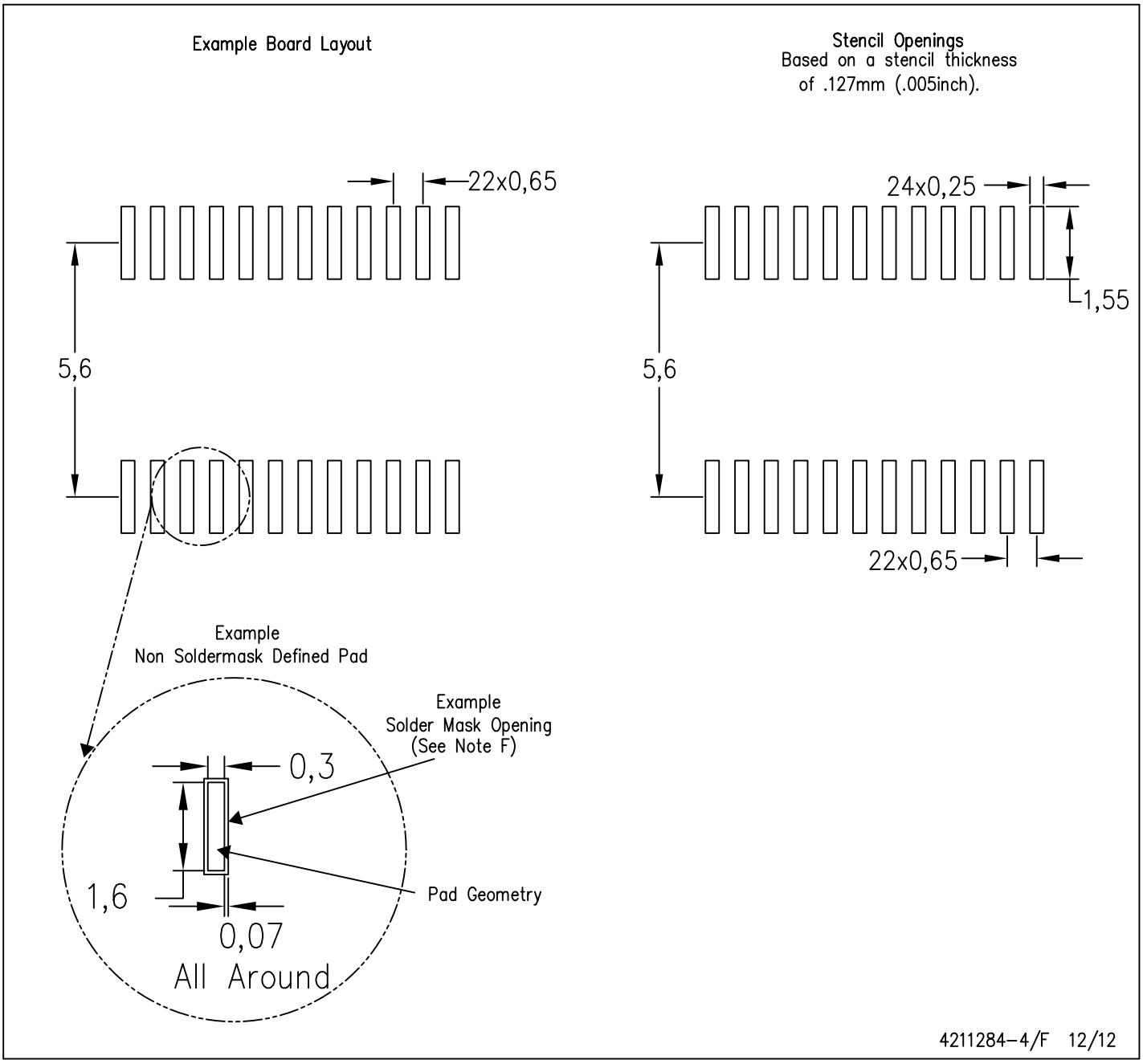
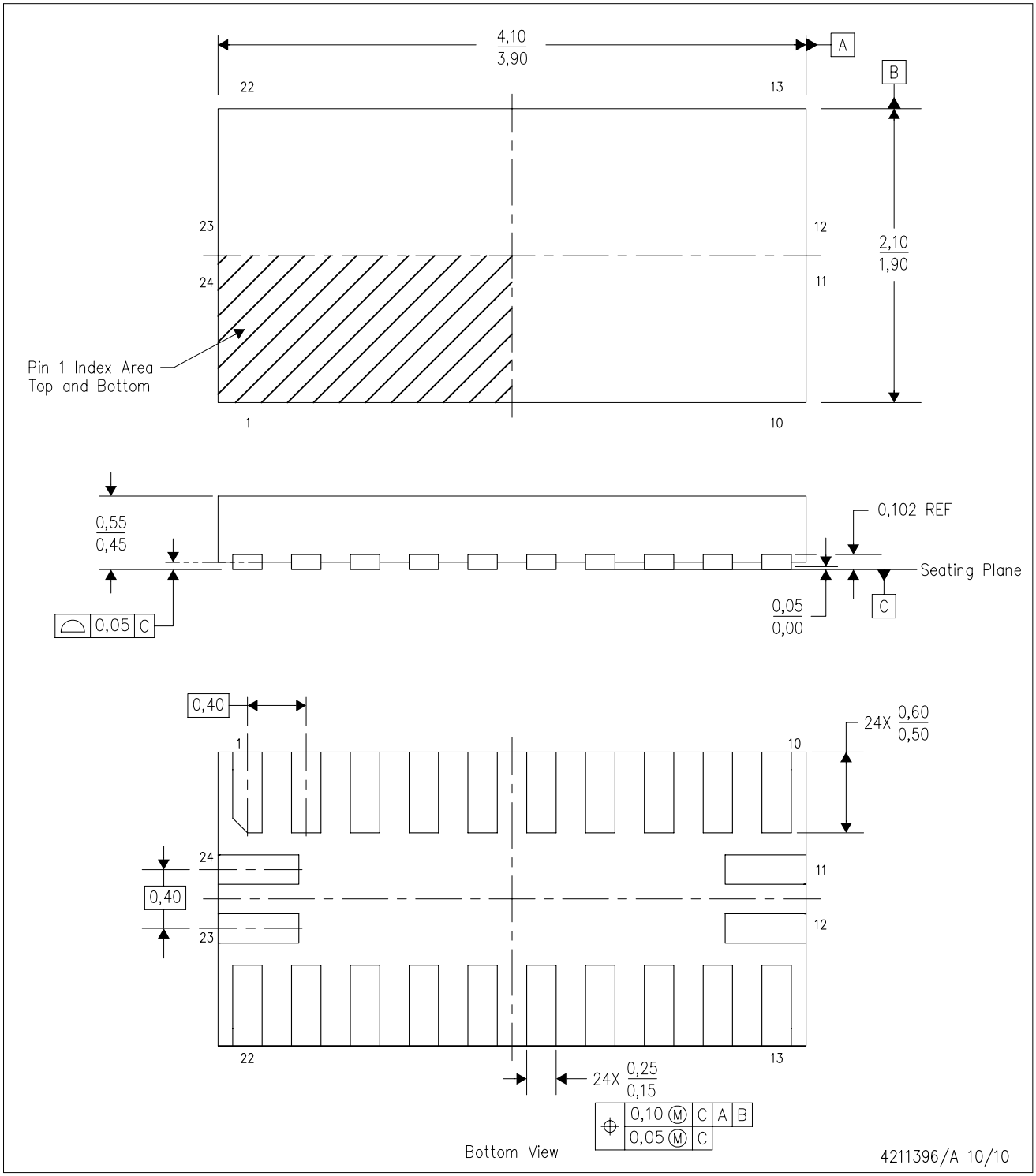
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

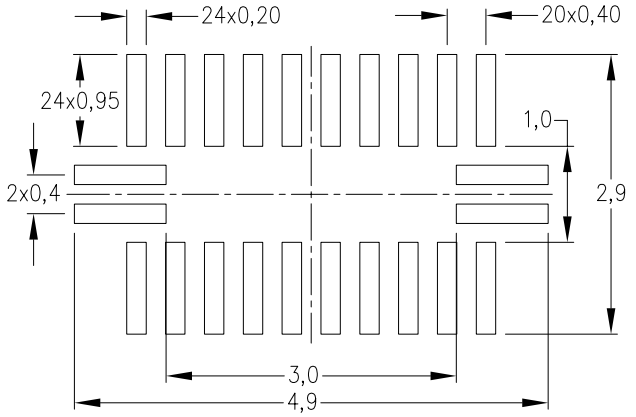
RKT (R–PUQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



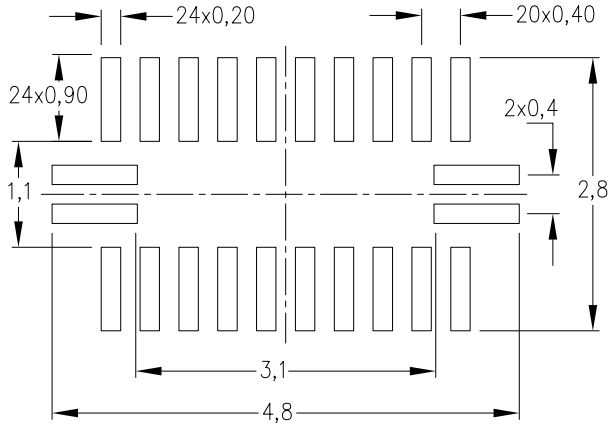
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.

RKT (R–PUQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

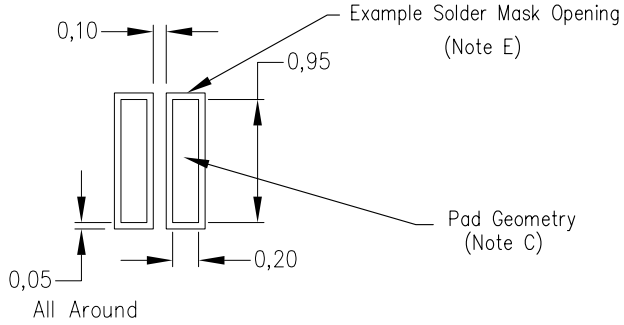
Example Board Layout



Example Stencil Design
0.125 Thick Stencil
(Note D)



Non Solder Mask Defined Pad



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances between and around signal pads

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