Features

- **Pin-programmable Mode**
- **Supply Voltage Range 1.55V to 3.6V**
- **PHY IC_USB1.0 Downstream Port**
- **Bridge USB2.0 Section 7 to IC_USB1.0**
- **Bridge IC_USB1.0 to USB2.0 Section 7**
- **3.3V Voltage Reference**
- **Two 70mA LDO Voltage Regulators**
- **Less Than 5µA Static Current on Each Supply**
- **Slew Rate Control to Minimize Radiated EMI**
- **ESD 4kV Compliant with USB UICC**
- **Applications:**
  - **Mobile USB UICC (ETSI 102 600), PC USB UICC, Token USB**

Description

The AT73C260 is an Inter Chip USB transceiver fully compliant with the Universal Serial Bus Specification, and more specifically with the IC_USB1.0 supplement. The AT73C260 is a bidirectional differential interface. The AT73C260 is ideal for applications in mobile devices, PCs and USB tokens making use of an USB UICC.

The AT73C260's upstream facing port may be connected to three different interfaces:

- Digital
- USB2.0 section 7 with or without cable
- IC_USB1.0

The AT73C260's downstream port complies with IC_USB1.0. The AT73C260's mode is selected by three pins. When PVCC is powered by 3.3V and pull down resistors are added on PDM and PDP, the AT73C260's downstream port complies with USB2.0 section 7.

The AT73C260 includes a 3.5V Supply Monitor, a Low Power Band-Gap, a 3.3V 70mA Linear Voltage Regulator and a 1.8V-3.0V 70mA Linear Voltage Regulator SIM FTA compliant Test 27.17.2.1.

The AT73C260 is specified over the industrial temperature range - 40°C to +85°C.

The AT73C260 is available in a 3 X 3 mm, 0.5mm pitch, QFN16 package.

Power Management and Analog Companions (PMAAC)

AT73C260

Interchip USB Transceiver

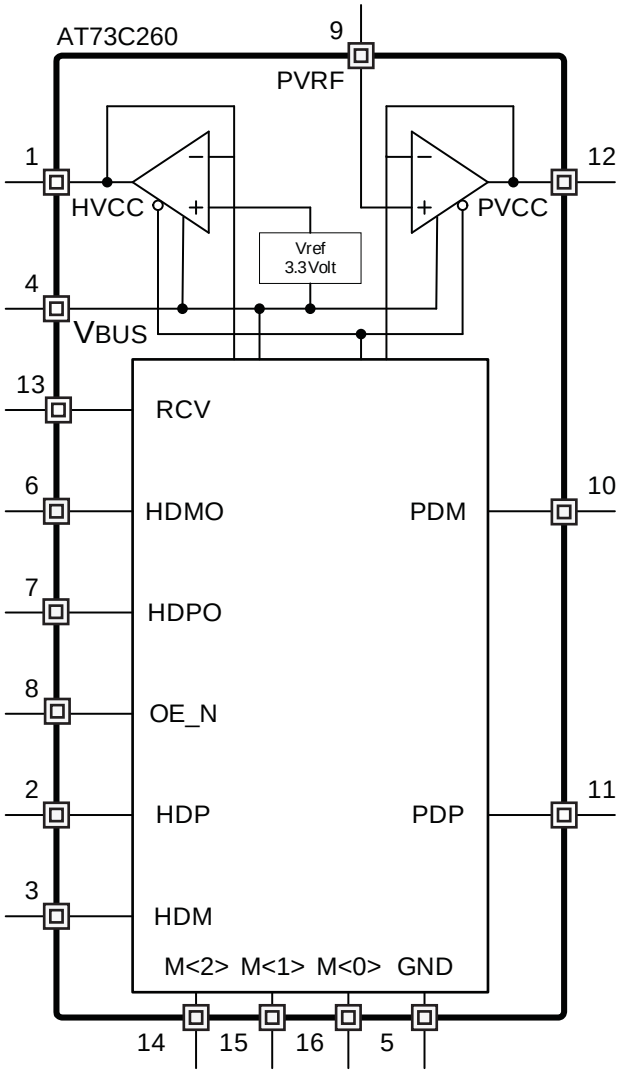
(PHY - IC_USB1.0, Voltage Class Converter, USB2.0 - IC_USB1.0 Bridges)

Preliminary

11030A–PMAAC–13-Sep-10

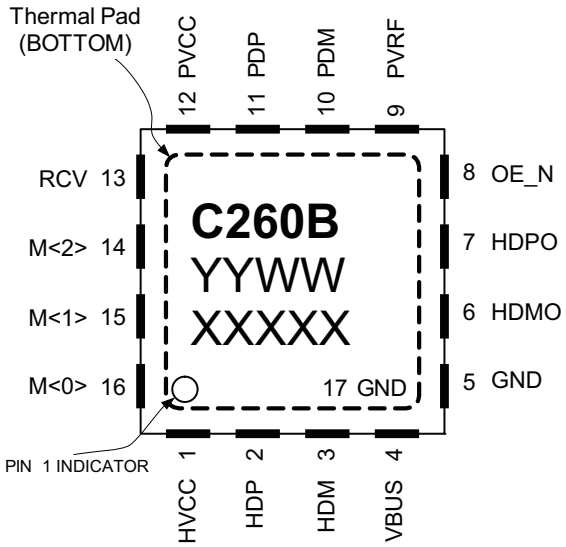
1. Block Diagram

Figure 1-1. AT73C260 functional block diagram



2. Package and Pinout

Figure 2-1. AT73C260 QFN16 package pinout - top view



3. Pin Description

Table 3-1. AT73C260 Pin Description

Pin Name	I/O	Pin Number	Type	Function
HVCC	Output	1	Analog	Host Side VCC •When pin 4 (VBUS) is grounded. The LDO on pin HVCC is in standby and its output is isolated. The Host supplies HVCC with the appropriate voltage to the AT73C260's upstream transceiver. •When pin 4 (VBUS) is connected to a voltage source the internal voltage reference 3.3V and both LDO are activated. The LDO on pin 1 provides power at 3.3V to the AT73C260's upstream transceiver and it may source up to 70mA.
HDP	I/O	2	Digital	Bidirectional
HDM	I/O	3	Digital	Bidirectional
VBUS	Input	4	Analog	Supply, provides power to the LDOs on pin 1 and 12
GND	Ground	5	Analog	GND Ground for Digital and I/Os
HDMO	Output	6	Digital	Output
HDPO	Output	7	Digital	Output
OE_N	Input	8	Digital	Input
PVRF	Input	9	Analog	PVCC LDO input reference
PDM	I/O	10	Digital	Bidirectional pad
PDP	I/O	11	Digital	Bidirectional pad
PVCC	Input	12	Analog	Peripheral Side VCC •When pin 4 (VBUS) is grounded. The LDO on pin PVCC is in standby and its output is isolated. The application supplies PVCC with the appropriate voltage to the AT73C260's downstream transceiver. •When pin 4 (VBUS) is connected to a voltage source, the LDO on pin PVCC follows the voltage on pin PVRF. The LDO on pin PVCC provides power to the AT73C260's downstream transceiver and it may source up to 70mA.
RCV	Output	13	Digital	Output
M<2>	Input	14	Digital	Input. For mode configuration
M<1>	Input	15	Digital	Input. For mode configuration
M<0>	Input	16	Digital	Input. For mode configuration
GND	Ground	17	Analog	Analog Ground. Thermal Pad. Shall be connected to GND for electrical and power dissipation reasons.

4. Absolute Maximum Ratings

Table 4-1. Absolute Maximum Ratings

Operating Temperature (Industrial).....-40°C to + 85°C[1]	*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Storage Temperature.....-55°C to + 150°C	
Power Supply Input on H_{VCC}..... -0.3V to + 3.6V	
Power Supply Input on VBUS..... -0.3V to + 5.5V	
Digital I/O Input Voltage..... -0.3V to + 3.6V	
All Other Pins.....-0.3V to + 3.6V	
ESD (all pins).....4 KV HBM	

Notes: 1. Refer to Power Dissipation Rating section)

5. Recommended Operating Conditions

Table 5-1. Recommended Operating Conditions

Parameter	Condition	Min	Max	Units
Operating Ambient Temperature[1]		-40	85	°C
Power Supply Output	P_{VCC}	1.55	3.6	V
Power Supply Input	H_{VCC}	1.55	3.6	V
Power Supply Input	VBUS	4.0	5.5	V

Note: 1. Refer to Power Dissipation Rating section

6. Power Dissipation Ratings

Table 6-1. Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Units
Maximum Junction Temperature		-40	--	125	°C
R_{THjA}[1]	Package thermal junction to ambient resistance	--	--	90	°C / W
Maximum On-chip Power Dissipation	Ambient temperature = 85°C	--	--	400	mW

Note: 1. According to specification JESD51-5

7. Electrical Characteristics

7.1 I/Os DC Characteristics Referred to H_{VCC}

Table 7-1. H_{VCC} Referred I/Os: HDP, HDM, RCV, HDMO, HDPO, OE_N and M<2:0>

Symbol	Parameter	Comments	Min	Typ	Max	Units
H_{VCC}	Host Side Supply Voltage	220nF ceramic capacitor (1)	1.55	--	3.6	V
I_{HVCC}	Operating H_{VCC} Supply Current	Full Speed Transceiver / Receiver at 12Mbps, C_{LOAD} = 18pF on HDP and HDM during transmit	--	--	2	mA
V_{IH}	Input High-Level Voltage	$V_{OH} > V_{OH\_MIN}$	0.65 x H_{VCC}	--	H_{VCC} + 0.3	V
V_{IL}	Input Low-Level Voltage	$V_{OH} < V_{OL\_MAX}$	-0.3	--	0.35 x H_{VCC}	V
V_{OH}	Output High-Level Voltage	I_{OH} = - 2mA	H_{VCC} - 0.45	--	--	V
V_{OL}	Output Low-Level Voltage	I_{OL} = 2mA	--	--	0.45	V
R_{PDP}	Pull-Down Resistors on HDP, HDM	All Cases	30	--	80	kΩ
R_{PU1} (2)	Upstream Pull-Up Resistors on HDP	M<0> = 0 M<2:1> = connected to H_{VCC}	0.9	--	3.09	kΩ
R_{PU2} (3)	Upstream Pull-Up Resistors on HDP	M<2:0> = connected to H_{VCC}	1	--	150	kΩ

Notes:
1. A 220nF ceramic capacitor is connected between the pin H_{VCC} and the pin GND and closest to H_{VCC} pin.
2. R_{PU1} Pull Up resistor is as per the ECN “Pull-up/pull-down resistors” published by the USB-IF. R_{PU1} value is between 900Ω and 1575Ω when the bus is idle and between 1425Ω and 3090Ω when the upstream device is transmitting
3. R_{PU2} Pull Up resistor is as per the IC_USB1.0 published by the USB-IF. R_{PU2} value is between 1kΩ and 3kΩ to attach and between 30kΩ and 150kΩ during idle.

7.2 I/Os DC Characteristics Referred to P_{VCC}

Table 7-2. P_{VCC} Referred I/Os: PDP, PDM

Symbol	Parameter	Comments	Min	Typ	Max	Units
P_{VCC}	Peripheral Side Supply Voltage	220nF ceramic capacitor (1)	1.55	--	3.6	V
I_{PVCC}	Operating P_{VCC} Supply Current	Full Speed Transceiver / Receiver at 12Mbps, C_{LOAD} = 18pF on PDP and PDM during transmit	--	--	2	mA
V_{IH}	Input High-Level Voltage	$V_{OH} > V_{OH\_MIN}$	0.65 x P_{VCC}	--	P_{VCC} + 0.3	V
V_{IL}	Input Low-Level Voltage	$V_{OH} < V_{OL\_MAX}$	-0.3	--	0.35 x P_{VCC}	V
V_{OH}	Output High-Level Voltage	I_{OH} = - 2mA	P_{VCC} - 0.45	--	--	V
V_{OL}	Output Low-Level Voltage	I_{OL} = 2mA	--	--	0.45	V
R_{PDH}	Pull-Down Resistors	All Cases for PDP, PDM	30	--	80	kΩ

Notes:
1. A 220nF ceramic capacitor is connected between the pin P_{VCC} and the pin GND and closest to P_{VCC} pin.

7.3 Timing Characteristics Table

Table 7-3. Timing Table

Symbol	Parameter	Comments	Min	Typ	Max	Units
T_{DELAY}	Propagation Delay Time	H_{VCC} = 3.3V and P_{VCC} = 3.0V	--	37	--	ns
		H_{VCC} = 3.3V and P_{VCC} = 1.8V	--	42	--	ns
$T_{SLEW\_R\_P}$	Slew Rate, Rise Time on PDP	10%-90%, C_{LOAD}=33pF, P_{VCC}=3.0V	--	5.7	--	ns
		10%-90%, C_{LOAD}=33pF, P_{VCC}=1.8V	--	10.5	--	
$T_{SLEW\_R\_M}$	Slew Rate, Rise Time on PDM	10%-90%, C_{LOAD}=33pF, P_{VCC}=3.0V	--	5.6	--	
		10%-90%, C_{LOAD}=33pF, P_{VCC}=1.8V	--	10.6	--	
$T_{SLEW\_F\_P}$	Slew Rate, Fall Time on PDP	10%-90%, C_{LOAD}=33pF, P_{VCC}=3.0V	--	6.1	--	
		10%-90%, C_{LOAD}=33pF, P_{VCC}=1.8V	--	7.6	--	
$T_{SLEW\_F\_M}$	Slew Rate, Fall Time on PDM	10%-90%, C_{LOAD}=33pF, P_{VCC}=3.0V	--	6.1	--	
		10%-90%, C_{LOAD}=33pF, P_{VCC}=1.8V	--	7.7	--	
T_{ATTACH}	Attachment Transit Time	M<2:0>=110, H_{VCC} = 3.3V and P_{VCC} = 3.0V	--	400	--	ns
T_{ATTACH}	Attachment Transit Time	M<2:0>=111, H_{VCC} = 1.8V and P_{VCC} = 3.3V	--	400	--	ns

Notes: 1. External Capacitor is a 1µF or higher ceramic capacitor connected between the pin V_{BUS} and the pin GND and closest to V_{BUS} pin

7.4 V_{BUS} Supply Characteristics

Table 7-4. V_{BUS} Supply Monitor

Symbol	Parameter	Comments	Min	Typ	Max	Units
V_{BUS}	Input Supply Voltage Range	1µF ceramic capacitor (1)	4.0	5.0	5.5	V
V_{TP}	Positive Threshold		3.36	3.5	3.64	V
V_{TN}	Negative Threshold		3.02	3.15	3.28	V
V_{HYS}	Hysteresis		348	361	374	mV

Notes: 1. External Capacitor is a 1µF or higher ceramic capacitor connected between the pin V_{BUS} and the pin GND and closest to V_{BUS} pin

.

Table 7-5. V_{BUS} Current Consumption

Symbol	Parameter	Comments	Min	Typ	Max	Units
V_{BUS}	Input Supply Voltage Range	1µF ceramic capacitor (1)	4.0	5.0	5.5	V
I_{VBUS}	V_{BUS} Supply Current	V_{BUS} active • H_{VCC}= 3.3V nominal • 1.55V < P_{VRF} < 3.6V • Loads = 0mA • Idle	--	100	150	µA

Notes: 1. External Capacitor is a 1µF or higher ceramic capacitor connected between the pin V_{BUS} and the pin GND and closest to V_{BUS} pin.

7.5 H_{VCC} and P_{VCC} Supplies Characteristics

7.5.1 H_{VCC} and P_{VCC} Current Consumption

Table 7-6. P_{VCC} and H_{VCC} Current Consumption

Symbol	Parameter	Comments	Min	Typ	Max	Units
H_{VCC}	Host Supply Voltage		1.55	--	3.6	V
P_{VCC}	Peripheral Supply Voltage		1.55	--	3.6	V
I_{VCC}	X_{VCC} Supply Current	V_{BUS} = 0V, P_{VRF} = 0V • Loads = 0mA • Idle • H_{VCC} forced at 3.6V • P_{VCC} forced at 3.3V	--	--	5	µA

7.5.2 3.3V Supplied on H_{VCC}

When V_{BUS} is greater than 3.5V nominal, an internal LDO voltage regulator provides a 3.3V nominal voltage source on pin H_{VCC}.

Table 7-7. H_{VCC} LDO Characteristics

Symbol	Parameter	Comments	Min	Typ	Max	Units
H_{VCC} (1)	Output Voltage	- Enabled when V_{BUS} is greater than 3.5V typical. - Disabled when V_{BUS} goes below 3.15V typical	3.0	3.3	3.6	V
I_O	Output Current		0	--	70	mA
Δ_{VDD_IL}	Static Load Regulation	• V_{BUS} > 4.5V • I_O = 10% to 90%	--	--	10	mV
	Dynamic Load Regulation	• V_{BUS} > 4.5V • I_O = 10% to 90% • T_{RISE} = T_{FALL} = 5µs	--	50	--	mV
Δ_{VDD_VIN}	Static Line Regulation	• V_{BUS} from 4.3V to 5.5V • I_O = Max	--	--	20	mV
		• V_{BUS} from 4.0V to 5.5V • I_O = 7 mA	--	--	20	mV
T_{START}	Start-up Time	• V_{BUS} From 0V to 5.0V • T_{RISE} = 10µs • I_O = 0mA • V_{OUT} > 3.0V	--	--	60	µs

Notes: 1. When V_{BUS} is present and greater than V_{TP}, 10kΩ pull down is removed on H_{VCC} and on P_{VCC} and LDO are started. When V_{BUS} goes below V_{TP}, a 10kΩ pull down is connected on H_{VCC} and P_{VCC} and LDO are disabled. When V_{BUS} = 0V and H_{VCC} and P_{VCC} within their normal range the 10kΩ pull down are disconnected.

7.5.3 Voltage Supplied on P_{VCC}

When V_{BUS} is greater than 3.5V nominal, an internal LDO Follower provides a voltage source on pin P_{VCC}. The voltage on pin P_{VCC} is equal to the voltage on pin P_{VRF}.

P_{VCC} LDO is in accordance with FTA Test 3GPP - 27.17.2.1 dedicated for Subscriber Identity Module (SIM) application.

Table 7-8. P_{VCC} LDO Characteristics

Symbol	Parameter	Comments	Min	Typ	Max	Units
V_{BUS}	Supply Input Voltage	On pin V_{BUS}	4.0	5.0	5.5	V
P_{VCC} (1)	Output Voltage	- Enabled when V_{BUS} is greater than 3.5V typical. - Disabled when V_{BUS} goes below 3.15V typical - 1.55V < P_{VRF} < 3.6V	1.55	--	3.6	V
V_{OFF}	Follower Offset Voltage	P_{VCC} - P_{VRF}	-40	--	40	mV
I_O	Output Current		0	--	70	mA
Δ_{VDD_IL}	Static Load Regulation	• V_{BUS} > 4.5V • I_O = 10% to 90%	--	--	10	mV
	Dynamic Load Regulation	• V_{BUS} > 4.5V • I_O = 10% to 90% • T_{RISE} = T_{FALL} = 5µs	--	30	--	mV
Δ_{VDD_VIN}	Static Line Regulation	• V_{BUS} from 4.3V to 5.5V • I_O = Max	--	--	20	mV
		• V_{BUS} from 4.0V to 5.5V • I_O = 7 mA	--	--	20	mV
T_{START}	Start-up Time	• V_{BUS} is set at 5.0V • P_{VRF} 0V to 1.8V with T_{RISE} = 5µs • I_O = 10mA • V_{OUT} > 1.62V	--	20	35	µs
		• V_{BUS} is set at 5.0V • P_{VRF} 0V to 3.0V with T_{RISE} = 5µs • I_O = 10mA • V_{OUT} > 2.7V	--	32	50	µs
T_{STOP} (2)	Power-Off Time	• V_{BUS} is set at 5.0V • P_{VRF} 3.0V to 0V with T_{FALL} = 5µs • R_{LOAD} = 1KΩ. C_{OUT}=220nF/ X5R • V_{OUT} < 0.4V	--	--	525	µs
		• V_{BUS} is set at 5.0V • P_{VRF} 3.0V to 0V with T_{FALL} = 5µs • I_O = 7mA. C_{OUT}=220nF/ X5R • V_{OUT} < 0.4V	--	--	225	µs

Notes:
1. When V_{BUS} is present and greater than V_{TP}, 10kΩ pull down is removed on H_{VCC} and on P_{VCC} and LDO are started. When V_{BUS} goes below V_{TP}, a 10kΩ pull down is connected on H_{VCC} and P_{VCC} and LDO are disabled. When V_{BUS} = 0V and H_{VCC} and P_{VCC} within their normal range the 10kΩ pull down are disconnected.
2. Off time is described in Section 9.3.4 on page 16. To reduce T_{STOP} time an external reisitor is recommended. This value depends on C_{OUT} and load applied on the system.

8. Components List.

Table 8-1. AT73C260 External Components List

Component Name	Component Type	Value / Tol.	Reference	Reference
R_1, R_2	Resistor	33 Ω +/- 5%	CRG0402J33R	
R_3	Resistor	10 Ω +/- 5%	CRG0603J10R	
R_4	Resistor	10kΩ +/- 1%	CPF0402F10KE1	
R_5	Resistor	100kΩ +/- 1%	CPF0603F100KC1	
R_6, R_7	Resistor	22kΩ +/- 5%	CRG0402J22K	
C_1, C_2	Ceramic Capacitor COG	22pF +/- 20%	C1005COG1H220J	GRM1555C1H220JZ01
C_3	Ceramic Capacitor X5R	1µF +/- 20%	C1005X5R0J105K	GRM155R60J105KE19
C_4	Ceramic Capacitor X5R	220nF +/- 20%	C1005X5R1C224KT	GRM155R60J224KE01
C_5	Ceramic Capacitor X5R	220nF +/- 20%	C1005X5R1C224KT	GRM155R60J224KE01

9. Functional Description

9.1 AT73C260's Upstream and Downstream Ports

This section relates to either upstream or downstream ports with digital, IC_USB1.0 or USB2.0 section 7 electrical characteristics.

Table 9-1 shows the configuration of the upstream and downstream ports based on pins 14, 15 and 16 voltages.

- 0 is when the pin is connected to GND.
- 1 is when the pin is connected to H_{VCC}.

Table 9-1. Upstream and Downstream Ports

M<2> Pin 14	M<1> Pin 15	M<0> Pin 16	Upstream Port	Downstream Port
0	0	0	Digital	IC_USB1.0
0	0	1	Digital	IC_USB1.0
0	1	0	Digital	IC_USB1.0
0	1	1	Digital	IC_USB1.0
1	0	0	Not Used	Not Used
1	0	1	Digital	IC_USB1.0
1	1	0	Section 7	IC_USB1.0
1	1	1	IC_USB1.0	Section 7 [(1)] / IC_USB1.0

Notes: 1. P_{VCC} is set to 3.3V and external pull down resistors of 22kΩ ± 5% are connected, one between PDP and GND and the other between PDM and GND.

9.2 AT73C260 Pull Up and Pull Down Resistors

Pull down resistors $\mathbf{R_{PDP}}$ and $\mathbf{R_{PDH}}$ values and behaviors comply with the IC_USB1.0 specification published by the USB-IF.

9.2.1 AT73C260 Upstream Port Connectivity (H_{VCC}, H_{DP}, H_{DM}):

The host, IC_USB1.0 or USB2.0 section 7, is connected to the AT73C260's upstream port.

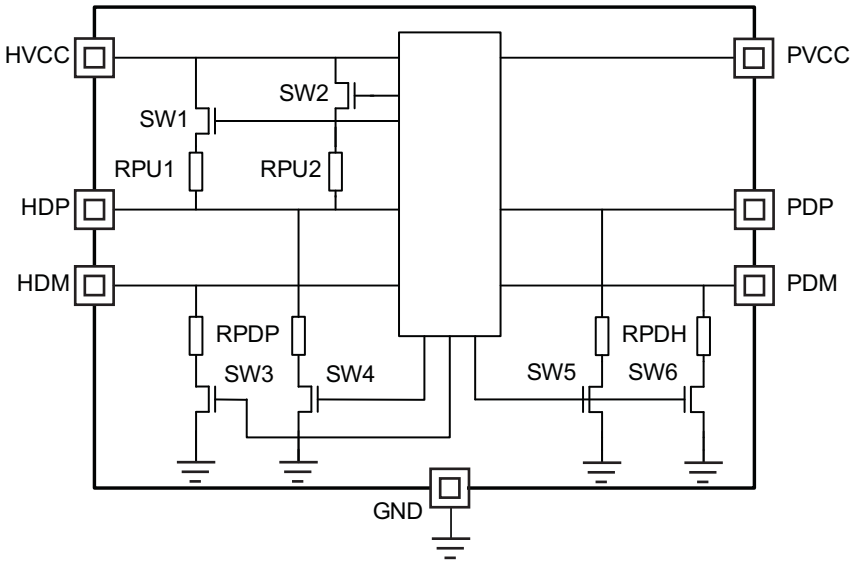
- When in IC_USB 1.0 $\mathbf{R_{PU2}}$ is selected.
- When in USB2.0 section 7 $\mathbf{R_{PU1}}$ is selected.

9.2.2 AT73C260 Downstream Port Connectivity (P_{VCC}, P_{DP}, P_{DM}):

The peripheral, IC_USB1.0 or USB2.0 section 7, is connected to the AT73C260's downstream port.

- An IC_USB1.0 peripheral is connected to the AT73C260's downstream port.
- An USB2.0 section 7 peripheral is connected to the AT73C260's downstream port with external pull down resistors as per precedent note [(1)] (See Table 9-1 on page 11).

Figure 9-1. AT73C260 Downstream and Upstream Ports



9.3 Theory Of Operation

9.3.1 Remote Wake Up

The AT73C260 does not support remote wake up.

9.3.2 Slew Rate Control

When the AT73C260 drives an IC_USB bus section the output buffer on each line (Figure 9-2) drives the pin with a slew rate control to minimize radiated EMI.

Figure 9-2. AT73C260 Output Buffer

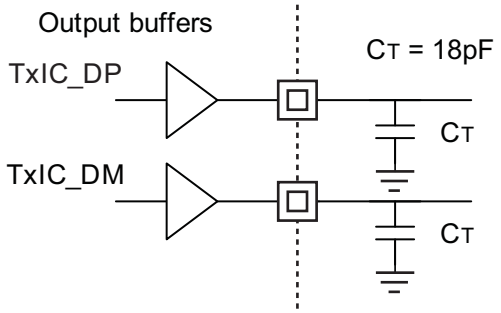
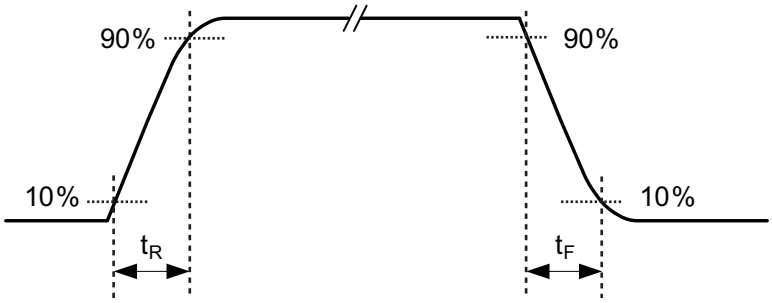


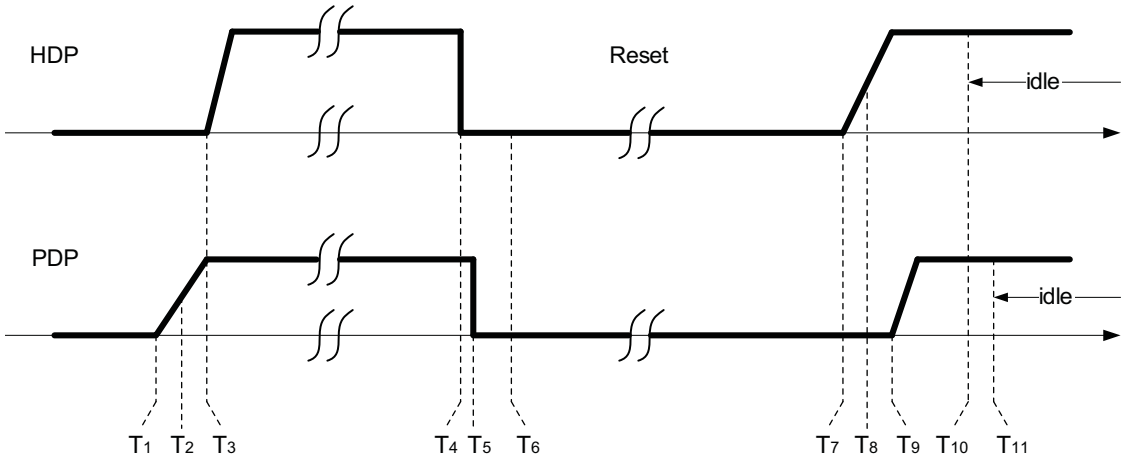
Figure 9-3. AT73C260 Output Buffer Slew Rate



Note: See Table 7-3 on page 7 for timing values.

9.3.3 Attach

Figure 9-4. AT73C260 Attach Sequence



In the following paragraphs, two different attach sequences are described according the mode selected. Mode VCC and Mode S7_ICC_TK are explained.

9.3.3.1 *Attach Sequence "Mode VCC"*

The following sequence describes the AT73C260 with an IC_USB upstream connection and an IC_USB downstream connection (**Mode VCC**). For hardware connection refers to "Mode: Voltage Class Converter: VCC" on page 34.

- H_{VCC} and P_{VCC} are present and are in their dedicated voltage range.
- R_{PU1} is not used (SW1 always open). (For more information about switches, refers to Figure 9-1 on page 12)
- Before T_1, R_{PDP} and R_{PDH} are connected. R_{PU2} is disconnected. (For more information about resistors, refers to Figure 9-1 on page 12)
- **T_1**: Peripheral event.

  Beyond T_1, PDP is driven high by the IC_USB peripheral's pull-up resistor.
- **T_2**: AT73C260 event.

  The signal is above V_{IH}. The AT73C260 verifies that the condition PDP is high lasts more than 200ns nominal. This information is passed to the AT73C260's Host side.
- **T_3**: AT73C260 event.

  Beyond T_3, R_{PU2} (2k nominal) is connected while R_{PDP} on HDP is disconnected.
- **T_4**: Host event.

  From T_4 the host drives the reset with SE0.
- **T_5**: AT73C260 event.

  It takes 40 ns nominal beyond T_4 for PDP to be driven low.
- **T_6**: AT73C260 event.

  During reset the AT73C260 detects a SE0 for more than 1µs nominal. Beyond T_6 both R_{PDH} are disconnected.

- **T_7**: Host event.

  Host stops driving SE0. The AT73C260 with its 2k nominal resistor, pulls-up HDP.

- **T_8**: AT73C260 event.

  The signal is above V_{IH}.(on HDP)

- **T_9**: AT73C260 event.

  40ns nominal after T_8. From T_9, the AT73C260 drives high until V_{IH} (on PDP) is reached plus 100ns nominal until T_{11}.

- **T_{10}**: AT73C260 event.

  Between T_7 and T_{10}. HDP is pulled-up with 2k nominal until V_{IH} (on HDP) is reached plus 100ns. At T_{10} R_{PU2} becomes 50k nominal.

9.3.3.2 *Attach Sequence Mode S7_ICC_TK*

The following sequence describes the AT73C260 with an USB2.0 section 7 upstream connection and an IC_USB downstream connection (**Mode S7_ICC_TK**). For hardware connection refers to “Mode: USB2.0 section 7 to IC_USB1.0 with PVCC fixed by PVRF: S7_ICC_TK” on page 38.

- H_{VCC} = 3.3V and P_{VCC} are present and are in their dedicated voltage range.
- R_{PU2} is not used (SW2 always open). R_{PDP} are not used (SW3 and SW4 always open).(For more information about switches, refers to Figure 9-1 on page 12)
- Before T_1, R_{PDH} are connected. R_{PU2} is disconnected. (For more information about resistors, refers to Figure 9-1 on page 12)
- **T_1**: Peripheral event.

  Beyond T_1, PDP is driven high by the IC_USB peripheral’s pull-up resistor.

- **T_2**: AT73C260 event.

  The signal is above V_{IH}. The AT73C260 verifies that the condition PDP is high lasts more than 200ns nominal. This information is passed to the AT73C260’s Host side.

- **T_3**: AT73C260 event.

  Beyond T_3, R_{PU1} 1.2k nominal, is connected.

- **T_4**: Host event.

  From T_4 the host drives the reset with SE0.

- **T_5**: AT73C260 event.

  R_{PU1} becomes 2.2k nominal. It takes 40 ns nominal beyond T_4 for PDP to be driven low.

- **T_6**: AT73C260 event.

  During reset the AT73C260 detects a SE0 for more than 1µs nominal. Beyond T_6 both R_{PDH} are disconnected.

- **T_7**: Host event.

  Host stops driving SE0. The AT73C260 with its 2k nominal resistor, pulls-up HDP.

- **T_8**: AT73C260 event.

  The signal is above V_{IH}.(on HDP)

- **T_9**: AT73C260 event.

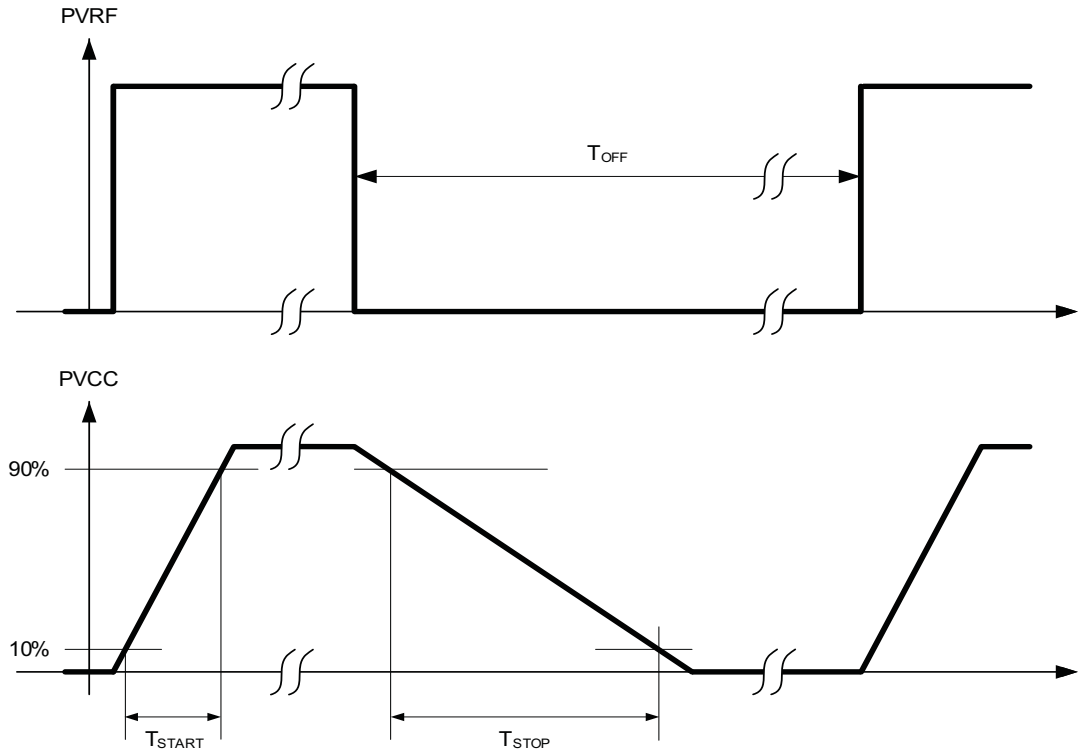
  40ns nominal after T_8. From T_9, the AT73C260 drives high until V_{IH} (on PDP) is reached plus 100ns nominal until T_{11}.

- **T_{10}**: AT73C260 event.

  Between T_7 and T_{10}. HDP is pulled-up with 2.2k nominal until V_{IH} (on HDP) is reached plus 100ns. At T_{10} R_{PU1} becomes 1.2k nominal.

9.3.4 PVRF Driving PVCC

Figure 9-5. AT73C260 PVRF driving PVCC



When V_{BUS}, pin 4, is providing power to the USB UICC via the LDOs, the voltage on P_{VCC} (pin 12) is following the voltage on P_{VRF} (pin 9).

T_{START} is mostly related to the capacitive load on P_{VCC} and the strength of the LDO's PMOS.

T_{START} as mentioned in Table 7-8 on page 9 is less than 50µs.

T_{STOP} is mostly related to the load on P_{VCC} since the LDO's PMOS is off when starts T_{OFF}.

Certain applications may require P_{VCC} to fall below a minimum voltage in less than T_{OFF} and guarantee a Power On Reset sequence in the USB UICC when P_{VCC} is set again. For these applications an extra load, such as a resistor across P_{VCC} and GND in parallel with the USB UICC and the decoupling capacitor C5 may be required.

As an example, for T_{OFF} = 0.4ms, a decoupling capacitor C5 of 220nF and an USB UICC in standby (less than 100µA) the extra resistor shall be less than 1kΩ.

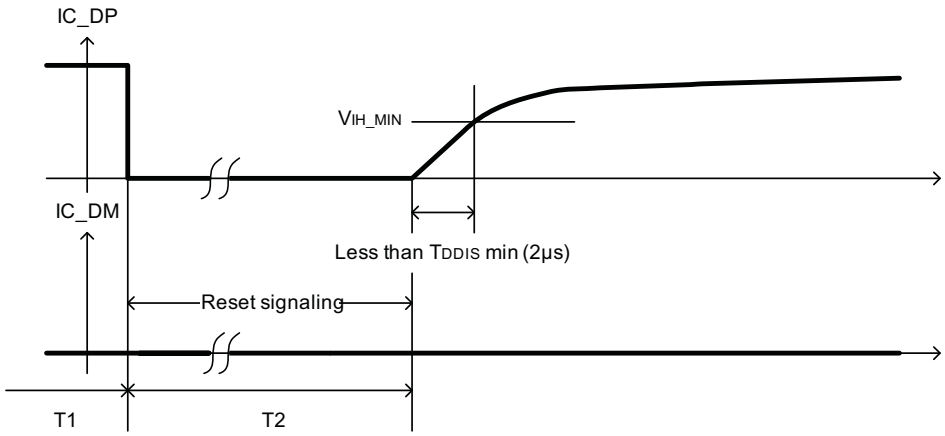
9.3.5 Reset Signaling

At the end of the Reset signaling on AT73C260's host side and peripheral sides the pulled up data line voltage has to reach V_{IH_MIN} in less than T_{DDIS}, see Figure 9-6. If it is not the case, the host may see a disconnect condition.

Reset is forced during T2.

If a 100kΩ pull up resistor is used while the capacitive load is more than 20pF, the time constant is greater than 2µs. To avoid any disconnect condition, the AT73C260 pulls up the appropriate data line during about one bit duration with extra strength making the disconnect condition unlikely.

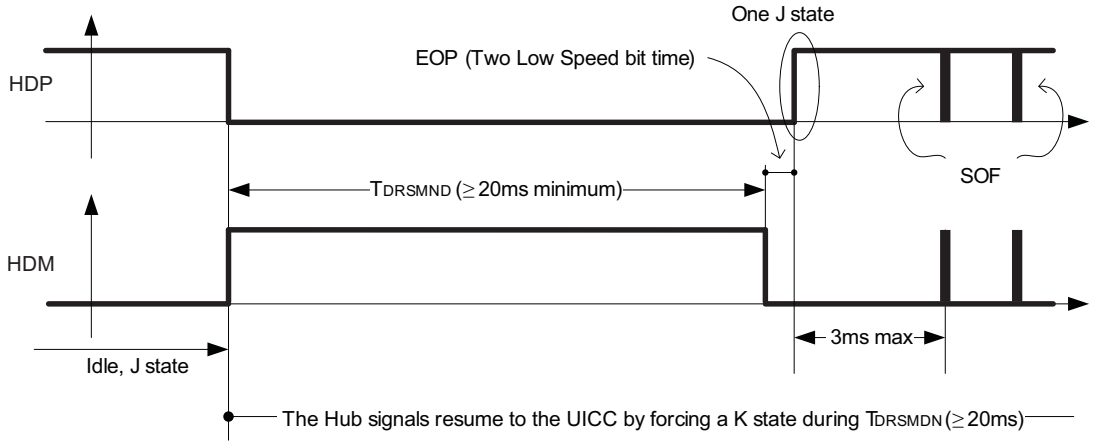
Figure 9-6. AT73C260 Reset Signaling



9.3.6 Resume Signaling

The AT73C260 supports resume signaling. The timings on IC_DP and IC_DM are those on HDP and HDM delayed by 40ns nominal.

Figure 9-7. AT73C260 Resume Signaling



Notes:
1. J state means that HDP = 1 and HDM = 0.
2. K state means that HDP = 0 and HDM = 1.
3. SOF = Start Of Frame

9.4 General Description

The AT73C260 covers four main functions:

- PHY (described in Section 9.4.3 on page 20)
- Bridge (described in Section 9.4.4 on page 30)
- IC_USB1.0 Voltage Class Converter (described in Section 9.4.5 on page 34)
- Bridge with LDOs for two specific applications (described in Section 9.4.6 on page 36),

and one extra function from many described as an example where the AT73C260 is an inter-chip PHY in a digital implementation (FPGA) of a peripheral.

9.4.1 Application Modes

The following Table 9-2 lists the applications and pin settings.

Table 9-2. AT73C260 Application Modes [4]

Mode	Application	M<2> Pin 14	M<1> Pin 15	M<0> Pin 16	Function
PHY_6_SE0	Digital six wires unidirectional DAT_SE0 to IC_USB1.0	0	0	0	PHY
PHY_4_SE0	Digital four wires bidirectional DAT_SE0 to IC_USB1.0	0	0	1	PHY
PHY_6_DPDM	Digital six wires unidirectional DP_DM to IC_USB1.0	0	1	0	PHY
PHY_4_DPDM	Digital four wires bidirectional DP_DM to IC_USB1.0	0	1	1	PHY
PHY_3_ULPI	Digital three wires bidirectional (DAT, SE0, OE_N) to IC_USB1.0	1	0	1	PHY
S7_ICC	USB2.0 section 7 without cable to IC_USB1.0	1	1	0	Bridge
S7_ICC_DBB	USB2.0 section 7 with cable to IC_USB1.0, LDOs ON VCC driven by the Digital Base Band [2]	1	1	0	Bridge with LDOs
S7_ICC_TK	USB2.0 section 7 with cable to IC_USB1.0, LDOs ON VCC fixed by PVRF [3]	1	1	0	Bridge with LDOs
ICC_S7	IC_USB1.0 to USB2.0 section 7 [1]	1	1	1	Bridge
VCC	IC_USB1.0 to IC_USB1.0	1	1	1	Voltage Class Converter

Notes:
1. 22kΩ Pull down on pins 10 and 11
2. PC with Digital Base Band
3. Token
4. M<2:0> code”100” is not used

9.4.2 Function Descriptions

9.4.2.1 Downstream Port PHY:

A set of digital signals generated by an FPGA or an ASIC with I/O powered by a first power supply drive the AT73C260 which converts these signals into analog signals IC_DP and IC_DM as per IC_USB1.0 powered by a second power supply.

9.4.2.2 Bridge:

Two cases are supported: USB2.0 section 7 to IC_USB1.0 and IC_USB1.0 to USB2.0 section 7.

- USB2.0 section 7 to IC_USB1.0

Downstream D+ and D- signals drive the AT73C260 which converts these signals into analog signals IC_DP and IC_DM as per IC_USB1.0.

- IC_USB1.0 to USB2.0 section 7

Downstream IC_USB1.0 signals drive the AT73C260 which converts these signals into analog signals D+ and D- as per USB2.0 section 7.

9.4.2.3 Voltage Class Converter:

The following applications enable communications between an IC_USB1.0 compliant downstream port with a first voltage class V_1 and an IC_USB1.0 compliant peripheral with a second voltage class V_{CC}.

The range of the supplies, respectively Host and Device, are: H_{VCC} (1.55V - 3.6V) and P_{VCC} (1.55V - 3.6V)

9.4.2.4 Bridge with LDOs:

Two cases are supported: one for PC with embedded Digital Base Band and one for Token.

- PC with embedded Digital Base Band

The AT73C260 provides up to 70mA from V_{BUS} to the UICC under the V_{CC} required by the DBB.

Also the AT73C260 converts D+ and D- signals into analog signals IC_DP and IC_DM as per IC_USB1.0.

- Token

The AT73C260 provides up to 70mA from V_{BUS} to the UICC under V_{CC}.

This voltage is generated by P_{VCC} LDO and set by an external resistor bridge supplied by 3.3V voltage reference (H_{VCC}).

Also the AT73C260 converts D+ and D- signals into analog signals IC_DP and IC_DM as per IC_USB1.0.

9.4.3 Downstream Port PHY

In mobile applications, the USB UICC is handled by the user and special care should be taken in the ESD protection on the downstream port facing the USB UICC. The AT73C260 downstream port is protected against 4kV ESD.

Also, the host and the USB UICC may not be located on the same board with a flex connecting the two PCBs. The AT73C260 should be located next to the host. The flex is between the AT73C260's downstream port and the USB UICC upstream port. The AT73C260 downstream port has slew rate control on both P_{DM} and P_{DP} to minimize the radiated EMI.

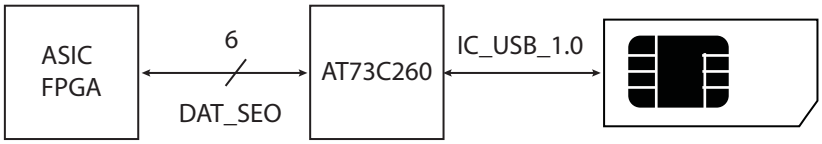
Pins V_{BUS} and P_{VRF} are connected to GND and LDO outputs are isolated and in standby.

9.4.3.1 Mode: Digital six wires unidirectional DAT_SE0 to IC_USB1.0: PHY_6_SE0

Description

This application allows a Host, ASIC or FPGA, with the digital unidirectional Philips PDIUSBP11A (MODE pin = 0) six wires interface to drive an IC_USB downstream port.

Figure 9-8. PHY_6_SE0 Block Diagram



Hardware Configuration

In the following tables, the pin and the hardware configuration are described.

Table 9-3. AT73C260 Hardware Configuration

Mode	M<2> Pin 14	M<1> Pin 15	M<0> Pin 16	Application
PHY_6_SE0	0	0	0	Digital six wires unidirectional DAT_SE0 to IC_USB1.0

Table 9-4. AT73C260 Pin description and configuration

Pin Number	Pin Name	I/O Type	Polarity	Function
1	HVCC	A-Power	--	Supply by ASIC FPGA I/O Ring (1.55V to 3.6V)
2	TX_DAT	D-Input	--	Unidirectional Transmit Data
3	TX_SEO	D-Input	--	Unidirectional Transmit Single Ended 0
4	VBUS	A-Input	--	Not Used and Connected to Ground
6	RX_DM	D-Output	--	Unidirectional Receiving DM
7	RX_DP	D-Output	--	Unidirectional Receiving DP
8	TX_ENABLE_N	D-Input	Low	Tx Enable N
9	PVRF	A-Input	--	Connected to Ground
10	PDM	D-I/O	--	Downstream Port for USB Device

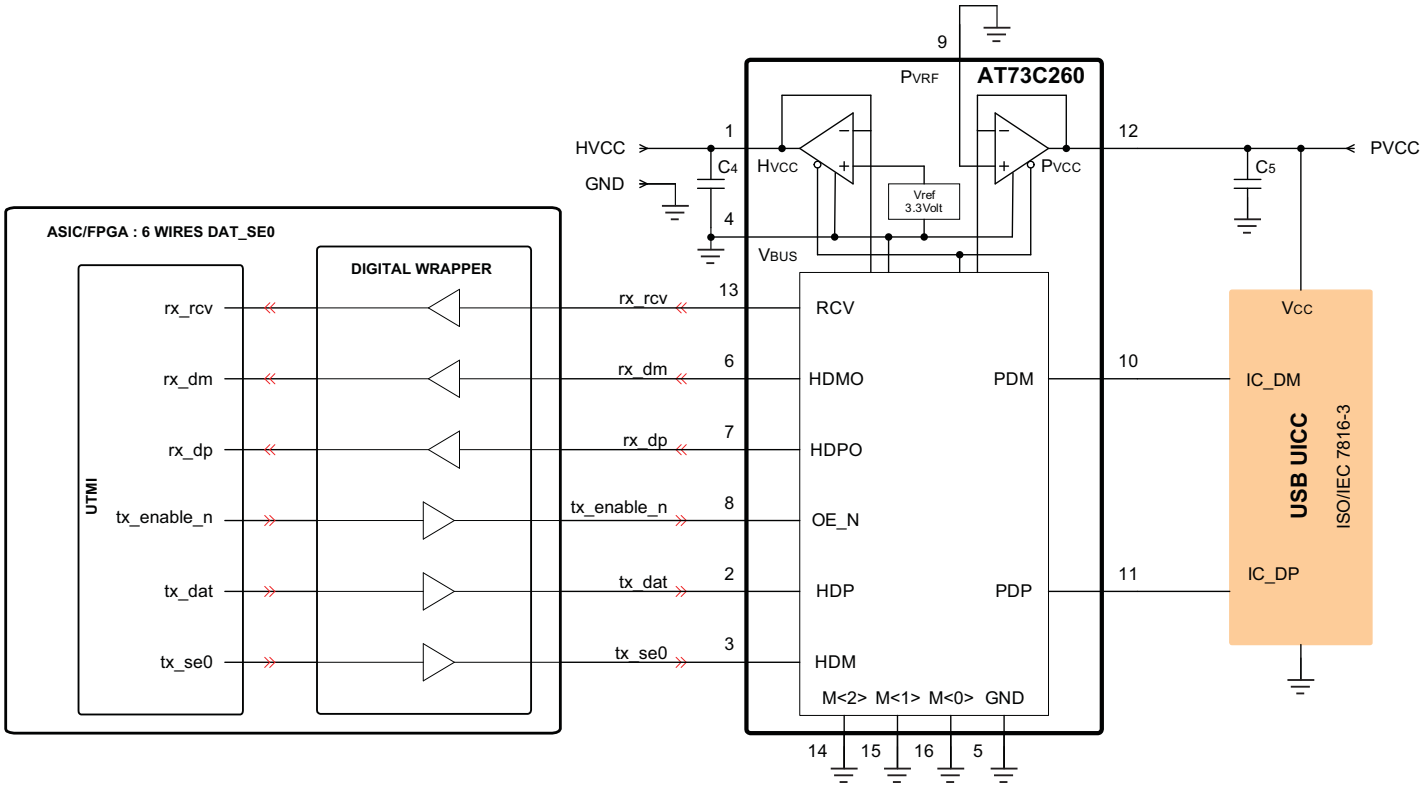
Table 9-4. AT73C260 Pin description and configuration

Pin Number	Pin Name	I/O Type	Polarity	Function
11	PDP	D-I/O	--	Downstream Port for USB Device
12	PVCC	A-Power	--	Same as peripheral's power (1.8V or 3V typical)
13	RX_RCV	D-Output	--	Unidirectional Receiving RCV
14, 15, 16	M<2:0>	D-Inputs	Low	Connected to Ground

Application Diagram

In the following figure, the hardware configuration is described.

Figure 9-9. AT73C260: PHY - 6 wires DAT_SE0 to IC_USB1.0 - application diagram



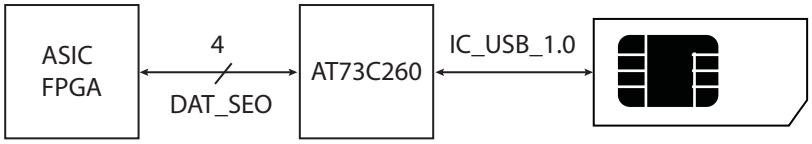
Note: All external components are defined in component list Table 8-1 on page 10

9.4.3.2 Mode: Digital four wires bidirectional DAT_SE0 to IC_USB1.0: PHY_4_SE0

Description

This application allows a Host, ASIC or FPGA, with the digital bidirectional UTMIfs, DAT_SE0, four wires interface to drive an IC_USB downstream port.

Figure 9-10. PHY_4_SE0 Block Diagram



Hardware Configuration

In the following tables, the pin and the hardware configuration are described.

Table 9-5. AT73C260 Hardware Configuration

Mode	M<2> Pin 14	M<1> Pin 15	M<0> Pin 16	Application
PHY_4_SE0	0	0	H_{VCC}	Digital four wires bidirectional DAT_SE0 to IC_USB1.0

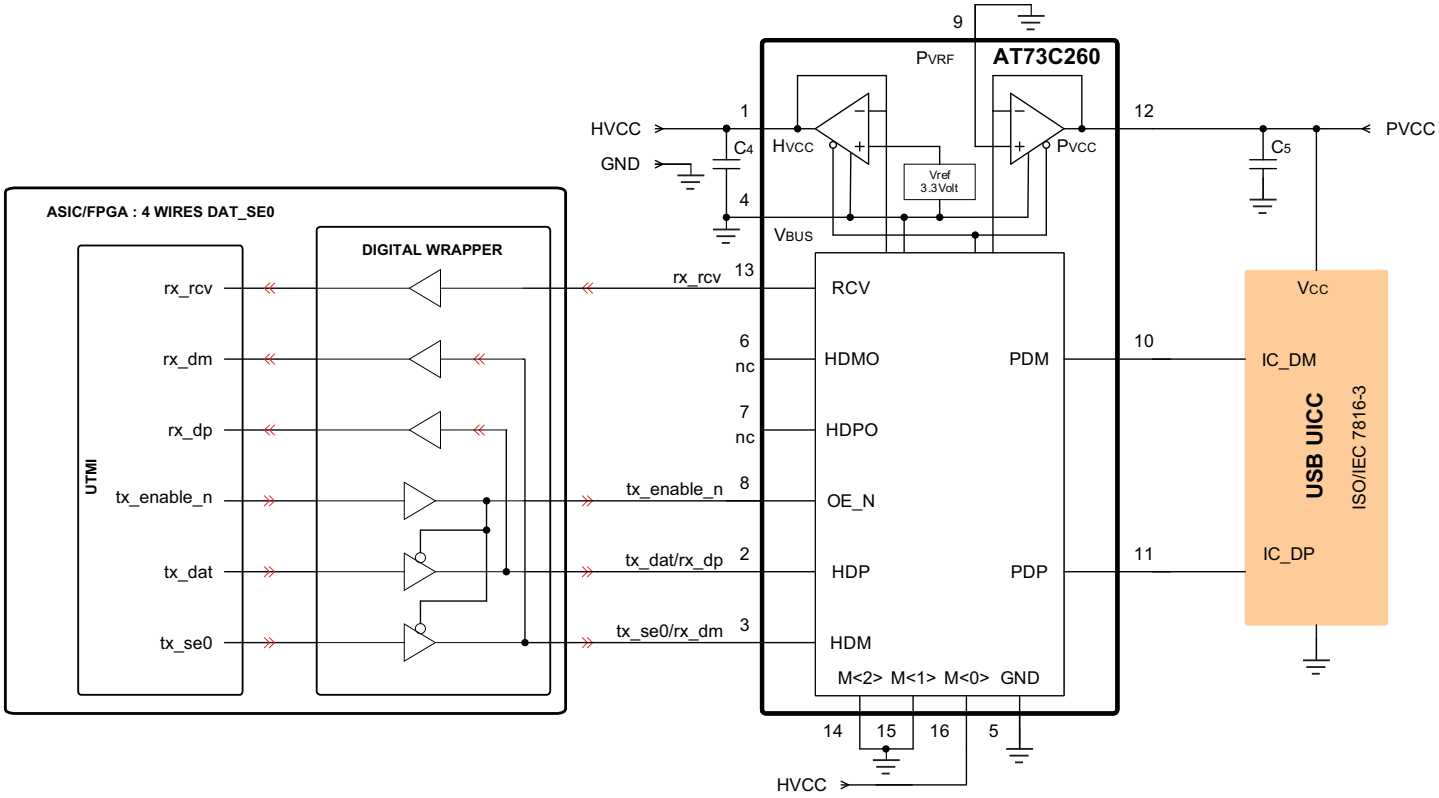
Table 9-6. AT73C260 Pin description and configuration

Pin Number	Pin Name	I/O Type	Polarity	Function
1	HVCC	A-Power	--	Supply by ASIC FPGA I/O Ring (1.55V to 3.6V)
2	TX_DAT/RX_DP	D-I/O	--	Bidirectional Rx_Dp/Tx_Data
3	TX_SE0/RX_DM	D-I/O	--	Bidirectional Rx_DM/Tx_Single Ended 0
4	VBUS	A-Input	--	Not Used and Connected to Ground
6	HDMO	D-Output	HiZ	Not Connected
7	HDPO	D-Output	HiZ	Not Connected
8	TX_ENABLE_N	D-Input	Low	Tx Enable N
9	PVRF	A-Input	--	Connected to Ground
10	PDM	D-I/O	--	Downstream Port for USB Device
11	PDP	D-I/O	--	Downstream Port for USB Device
12	PVCC	A-Power	--	Same as peripheral's power (1.8V or 3V typical)
13	RX_RCV	D-Output	--	Unidirectional Receiving RCV
14, 15	M<2:1>	D-Inputs	Low	Connected to Ground
16	M<0>	D-Input	High	Connected to H_{VCC}

Application Diagram

In the following figure, the hardware configuration is described.

Figure 9-11. AT73C260: PHY - 4 wires DAT_SE0 to IC_USB1.0 - application diagram



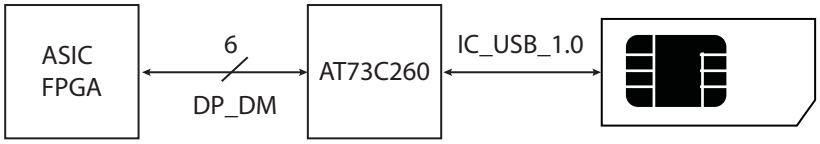
Note: All external components are defined in component list Table 8-1 on page 10

9.4.3.3 Mode: Digital six wires unidirectional DP_DM to IC_USB1.0: PHY_6_DPDM

Description

This application allows a Host, ASIC or FPGA, with the digital unidirectional Philips PDIUSBP11A (MODE pin = 1) six wires interface to drive an IC_USB downstream port.

Figure 9-12. PHY_6_DPDM Block Diagram



Hardware Configuration

In the following tables, the pin and the hardware configuration are described.

Table 9-7. AT73C260 Hardware Configuration

Mode	M<2> Pin 14	M<1> Pin 15	M<0> Pin 16	Application
PHY_6_DPDM	0	H_{VCC}	0	Digital six wires unidirectional DP_DM to IC_USB1.0

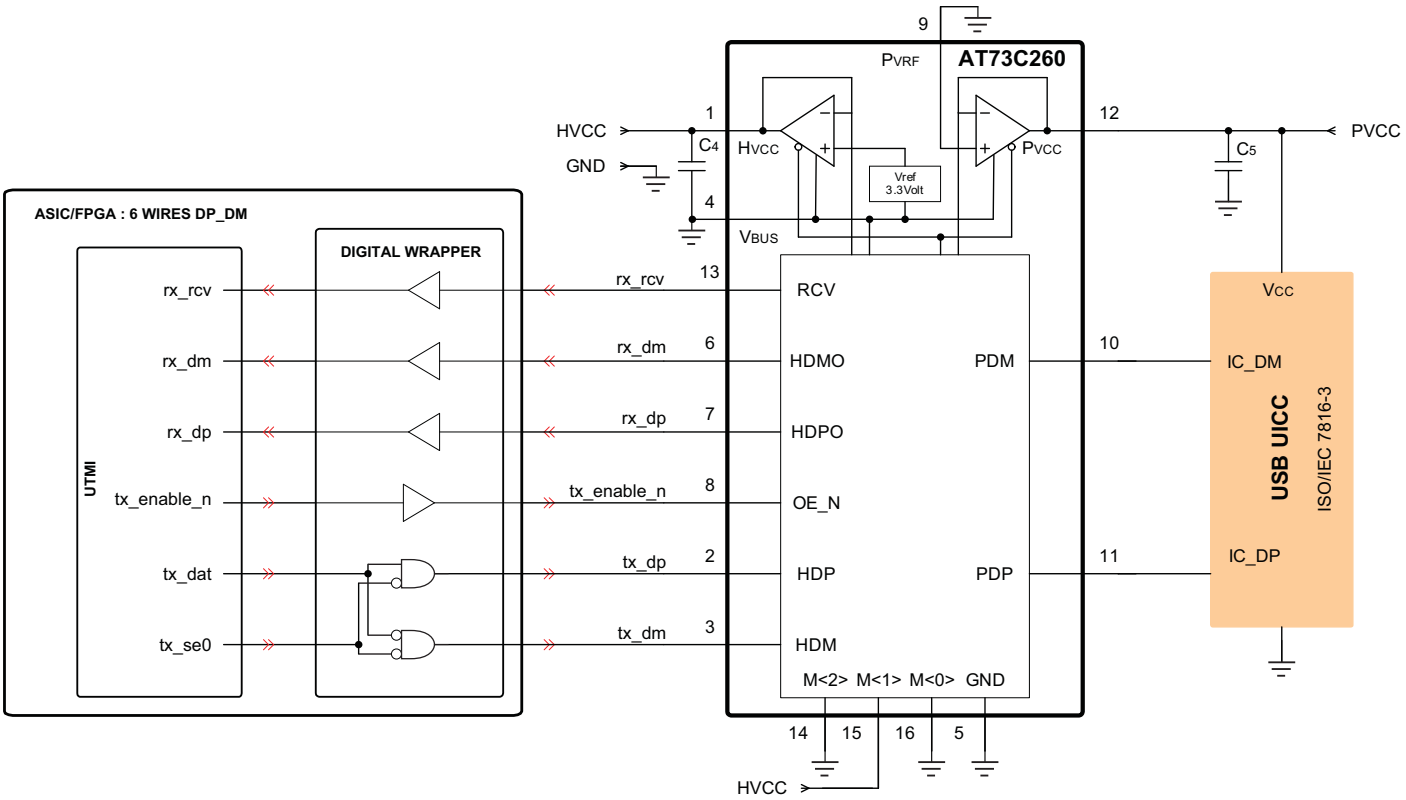
Table 9-8. AT73C260 Pin description and configuration

Pin Number	Pin Name	I/O Type	Polarity	Function
1	HVCC	A-Power	--	Supply by ASIC FPGA I/O Ring (1.55V to 3.6V)
2	TX_DP	D-Input	--	Unidirectional Tx DP
3	TX_DM	D-Input	--	Unidirectional Tx DM
4	VBUS	A-Input	--	Not Used and Connected to Ground
6	RX_DM	D-Output	--	Unidirectional Rx DM
7	RX_DP	D-Output	--	Unidirectional Rx DP
8	TX_ENABLE_N	D-Input	Low	Tx Enable N
9	PVRF	A-Input	--	Connected to Ground
10	PDM	D-I/O	--	Downstream Port for USB Device
11	PDP	D-I/O	--	Downstream Port for USB Device
12	PVCC	A-Power	--	Same as peripheral's power (1.8V or 3V typical)
13	RX_RCV	D-Output	--	Unidirectional Receiving RCV
14	M<2>	D-Input	Low	Connected to Ground
15	M<1>	D-Input	High	Connected to H_{VCC}
16	M<0>	D-Input	Low	Connected to Ground

Application Diagram

In the following figure, the hardware configuration is described.

Figure 9-13. AT73C260: PHY - 6 wires DP_ DM to IC_USB1.0 - application diagram



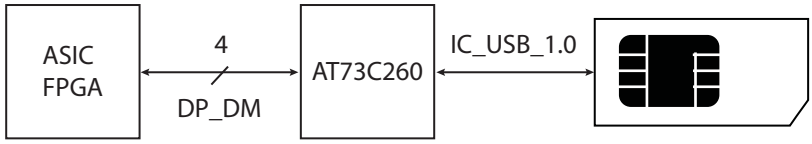
Note: All external components are defined in component list Table 8-1 on page 10

9.4.3.4 Mode: Digital four wires bidirectional DP_DM to IC_USB1.0: PHY_4_DPDM

Description

This application allows a Host, ASIC or FPGA, with the digital bidirectional UTMIfs, DP_DM, four wires interface to drive an IC_USB downstream port.

Figure 9-14. PHY_4_DPDM Block Diagram



Hardware Configuration

In the following tables, the pin and the hardware configuration are described.

Table 9-9. AT73C260 Hardware Configuration

Mode	M<2> Pin 14	M<1> Pin 15	M<0> Pin 16	Application
PHY_4_DPDM	0	H_{VCC}	H_{VCC}	Digital four wires bidirectional DP_DM to IC_USB1.0

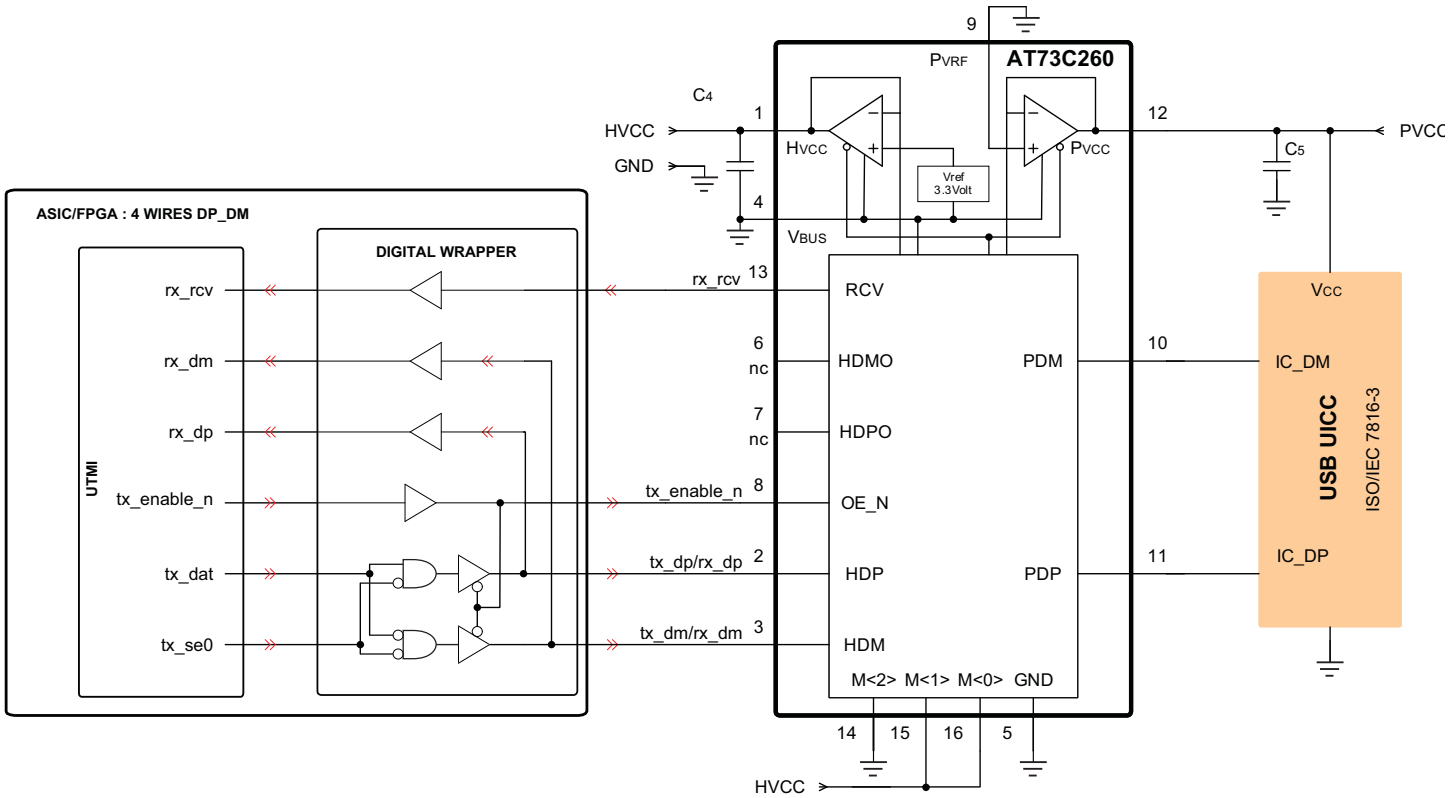
Table 9-10. AT73C260 Pin description and configuration

Pin Number	Pin Name	I/O Type	Polarity	Function
1	HVCC	A-Power	--	Supply by ASIC FPGA I/O Ring (1.55V to 3.6V)
2	TX_DP/RX_DP	D-I/O	--	Bidirectional Tx_Dp/Dx_DP
3	TX_DM/RX_DM	D-I/O	--	Bidirectional Tx_Dm/Dx_DM
4	VBUS	A-Input	--	Not Used and Connected to Ground
6	HDMO	D-Output	HiZ	Not Connected
7	HDPO	D-Output	HiZ	Not Connected
8	TX_ENABLE_N	D-Input	Low	Tx Enable N
9	PVRF	A-Input	--	Connected to Ground
10	PDM	D-I/O	--	Downstream Port for USB Device
11	PDP	D-I/O	--	Downstream Port for USB Device
12	PVCC	A-Power	--	Same as peripheral's power (1.8V or 3V typical)
13	RX_RCV	D-Output	--	Unidirectional Receiving RCV
14	M<2>	D-Input	Low	Connected to Ground
15,16	M<1:0>	D-Inputs	High	Connected to H_{VCC}

Application Diagram

In the following figure, the hardware configuration is described.

Figure 9-15. AT73C260: PHY - 4 wires DP_ DM to IC_USB1.0 - application diagram



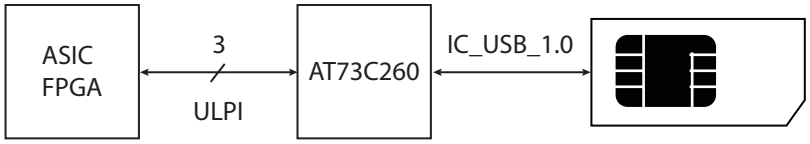
Note: All external components are defined in component list Table 8-1 on page 10

9.4.3.5 Mode: Digital three wires bidirectional (DAT, SE0, OE_N) to IC_USB1.0: PHY_3_ULPI

Description

This application allows a Host, ASIC or FPGA, with the digital bidirectional ULPI serial support, DAT, SE0, and OE_N, three wires interface to drive an IC_USB downstream port.

Figure 9-16. PHY_3_ULPI Block Diagram



Hardware Configuration

In the following tables, the pin and the hardware configuration are described.

Table 9-11. AT73C260 Hardware Configuration

Mode	M<2> Pin 14	M<1> Pin 15	M<0> Pin 16	Application
PHY_3_ULPI	H_{VCC}	0	H_{VCC}	Digital three wires bidirectional DAT, SE0, OE_N to IC_USB1.0

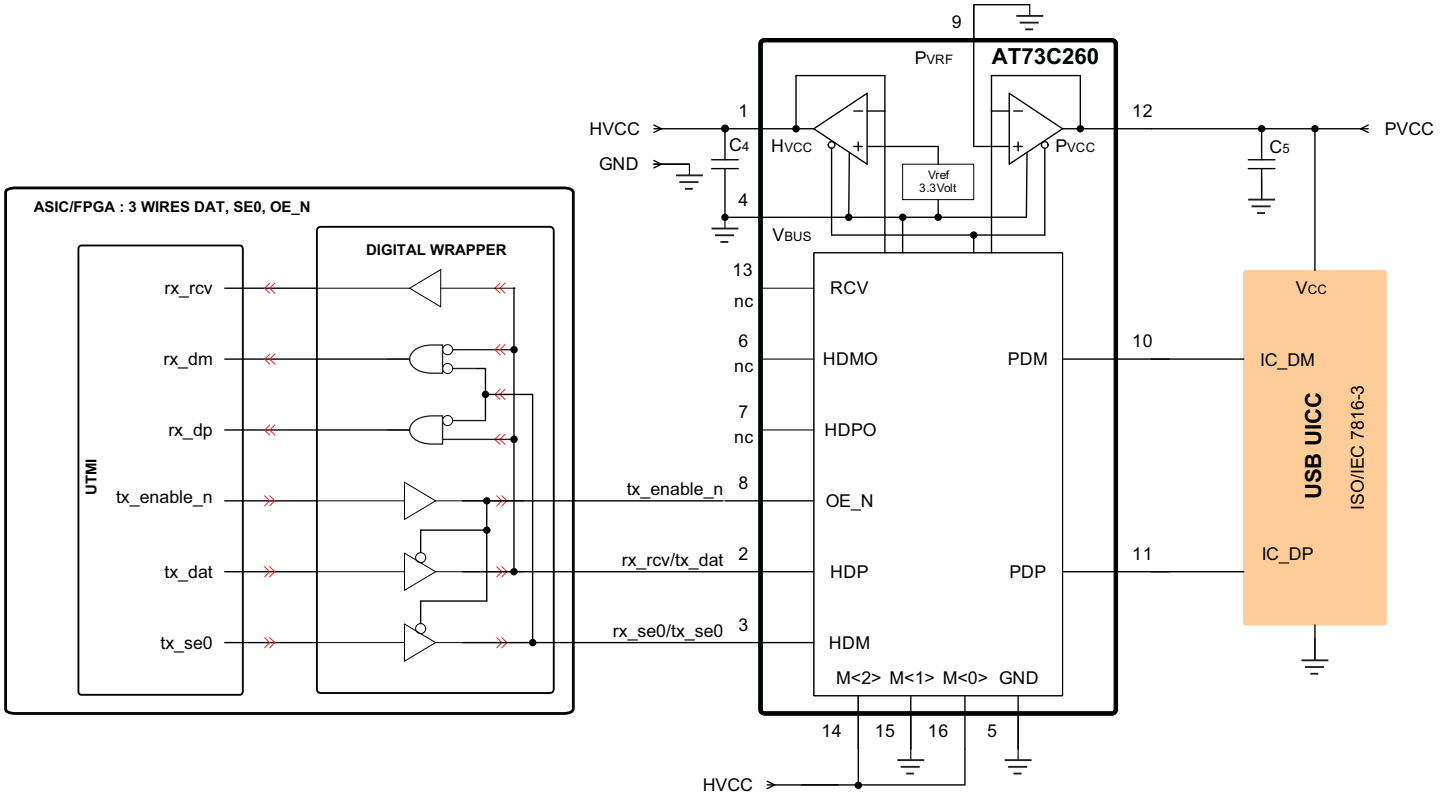
Table 9-12. AT73C260 Pin description and configuration

Pin Number	Pin Name	I/O Type	Polarity	Function
1	HVCC	A-Power	--	Supply by ASIC FPGA I/O Ring (1.55V to 3.6V)
2	RX_RCV/TX_DAT	D-I/O	--	Bidirectional Rx_RCV / Tx_Data
3	RX_SE0/TX_SE0	D-I/O	--	Bidirectional Rx_SE0/Tx_SE0
4	VBUS	A-Input	--	Not Used and Connected to Ground
6	HDMO	D-Output	HiZ	Not Connected
7	HDPO	D-Output	HiZ	Not Connected
8	TX_ENABLE_N	D-Input	Low	Tx Enable N
9	PVRF	A-Input	--	Connected to Ground
10	PDM	D-I/O	--	Downstream Port for USB Device
11	PDP	D-I/O	--	Downstream Port for USB Device
12	PVCC	A-Power	--	Same as peripheral's power (1.8V or 3V typical)
13	RCV	D-Output	HiZ	Not Connected
14	M<2>	D-Input	High	Connected to H_{VCC}
15	M<1>	D-Inputs	Low	Connected to Ground
16	M<0>	D-Inputs	High	Connected to H_{VCC}

Application Diagram

In the following figure, the hardware configuration is described.

Figure 9-17. AT73C260: PHY - 3 wires DAT, SE0, OE_N to IC_USB1.0 - application diagram



Note: All external components are defined in component list Table 8-1 on page 10

9.4.4 Bridge

Pins V_{BUS} and P_{VRF} are connected to GND and LDO outputs are isolated and in standby.

Pin OE_N is connected to H_{VCC}.

The following applications enable communications between.

- **S7_ICC**: an USB2.0 section 7 compliant downstream port and an IC_USB1.0 compliant peripheral
- **ICC_S7**: an IC_USB1.0 compliant downstream port and an USB2.0 section 7 compliant peripheral

9.4.4.1 Mode: USB2.0 section 7 downstream port to IC_USB1.0 peripheral: S7_ICC

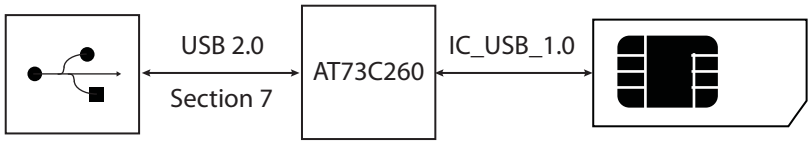
Description

This application establishes a communication path between an USB2.0 section 7 downstream port and an IC_USB peripheral.

An external 3.3V voltage source is applied on H_{VCC}. AT73C260's D+ and D- input pins are compliant with USB2.0 core specification.

This application is particularly well suited for mobile devices where the host may not have an IC_USB1.0 downstream port.

Figure 9-18. S7_ICC Block Diagram



Hardware Configuration

In the following tables, the pin and the hardware configuration are described.

Table 9-13. AT73C260 Hardware Configuration

Mode	M<2> Pin 14	M<1> Pin 15	M<0> Pin 16	Application
S7_ICC	H_{VCC}	H_{VCC}	0	USB2.0 section 7 downstream port to IC_USB1.0 peripheral

Table 9-14. AT73C260 Pin description and configuration

Pin Number	Pin Name	I/O Type	Polarity	Function
1	HVCC	A-Power	--	Supplied by host at 3.3V
2	D+	D-I/O	--	Bidirectional D+
3	D-	D-I/O	--	Bidirectional D-
4	VBUS	A-Input	--	Not Used and Connected to Ground
6	HDMO	D-Output	HiZ	Not Connected
7	HDPO	D-Output	HiZ	Not Connected
8	OE_N	D-Input	High	Connected to H_{VCC}

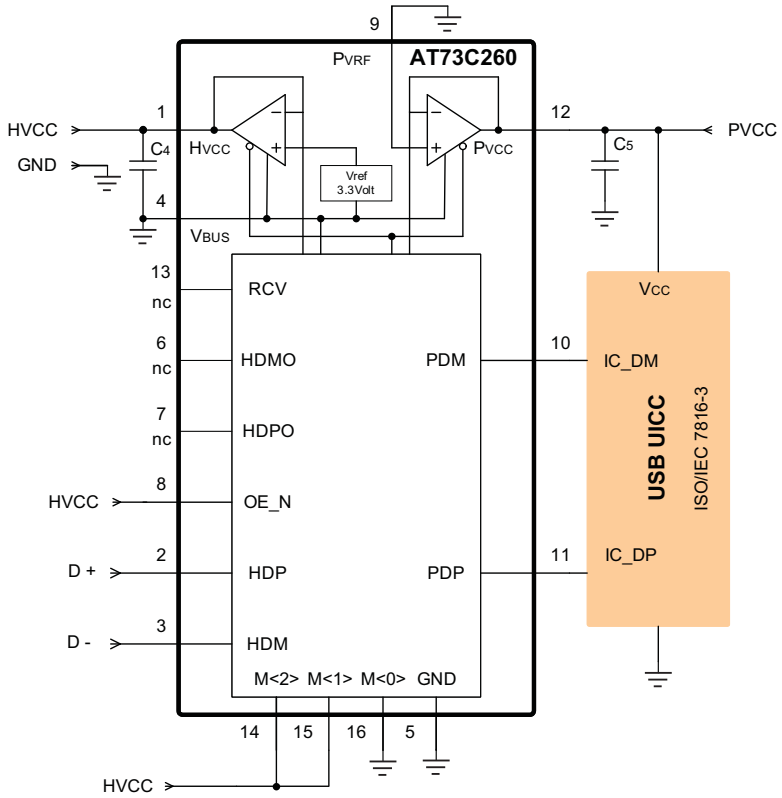
Table 9-14. AT73C260 Pin description and configuration

Pin Number	Pin Name	I/O Type	Polarity	Function
9	PVRF	A-Input	--	Connected to Ground
10	PDM	D-I/O	--	Downstream Port for USB Device
11	PDP	D-I/O	--	Downstream Port for USB Device
12	PVCC	A-Power	--	Same as peripheral's power (1.8V or 3V typical)
13	RCV	D-Output	HiZ	Not Connected
14	M<2>	D-Input	High	Connected to H_{VCC}
15	M<1>	D-Inputs	High	Connected to H_{VCC}
16	M<0>	D-Inputs	Low	Connected to Ground

Application Diagram

In the following figure, the hardware configuration is described.

Figure 9-19. AT73C260: Bridge - USB2.0 section 7 downstream port to IC_USB1.0 -application diagram



Note: All external components are defined in component list Table 8-1 on page 10

9.4.4.2 Mode: IC_USB1.0 downstream port to USB2.0 section 7 peripheral: ICC_S7

Description

This application establishes a communication path between an IC_USB1.0 downstream port and an USB2.0 section 7 peripheral.

Figure 9-20. ICC_S7 Block Diagram

Hardware Configuration

In the following tables, the pin and the hardware configuration are described.

Table 9-15. AT73C260 Hardware Configuration

Mode	M<2> Pin 14	M<1> Pin 15	M<0> Pin 16	Application
ICC_S7	H_{VCC}	H_{VCC}	H_{VCC}	IC_USB1.0 downstream port to USB2.0 section 7 peripheral

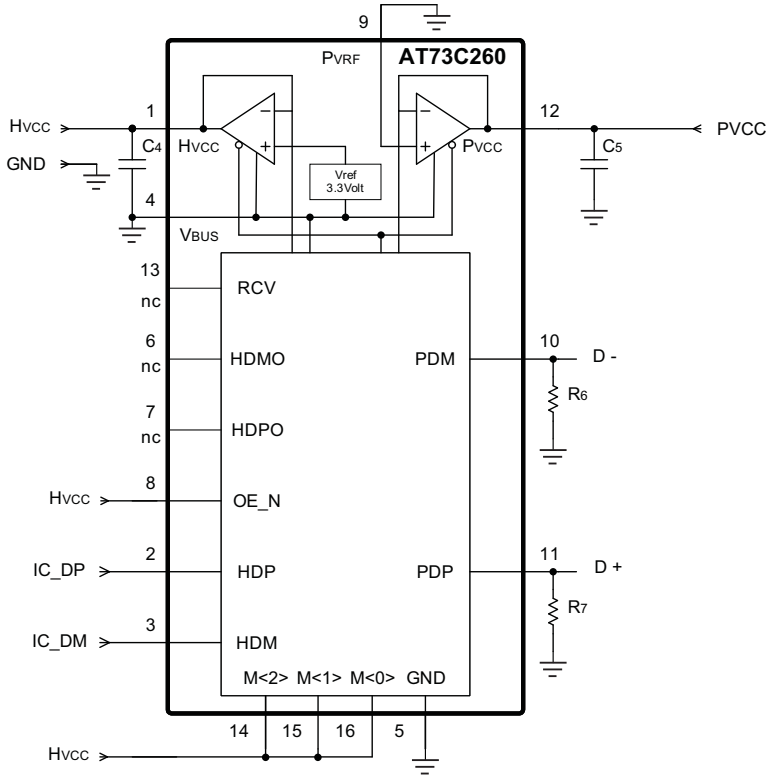
Table 9-16. AT73C260 Pin description and configuration

Pin Number	Pin Name	I/O Type	Polarity	Function
1	HVCC	A-Power	--	Same as host I/O Ring Power (1.8V to 3V typical)
2	IC_DP	D-I/O	--	Bidirectional IC_DP
3	IC_DM	D-I/O	--	Bidirectional IC_DM
4	VBUS	A-Input	--	Not Used and Connected to Ground
6	HDMO	D-Output	HiZ	Not Connected
7	HDPO	D-Output	HiZ	Not Connected
8	OE_N	D-Input	High	Connected to H_{VCC}
9	PVRF	A-Input	--	Connected to Ground
10	D-	D-I/O	--	Downstream Port for USB Device
11	D+	D-I/O	--	Downstream Port for USB Device
12	PVCC	A-Power	--	Supplied at 3.3V
13	RCV	D-Output	HiZ	Not Connected
14	M<2>	D-Input	High	Connected to H_{VCC}
15	M<1>	D-Inputs	High	Connected to H_{VCC}
16	M<0>	D-Inputs	High	Connected to H_{VCC}

Application Diagram

In the following figure, the hardware configuration is described.

Figure 9-21. AT73C260: Bridge - IC_USB1.0 downstream port to USB2.0 section 7 - application diagram



Note: R_6 and R_7 are defined in component list Table 8-1 on page 10

9.4.5 Mode: Voltage Class Converter: VCC

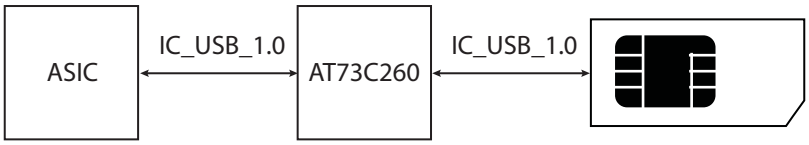
Description

Pins V_{BUS} and P_{VRF} are connected to GND and LDO outputs are isolated and in standby.

Pin OE_N is connected to H_{VCC}.

The following applications enable communications between an IC_USB1.0 compliant downstream port with a first voltage class H_{VCC} and an IC_USB1.0 compliant peripheral with a second voltage class P_{VCC}.

Figure 9-22. Voltage Class Converter Block Diagram



Hardware Configuration

In the following tables, the pin and the hardware configuration are described.

Table 9-17. AT73C260 Hardware Configuration

Mode	M<2> Pin 14	M<1> Pin 15	M<0> Pin 16	Application
VCC	H_{VCC}	H_{VCC}	H_{VCC}	IC_USB1.0 to IC_USB1.0 Voltage Class Converter

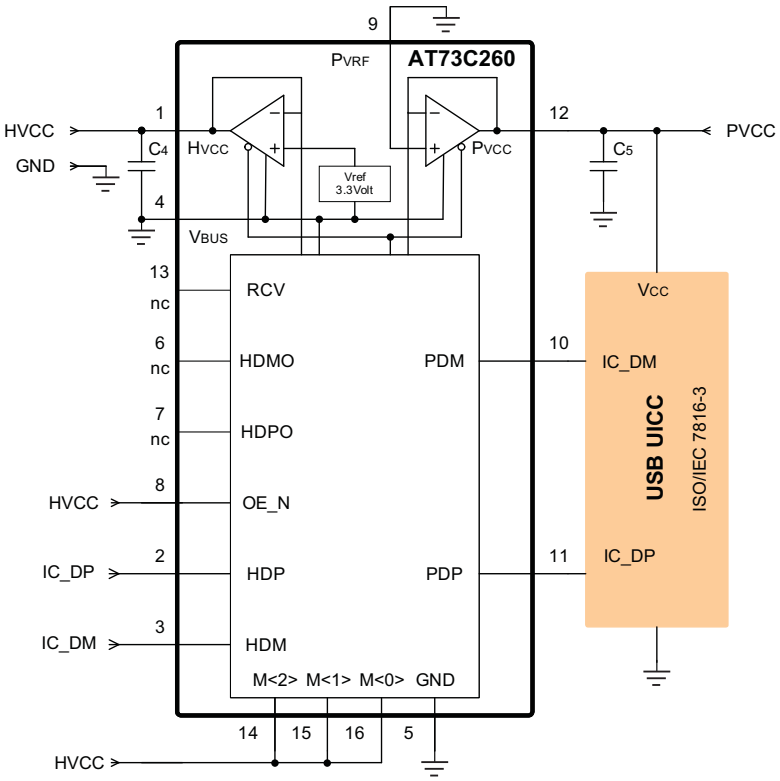
Table 9-18. AT73C260 Pin description and configuration

Pin Number	Pin Name	I/O Type	Polarity	Function
1	HVCC	A-Power	--	Same as host I/O Ring Power (1.8V to 3V typical)
2	IC_DP	D-I/O	--	Bidirectional IC_DP
3	IC_DM	D-I/O	--	Bidirectional IC_DM
4	VBUS	A-Input	--	Connected to Ground
6	HDMO	D-Output	HiZ	Not Connected
7	HDPO	D-Output	HiZ	Not Connected
8	OE_N	D-Input	High	Connected to H_{VCC}
9	PVRF	A-Input	--	Connected to Ground
10	PDM	D-I/O	--	Downstream Port for USB Device
11	PDP	D-I/O	--	Downstream Port for USB Device
12	PVCC	A-Power	--	Same as peripheral's power (1.8V or 3V typical)
13	RCV	D-Output	HiZ	Not Connected
14	M<2>	D-Input	High	Connected to H_{VCC}
15	M<1>	D-Inputs	High	Connected to H_{VCC}
16	M<0>	D-Inputs	High	Connected to H_{VCC}

Application Diagram

In the following figure, the hardware configuration is described.

Figure 9-23. AT73C260: Voltage Class Converter - IC_USB1.0 to IC_USB1.0 - application diagram



Note: All external components are defined in component list Table 8-1 on page 10

9.4.6 Bridge With LDOs

LDOs are enabled.

AT73C260's pin V_{BUS} is connected to the USB signal V_{BUS} through a low pass filter.

9.4.6.1 Mode: PC's USB2.0 section 7 to IC_USB1.0 with VCC driven by the DBB: S7_ICC_DBB

Description

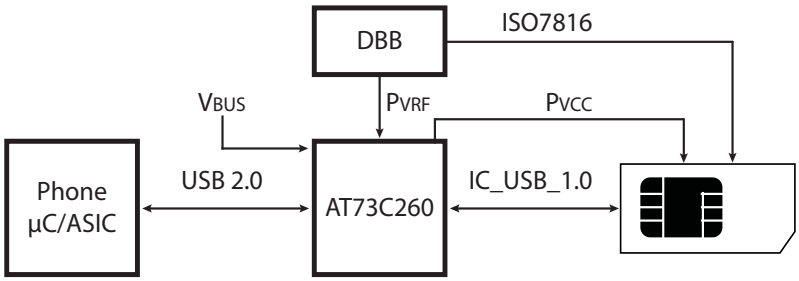
The PC's Digital Base Band may not provide enough power to a USB UICC with mass storage.

The V_{BUS} power supply voltage will make available that extra power, up to 70mA, through the AT73C260's LDO if needed by the USB UICC.

The PC's Digital Base Band supplies on pin 9 the power sequence required by ETSI. The AT73C260 buffers the signal on P_{VRF} to P_{VCC}. P_{VCC} sources power from V_{BUS} to V_{CC}.

On the Host side H_{VCC} generates 3.3V from V_{BUS}.

Figure 9-24. S7_ICC_DBB Block Diagram



Hardware Configuration

In the following tables, the pin and the hardware configuration are described.

Table 9-19. AT73C260 Hardware Configuration

Mode	M<2> Pin 14	M<1> Pin 15	M<0> Pin 16	Application
S7_ICC_DBB	H_{VCC}	H_{VCC}	0	PC's USB2.0 section 7 to IC_USB1.0 with V_{CC} driven by DBB

Table 9-20. AT73C260 Pin description and configuration

Pin Number	Pin Name	I/O Type	Polarity	Function
1	HVCC	A-Output	--	Delivered by AT73C260 from VBUS at 3.3V
2	D+	D-I/O	--	Bidirectional D +
3	D-	D-I/O	--	Bidirectional D -
4	VBUS	A-Input	--	Supplied by USB Power Line
6	HDMO	D-Output	HiZ	Not Connected
7	HDPO	D-Output	HiZ	Not Connected
8	OE_N	D-Input	High	Connected to H_{VCC}
9	PVRF	A-Input	--	Control by Digital Base Band

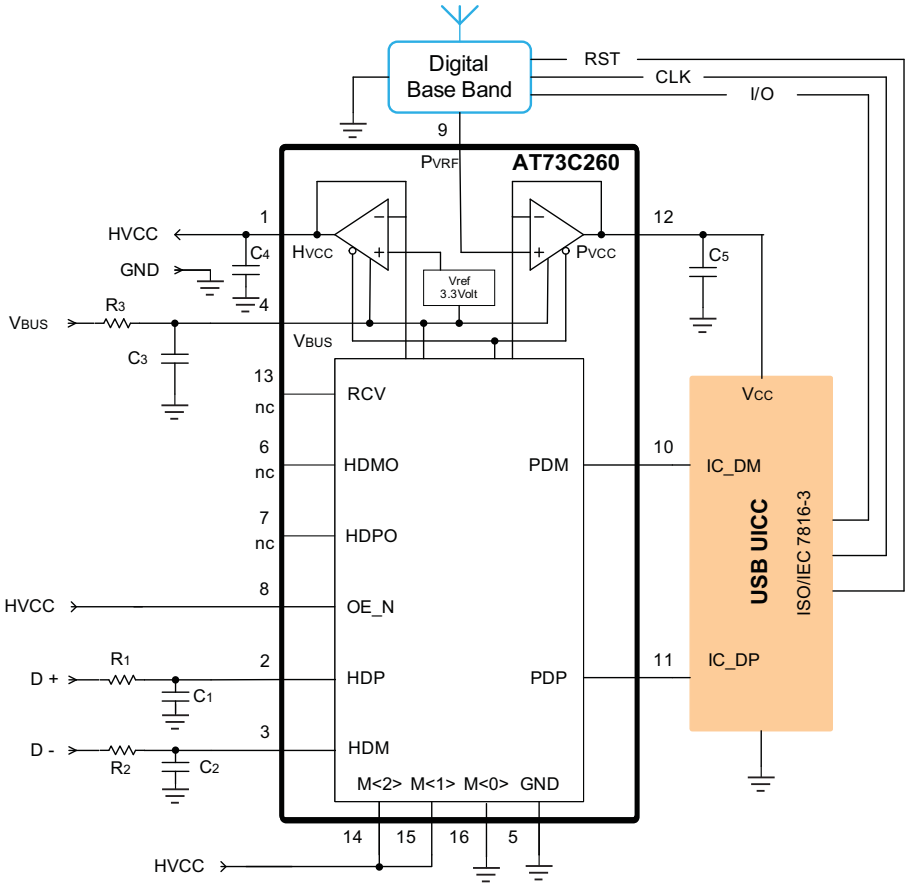
Table 9-20. AT73C260 Pin description and configuration

Pin Number	Pin Name	I/O Type	Polarity	Function
10	PDM	D-I/O	--	Downstream Port for USB Device
11	PDP	D-I/O	--	Downstream Port for USB Device
12	PVCC	A-Output	--	Delivered by AT73C260 from VBUS and control by DBB
13	RCV	D-Output	HiZ	Not Connected
14	M<2>	D-Input	High	Connected to H_{VCC}
15	M<1>	D-Inputs	High	Connected to H_{VCC}
16	M<0>	D-Inputs	Low	Connected to Ground

Application Diagram

In the following figure, the hardware configuration is described.

Figure 9-25. AT73C260: Bridge with LDO - USB2.0 section 7 to IC_USB1.0 with V_{CC} driven by DBB - application diagram



Notes: 1. P_{VCC} LDO regulator is compliant with SIM FTA 27.17.2.1 Tests Series.
2. All external components are defined in component list Table 8-1 on page 10

9.4.6.2 Mode: USB2.0 section 7 to IC_USB1.0 with PVCC fixed by PVRF: S7_ICC_TK

Description

This is a token application where an USB UICC is connected to an USB2.0 section 7 downstream port.

The AT73C260's LDOs supply H_{VCC} set at 3.3V and P_{VCC} set at the power supply voltage required by the USB UICC.

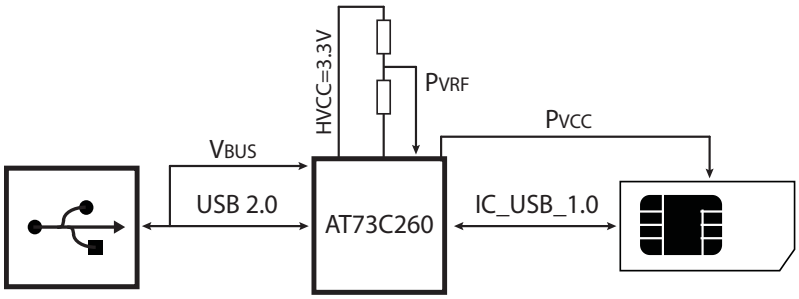
This application establishes a communication path between a USB2.0 section 7 downstream port and the USB UICC's. The power to the USB UICC is provided by V_{BUS} using an LDO able to source up to 70mA.

This is the typical electrical schematic for a USB UICC used in a USB Token to be connected to a USB2.0 series A receptacle.

The voltage divider R_4/R_5 generates for example 3.0V buffered by the LDO to the downstream side of the transceiver and to the USB UICC P_{VCC}.

This set up allows passing USB CV tests to the USB UICC under tests.

Figure 9-26. S7_ICC_TK Block Diagram (Token Application)



Hardware Configuration

In the following tables, the pin and the hardware configuration are described.

Table 9-21. AT73C260 Hardware Configuration

Mode	M<2> Pin 14	M<1> Pin 15	M<0> Pin 16	Application
S7_ICC_TK	H_{VCC}	H_{VCC}	0	USB2.0 section 7 to IC_USB1.0 with P_{VCC} fixed by P_{VRF}

Table 9-22. AT73C260 Pin description and configuration

Pin Number	Pin Name	I/O Type	Polarity	Function
1	HVCC	A-Output	--	Delivered by AT73C260 from VBUS at 3.3V
2	D+	D-I/O	--	Bidirectional D +
3	D-	D-I/O	--	Bidirectional D -
4	VBUS	A-Input	--	Supplied by USB Power Line
6	HDMO	D-Output	HiZ	Not Connected
7	HDPO	D-Output	HiZ	Not Connected

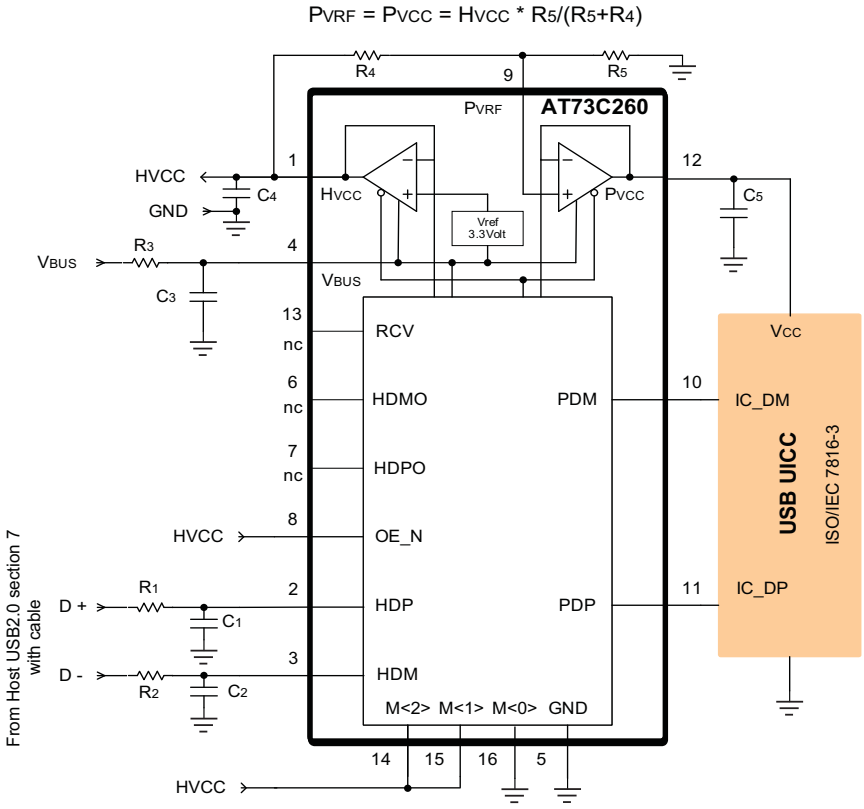
Table 9-22. AT73C260 Pin description and configuration

Pin Number	Pin Name	I/O Type	Polarity	Function
8	OE_N	D-Input	High	Connected to H_{VCC}
9	PVRF	A-Input	--	Fixed by external resistor bridge divider
10	PDM	D-I/O	--	Downstream Port for USB Device
11	PDP	D-I/O	--	Downstream Port for USB Device
12	PVCC	A-Output	--	Delivered by AT73C260 from VBUS according external resistor ratio
13	RCV	D-Output	HiZ	Not Connected
14	M<2>	D-Input	High	Connected to H_{VCC}
15	M<1>	D-Inputs	High	Connected to H_{VCC}
16	M<0>	D-Inputs	Low	Connected to Ground

Application Diagram

In the following figure, the hardware configuration is described.

Figure 9-27. AT73C260: Bridge with LDO - USB2.0 section 7 to IC_USB1.0 with V_{CC} fixed by P_{VRF} - application diagram



Notes: 1. P_{VCC} LDO regulator is compliant with SIM FTA 27.17.2.1 Tests Series.
2. All external components are defined in component list Table 8-1 on page 10

3. External resistors shall be in the following range: 100KΩ < R4 + R5 < 330KΩ in order to minimize current consumption and to reach a good accuracy on P_{VCC}. The bias current of P_{VRF} follower is less than +/-100nA.

9.4.7 Example of an Extra Function

For an FPGA implementation of a USB device, there is a need for an upstream IC_USB 1.0 PHY.

For this requirement the AT73C260 product can be configured as described below.

Pins V_{BUS} and P_{VRF} are connected to GND and LDO outputs are isolated and in standby.

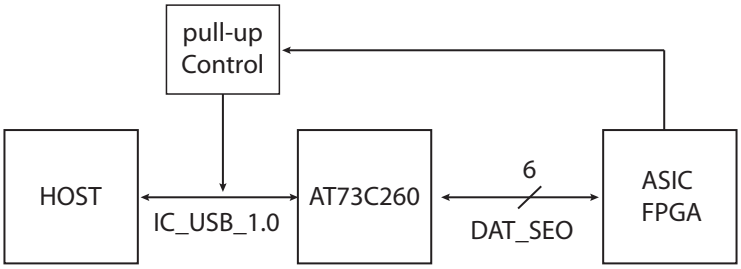
9.4.7.1 Mode: Digital six wires unidirectional DAT_SE0 to IC_USB1.0 upstream: Extra Function

Description

This application allows a peripheral based on an ASIC or an FPGA with the digital unidirectional six wires interface to be connected to an IC_USB 1.0 downstream port.

Here below, an example is shown. Other digital interfaces are compatible with this upstream IC_USB 1.0 port.

Figure 9-28. PHY_6_SE0 Block Diagram



Hardware Configuration

In the following tables, the pin and the hardware configuration are described.

Table 9-23. AT73C260 Hardware Configuration

Mode	M<2> Pin 14	M<1> Pin 15	M<0> Pin 16	Application
Extra Mode (as an example)	0	0	0	Digital six wires unidirectional DAT_SE0 to IC_USB1.0 upstream

Table 9-24. AT73C260 Pin description and configuration

Pin Number	Pin Name	I/O Type	Polarity	Function
1	HVCC	A-Power	--	Same as peripheral I/O ring (1.55V to 3.6V typical)
2	TX_DAT	D-Input	--	Unidirectional Transmit Data
3	TX_SEO	D-Input	--	Unidirectional Transmit Single Ended 0
4	VBUS	A-Input	--	Not Used and Connected to Ground
6	RX_DM	D-Output	--	Unidirectional Receiving DM
7	RX_DP	D-Output	--	Unidirectional Receiving DP
8	TX_ENABLE_N	D-Input	Low	Tx Enable N

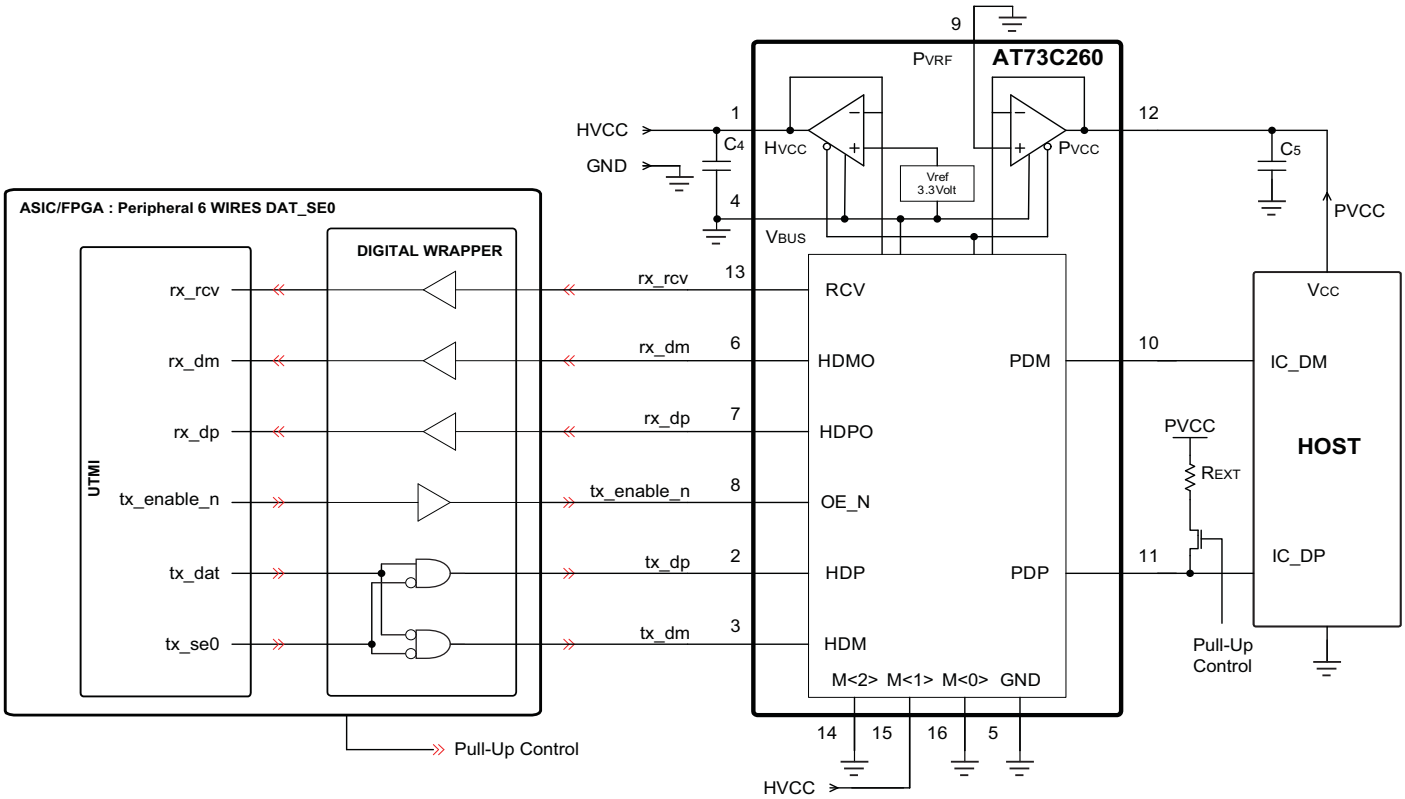
Table 9-24. AT73C260 Pin description and configuration

Pin Number	Pin Name	I/O Type	Polarity	Function
9	PVRF	A-Input	--	Connected to Ground
10	PDM	D-I/O	--	Downstream Port for USB Device
11	PDP	D-I/O	--	Downstream Port for USB Device
12	PVCC	A-Power	--	Same power as host VCC (1.8 or 3V typical)
13	RX_RCV	D-Output	--	Unidirectional Receiving RCV
14, 15, 16	M<2:0>	D-Inputs	Low	Connected to Ground

Application Diagram

In the following figure, the hardware configuration is described.

Figure 9-29. AT73C260: Extra Mode - PHY of a 6-wire FPGA peripheral implementation - application diagram

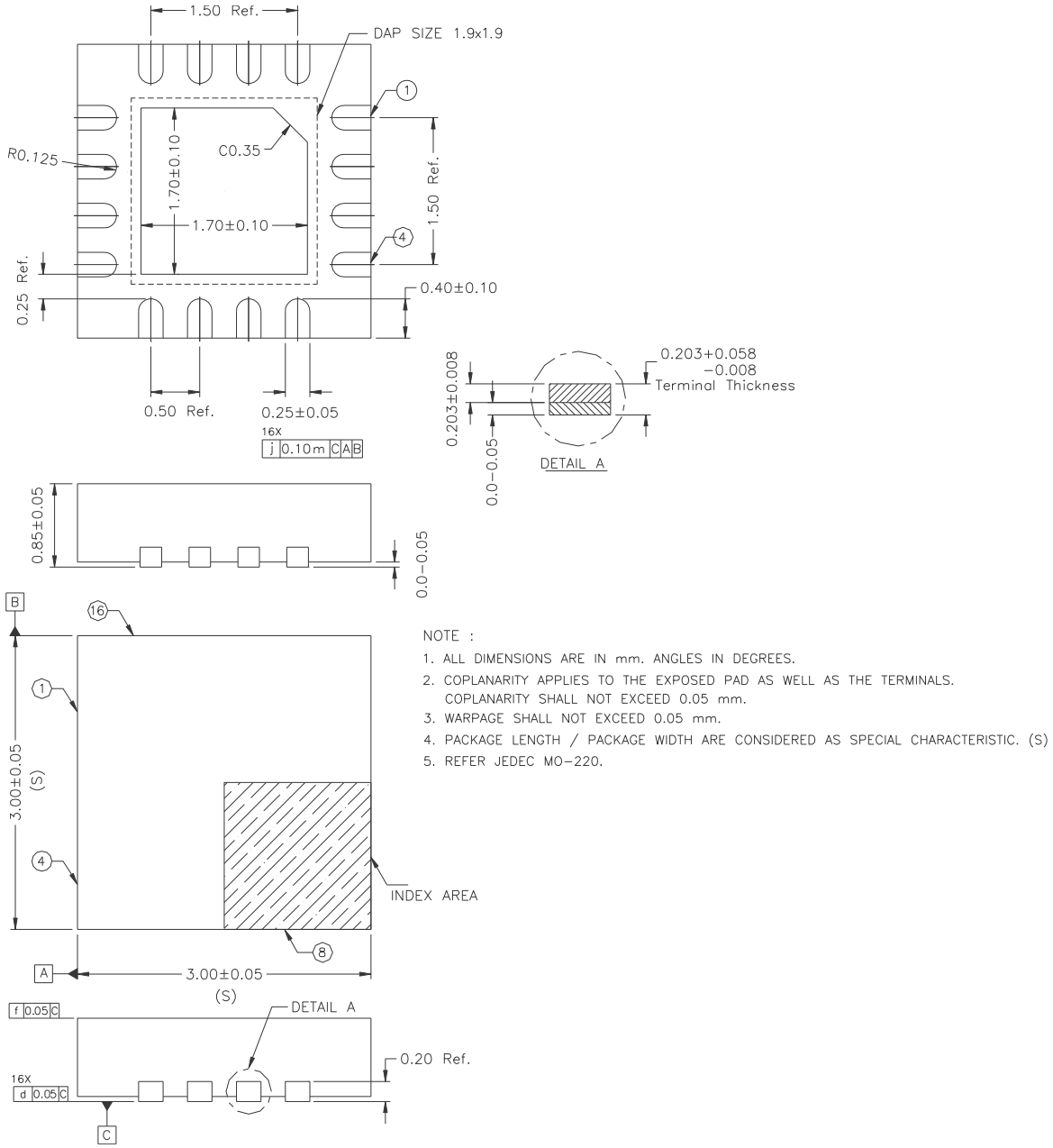


Notes: 1. All external components are defined in component list Table 8-1 on page 10

2. In Upstream port configuration, the software must drive the R_{EXT} pull-up resistor.

10. Package Information

Figure 10-1. Mechanical Package Drawing for 16-lead Quad Flat No Lead Package



Note: All the dimensions are in mm

11. Ordering Information

Table 11-1. Ordering Information

Ordering Code	Package	Package Type	Temperature Operating Range
AT73C260	QFN16 3 x 3 mm	Green	-40°C to +85°C

12. Revision History

Doc. Rev	Date	Comments	Change Request Ref.
11030A	13-Sep-10	First revision	

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