austriamicrosystems AG

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ams AG

The technical content of this austriamicrosystems datasheet is still valid.

Contact information:

Headquarters:
ams AG
Tobelbaderstrasse 30
8141 Unterpremstaetten, Austria
Tel: +43 (0) 3136 500 0
e-Mail: ams_sales@ams.com

Please visit our website at **www.ams.com**

AS1119

144-LED Cross-Plexing Driver with 320mA Charge-Pump

1 General Description

The AS1119 is a compact LED driver for 144 (90) single LEDs. The devices can be programmed via an I²C compatible interface.

The AS1119 offers two blocks driving each 72 LEDs (3 blocks each 30LEDs) with 1/9 (1/6) cycle rate. The required lines to drive all 144 (90)LEDs are reduced to 18 by using the cross-plexing feature optimizing space on the PCB. Every block driving 72(30) LEDs can be analog dimmed from 1 to 30mA in 256 steps (8 bit).

Additionally each of the 144 (90) LEDs can be dimmed individually with 8-bit allowing 256 steps of linear dimming. To reduce CPU usage up to 6 frames can be stored with individual time delays between frames to play small animations automatically.

The AS1119 operates from 2.7V to 5.5V and includes a 320mA charge-pump to drive also white LEDs. The charge-pump operates in 2:3 and 1:2 mode.

The AS1119 features very low shutdown and operational current.

The device is available in a ultrasmall 36-pin WL-CSP.

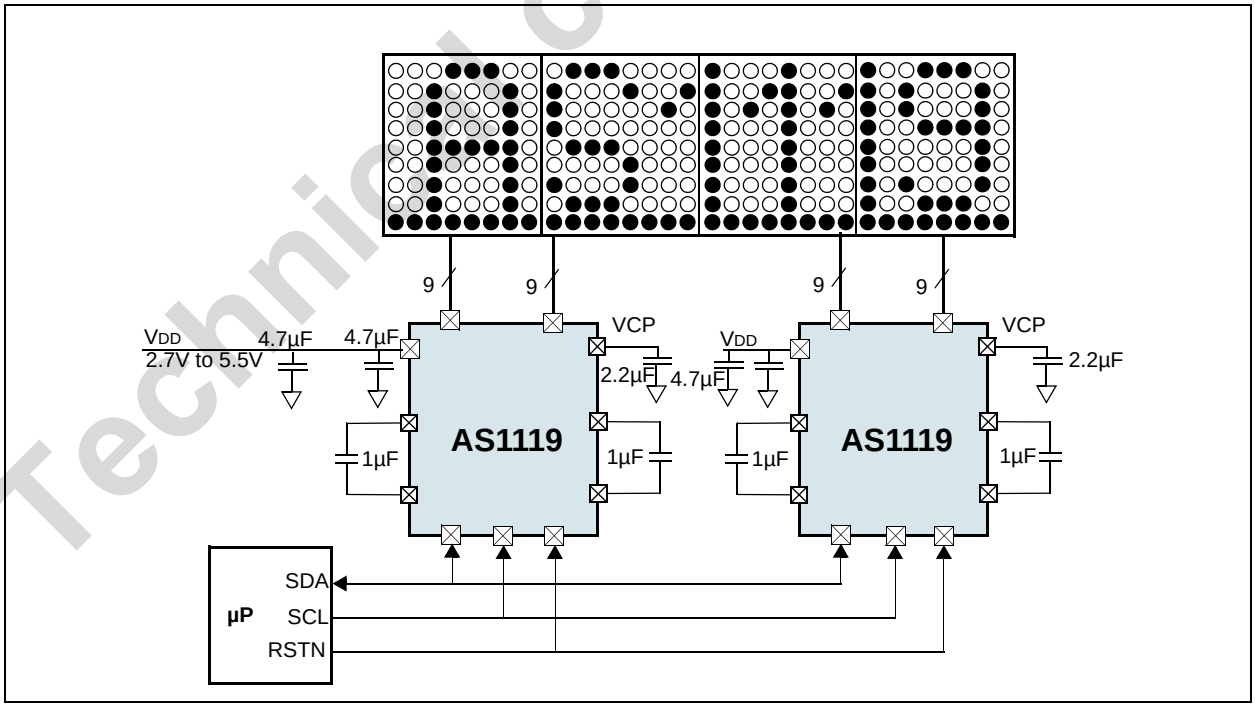
2 Key Features

- 1MHz I²C-Compatible Interface
- Open and Shorted LED Error Detection
- 144 LEDs in Dot Matrix
- Low-Power Shutdown Current
- Individual 8-bit LED PWM Control
- 8-bit Analog Brightness Control
- (1:1), 2:3, 1:2 320mA Charge Pump
- 6 Frames Memory for Animations
- System-clk synchronisation for multiple devices
- Supply Voltage Range: 2.7V to 5.5V
- Minimum PCB space required
- 36-pin WL-CSP package

3 Applications

The AS1119 is ideal for dot matrix displays in mobile phones, personal electronic and toys.

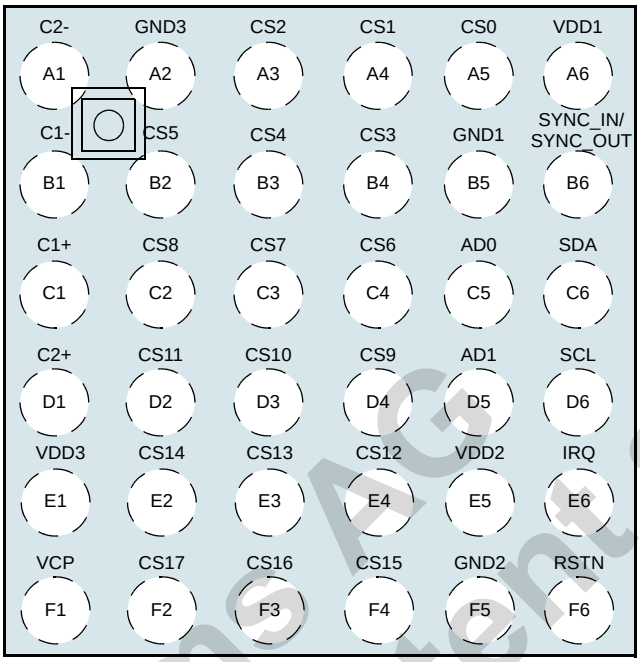
Figure 1. AS1119 - Typical Application Diagram



4 Pinout

Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Number	Description
VDD1, VDD2, VDD3	A6, E5, E1	**Positive Supply Voltage.** Connect to a +2.7V to +5.5V supply. Bypass this pin with 10µF capacitance to GND1, GND2, GND3.
VCP	F1	**Charge-Pump Output Voltage.** Connect a 2.2µF capacitor to GND3.
C1-, C1+	B1, C1	**Flying Cap 1.** Connect a 1µF capacitor.
C2-, C2+	A1, D1	**Flying Cap 2.** Connect a 1µF capacitor.
GND1	B5	**Ground for VDD1.** Used for CS0-CS8
GND2	F5	**Ground for VDD2.** Used for CS9-CS17
GND3	A2	**Ground for VDD3.** Used for Charge-Pump
SDA	C6	**Serial-Data I/O.** Open drain digital I/O I²C data pin.
SCL	D6	**Serial-Clock Input.**
AD0	C5	**I²C Address for bit 0.** Put to GND or VDD to set I²C addresses.
AD1	D5	**I²C Address for bit 1.** Put to GND or VDD to set I²C addresses.
RSTN	F6	**Reset Input.** Pull this pin to logic low to reset all control registers (set to default values) and to put the device into power-down. For normal operation pull this pin to VDD.
SYNC_IN, SYNC_OUT	B6	**Synchronization Clock Input or Output**
IRQ	E6	**Interrupt Request.** Open drain digital Output.

Table 1. Pin Descriptions

Pin Name	Pin Number		Description
CS0 - CS8	A5-A3, B4-B2, C4-C2	2 Matrixes	Sinks and Sources for 72 LEDs each matrix.
CS9 - CS17	D4-D2, E4-E2, F4-F2		
CS0 - CS5	A5-A3, B4-B2	3 Matrixes	Sinks and Sources for 30 LEDs each matrix.
CS6 - CS11	C4-C2, D4-D2		
CS12 - CS17	E4-E2, F4-F2		

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 5 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Electrical Parameters				
VDD to GND	-0.3	7	V	
All other pins to GND	-0.3	7 or V_{DD} + 0.3	V	
Sink Current		500	mA	
Segment Current		100	mA	
Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC 78
Electrostatic Discharge				
Electrostatic Discharge HBM	1.5		kV	Norm: MIL 883 E method 3015
Temperature Ranges and Storage Conditions				
Junction Temperature		+125	ºC	
Storage Temperature Range	-55	+125	ºC	
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/ JEDEC J-STD-020"Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".*
Humidity non-condensing	5	85	%	
Moisture Sensitive Level	1			Represents a max. floor life time of unlimited

6 Electrical Characteristics

VDD = 2.7V to 5.5V, TAMB = -40°C to +85°C, typ. values are at TAMB = +25ºC (unless otherwise specified).

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TAMB	Operating Temperature Range			-40		85	°C
VDD	Operating Supply Voltage			2.7		5.5	V
IDDSD	Software Shutdown Supply Current	All digital inputs at VDD or GND, VDD = 5.5V, TAMB = +25ºC			7		µA
IDDFSD	Full Shutdown Supply Current	Pin RSTN = 0V, TAMB = +25ºC			0.1	1	µA
IDD	Operating Supply Current (all current sources turned off)	CP disabled @ VDD = 5.5V			1.4		mA
		With CP in 2:3 mode @ VDD = 2.7V			3		
		With CP in 1:2 mode @ VDD = 2.7V			4		
ISTART	max. Peak Inrush Current				1.5		A
	max. DC Current				700		mA
IDIGIT	Digit Drive Sink Current (Drive capability of all sources of one digit[1,2])	CP disabled				500	mA
		CP enabled	VDD < 3.3V			160	
			VDD ≥ 3.3V			320	
ISEG	Segment Drive Source Current LED	VOUT = 1.8V to VDD-400mV		28	30	32	mA
ΔISEG	Segment Drive Current Matching LED[3]				2		%
VDSSAT	Saturation Voltage	Current = 30mA, VDD = 5V			100		mV
RDSON(N)	Resistance for NMOS				0.5	1	Ω
fOSC	Oscillator Frequency			0.9	1	1.1	MHz
fREFRESH	Display Scan Rate	2 time 9x8 matrixes		0.39	0.43	0.48	kHz

1. Not all sources are allowed to be fully on at the same time.
2. guaranteed by design
3. $I_{SEG} = \frac{I_{max} - I_{min}}{I_{max} + I_{min}} \times 100$

Table 4. Logic Inputs/Outputs Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IIH, IIL	Logic Input Current	VIN = 0V or VDD	-1		1	µA
VIH	Logic High Input Voltage		1.6			V
VIL	Logic Low Input Voltage				0.6	V
ΔVI	Hysteresis Voltage			0.1		V
VOL(SDA)	SDA Output Low Voltage	ISINK = 3mA			0.4	V
VOL(IRQ)	IRQ Output Low Voltage	ISINK = 3mA			0.4	V
VOL(SYNC_OUT)	Sync Clock Output Low Voltage	ISINK = 1mA			0.4	V
VOH(SYNC_OUT)	Sync Clock Output High Voltage	ISOURCE = 1mA			VDD-0.4	V
	Open Detection Level Threshold		VDD-0.4	VDD-0.1		V
	Short Detection Level Threshold			0.9	1.2	V
	Capacitive Load for Each Bus Line	SCL Frequency = 400kHz			400	pF
		SCL Frequency = 1000kHz			100	

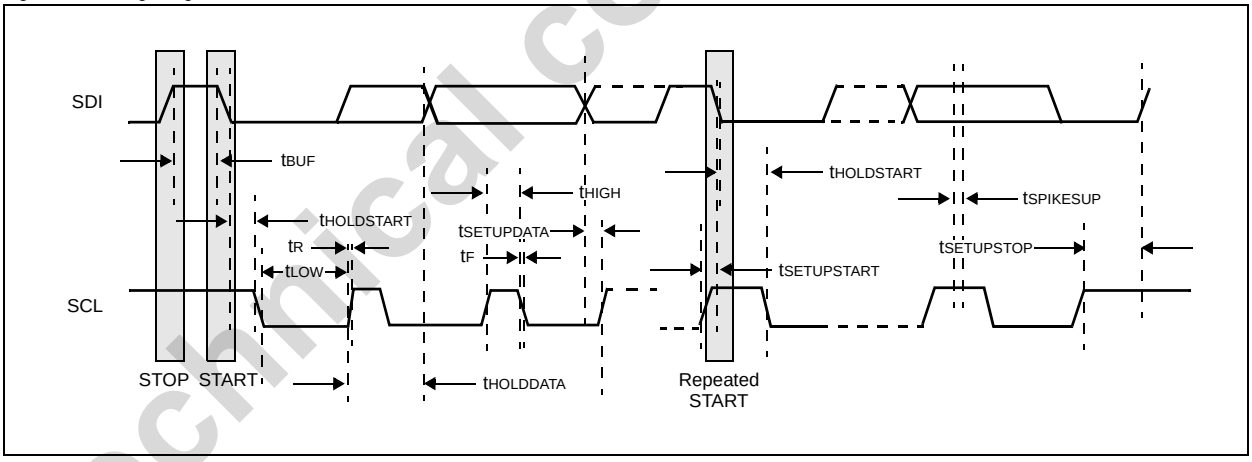
Table 5. I²C Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fSCL	SCL Frequency		100		1000	kHz
tBUF	Bus Free Time Between STOP and START Conditions		1.3			µs
tHOLDSTART	Hold Time for Repeated START Condition		160			ns
tLOW	SCL Low Period		50		75	ns
tHIGH	SCL High Period		50		75	ns
tSETUPSTART	Setup Time for Repeated START Condition		100			ns
tSETUPDATA	Data Setup Time		10			ns
tHOLDDATA	Data Hold Time				70	ns
tRISE(SCL)	SCL Rise Time		10		40	ns
tRISE(SCL1)	SCL Rise Time after Repeated START Condition and After an ACK Bit		10		80	ns
tFALL(SCL)	SCL Fall Time		10		40	ns
tRISE(SDA)	SDA Rise Time		20		80	ns
tFALL(SDA)	SDA Fall Time		20		80	ns
tSETUPSTOP	STOP Condition Setup Time		160			ns
tSPIKESUP	Pulse Width of Spike Suppressed			50		ns

Notes:

1. The Min / Max values of the Timing Characteristics are guaranteed by design.
2. All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 3. Timing Diagram



7 Typical Operating Characteristics

Figure 4. Segment Drive Current vs. Supply Voltage

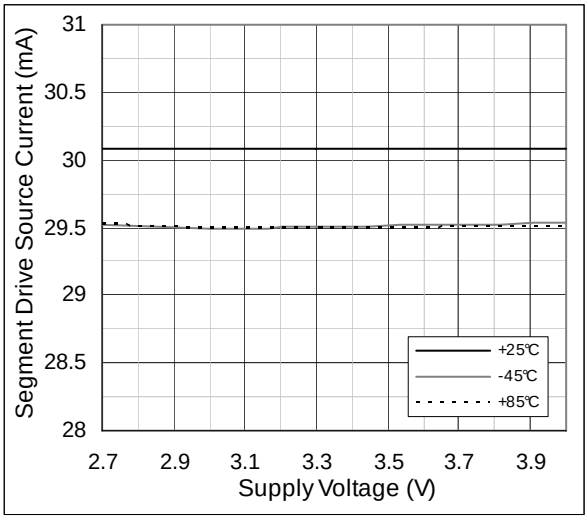


Figure 5. Segment Drive Current vs. Temperature

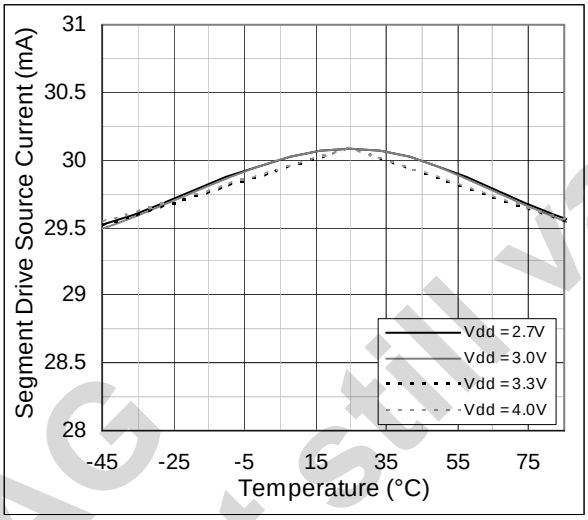


Figure 6. Segment Drive Current vs. Output Voltage

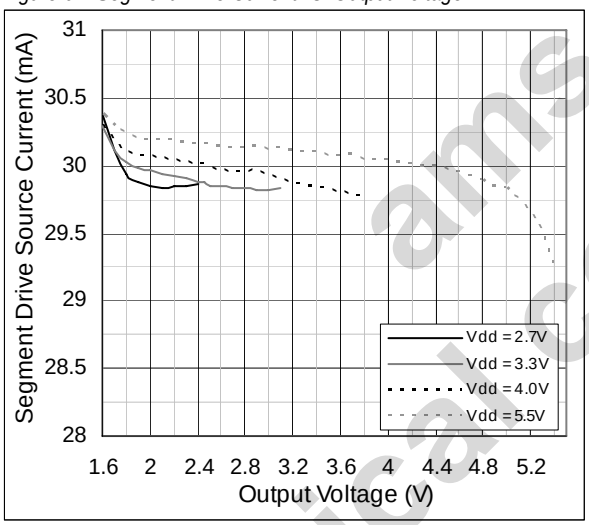


Figure 7. RONNMOS vs. Supply Voltage

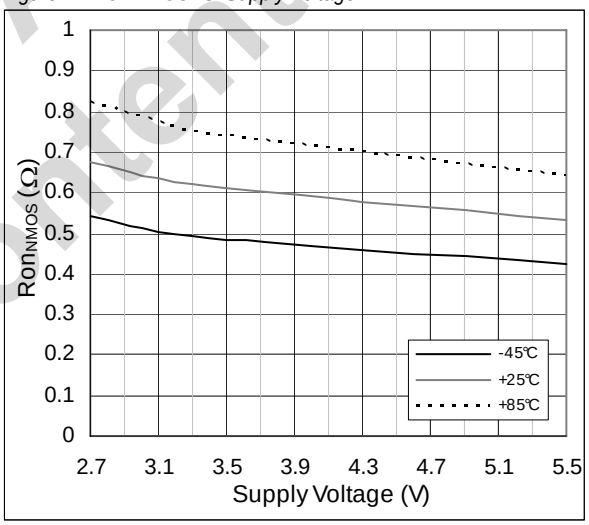


Figure 8. Open Detection Level vs. Supply Voltage

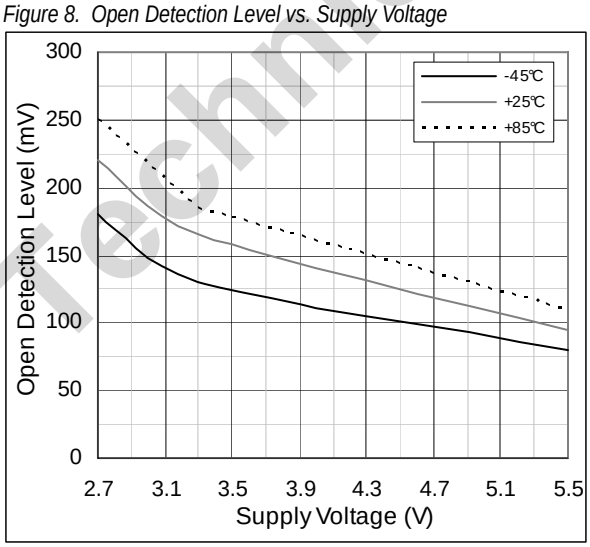


Figure 9. Short Detection Level vs. Supply Voltage

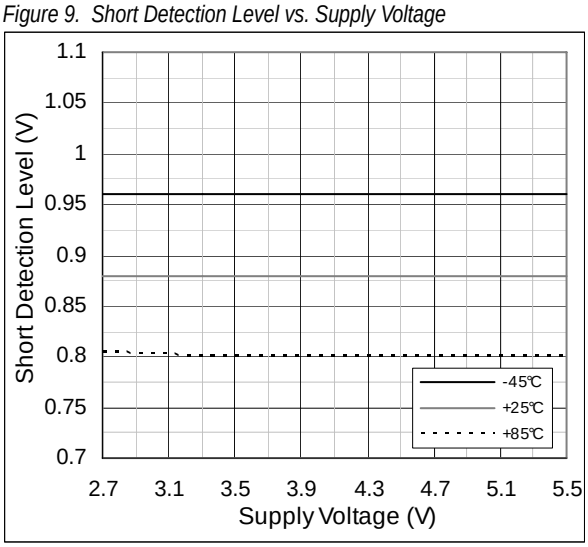


Figure 10. Efficiency vs. Supply Voltage

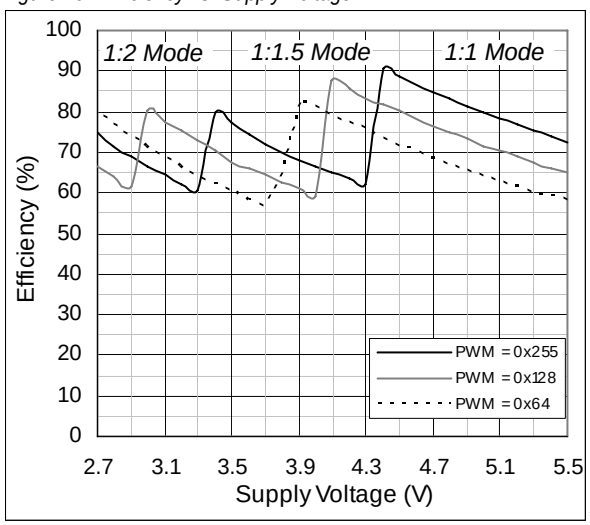


Figure 11. Logic Input Voltage Levels

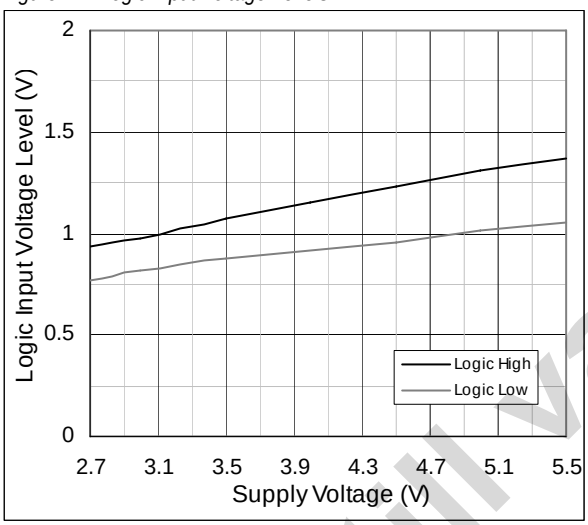
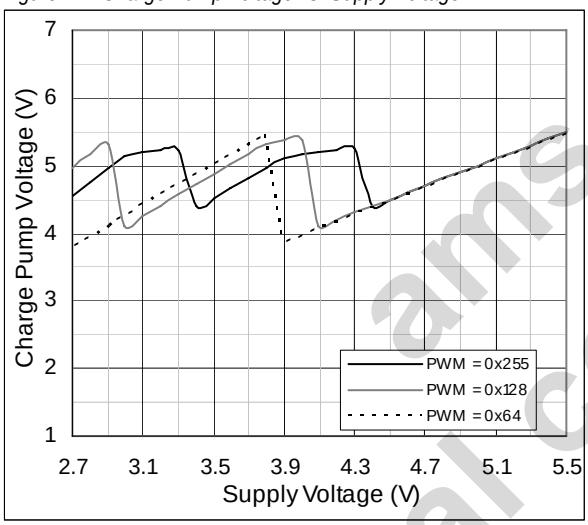


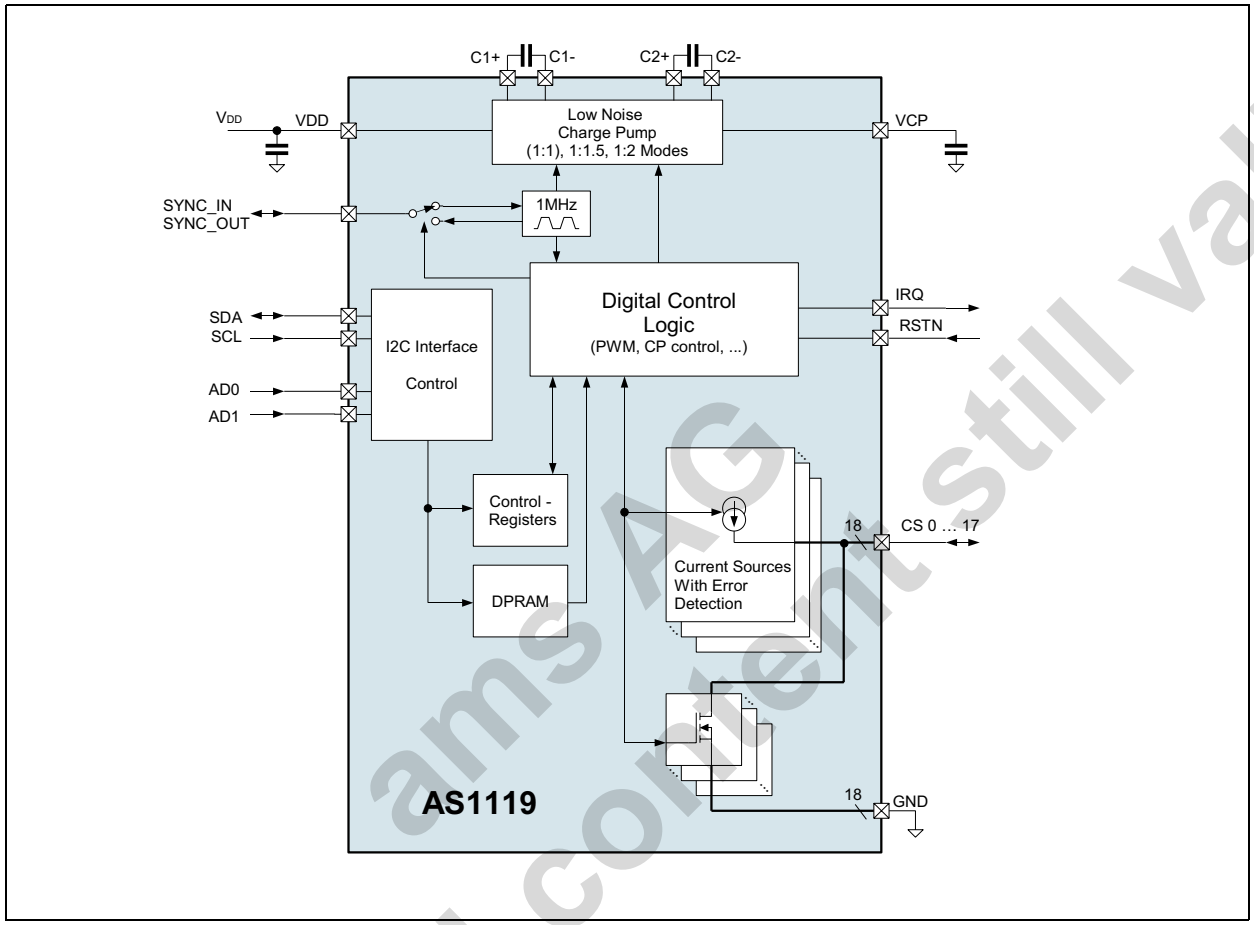
Figure 12. Charge Pump Voltage vs. Supply Voltage



8 Detailed Description

Block Diagram

Figure 13. AS1119 - Block Diagram



I²C Interface

The AS1119 supports the I²C serial bus and data transmission protocol in fast mode at 1MHz. The AS1119 operates as a slave on the I²C bus. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. Connections to the bus are made via the open-drain I/O pins SCL and SDA.

Figure 14. I²C Interface Initialisation

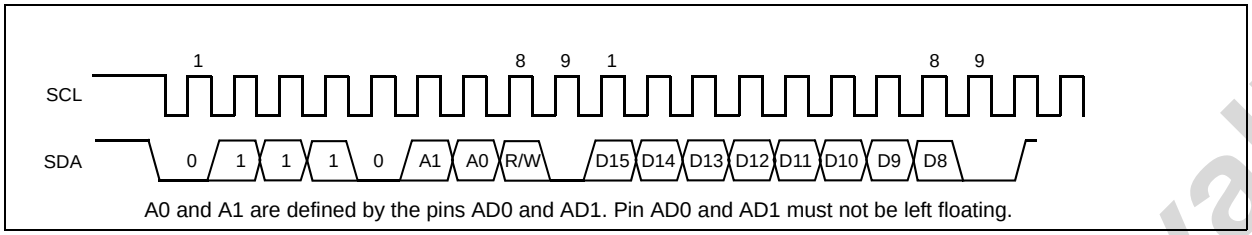
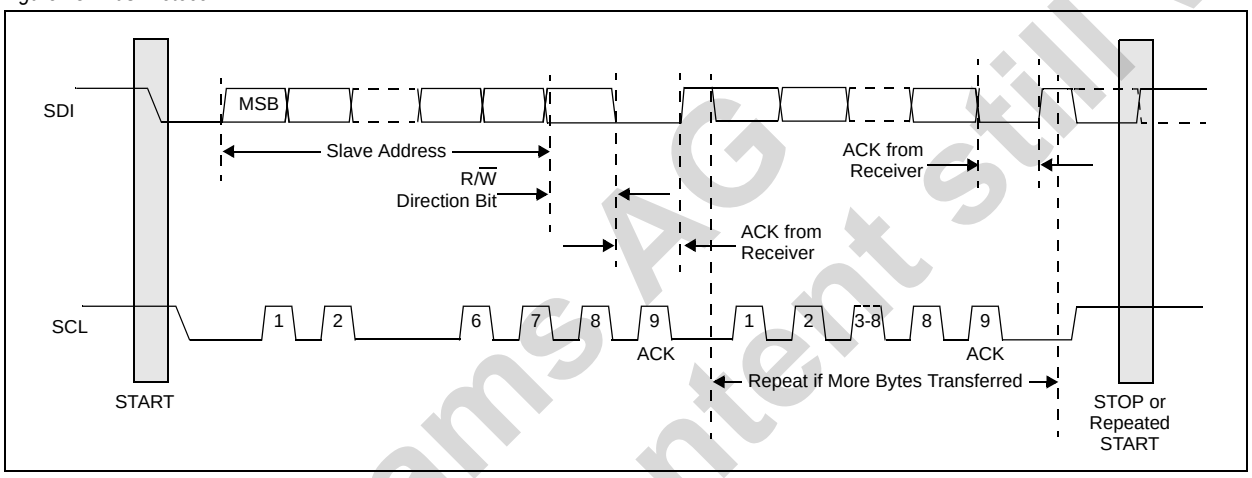


Figure 15. Bus Protocol



The bus protocol (as shown in Figure 15) is defined as:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The bus conditions are defined as:

- **Bus Not Busy**. Data and clock lines remain HIGH.
- **Start Data Transfer**. A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.
- **Stop Data Transfe**r. A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.
- **Data Valid**. The state of the data line represents valid data, when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.
  Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth-bit.
  Within the I²C bus specifications a high-speed mode (3.4MHz clock rate) is defined.
- **Acknowledge**: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an

acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

- Figure 15 on page 10 details how data transfer is accomplished on the I²C bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:
- **Master Transmitter to Slave Receiver**. The first byte transmitted by the master is the slave address, followed by a number of data bytes. The slave returns an acknowledge bit after the slave address and each received byte.
- **Slave Transmitter to Master Receiver**. The first byte, the slave address, is transmitted by the master. The slave then returns an acknowledge bit. Next, a number of data bytes are transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not-acknowledge is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The AS1119 can operate in the following slave modes:

- **Slave Receiver Mode**. Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
- **Slave Transmitter Mode**. The first byte (the slave address) is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the AS1119 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

I²C Device Address Byte

The address byte (see Figure 16) is the first byte received following the START condition from the master device.

Figure 16. I²C Device Address Byte

	MSB	6	5	4	3	2	1	LSB
address:	0	1	1	1	0	AD1	AD0	R/$\overline{W}$

- The bit 1 and bit 2 of the address byte are the device select pins AD0 and AD1, which must be set to V_{DD} or to GND. A maximum of four devices with the same pre-set code can therefore be connected on the same bus at one time.
- The last bit of the address byte (R/$\overline{W}$) define the operation to be performed. When set to a 1 a read operation is selected; when set to a 0 a write operation is selected.

Following the START condition, the AS1119 monitors the I²C bus, checking the device type identifier being transmitted. Upon receiving the address code, and the R/$\overline{W}$ bit, the slave device outputs an acknowledge signal on the SDA line.

Command Byte

The AS1119 operation, (see Table 15 on page 21) is determined by a command byte (see Table 17).

Figure 17. Command Byte

MSB	6	5	4	3	2	1	LSB
A7	A6	A5	A4	A3	A2	A1	A0

Figure 18. Command and Single Data Byte received by AS1119

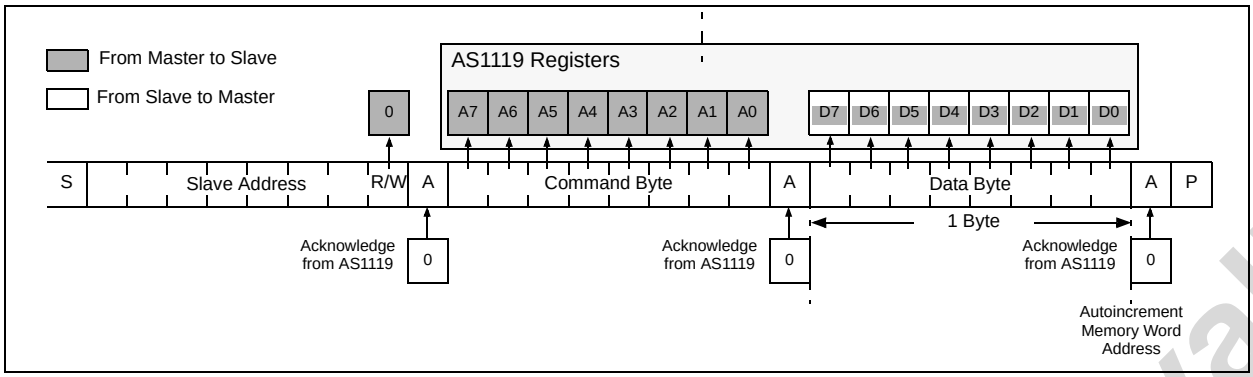


Figure 19. Setting the Pointer to a Address Register to select a Data Register for a Read Operation

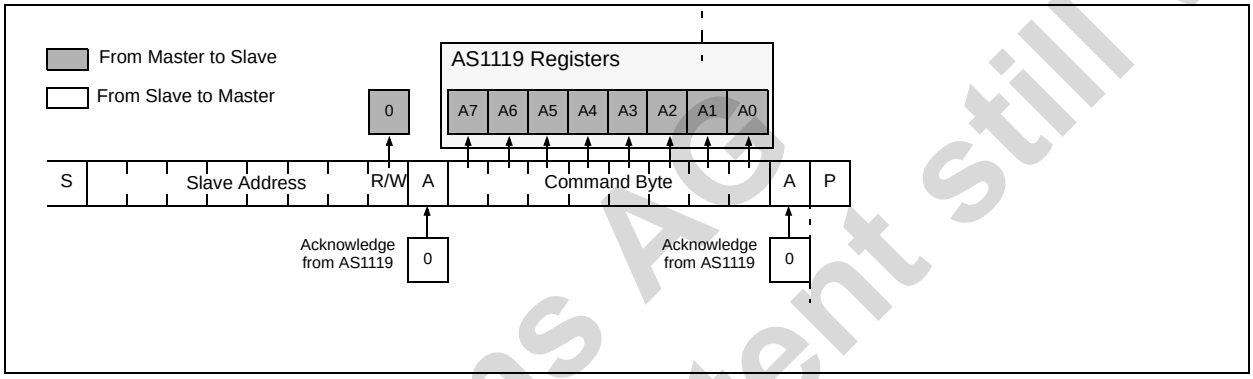
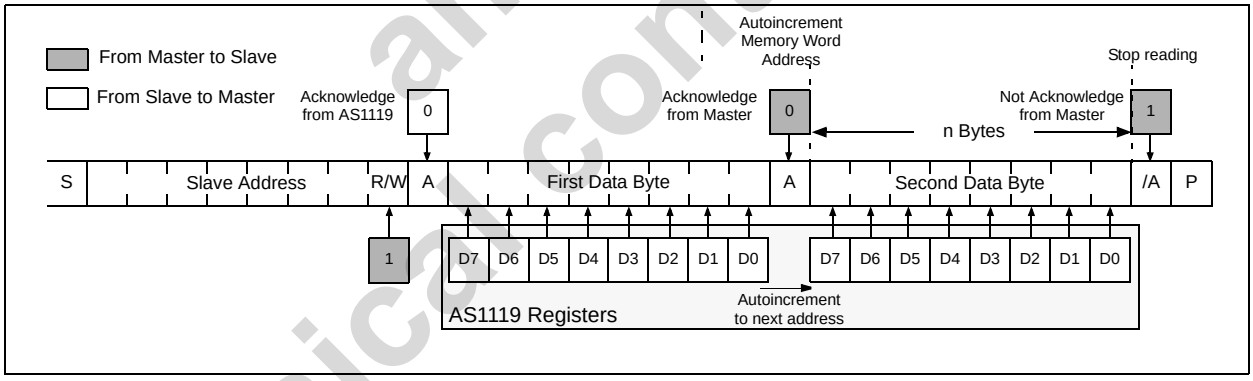


Figure 20. Reading n Bytes from AS1119



Initial Power-Up

On initial power-up, the AS1119 registers are reset to their default values, the display is blanked, and the device goes into shutdown mode. At this time, all registers should be programmed for normal operation.

Note: The default settings enable only scanning of one digit; the internal decoder is disabled and the Intensity Control Register (see page 16) and (see page 20) is set to the minimum values.

Shutdown Mode

The AS1119 device features two different shutdown modes. A software shutdown via shutdown register (see Shutdown Register (0x0A) on page 26) and a hardware shutdown via the RSTN pin.

The software shutdown disables all LED's and stops the internal operation of the logic. A shutdown mode via the RSTN pin additionally powers down the power-on-reset (PO) of the device. In this shutdown mode the AS1119 consumes only 100nA (typ.).

9 Register Description

Register Selection

Within this register the access to one of the RAM sections or to the Control register is selected. After one section is selected this section is valid as long as an other section is selected.

Table 6. Register Selection Address Map

Register Section	Address									Data									Description
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	HEX	D7	D6	D5	D4	D3	D2	D1	D0	
NOP	253	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	No operation
Data Frame 0										1	0	0	0	0	0	0	0	1	Selection of RAM section for frame
Data Frame 1										2	0	0	0	0	0	0	1	0	
Data Frame 2										3	0	0	0	0	0	0	1	1	
Data Frame 3										4	0	0	0	0	0	1	0	0	
Data Frame 4										5	0	0	0	0	0	1	0	1	
Data Frame 5										6	0	0	0	0	0	1	1	0	
Control Register										11	0	0	0	0	1	0	1	1	Selection of Control Register

Data Definition of the single frames

One frame consits of 2 blocks (à 8x9 LED-matrix) or 3 blocks (à 5x6 LED-matrix). This configuration is set in the AS1119 config register (see Table 20 on page 24).

In the internal DPRAM of the device 6 frames can be stored. For each frame the following parameters have to be stored.

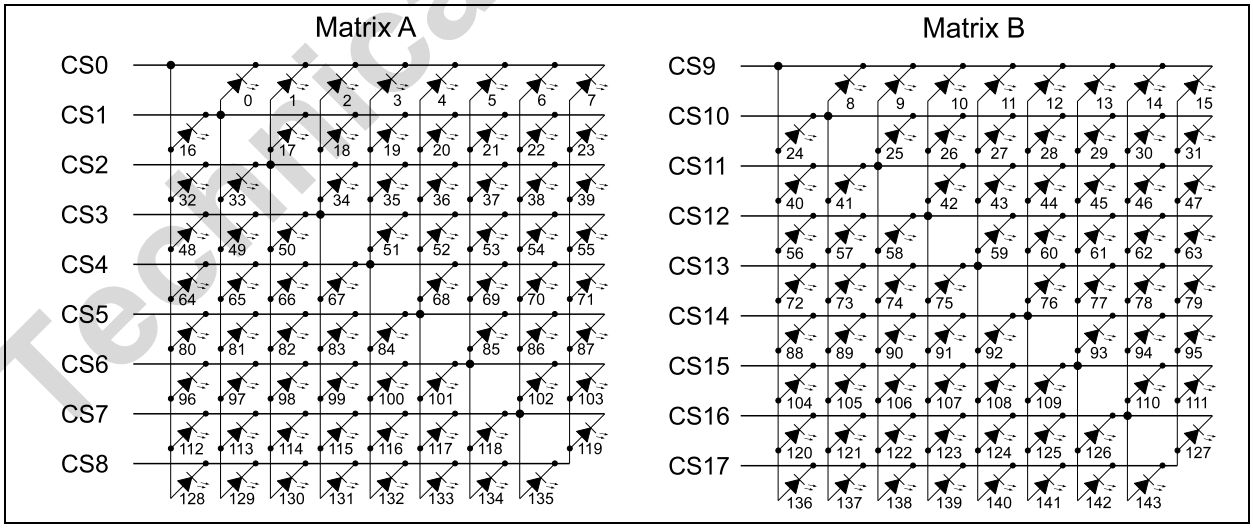
- LED is ON or OFF.
- LED is steady ON or blinking.
- The intensity of every single LED can be set via a 8 bits PWM.

Note: After power-up the data in the DPRAM is undefined (either '0' or '1').

2 Blocks with 8x9 LED Matrix

The AS1119 can be configured to control two seperated blocks of LEDs matrixes. This must be set via the bit D0 in the AS1119 config register (see AS1119 Config Register (0x04) on page 24).

Figure 21. 8x9 LED Matrix with two blocks



The adress structure (as shown in Table 7) within on frame is always the same independent which frame was selected via the register selection (see Table 6 on page 13).

Table 7. Dataframe Adress Structure for 2 Matrixes

		Adresses within frame (HEX code)					
Current Source		**On / Off**		**Blink**		**Intensity**	
Matrix A	Matrix B	**Matrix A**	Matrix B	**Matrix A**	Matrix B	**Matrix A**	Matrix B
CS0	CS9	0x00	0x01	0x12	0x13	0x24-0x2B	0x2C-0x33
CS1	CS10	0x02	0x03	0x14	0x15	0x34-0x3B	0x3C-0x43
CS2	CS11	0x04	0x05	0x16	0x17	0x44-0x4B	0x4C-0x53
CS3	CS12	0x06	0x07	0x18	0x19	0x54-0x5B	0x5C-0x63
CS4	CS13	0x08	0x09	0x1A	0x1B	0x64-0x6B	0x6C-0x73
CS5	CS14	0x0A	0x0B	0x1C	0x1D	0x74-0x7B	0x7C-0x83
CS6	CS15	0x0C	0x0D	0x1E	0x1F	0x84-0x8B	0x8C-0x93
CS7	CS16	0x0E	0x0F	0x20	0x21	0x94-0x9B	0x9C-0xA3
CS8	CS17	0x10	0x11	0x22	0x22	0xA4-0xAB	0xAC-0xB3

In Table 8 it's described which databit represents which LED in the matrix. Per default all databits are '0', meaning no LED is on. A '1' puts the LED on.

Table 8. LEDs ON/OFF Register Format for 2 Matrixes Setup

Matrix	Current Source	Adress									Data							
		HEX	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
A	CS0	0x00	0	0	0	0	0	0	0	0	LED7	LED 6	LED 5	LED 4	LED 3	LED 2	LED 1	LED 0
B	CS9	0x01	0	0	0	0	0	0	0	1	LED 15	LED 14	LED 13	LED 12	LED 11	LED 10	LED 9	LED 8
A	CS1	0x02	0	0	0	0	0	0	1	0	LED 23	LED 22	LED 21	LED 20	LED 19	LED 18	LED 17	LED 16
B	CS10	0x03	0	0	0	0	0	0	1	1	LED 31	LED 30	LED 29	LED 28	LED 27	LED 26	LED 25	LED 24
A	CS2	0x04	0	0	0	0	0	1	0	0	LED 39	LED 38	LED 37	LED 36	LED 35	LED 34	LED 33	LED 32
B	CS11	0x05	0	0	0	0	0	1	0	1	LED 47	LED 46	LED 45	LED 44	LED 43	LED 42	LED 41	LED 40
A	CS3	0x06	0	0	0	0	0	1	1	0	LED 55	LED 54	LED 53	LED 52	LED 51	LED 50	LED 49	LED 48
B	CS12	0x07	0	0	0	0	0	1	1	1	LED 63	LED 62	LED 61	LED 60	LED 59	LED 58	LED 57	LED 56
A	CS4	0x08	0	0	0	0	1	0	0	0	LED 71	LED 70	LED 69	LED 68	LED 67	LED 66	LED 65	LED 64
B	CS13	0x09	0	0	0	0	1	0	0	1	LED 79	LED 78	LED 77	LED 76	LED 75	LED 74	LED 73	LED 72
A	CS5	0x0A	0	0	0	0	1	0	1	0	LED 87	LED 86	LED 85	LED 84	LED 83	LED 82	LED 81	LED 80
B	CS14	0x0B	0	0	0	0	1	0	1	1	LED 95	LED 94	LED 93	LED 92	LED 91	LED 90	LED 89	LED 88
A	CS6	0x0C	0	0	0	0	1	1	0	0	LED 103	LED 102	LED 101	LED 100	LED 99	LED 98	LED 97	LED 96
B	CS15	0x0D	0	0	0	0	1	1	0	1	LED 111	LED 110	LED 109	LED 108	LED 107	LED 106	LED 105	LED 104
A	CS7	0x0E	0	0	0	0	1	1	1	0	LED 119	LED 118	LED 117	LED 116	LED 115	LED 114	LED 113	LED 112
B	CS16	0x0F	0	0	0	0	1	1	1	1	LED 127	LED 126	LED 125	LED 124	LED 123	LED 122	LED 121	LED 120

Table 8. LEDs ON/OFF Register Format for 2 Matrixes Setup

Matrix	Current Source	Adress									Data							
		HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
A	CS8	0x10	0	0	0	1	0	0	0	0	LED 135	LED 134	LED 133	LED 132	LED 131	LED 130	LED 129	LED 128
B	CS17	0x11	0	0	0	1	0	0	0	1	LED 143	LED 142	LED 141	LED 140	LED 139	LED 138	LED 137	LED 136

In the blink register (see Table 9) every single LED can be set to blink. The blink period is set in the display option register (see Display Option Register (0x03) on page 23).

Table 9. LEDs Blink Register Format for 2 Matrixes Setup

Matrix	Current Source	Adress									Data							
		HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
A	CS0	0x12	0	0	0	1	0	0	1	0	LED 7	LED 6	LED 5	LED 4	LED 3	LED 2	LED 1	LED 0
B	CS9	0x13	0	0	0	1	0	0	1	1	LED 15	LED 14	LED 13	LED 12	LED 11	LED 10	LED 9	LED 8
A	CS1	0x14	0	0	0	1	0	1	0	0	LED 23	LED 22	LED 21	LED 20	LED 19	LED 18	LED 17	LED 16
B	CS10	0x15	0	0	0	1	0	1	0	1	LED 31	LED 30	LED 29	LED 28	LED 27	LED 26	LED 25	LED 24
A	CS2	0x16	0	0	0	1	0	1	1	0	LED 39	LED 38	LED 37	LED 36	LED 35	LED 34	LED 33	LED 32
B	CS11	0x17	0	0	0	1	0	1	1	1	LED 47	LED 46	LED 45	LED 44	LED 43	LED 42	LED 41	LED 40
A	CS3	0x18	0	0	0	1	1	0	0	0	LED 55	LED 54	LED 53	LED 52	LED 51	LED 50	LED 49	LED 48
B	CS12	0x19	0	0	0	1	1	0	0	1	LED 63	LED 62	LED 61	LED 60	LED 59	LED 58	LED 57	LED 56
A	CS4	0x1A	0	0	0	1	1	0	1	0	LED 71	LED 70	LED 69	LED 68	LED 67	LED 66	LED 65	LED 64
B	CS13	0x1B	0	0	0	1	1	0	1	1	LED 79	LED 78	LED 77	LED 76	LED 75	LED 74	LED 73	LED 72
A	CS5	0x1C	0	0	0	1	1	1	0	0	LED 87	LED 86	LED 85	LED 84	LED 83	LED 82	LED 81	LED 80
B	CS14	0x1D	0	0	0	1	1	1	0	1	LED 95	LED 94	LED 93	LED 92	LED 91	LED 90	LED 89	LED 88
A	CS6	0x1E	0	0	0	1	1	1	1	0	LED 103	LED 102	LED 101	LED 100	LED 99	LED 98	LED 97	LED 96
B	CS15	0x1F	0	0	1	1	1	1	1	1	LED 111	LED 110	LED 109	LED 108	LED 107	LED 106	LED 105	LED 104
A	CS7	0x20	0	0	1	0	0	0	0	0	LED 119	LED 118	LED 117	LED 116	LED 115	LED 114	LED 113	LED 112
B	CS16	0x21	0	0	1	0	0	0	0	1	LED 127	LED 126	LED 125	LED 124	LED 123	LED 122	LED 121	LED 120
A	CS8	0x22	0	0	1	0	0	0	1	0	LED 135	LED 134	LED 133	LED 132	LED 131	LED 130	LED 129	LED 128
B	CS17	0x23	0	0	1	0	0	0	1	1	LED 143	LED 142	LED 141	LED 140	LED 139	LED 138	LED 137	LED 136

In the intensity register (see Table 10) the brightness of every single LED can bes set via a 8bit PWM (255 steps).

Table 10. LEDs Intensity Register Format for 2 Matrixes Setup

Matrix	Current Source		Adress									Data							
			HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
A	CS0	LED0	0x24	0	0	1	0	0	1	0	0	255 steps for intensity each single LED							
		LED1	0x25	0	0	1	0	0	1	0	1								
		LED2	0x26	0	0	1	0	0	1	1	0								
		LED3	0x27	0	0	1	0	0	1	1	1								
		LED4	0x28	0	0	1	0	1	0	0	0								
		LED5	0x29	0	0	1	0	1	0	0	1								
		LED6	0x2A	0	0	1	0	1	0	1	0								
		LED7	0x2B	0	0	1	0	1	0	1	1								
B	CS9	LED8	0x2C	0	0	1	0	1	1	0	0								
		LED9	0x2D	0	0	1	0	1	1	0	1								
		LED10	0x2E	0	0	1	0	1	1	1	0								
		LED11	0x2F	0	0	1	0	1	1	1	1								
		LED12	0x30	0	0	1	1	0	0	0	0								
		LED13	0x31	0	0	1	1	0	0	0	1								
		LED14	0x32	0	0	1	1	0	0	1	0								
		LED15	0x33	0	0	1	1	0	0	1	1								
A	CS1	LED16	0x34	0	0	1	1	0	1	0	0	255 steps for intensity each single LED							
		LED17	0x35	0	0	1	1	0	1	0	1								
		LED18	0x36	0	0	1	1	0	1	1	0								
		LED19	0x37	0	0	1	1	0	1	1	1								
		LED20	0x38	0	0	1	1	1	0	0	0								
		LED21	0x39	0	0	1	1	1	0	0	1								
		LED22	0x3A	0	0	1	1	1	0	1	0								
		LED23	0x3B	0	0	1	1	1	0	1	1								
B	CS10	LED24	0x3C	0	0	1	1	1	1	0	0								
		LED25	0x3D	0	0	1	1	1	1	0	1								
		LED26	0x3E	0	0	1	1	1	1	1	0								
		LED27	0x3F	0	0	1	1	1	1	1	1								
		LED28	0x40	0	1	0	0	0	0	0	0								
		LED29	0x41	0	1	0	0	0	0	0	1								
		LED30	0x42	0	1	0	0	0	0	1	0								
		LED31	0x43	0	1	0	0	0	0	1	1								

Table 10. LEDs Intensity Register Format for 2 Matrixes Setup

Matrix	Current Source		Adress									Data							
			HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
A	CS2	LED32	0x44	0	1	0	0	0	1	0	0	255 steps for intensity each single LED							
		LED33	0x45	0	1	0	0	0	1	0	1								
		LED34	0x46	0	1	0	0	0	1	1	0								
		LED35	0x47	0	1	0	0	0	1	1	1								
		LED36	0x48	0	1	0	0	1	0	0	0								
		LED37	0x49	0	1	0	0	1	0	0	1								
		LED38	0x4A	0	1	0	0	1	0	1	0								
		LED39	0x4B	0	1	0	0	1	0	1	1								
B	CS11	LED40	0x4C	0	1	0	0	1	1	0	0								
		LED41	0x4D	0	1	0	0	1	1	0	1								
		LED42	0x4E	0	1	0	0	1	1	1	0								
		LED43	0x4F	0	1	0	0	1	1	1	1								
		LED44	0x50	0	1	0	1	0	0	0	0								
		LED45	0x51	0	1	0	1	0	0	0	1								
		LED46	0x52	0	1	0	1	0	0	1	0								
		LED47	0x53	0	1	0	1	0	0	1	1								
.....																			
A	CS8	LED128	0xA4	1	0	1	0	0	1	0	0	255 steps for intensity each single LED							
		LED129	0xA5	1	0	1	0	0	1	0	1								
		LED130	0xA6	1	0	1	0	0	1	1	0								
		LED131	0xA7	1	0	1	0	0	1	1	1								
		LED132	0xA8	1	0	1	0	1	0	0	0								
		LED133	0xA9	1	0	1	0	1	0	0	1								
		LED134	0xAA	1	0	1	0	1	0	1	0								
		LED135	0xAB	1	0	1	0	1	0	1	1								
B	CS17	LED136	0xAC	1	0	1	0	1	1	0	0								
		LED137	0xAD	1	0	1	0	1	1	0	1								
		LED138	0xAE	1	0	1	0	1	1	1	0								
		LED139	0xAF	1	0	1	0	1	1	1	1								
		LED140	0xB0	1	0	1	1	0	0	0	0								
		LED141	0xB1	1	0	1	1	0	0	0	1								
		LED142	0xB2	1	0	1	1	0	0	1	0								
		LED143	0xB3	1	0	1	1	0	0	1	1								

3 Blocks with 5x6 LED Matrix

The AS1119 can be configured to control three seperated blocks of LEDs matrixes. This must be set via the bit D0 in the AS1119 config register (see AS1119 Config Register (0x04) on page 24).

Figure 22. 5x6 LED Matrix with 3 Matrixes

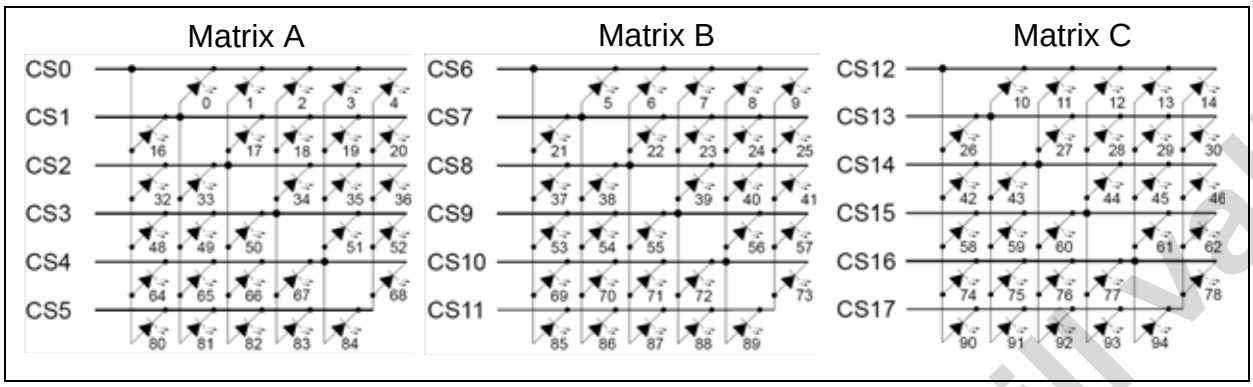


Table 11. Dataframe Adress Structure for 3 Matrixes

			Adresses (HEX code)											
Current Source			On / Off			Blink			Intensity					
Matrix			Matrix			Matrix			Matrix					
A	B	C	A	B	C	A	B	C	A	B	C			
CS0	CS6	CS12	0x00	0x01		0x12	0x13		0x24-0x2B	0x2C-0x33				
CS1	CS7	CS13	0x02	0x03		0x14	0x15		0x34-0x3B	0x3C-0x43				
CS2	CS8	CS14	0x04	0x05		0x16	0x17		0x44-0x4B	0x4C-0x53				
CS3	CS9	CS15	0x06	0x07		0x18	0x19		0x54-0x5B	0x5C-0x63				
CS4	CS10	CS16	0x08	0x09		0x1A	0x1B		0x64-0x6B	0x6C-0x73				
CS5	CS11	CS17	0x0A	0x0B		0x1C	0x1D		0x74-0x7B	0x7C-0x83				

In Table 12 it's described which databit represents which LED in the matrix. Per default all databits are '0', meaning no LED is on. A '1' puts the LED on.

Note: LED A01 is the first LED of the Current Source 0 in the Matrix A. LED B01 is the first LED of the Current Source 6 in the Matrix B. and so on.

Table 12. LEDs ON/OFF Register Format for 3 Matrixes Setup

Current Source	Adress									Data							
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
CS0, CS6, CS12	0x00	0	0	0	0	0	0	0	0	LED 7	LED 6	LED 5	LED 4	LED 3	LED 2	LED 1	LED 0
	0x01	0	0	0	0	0	0	0	1	X	LED 14	LED 13	LED 12	LED 11	LED 10	LED 9	LED 8
CS1, CS7, CS13	0x02	0	0	0	0	0	0	1	0	LED 23	LED 22	LED 21	LED 20	LED 19	LED 18	LED 17	LED 16
	0x03	0	0	0	0	0	0	1	1	X	LED 30	LED 29	LED 28	LED 27	LED 26	LED 25	LED 24
CS2, CS8, CS14	0x04	0	0	0	0	0	1	0	0	LED 39	LED 38	LED 37	LED 36	LED 35	LED 34	LED 33	LED 32
	0x05	0	0	0	0	0	1	0	1	X	LED 46	LED 45	LED 44	LED 43	LED 42	LED 41	LED 40

Table 12. LEDs ON/OFF Register Format for 3 Matrixes Setup

Current Source	Adress									Data							
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
CS3, CS9, CS15	0x06	0	0	0	0	0	1	1	0	LED 55	LED 54	LED 53	LED5 2	LED 51	LED 50	LED 49	LED 48
	0x07	0	0	0	0	0	1	1	1	X	LED 62	LED 61	LED 60	LED 59	LED 58	LED 57	LED 56
CS4, CS10, CS16	0x08	0	0	0	0	1	0	0	0	LED 71	LED 70	LED 69	LED6 8	LED 67	LED 66	LED 65	LED 64
	0x09	0	0	0	0	1	0	0	1	X	LED 78	LED 77	LED 76	LED 75	LED 74	LED 73	LED 72
CS5, CS11, CS17	0x0A	0	0	0	0	1	0	1	0	LED 87	LED 86	LED 85	LED8 4	LED 83	LED 82	LED 81	LED 80
	0x0B	0	0	0	0	1	0	1	1	X	LED 94	LED 93	LED 92	LED 91	LED 90	LED 89	LED 88

In the blink register (see Table 13) every single LED can be set to blink. The blink period is set in the display option register (see Display Option Register (0x03) on page 23).

Table 13. LEDs Blink Register Format for 3 Matrixes Setup

Current Source	Adress									Data							
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
CS0, CS6, CS12	0x12	0	0	0	0	0	0	0	0	LED 7	LED 6	LED 5	LED 4	LED 3	LED 2	LED 1	LED 0
	0x12	0	0	0	0	0	0	0	1	X	LED 14	LED 13	LED 12	LED 11	LED 10	LED 9	LED 8
CS1, CS7, CS13	0x14	0	0	0	0	0	0	1	0	LED 23	LED 22	LED 21	LED 20	LED 19	LED 18	LED 17	LED 16
	0x15	0	0	0	0	0	0	1	1	X	LED 30	LED 29	LED 28	LED 27	LED 26	LED 25	LED 24
CS2, CS8, CS14	0x16	0	0	0	0	0	1	0	0	LED 39	LED 38	LED 37	LED 36	LED 35	LED 34	LED 33	LED 32
	0x17	0	0	0	0	0	1	0	1	X	LED 46	LED 45	LED 44	LED 43	LED 42	LED 41	LED 40
CS3, CS9, CS15	0x18	0	0	0	0	0	1	1	0	LED 55	LED 54	LED 53	LED5 2	LED 51	LED 50	LED 49	LED 48
	0x19	0	0	0	0	0	1	1	1	X	LED 62	LED 61	LED 60	LED 59	LED 58	LED 57	LED 56
CS4, CS10, CS16	0x1A	0	0	0	0	1	0	0	0	LED 71	LED 70	LED 69	LED6 8	LED 67	LED 66	LED 65	LED 64
	0x1B	0	0	0	0	1	0	0	1	X	LED 78	LED 77	LED 76	LED 75	LED 74	LED 73	LED 72
CS5, CS11, CS17	0x1C	0	0	0	0	1	0	1	0	LED 87	LED 86	LED 85	LED8 4	LED 83	LED 82	LED 81	LED 80
	0x1D	0	0	0	0	1	0	1	1	X	LED 94	LED 93	LED 92	LED 91	LED 90	LED 89	LED 88

In the intensity register (see Table 14) the brightness of every single LED can be set via a 8bit PWM (255 steps).

Table 14. LEDs Intensity Register Format for 3 Matrixes Setup

Matrix	Current Source		Address									Data							
			HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
A	CS0	LED0	0x24	0	0	1	0	0	1	0	0	255 steps for intensity each single LED							
		LED1	0x25	0	0	1	0	0	1	0	1								
		LED2	0x26	0	0	1	0	0	1	1	0								
		LED3	0x27	0	0	1	0	0	1	1	1								
		LED4	0x28	0	0	1	0	1	0	0	0								
B	CS6	LED5	0x29	0	0	1	0	1	1	0	0								
		LED6	0x2A	0	0	1	0	1	1	0	1								
		LED7	0x2B	0	0	1	0	1	1	1	0								
		LED8	0x2C	0	0	1	0	1	1	1	1								
		LED9	0x2D	0	0	1	1	0	0	0	0								
C	CS12	LED10	0x2E	0	0	1	0	1	1	0	0								
		LED11	0x2F	0	0	1	0	1	1	0	1								
		LED12	0x30	0	0	1	0	1	1	1	0								
		LED13	0x31	0	0	1	0	1	1	1	1								
		LED14	0x32	0	0	1	1	0	0	0	0								
A	CS1	LED16	0x34	0	0	1	1	0	1	0	0								
		LED17	0x35	0	0	1	1	0	1	0	1								
		LED18	0x36	0	0	1	1	0	1	1	0								
		LED19	0x37	0	0	1	1	0	1	1	1								
		LED20	0x38	0	0	1	1	1	0	0	0								
B	CS7	LED21	0x39	0	0	1	1	1	0	0	1								
		LED22	0x3A	0	0	1	1	1	0	1	0								
		LED23	0x3B	0	0	1	1	1	0	1	1								
		LED24	0x3C	0	0	1	1	1	1	0	0								
		LED25	0x3D	0	0	1	1	1	1	0	1								
C	CS13	LED26	0x3E	0	0	1	1	1	1	1	0								
		LED27	0x3F	0	0	1	1	1	1	1	1								
		LED28	0x40	0	1	0	0	0	0	0	0								
		LED29	0x41	0	1	0	0	0	0	0	1								
		LED30	0x42	0	1	0	0	0	0	1	0								
A	CS2	LED32	0x44	0	1	0	0	0	1	0	0								
		LED33	0x45	0	1	0	0	0	1	0	1								
		LED34	0x46	0	1	0	0	0	1	1	0								
		LED35	0x47	0	1	0	0	0	1	1	1								
		LED36	0x48	0	1	0	0	1	0	0	0								
B	CS8	LED37	0x49	0	1	0	0	1	0	0	1								
		LED38	0x4A	0	1	0	0	1	0	1	0								
		LED39	0x4B	0	1	0	0	1	0	1	1								
		LED40	0x4C	0	1	0	0	1	1	0	0								
		LED41	0x4D	0	1	0	0	1	1	0	1								
C	CS14	LED42	0x4E	0	1	0	0	1	1	1	0								
		LED43	0x4F	0	1	0	0	1	1	1	1								
		LED44	0x50	0	1	0	1	0	0	0	0								
		LED45	0x51	0	1	0	1	0	0	0	1								
		LED46	0x52	0	1	0	1	0	0	1	0								
.....																			

Table 14. LEDs Intensity Register Format for 3 Matrixes Setup

Matrix	Current Source		Address									Data							
			HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
A	CS5	LED80	0xA4	1	0	1	0	0	1	0	0	255 steps for intensity each single LED							
		LED81	0xA5	1	0	1	0	0	1	0	1								
		LED82	0xA6	1	0	1	0	0	1	1	0								
		LED83	0xA7	1	0	1	0	0	1	1	1								
		LED84	0xA8	1	0	1	0	1	0	0	0								
B	CS11	LED85	0xA9	1	0	1	0	1	0	0	1								
		LED86	0xAA	1	0	1	0	1	0	1	0								
		LED87	0xAB	1	0	1	0	1	0	1	1								
		LED88	0xAC	1	0	1	0	1	1	0	0								
		LED89	0xAD	1	0	1	0	1	1	0	1								
C	CS17	LED90	0xAE	1	0	1	0	1	1	1	0								
		LED91	0xAF	1	0	1	0	1	1	1	1								
		LED92	0xB0	1	0	1	1	0	0	0	0								
		LED93	0xB1	1	0	1	1	0	0	0	1								
		LED94	0xB2	1	0	1	1	0	0	1	0								

Control-Registers

The AS1119 devices contain 13 control-registers which are listed in Table 15. All registers are selected using a 8-bit address word, and communication is done via the serial interface. Select the Control Register via the Register Selection (see Table 6 on page 13).

Table 15. Control Register Address Map

Register Name	HEX	Register Address								Register Data
		A7	A6	A5	A4	A3	A2	A1	A0	D7:D0
Frame Address	0x00	0	0	0	0	0	0	0	0	(see Table 16 on page 22)
Frame Play	0x01	0	0	0	0	0	0	0	1	(see Table 17 on page 22)
Frame Time	0x02	0	0	0	0	0	0	1	0	(see Table 18 on page 23)
Display Option	0x03	0	0	0	0	0	0	1	1	(see Table 19 on page 23)
AS1119 Config	0x04	0	0	0	0	0	1	0	0	(see Table 20 on page 24)
Current Source Matrix A	0x05	0	0	0	0	0	1	0	1	(see Table 21 on page 25)
Current Source Matrix B	0x06	0	0	0	0	0	1	1	0	
Current Source Matrix C	0x07	0	0	0	0	0	1	1	1	
Chare Pump Config	0x08	0	0	0	0	1	0	0	0	(see Table 22 on page 25)
Open/Short Test	0x09	0	0	0	0	1	0	0	1	(see Table 23 on page 26)
Shutdown	0x0A	0	0	0	0	1	0	1	0	(see Table 24 on page 26)
I²C Interface Monitoring	0x0B	0	0	0	0	1	0	1	1	(see Table 25 on page 26)
Open/Short Status	0x0C	0	0	0	0	1	1	0	0	(see Table 26 on page 27)
AS1119 Status	0x0D	0	0	0	0	1	1	0	1	(see Table 27 on page 27)

Frame Address Register (0x00)

In this register it must be set if a picture or a movie is to display on the LED matrix. Also the start address of the the movie or the picture which should be displayed must be set within this register. The default setting of this register is 0x00.

Table 16. Frame Address Register Format

0x00 Frame Address Register				
Bit	Bit Name	Default	Access	Bit Description
7	Play Movie	0	R/W	0: no movie 1: play movie
6	Display Picture	0	R/W	0: no picture 1: display picture
5:3	Start Address for movie	000	R/W	000: Frame 0 001: Frame 1 010: Frame 2 011: Frame 3 100: Frame 4 101: Frame 5
2:0	Address of Picture	000	R/W	000: Frame 0 001: Frame 1 010: Frame 2 011: Frame 3 100: Frame 4 101: Frame 5

Note: If bit 6 and 7 are set to '1' the AS1119 will play the movie first and than the picture will be displayed.

Frame Play Register (0x01)

Within this register two movie play obtions can be set. Per default this register is set to 0x00.

- The number of frames which are displayed in one movie.
- The number of loops to play in a movie.

Table 17. Frame Play Register Format

0x01 Frame Play Register				
Bit	Bit Name	Default	Access	Bit Description
7:6	-	00	n/a	
5:3	Number of loops played in one movie	000	R/W	000: no loop 001: 1 loop 010: 2 loops 011: 3 loops 100: 4 loops 101: 5 loops 110: 6 loops 111: play endless
2:0	Number of frames to played in a movie	000	R/W	000: 1 frame 001: 2 frames 010: 3 frames 011: 4 frames 100: 5 frames 101: 6 frames

Note: To stopp a movie in *play endless* mode, bits D5:D3 have to be set to a value between 000 to 110.

Frame Time Register (0x02)

Every single frame in a movie is displayed for a certain time before the next frame is displayed. This time can be set within this register with 4 bits. The stated values in Table 18 are typical values. Per default this register is set to 0x00.

Table 18. Frame Time Register Format

0x02 Frame Time Register				
Bit	Bit Name	Default	Access	Bit Description
7:4	-	00	n/a	
3:0	Delay between frame change in a movie	000	R/W	0000:play frame only one time 0001: 32.5ms 0010: 65ms 0011: 97.5ms 0100: 130ms 0101: 162.5ms 0110: 195ms 0111: 227.5ms 1000: 260ms 1001: 292.5ms 1010: 325ms 1011:357.5ms 1100: 390ms 1101: 422.5ms 1110: 455ms 1111: 487.5ms

Display Option Register (0x03)

With the scan-limit it can be controlled how many digits are displayed in each matrix. When all 18 digits in the 2 matrix configuration are displayed, the display scan rate is 430Hz (typ.). If the number of digits to display is reduced, the update frequency is increased. Per default this register is set to 0x07.

Table 19. Display Option Register Format

0x03 Display Option Register				
Bit	Bit Name	Default	Access	Bit Description
7	-	0	n/a	
6	intensity setting	0	R/W	0: use intensity setting of frame 0 for all other frames 1: set the intensity of each frame independently
5	start with blink	0	R/W	0: start blinking with LED on 1: start blinking with LED off
4	blink period	0	R/W	0: 1.5s 1: 3s

Table 19. Display Option Register Format

0x03 Display Option Register						
Bit	Bit Name	Default	Access	Bit Description		
3:0	number of displayed current sources in one frame (scan-limit)	0111	R/W	2 Matrix setting		
				Matrix A	Matrix B	
				0000: CS0 0001: CS0 to CS1 0010: CS0 to CS2 0011: CS0 to CS3 0100: CS0 to CS4 0101: CS0 to CS5 0110: CS0 to CS6 0111: CS0 to CS7 1000: CS0 to CS8	0000: CS0 0001: CS0 to CS1 0010: CS0 to CS2 0011: CS0 to CS3 0100: CS0 to CS4 0101: CS0 to CS5 0110: CS0 to CS6 0111: CS0 to CS7 1000: CS0 to CS8	
				3 Matrixes setting		
				Matrix A	Matrix B	Matrix C
				0000: CS0 0001: CS0 to CS1 0010: CS0 to CS2 0011: CS0 to CS3 0100: CS0 to CS4 0101: CS0 to CS5	0000: CS6 0001: CS6 to CS7 0010: CS6 to CS8 0011: CS6 to CS9 0100: CS6 to CS10 0101: CS6 to CS11	0000: CS12 0001: CS12 to CS13 0010: CS12 to CS14 0011: CS12 to CS15 0100: CS12 to CS16 0101: CS12 to CS17

AS1119 Config Register (0x04)

In this register the configuration of the charge pumps is set to 2 or 3 blocks. The direction of the SYNC_IN/SYNC_OUT pin (input or output) is also set. Per default this register is set to 0x00.

Table 20. AS1119 Config Register Format

0x04 AS1119 Config Register				
Bit	Bit Name	Default	Access	Bit Description
7:3	-	00000	n/a	
2:1	Sync	00	R/W	00: internal oscillator is system-clk. No synchronisation on pin B6. Tie pin to high or low. 01: internal oscillator is system-clk. System-clk is available on pin B6 for synchronization. (output) 10: internal oscillator is disabled. Pin B6 is used as clk input for system-clk. 11: do not use
0	Matrix Configuration	0	R/W	0: 3 matrixes (à 5x6 LED-Matrix) 1: 2 matrixes (à 8x9 LED-Matrix)

Current Source Block A, B, C Registers (0x05, 0x06, 0x07)

Within this registers the current for every single LED in one block can be set from 0mA to 31mA in 255 steps (8 bits). Per default this register is set to 0x00.

Table 21. Current Sourcer Register Format

Current Source Registers				
Bit	Bit Name	Default	Access	Bit Description
Address 0x05				
7:0	Analog Current Matrix A	0000000	R/W	00000000: 0mA 11111111: 31mA
Address 0x06				
7:0	Analog Current Matrix B	0000000	R/W	00000000: 0mA 11111111: 31mA
Address 0x07				
7:0	Analog Current Matrix C	0000000	R/W	00000000: 0mA 11111111: 31mA

Charge Pump Config Register (0x08)

In this register the characteristics of the Charge Pump can be set. By the use of the charge pump (bit 0) the supply voltage for the LEDs can be boosted to 1.5- or 2-times of the device supply (V_{DD}), if required. Additionally bit1 offers the option to check periodically if the LED supply can be reduced again during operation. This period is defined by bit 4:2.

Alternatively, the LED supply can be (re)set to V_{DD} by disabling the charge pump for a short time. In this case the period can be defined by user (application). Per default this register is set to 0x1E.

Table 22. AS1119 Config Register Format

0x08 Charge Pump Config Register				
Bit	Bit Name	Default	Access	Bit Description
7:5	-	000	n/a	
4:2	Timeframe for reduce supply test	111	R/W	000: 0.3s 001: 0.5s 010: 0.8s 011: 1.0s 100: 1.3s 101: 1.6s 110: 1.8s 111: 2.1s
1	Reduce supply option	1	R/W	0: reduce supply option off 1: reduce supply option on
0	Charge Pump	0	R/W	0: Charge Pump disable 1: Charge Pump enable

Open/Short Test Register (0x09)

The AS1119 can detect open and shorted LEDs. To start this test the according bits have to be set. The result of the open/short test is written in the Open/Short staturs register (see Table 26). The default setting of this register is 0x00.

Table 23. Open/Short Test Register Format

0x09 Open/Short Test Register				
Bit	Bit Name	Default	Access	Bit Description
7:2	-	000000	n/a	
1	Full Matrix	0	R/W	0: all LED's are available in the matrixes 1: not all LED's are available in the matrixes
0	Error detection	0	R/W	0: start test 1: no test

The Open/Short test is only checking LEDs which are defined as ON in the Data Frame Registers Table 8 on page 14 or Table 12 on page 18. With the bit1 (Full Matrix) all LEDs of the matrixes will be defined as ON and will be tested intependently from the content of the Data Frame Register. The function of bit1 is only available during the open/short test and not during normal operation.

Shutdown Register (0x0A)

The default setting of this register is 0x00. To get the AS1119 operational the bit D0 has to be set to '1'.

Table 24. Shutdown Register Format

0x0A Shutdown Register				
Bit	Bit Name	Default	Access	Bit Description
7:1	-	0000000	n/a	
0	shutdown	0	R/W	0: shutdown 1: normal operation

I²C Interface Monitoring Register (0x0B)

This register is used to monitor the activity on the I²C bus. If a deadlock situation occurs (e.g. the bus SDA pin is pulled to low and no communication is possible) the chip will reset the I²C interface and the master is able to start the communication again.

The time window for the reset of the interface of the AS1119 can bes set via 7 bits from 256µs to 33ms. The default setting of this register is 0xFF.

Table 25. I²C Interface Monitoring Register Format

0x0B I²C Interface Monitoring Register				
Bit	Bit Name	Default	Access	Bit Description
7:2	Time out window	1111111	R/W	0 to 127 => 1 to 128x256µs 0000000: 256µs 1111111: 32.7ms
0	I²C Monitor	1	R/W	0: I²C monitoring off 1: I²C monitoring on

Open/Short Status Register (0x0C)

This is a read only register. Within this register the result of the open/short test can be read out. It's also stated if the test is completed or still running. The default setting of this register is 0x00.

Table 26. Open/Short Status Register Format

0x0C Open/Short Status Register				
Bit	Bit Name	Default	Access	Bit Description
7	-	0	n/a	
6	status	0	R	0: no test 1: test ongoing
5	short test result Matrix C	0	R	0: no error detected 1: short in Matrix C
4	short test result Matrix B	0	R	0: no error detected 1: short in Matrix B
3	short test result Matrix A	0	R	0: no error detected 1: short in Matrix A
2	open test result Matrix C	0	R	0: no error detected 1: open in Matrix C
1	open test result Matrix B	0	R	0: no error detected 1: open in Matrix B
0	open test result Matrix A	0	R	0: no error detected 1: open in Matrix A

AS1119 Status Register (0x0D)

This is a read only register. From this register the actual status of the AS1119 can be read out. The default setting of this register is 0x00. After an read command the bits 5:4 are set to '0' again automatically.

Table 27. AS1119 Status Register Register Format

0x0D AS1119 Status Register				
Bit	Bit Name	Default	Access	Bit Description
7	-	0	n/a	
6	Movie status		R	0: no movie is playing 1: one movie is playing
5:4	Interrupt	00	R	00: no Interrupt triggered 01: POR triggered an interrupt [1] 10: I²C monitor triggered an interrupt 11: both (I²C and POR) triggered an interrupt
3:0	actual displayed frame	000	R	000: frame 0 001: frame 1 010: frame 2 011: frame 3 100: frame 4 101: frame 5

1. The power-on reset is part of the start sequence, hence after start-up this bit is also set.

10 Package Drawings and Markings

Figure 23. 36-pin WL-CSP Marking

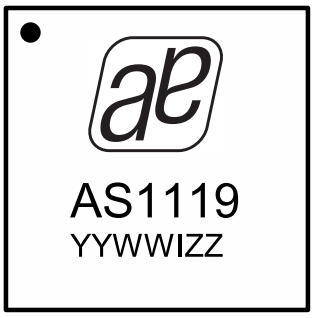
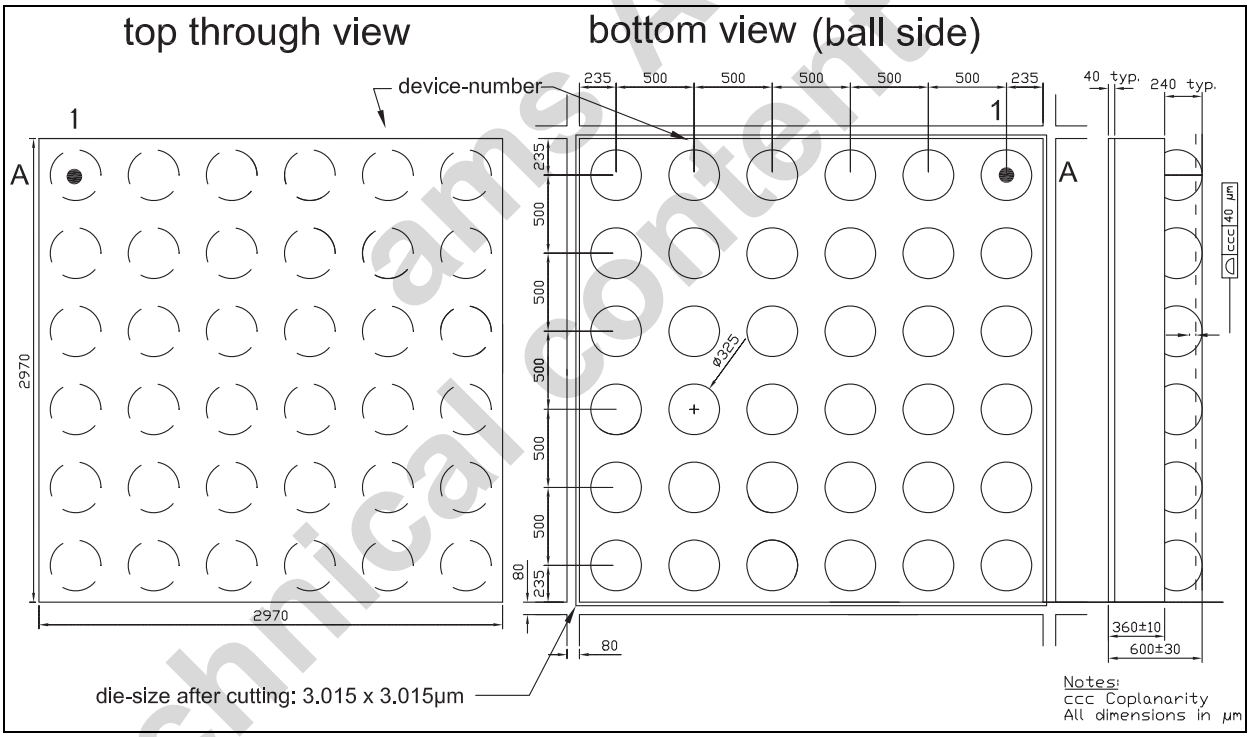


Table 28. Packaging Code YYWWIZZ

YY	WW	I	ZZ
last two digits of the current year	manufacturing week	plant identifier	free choice / traceability code

Figure 24. 36-pin WL-CSP



11 Ordering Information

The devices are available as the standard products shown in Table 29.

Table 29. Ordering Information

Ordering Code	Marking	Desciption	Delivery Form	Package
AS1119-BWLT	AS1119	144-LED Cross-Plexing Driver with 320mA Charge-Pump	Tape and Reel	36-pin WL-CSP

Note: All products are RoHS compliant and austriamicrosystems green.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

Technical Support is found at http://www.austriamicrosystems.com/Technical-Support

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austriamicrosystems

Contact Information

Headquarters

austriamicrosystems AG
Tobelbaderstrasse 30
A-8141 Unterpremstaetten, Austria

Tel: +43 (0) 3136 500 0
Fax: +43 (0) 3136 525 01

For Sales Offices, Distributors and Representatives, please visit:

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  Skype ameyasales1 ameyasales2

- ### Customer Service :

  Email service@ameya360.com

- ### Partnership :

  Tel +86 (21) 64016692-8333

  Email mkt@ameya360.com