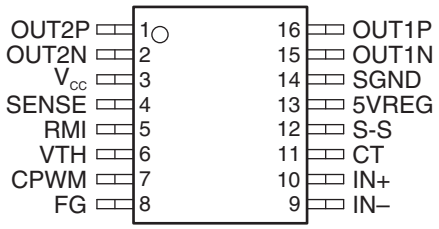
VARIABLE-SPEED SINGLE-PHASE FULL-WAVE FAN-MOTOR PRE-DRIVER

FEATURES

- **Single-Phase Full-Wave Driving Pre-Driver**
  - **Low saturation drive using external PNP-NMOS enables high efficiency low power consumption drive**
- **Variable Speed Control Possible With External PWM Input**
  - **Separately excited upper direct PWM (f = 30 kHz) control method ensures quiet speed control**
- **Current Limiter Circuit Incorporated**
  - **Chopper type current limiting made at startup and during lock**
- **Reactive Current Cut Circuit Incorporated**
  - **Reactive current before phase change is cut to enable silent and low-consumption drive**
- **Minimum-Speed Setting Pin**
  - **Minimum speed can be set with external resistor**
- **Soft-Start Setting Pin**
- **Lock Protection and Automatic Reset Circuits Incorporated**
- **Rotation Speed Detection (FG) and Lock Detection (RD) Output**
- **Thermal Shutdown Circuit Incorporated**

PW PACKAGE
(TOP VIEW)



DESCRIPTION/ ORDERING INFORMATION

The TMP815 is a single-phase bipolar driving motor pre-driver with a variable-speed function that is compatible with an external PWM signal. With few external parts, a highly efficient and quiet variable-drive fan motor with low power consumption can be achieved.

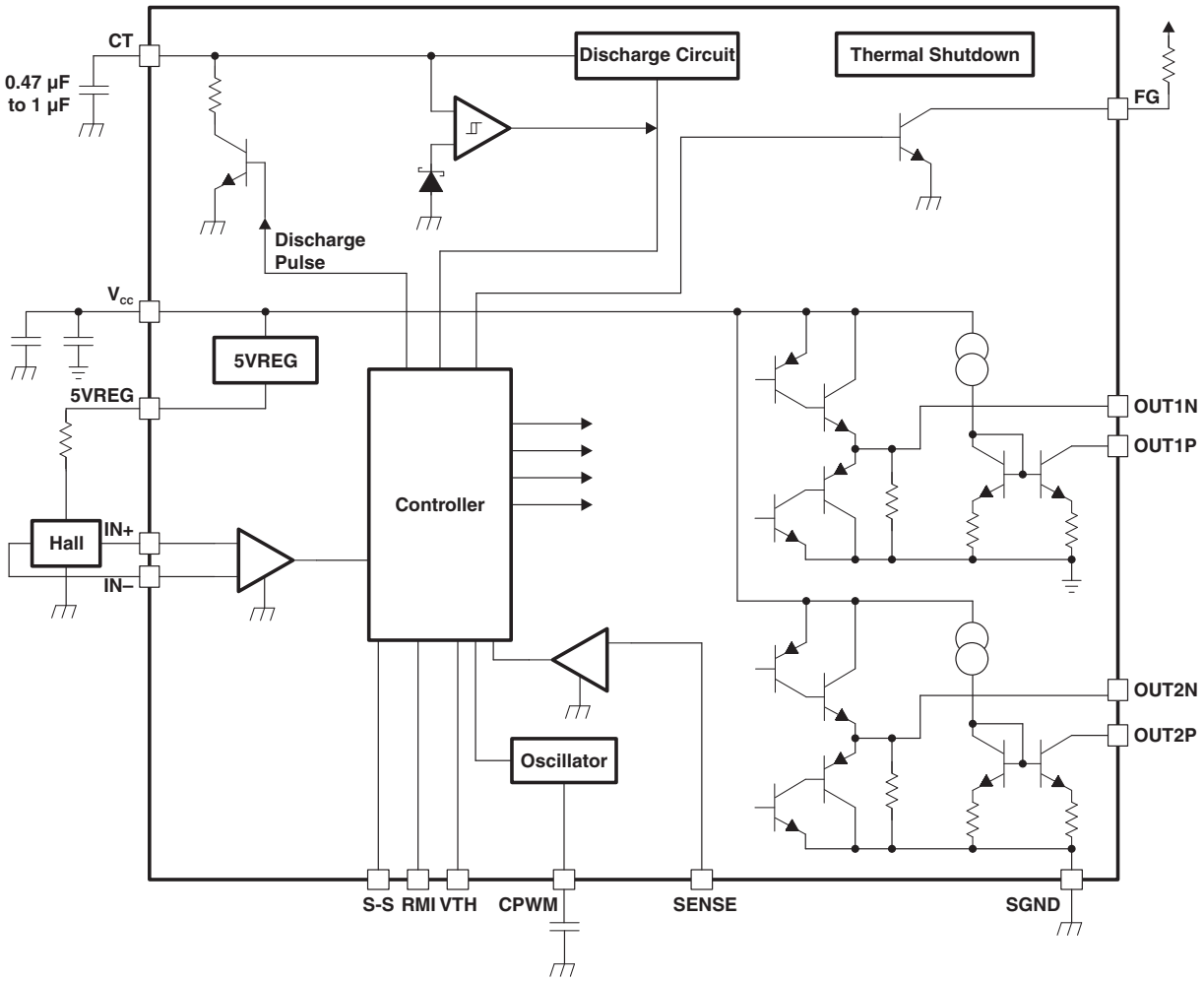
This device is best suited for driving of the servers requiring large air flow and large current or the fan motors of consumer appliances.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–30°C to 95°C	TSSOP – PW	Reel of 2000	TMP815PWR	TMP815

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/package.

BLOCK DIAGRAM



DRIVE LOCK TRUTH TABLE(1)

CPWM = H, VTH = RMI = S-S = L

IN–	IN+	CT	OUT1P	OUT1N	OUT2P	OUT2N	FG	MODE
H	L	L	L	L	OFF	H	L	OUT1 → 2 drive
L	H	L	OFF	H	L	L	OFF	OUT2 → 1 drive
H	L	H	OFF	L	OFF	H	L	Lock protection
L	H	H	OFF	H	OFF	L	OFF	

(1) For VTH, RMI, and S-S pins, see Figure 2.

SPEED CONTROL TRUTH TABLE(1)

CT = S-S = L

VTH, RMI	CPWM	IN–	IN+	OUT1P	OUT1N	OUT2P	OUT2N	MODE
L	H	H	L	L	L	OFF	H	OUT1 → 2 Drive
L	H	L	H	OFF	H	L	L	OUT2 → 1 Drive
H	L	H	L	OFF	L	OFF	H	Regeneration mode
H	L	L	H	OFF	H	OFF	L	

(1) For VTH, RMI, and S-S pins, see Figure 2.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
OUT2P	1	O	Upper-side driver output
OUT2N	2	O	Lower-side driver output
V_{CC}	3		Power supply For the power stabilization capacitor on the signal side (see *2 in Figure 1), use the capacitance of 1 µF or more. Connect V_{CC} and GND with a thick and short pattern. For the power stabilization capacitor on the power side (see *3 in Figure 1), use the capacitance of 1 µF or more. Connect the power supply on the power side and GND with a thick and short pattern.
SENSE	4	I	Current limiting detection (see *8 in Figure 1) When the pin voltage exceeds 0.2 V, the current is limited, and the operation enters the lower regeneration mode. Connect to GND if not used.
RMI	5	I	Minimum speed setting (see *6 in Figure 1) If the device power supply is likely to be turned off first when the pin is used with external power supply, insert a current-limiting resistor to prevent inflow of large current (also applies to VTH terminal). Connect to 5VREG with a pullup resistor if not used.
VTH	6	I	Speed control (see *7 in Figure 1) For control with pulse input, insert a current-limiting resistor and use the pin with a frequency of 20 kHz to 100 kHz (20 kHz to 50 kHz recommended). For the control method, see Figure 2. Connect to GND if not used (at full speed).
CPWM	7	O	Connection to capacitor for generation of PWM basic frequency (see *5 in Figure 1) CP = 220 pF causes oscillation at f = 30 kHz, which is the basic frequency of PWM. As this is used also for the current-limiting canceling signal, be sure to connect the capacitor even when speed control is not used.
FG	8	O	Rotation speed detection pin (see *9 in Figure 1) This is an open-collector output, which can detect the rotation speed from the FG output according to the phase change over. Keep this pin open when not used.
IN–	9	I	Hall input (*4)
IN+	10	I	Hall input. Make connecting traces as short as possible to prevent carrying of noise. To futher limit noise, insert a capacitor between IN+ and IN–. The Hall input circuit is a comparator having a hysteresis of 15 mV. Also includes a soft-switch section with ±30-mV input-signal differential voltage. It is recommended that the Hall input level is a minimum of 100 mV_{p-p}.
CT	11	O	Connection to the lock detection capacitor (see *10 in Figure 1) The constant current charge and discharge circuits cause locking when the pin voltage rises to 3 V and unlocking when pin voltage falls to 1.1 V. Connect to GND when not used (when locking is not necessary).
S-S	12	I	Connection to the soft-start setting capacitor (see *11 in Figure 1) Connect the capacitor between S-S and 5VREG to set the soft-start time, according to the capacitance that is chosen (see Figure 3 and Figure 4). Connect to GND when not used.
5VREG	13	O	5-V regulator output
SGND	14		System ground (see *1 in Figure 1) Connection to the control-circuit power-supply system
OUT1N	15	O	Lower-side driver output
OUT1P	16	O	Upper-side driver output

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
V_{CC}	Supply voltage		18	V
V_{OUT}	Output voltage	OUT1P, OUT1N, OUT2P, OUT2N	18	V
I_{OUT}	Continuous output current	OUT1N, OUT2N	–20	mA
		OUT1P, OUT2P	20	
V_{VTH} V_{RMI}	Input voltage	VTH, RMI	7	V
V_{S-S}	Input/output voltage	S-S	7	V
V_{FG}	Output voltage	FG	19	V
I_{FG}	Continuous output current	FG	10	mA
I_{5VREG}	Continuous output current	5VREG	–20	mA
θ_{JA}	Package thermal impedance(2)		108	°C/W
T_{stg}	Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

T_A = 25°C

		MIN	MAX	UNIT
V_{CC}	Supply voltage	6	16	V
V_{VTH} V_{RMI}	VTH, RMI input voltage	0	5	V
V_{ICM}	Hall input common phase input voltage	0.2	3	V
T_A	Operating free-air temperature	–30	95	°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 12 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{5VREG}	Output voltage	5VREG	I_{5VREG} = –5 mA	4.8	4.95	5.1	V
V_{LIM}	Current-limiting voltage	SENSE		185	200	215	mV
V_{CPWMH}	High-level output voltage	CPWM		2.8	3	3.2	V
V_{CPWML}	Low-level output voltage			0.9	1.1	1.3	V
I_{CPWM1}	Charge current		V_{CPWM} = 0.5 V	24	30	36	µA
I_{CPWM2}	Discharge current		V_{CPWM} = 3.5 V	21	27	33	µA
f_{PWM}	Oscillation frequency		CP = 220 pF		30		kHz
V_{CTH}	High-level output voltage	CT		2.8	3	3.2	V
V_{CTL}	Low-level output voltage			0.9	1.1	1.3	V
I_{CT1}	Charge current			1.6	2	2.5	µA
I_{CT2}	Discharge current			0.16	0.2	0.25	µA
R_{CT}	Charge/discharge current ratio			8	10	12	
I_{S-S}	Discharge current	S-S	V_{S-S} = 1 V	0.4	0.5	0.6	µA
V_{ONH}	High-level output voltage	OUT_N	I_{OH} = –10 mA	V_{CC} – 1	V_{CC} – 0.85		V
V_{ONL}	Low-level output voltage		I_{OL} = 10 mA		0.9	1	V
V_{OPL}	Low-level output voltage	OUT_P	I_{OL} = 10 mA		0.5	0.65	V
V_{HN}	Hall input sensitivity	IN+, IN-	IN+, IN– differential voltage (including offset and hysteresis)		±10	±20	mV
V_{FG}	Low-level output voltage	FG	I_{FG} = 5 mA		0.15	0.3	V
I_{FGL}	Output leakage current		V_{FG} = 19 V			20	µA
I_{VTH} I_{RMI}	Bias current	VTH, RMI	$V_{CPWM} = V_{VTH} = V_{RMI}$ = 2 V, V_{CT} = 0 V			0.1	µA
I_{CC}	Supply current	V_{CC}	During drive	4	7.5	9.5	mA
			During lock protection	4	7.5	9.5	

APPLICATION INFORMATION

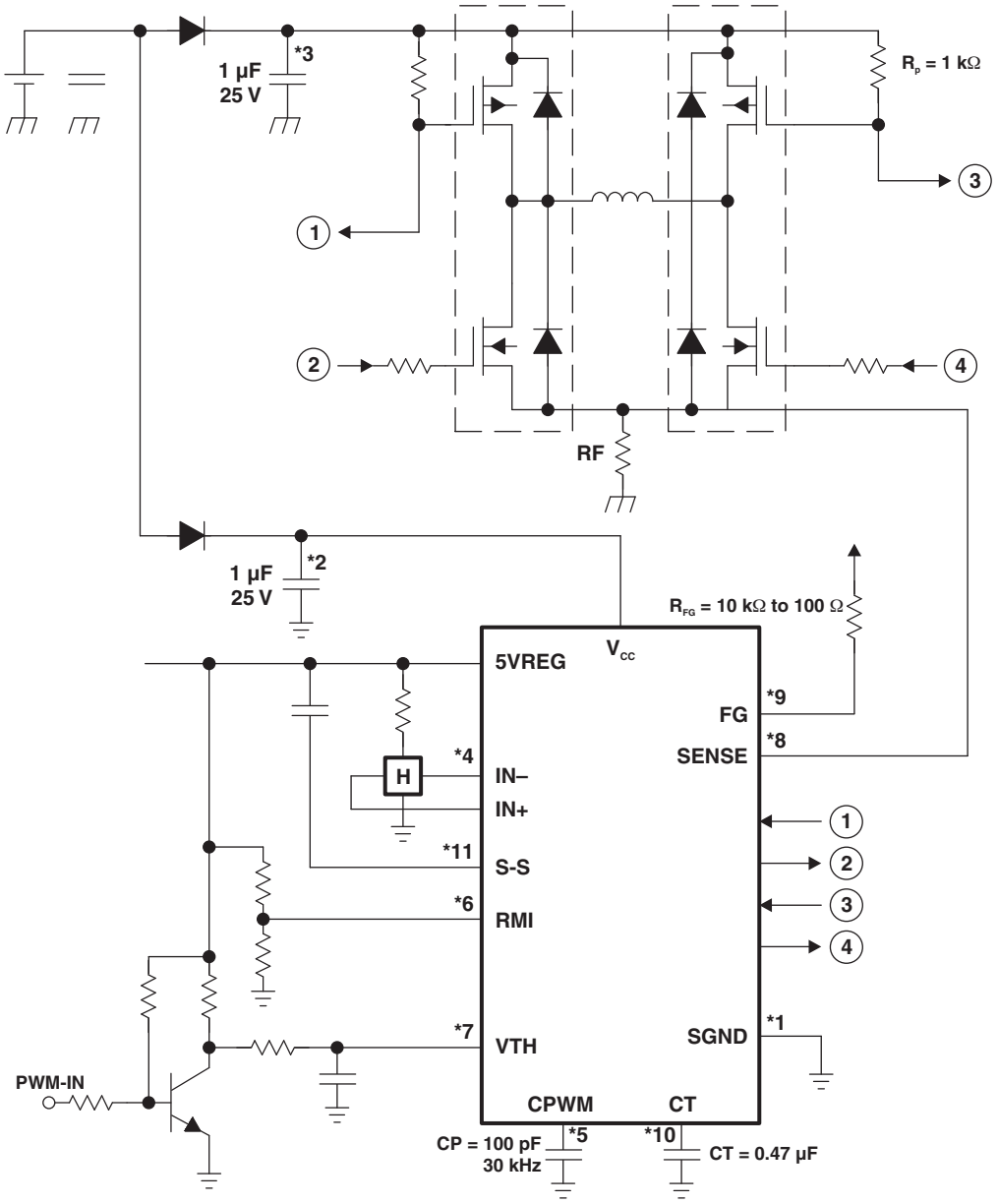
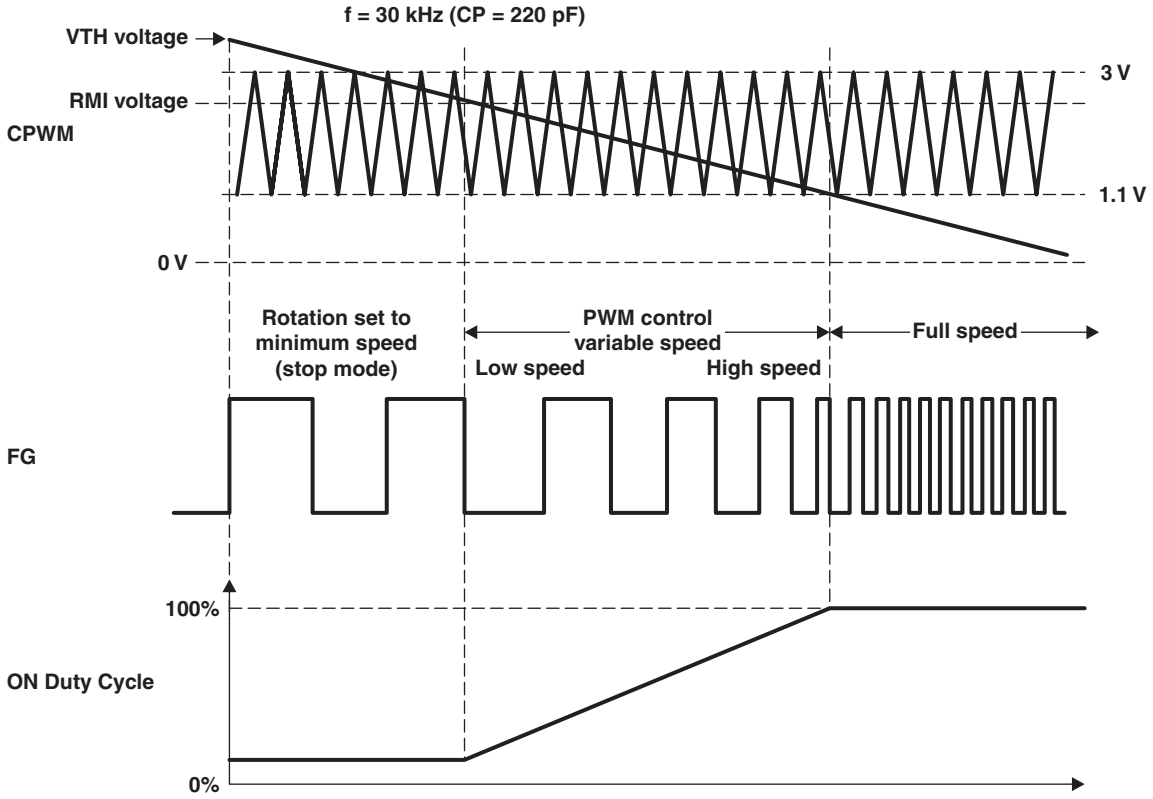


Figure 1. 12-V Sample Application Circuit



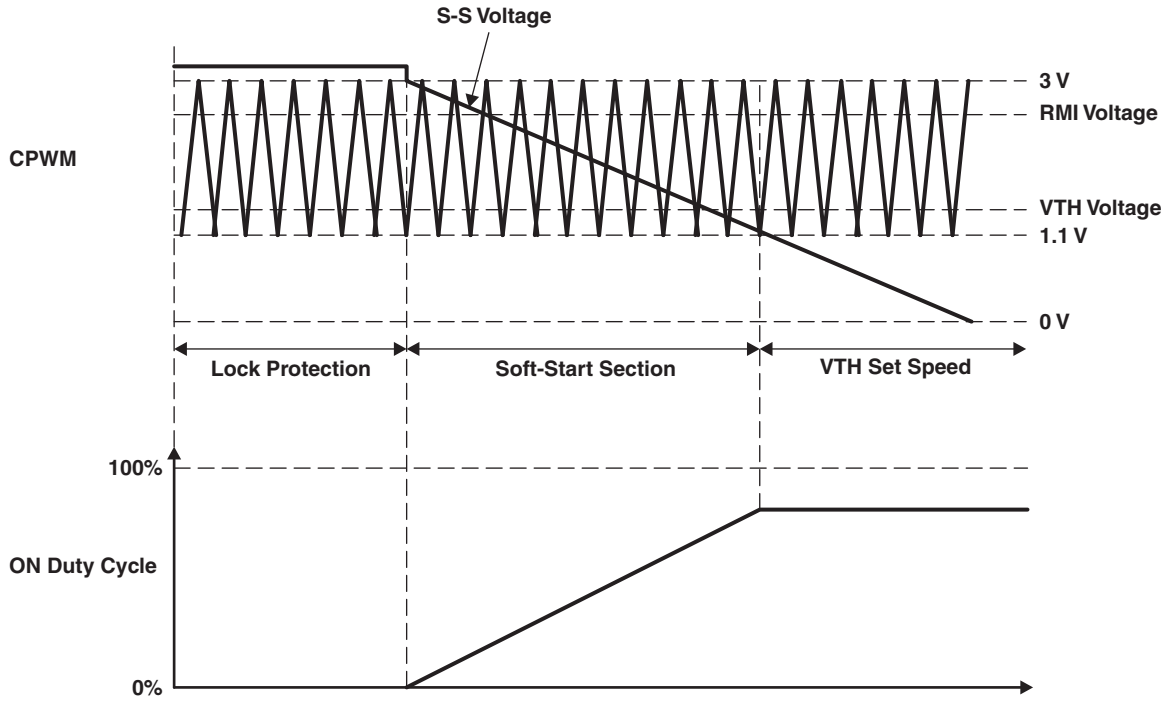
A. Minimum speed setting (stop) mode. The low speed fan rotation occurs at the minimum speed set with the RMI pin. When the minimum speed is not set (RMI pin pulled up to 5VREG), the motor stops.

B. Low ↔ high speed. PWM control is made by comparing the CPWM oscillation voltage (1.1 V ↔ 3 V) and VTH voltage. Both upper and lower output TRs are turned ON when the VTH voltage is low. The upper output TR is turned OFF when the VTH voltage is high, regenerating the coil current in the lower TR. Therefore, as the VTH voltage decreases, the output on duty cycle increases, causing an increase in the coil current, raising the motor rotation speed. The rotation speed can be monitored with the FG output.

C. Full-speed mode. The full-speed mode becomes effective with the VTH voltage of 1.65 V or less. (VTH must be equal to GND when the speed control is not used.)

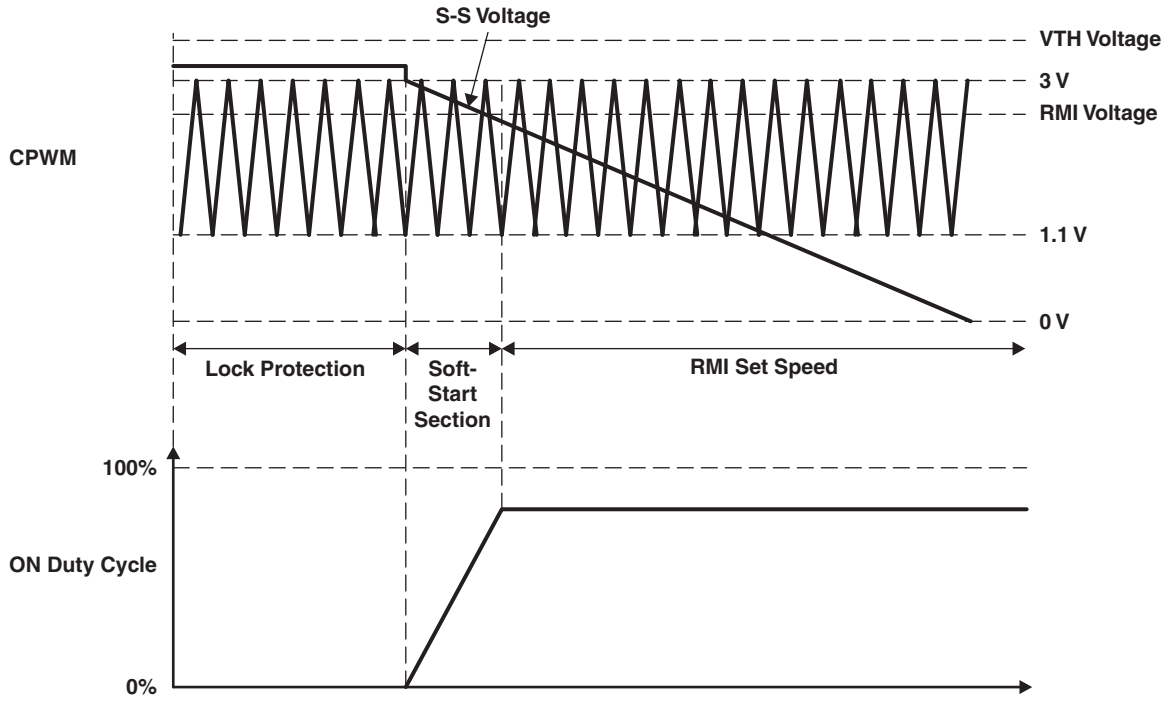
D. PWM-IN input disconnection mode. The full-speed mode becomes effective when the VTH voltage is 1.1 V or less. Set VTH = GND when the speed control is not used.

Figure 2. Speed Control Timing



A. Adjust the S-S pin voltage gradient by means of the capacitance of the oscillator between the S-S pin and 5VREG. Recommended capacitance is 0.1 μF to 1 μF.

Figure 3. Soft-Start Timing (VTH < RMI)

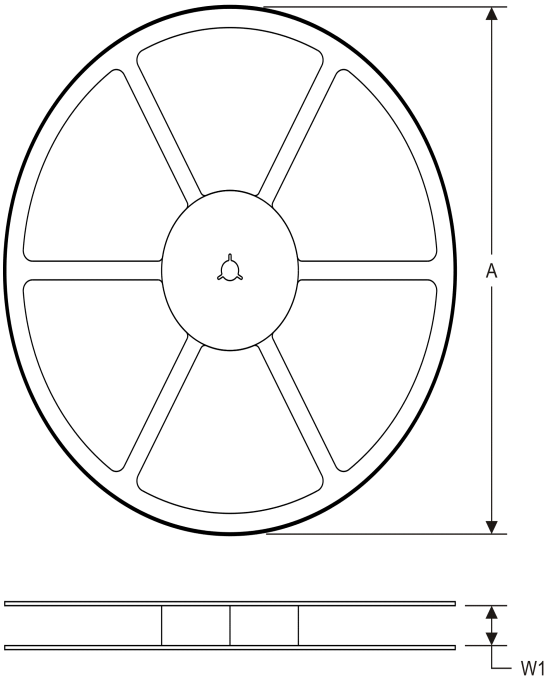


A. Adjust the S-S pin voltage gradient by means of the capacitance of the oscillator between the S-S pin and 5VREG. Recommended capacitance is 0.1 μF to 1 μF.

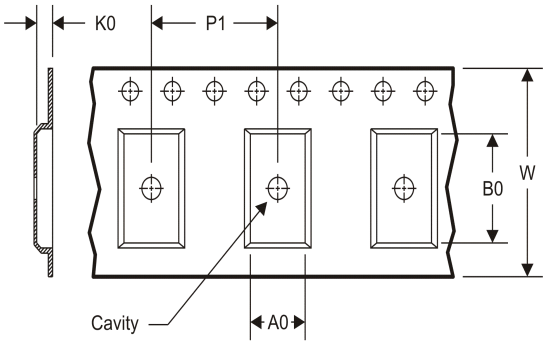
Figure 4. Soft-Start Timing (VTH > RMI)

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



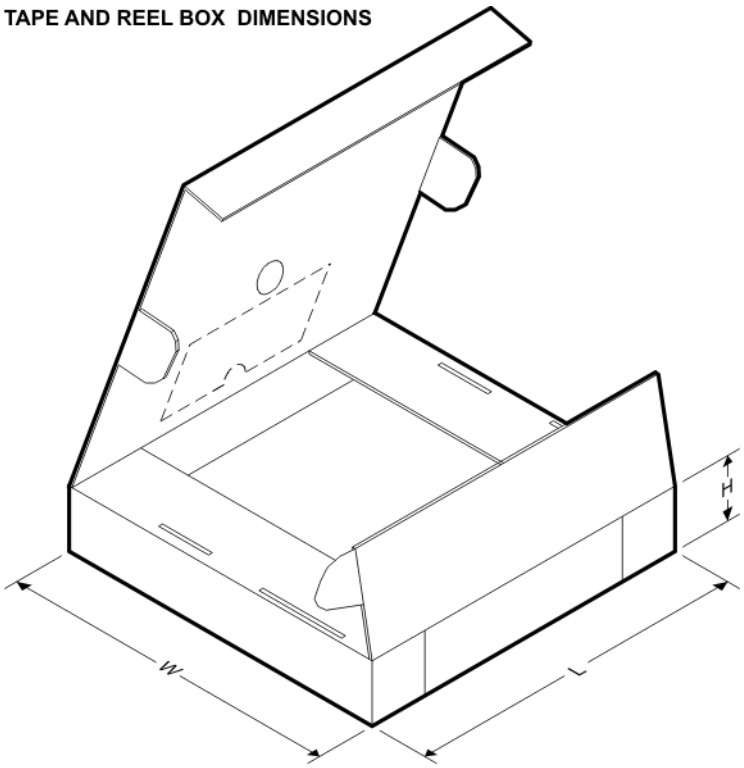
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP815PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

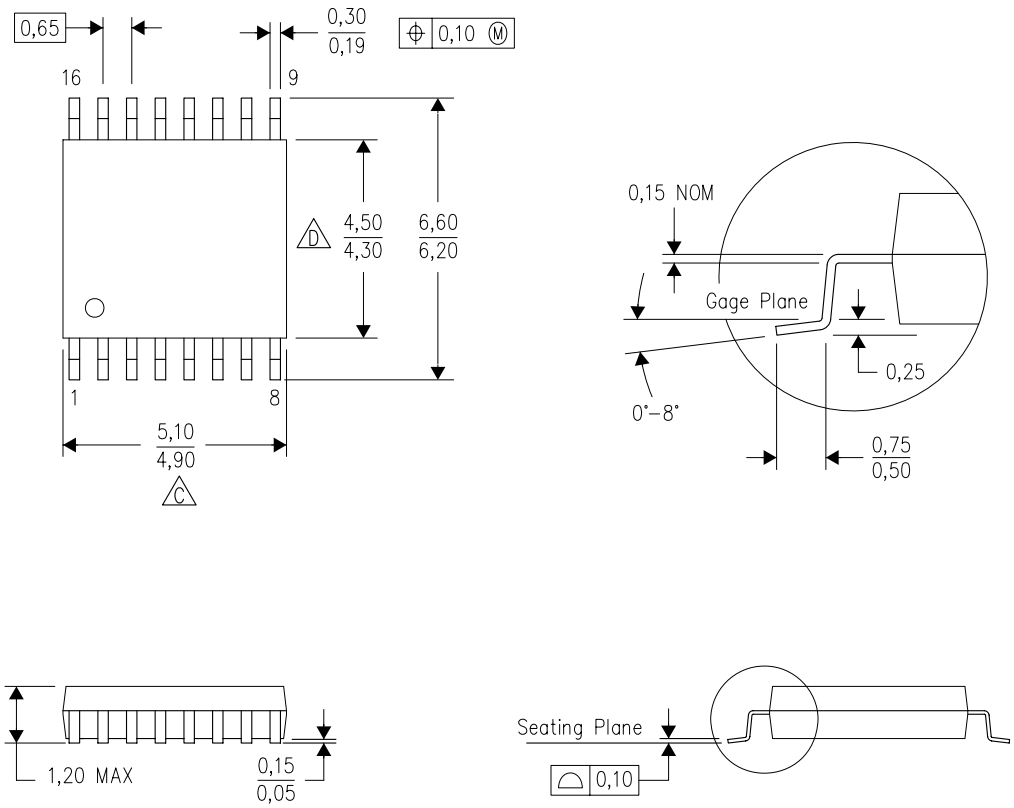
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP815PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



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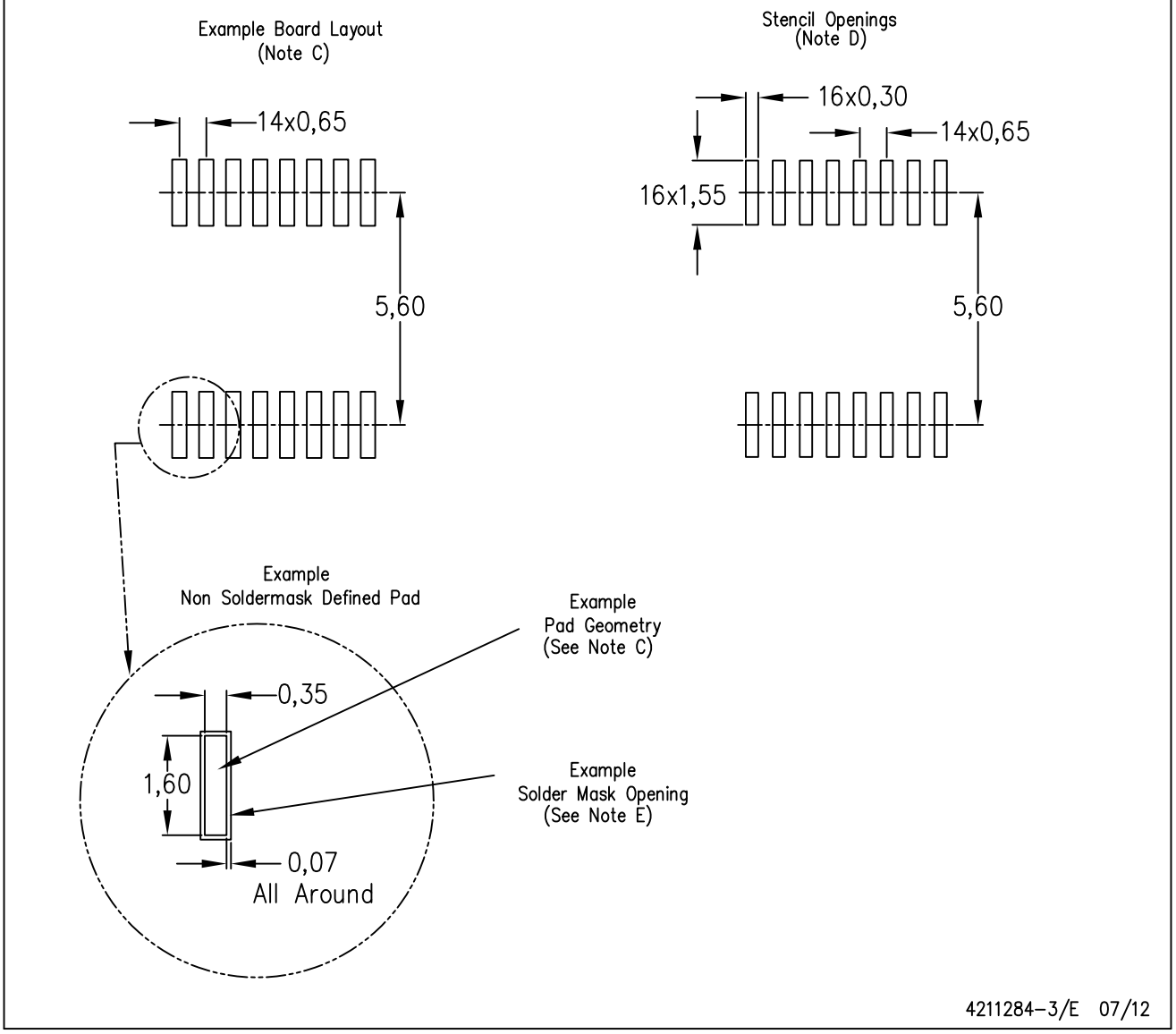
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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