

AN-2200 LM5017 Evaluation Board

1 Introduction

The LM5017 evaluation board provides the design engineer with a fully functional buck regulator, employing the constant on-time (COT) operating principle. This evaluation board provides a 10 V output over an input range of 12.5 V to 100 V.

The board's specifications are:

- Input Range: 12.5 V to 95 V, transients up to 100 V (absolute maximum)
- Output Voltage: 10 V
- Output Current: 600 mA
- Nominal Switching Frequency \sim 200 kHz
- Measured Efficiency: 92.4% at 400 mA and $V_{IN} = 24$ V
- Board size: 2.95 in. x 1.8 in.

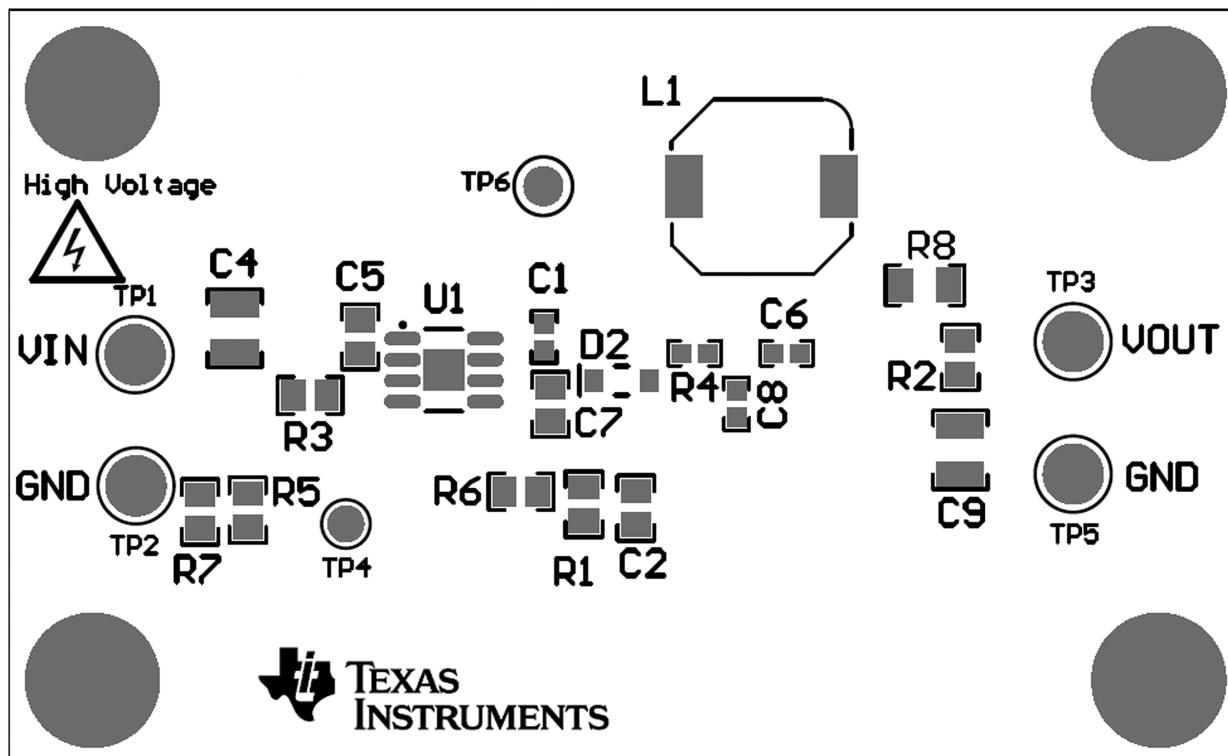


Figure 1. Evaluation Board (Top View)

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2 Theory of Operation

When the circuit is in regulation, the buck switch is turned on each cycle for a time determined by R3 and V_{IN} according to [Equation 1](#):

$$T_{ON} = \frac{10^{-10} \times R3}{V_{IN}} \quad (1)$$

The on-time of this evaluation board ranges from 5.56 μ s at $V_{IN} = 12$ V to 702 ns at $V_{IN} = 95$ V. The on-time varies inversely with input voltage. At the end of each on-time, the buck switch is off for at least 144 ns. In normal operation, the off-time is much longer. During the off-time, the load current is supplied by the output capacitor (C9). When the output voltage falls sufficiently that the voltage at FB is below 1.225 V, the regulation comparator initiates a new on-time period. For stable, fixed frequency operation, a minimum of 25 mV of ripple is required at FB to switch the regulation comparator. For a more detailed block diagram and a complete description of the various functional blocks, see the *LM5017 100V, 600mA Constant On-Time Synchronous Buck Regulator Data Sheet (SNVS783)*.

3 UVLO

The UVLO resistors (R5, R7) are selected using [Equation 2](#):

$$V_{IN(HYS)} = I_{HYS}R_5 \quad (2)$$

and [Equation 3](#):

$$V_{IN(UVLO,rising)} = 1.225V \times \left(\frac{R_5}{R_7} + 1 \right) \quad (3)$$

On this evaluation board, $R5 = 127$ k Ω and $R7 = 14.0$ k Ω , resulting in UVLO rising threshold at $V_{IN} = 12$ V and a hysteresis of 2.5 V.

[Figure 2](#) shows the evaluation board schematic.

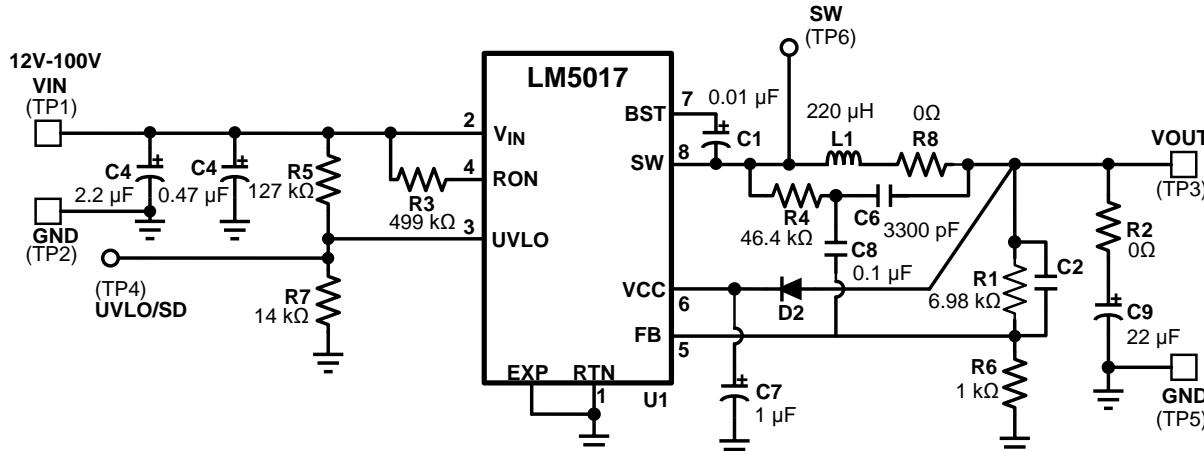


Figure 2. Complete Evaluation Board Schematic for LM5017-Based Buck Converter

4 Board Connection and Start-up

The input connections are made to the TP1 (V_{IN}) and TP2 (GND) terminals. The load is connected to the TP3 (V_{OUT}) AND TP5 (GND) terminals. Ensure the wires are adequately sized for the intended load current. Before start-up, a voltmeter should be connected to the input and output terminals. The load current should be monitored with an ammeter or a current probe. It is recommended that the input voltage be increased gradually to 12 V, at which time the output voltage should be 10 V. If the output voltage is correct, increase the input voltage as desired and proceed with evaluating the circuit. DO NOT EXCEED 100 V AT V_{IN} .

Table 1. Bill of Materials (BOM)

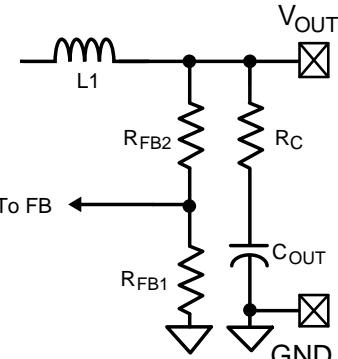
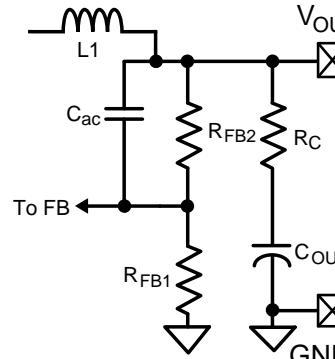
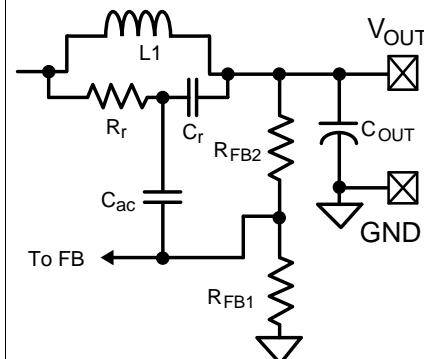
| Item | Description | Mfg. Part Number | Package | Value |
|------|--------------------------|-------------------------------|-------------------|--------------------------|
| U1 | Sync Switching Regulator | Texas Instruments, LM5017 | SO PowerPAD-8 | 100 V, 0.6A |
| L1 | Inductor | Wurth, 7447714221 | 10 mm x 10 mm | 220 μ H, 1.2A |
| | Alternate Inductor | Bourns, SRR1260-221k | 12.5 mm x 12.5 mm | 220 μ H, 1.38A |
| | Alternate Inductor | Coilcraft, MSS1246-224K | 12.3 mm x 12.3 mm | 220 μ H, 1.4A |
| D2 | Diode | Central Semi, CMMH1-40 | SOD-123F | 40 V, 1A |
| | Alternate Diode | NXP, BAS40H, 115 | SOD123F | 40 V, 120 mA |
| C1 | Ceramic Capacitor | Murata, GRM188R71C103KA01D | 0603 | 0.01 μ F, 16V, X7R |
| C2 | | | | NA |
| C4 | Ceramic Capacitor | Murata, GRM32ER72A225KA35L | 1210 | 2.2 μ F, 100 V, X7R |
| C5 | Ceramic Capacitor | Murata, GRM21BR72A474KA73L | 0805 | 0.47 μ F, 100 V, X7R |
| C6 | Ceramic Capacitor | TDK, C1608X7R1H332K | 0603 | 3300 pF, 50 V, X7R |
| C7 | Ceramic Capacitor | TDK, C2012X7R1C105K | 0805 | 1 μ F, 16 V, X7R |
| C8 | Ceramic Capacitor | Murata, GRM188R71E104KA01D | 0603 | 0.1 μ F, 25 V, X7R |
| C9 | Ceramic Capacitor | Murata, GRM32ER71E226KE15L | 1210 | 22 μ F, 25 V, X7R |
| R1 | Resistor | Vishay-Dale, CRCW08056K98FKEA | 0805 | 6.98k Ω , 1% |
| R2 | Resistor | Panasonic, ERJ-6GEY0R00V | 0805 | 0 Ω |
| R3 | Resistor | Panasonic, ERJ-6ENF4993V | 0805 | 499k Ω , 1% |
| R4 | Resistor | Panasonic, ERJ-3EKF4642V | 0603 | 46.4k Ω , 1% |
| R5 | Resistor | Vishay-Dale, CRCW0805127KFKEA | 0805 | 127k Ω , 1% |
| R6 | Resistor | Vishay-Dale, CRCW08051K00FKEA | 0805 | 1.0k Ω , 1% |
| R7 | Resistor | Vishay-Dale, CRCW080514K0FKEA | 0805 | 14.0k Ω , 1% |
| R8 | Resistor | Yageo, RC1206JR-070RL | 1206 | 0 Ω |

5 Ripple Configuration

The LM5017 is a COT buck and requires adequate ripple at feedback (FB) node. Three commonly used ripple generation methods are shown in [Table 2](#).

LM5017 evaluation board has been supplied with minimum ripple configuration (Type 3), but can be configured to Type 1 or Type 2 with modifications as suggested in [Table 2](#).

Table 2. Ripple Configuration

| Type 1 Lowest Cost Configuration | Type 2 Reduced Ripple Configuration | Type 3 Minimum Ripple Configuration |
|--|--|--|
|  |  |  |
| <p>R4, C6, C8 open. Select R2:</p> $R2 \geq \frac{40 \text{ mV}}{\Delta I_{L(\text{MIN})}} \times \frac{V_{\text{OUT}}}{V_{\text{REF}}} \quad (4)$ | <p>R4 open, C6 = 0 Ω. Select R2 and C8:</p> $C8 \geq \frac{5}{f_{\text{sw}} (R_1 \parallel R_6)}$ $R2 \geq \frac{40 \text{ mV}}{\Delta I_L} \quad (5)$ | <p>R2 = 0 Ω. Select R4, C6, and C8:</p> <p>C6 = 3300 pF C8 = 100 nF</p> $R4 \times C6 \leq \frac{(V_{\text{IN}(\text{MIN})} - V_{\text{OUT}}) T_{\text{ON}}}{40 \text{ mV}} \quad (6)$ |

6 Performance Curves

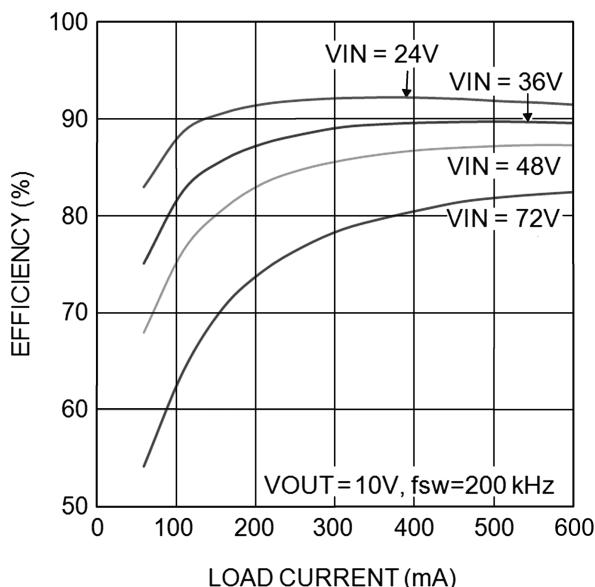


Figure 3. Efficiency vs Load Current

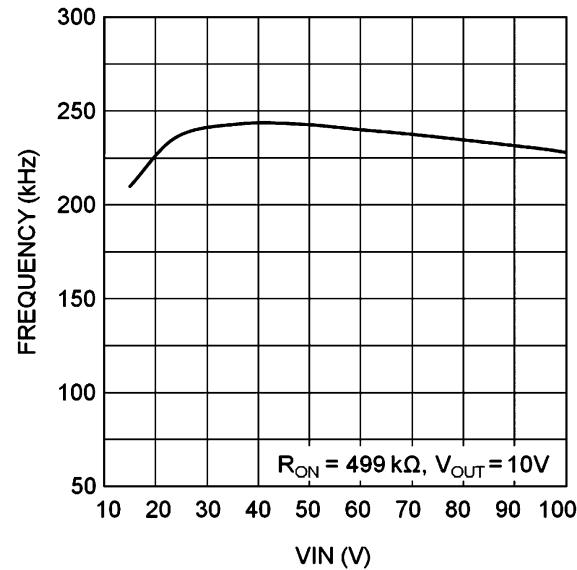


Figure 4. Frequency vs Input Voltage

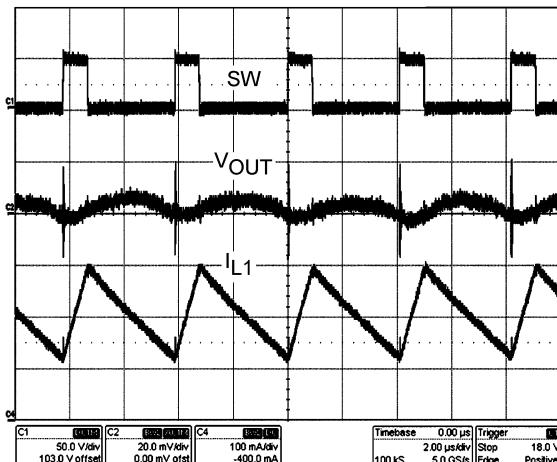


Figure 5. Typical Switching Waveform (V_{IN} = 48 V, I_{out} = 200 mA)

7 PC Board Layout

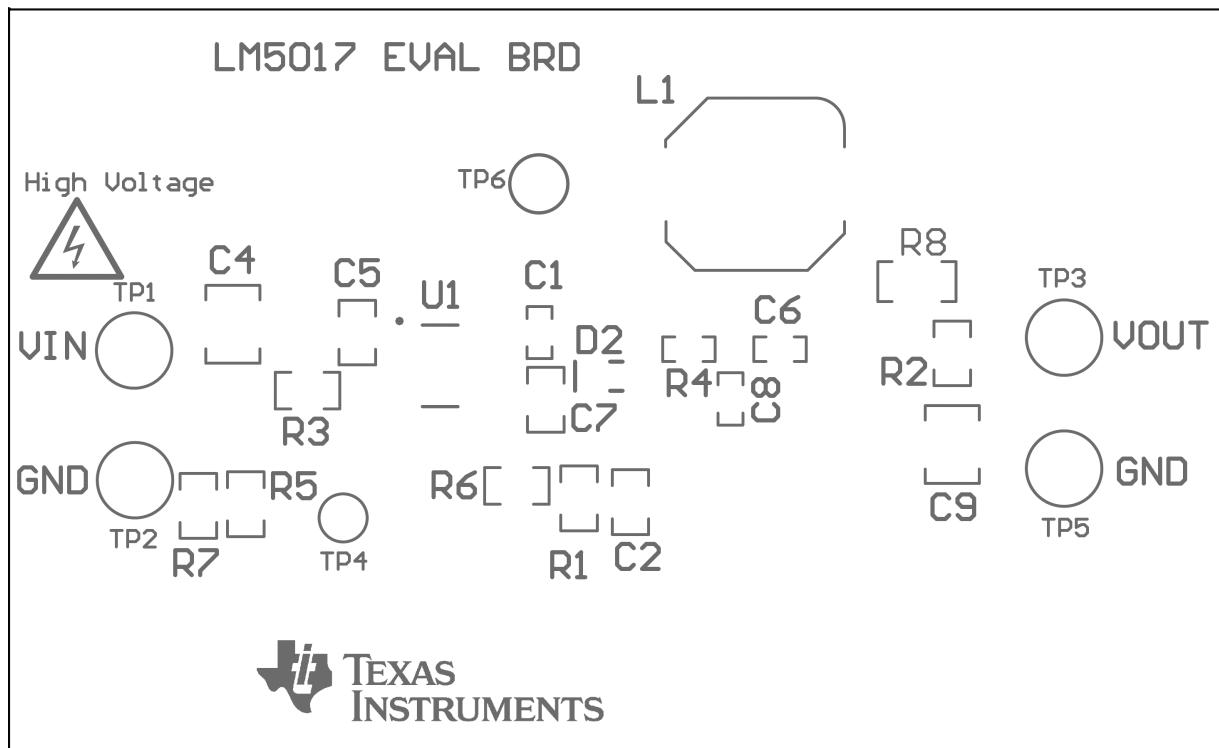


Figure 6. Board Silkscreen

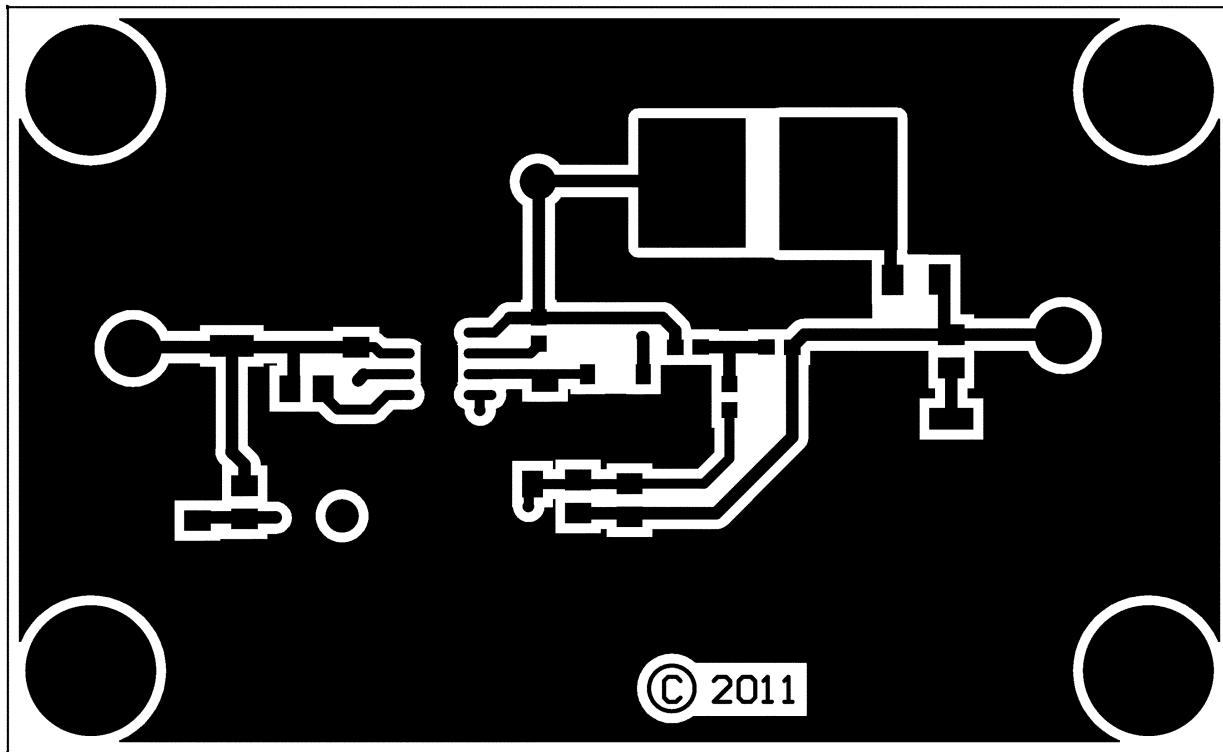


Figure 7. Board Top Layer

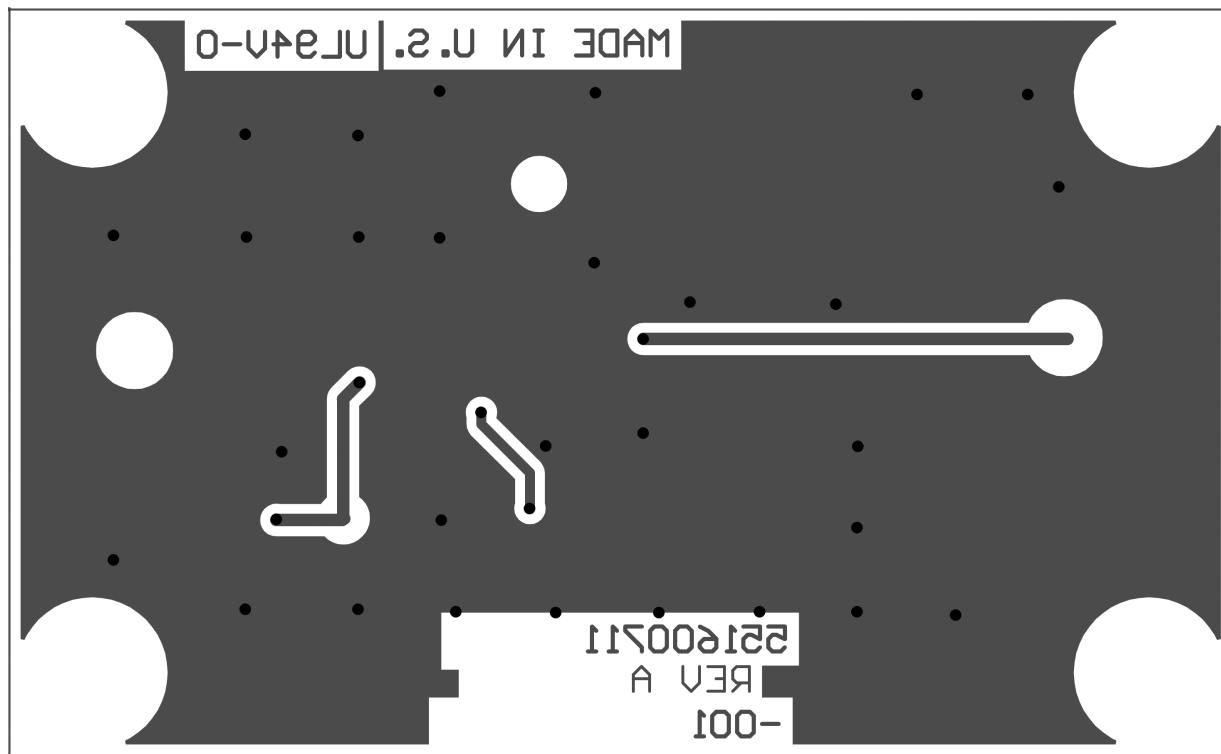


Figure 8. Board Bottom Layer

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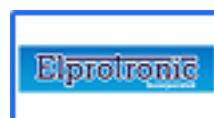
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