Isolated, Precision Half-Bridge Driver, 0.1 A Output

Data Sheet

ADuM1234

FEATURES

- Isolated high-side and low-side outputs
  - High side or low side relative to input: ±700 V peak
  - High-side/low-side differential: 700 V peak
- 0.1 A peak output current
- CMOS input threshold levels
- High frequency operation: 5 MHz maximum
- High common-mode transient immunity: >75 kV/µs
- High temperature operation: 105°C
- Wide body, RoHS-compliant, 16-lead SOIC
- Safety and regulatory approvals
  - UL recognition
    - 2500 V rms for 1 minute per UL 1577
  - VDE certificate of conformity
    - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
    - V_{IORM} = 560 V peak

APPLICATIONS

- Isolated IGBT/MOSFET gate drives
- Plasma displays
- Industrial inverters
- Switching power supplies

GENERAL DESCRIPTION

The ADuM1234[1] is an isolated, half-bridge gate driver that uses the Analog Devices, Inc., *i*Coupler® technology to provide independent and isolated high-side and low-side outputs. Combining high speed CMOS and monolithic transformer technology, this isolation component provides outstanding performance characteristics superior to optocoupler-based solutions.

By avoiding the use of LEDs and photodiodes, this *i*Coupler gate drive device is able to provide precision timing characteristics not possible with optocouplers. Furthermore, the reliability and performance stability problems associated with optocoupler LEDs are avoided.

In comparison to gate drivers that use high voltage level translation methodologies, the ADuM1234 offers the benefit of true galvanic isolation between the input and each output. Each output can be operated up to ±700 V peak relative to the input, thereby supporting low-side switching to negative voltages. The differential voltage between the high side and low side can be as high as 700 V peak.

As a result, the ADuM1234 provides reliable control over the switching characteristics of IGBT/MOSFET configurations over a wide range of positive or negative switching voltages.

FUNCTIONAL BLOCK DIAGRAM

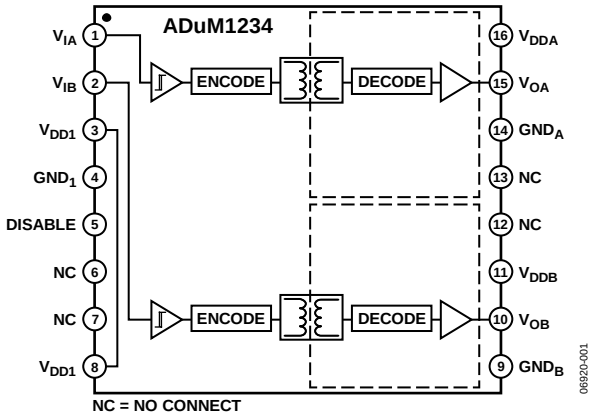

Figure 1.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075,329.

Rev. A

Document Feedback

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REVISION HISTORY

4/13—Rev. 0 to Rev. A

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Added DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 Insulation Characteristics Section ... 5
Added Table 5 and Figure 2; Renumbered Sequentially ... 5
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Updated Outline Dimensions ... 11

7/07—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

4.5 V ≤ V_{DD1} ≤ 5.5 V, 12 V ≤ V_{DDA} ≤ 18 V, 12 V ≤ V_{DDB} ≤ 18 V. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = 5 V, V_{DDA} = 15 V, V_{DDB} = 15 V. All voltages are relative to their respective grounds.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Supply Current, Quiescent	$I_{DDI(Q)}$		3.0	4.2	mA	
Output Supply Current A or Output Supply Current B, Quiescent	$I_{DDA(Q)}$, $I_{DDB(Q)}$		0.3	1.2	mA	
Input Supply Current, 10 Mbps	$I_{DDI(10)}$		6.0	9.0	mA	
Output Supply Current A or Output Supply Current B, 10 Mbps	$I_{DDA(10)}$, $I_{DDB(10)}$		16	22	mA	C_L = 200 pF
Input Currents	I_{IA}, I_{IB}, $I_{DISABLE}$	−10	+0.01	+10	µA	0 V ≤ V_{IA}, V_{IB}, $V_{DISABLE}$ ≤ V_{DD1}
Logic High Input Threshold	V_{IH}	0.7 × V_{DD1}			V	
Logic Low Input Threshold	V_{IL}			0.3 × V_{DD1}	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	V_{DDA} − 0.1, V_{DDB} − 0.1	V_{DDA}, V_{DDB}		V	I_{OA}, I_{OB} = −1 mA
Logic Low Output Voltages	V_{OAL}, V_{OBL}			0.1	V	I_{OA}, I_{OB} = +1 mA
Output Short-Circuit Pulsed Current[1]	$I_{OA(SC)}$, $I_{OB(SC)}$	100			mA	
SWITCHING SPECIFICATIONS						C_L = 200 pF
Minimum Pulse Width[2]	PW			100	ns	
Maximum Switching Frequency[3]		10			Mbps	
Propagation Delay[4]	t_{PHL}, t_{PLH}	97	124	160	ns	
Change vs. Temperature			100		ps/°C	
Pulse Width Distortion, $\lvert t_{PLH} - t_{PHL} \rvert$	PWD			8	ns	
Channel-to-Channel Matching, Rising or Falling Edges[5]				5	ns	
Channel-to-Channel Matching, Rising vs. Falling Edges[6]				13	ns	
Part-to-Part Matching, Rising or Falling Edges[7]				55	ns	Input t_R = 3 ns
Part-to-Part Matching, Rising vs. Falling Edges[8]				63	ns	Input t_R = 3 ns
Output Rise/Fall Time (10% to 90%)	t_R/t_F			25	ns	

[1] Short-circuit duration less than 1 sec.
[2] The minimum pulse width is the shortest pulse width at which the specified timing parameters are guaranteed.
[3] The maximum switching frequency is the maximum signal frequency at which the specified timing parameters are guaranteed.
[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[5] Channel-to-channel matching, rising or falling edges, is the magnitude of the propagation delay difference between two channels of the same part when the inputs are either both rising or falling edges. The supply voltages and the loads on each channel are equal.
[6] Channel-to-channel matching, rising vs. falling edges, is the magnitude of the propagation delay difference between two channels of the same part when one input is a rising edge and the other input is a falling edge. The supply voltages and loads on each channel are equal.
[7] Part-to-part matching, rising or falling edges, is the magnitude of the propagation delay difference between the same channels of two different parts when the inputs are either both rising or falling edges. The supply voltages, temperatures, and loads of each part are equal.
[8] Part-to-part matching, rising vs. falling edges, is the magnitude of the propagation delay difference between the same channels of two different parts when one input is a rising edge and the other input is a falling edge. The supply voltages, temperatures, and loads of each part are equal.

PACKAGE CHARACTERISTICS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input-to-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		2.0		pF	f = 1 MHz
Input Capacitance	C_I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance	θ_{JA}		45		°C/W	

[1] The device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

REGULATORY INFORMATION

The ADuM1234 is approved by the organizations listed in Table 3. Refer to Table 8 and the Insulation Lifetime section for more information about the recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 3.

UL	VDE
Recognized under UL 1577 component recognition program[1]	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]
Single/basic 2500 V rms isolation voltage	Reinforced insulation, 560 V peak
File E214100	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM1234 is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 sec (current leakage detection limit = 5 μA).
[2] In accordance with DIN V VDE V 0884-10 (VDE V 0884-10):2006-12, each ADuM1234 is proof tested by applying an insulation test voltage ≥ 1050 V peak for 1 sec (partial discharge detection limit = 5 pC). The asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		2500	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	3.5 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	3.5 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303, Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 INSULATION CHARACTERISTICS

This isolator is suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 approval for a 560 V peak working voltage.

Table 5.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1050	V peak
Input-to-Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	896	V peak
After Input and/or Safety Tests Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	672	V peak
Highest Allowable Overvoltage		V_{IOTM}	4000	V peak
Surge Isolation Voltage	V peak = 10 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	4000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Case Temperature		T_S	150	°C
Safety Total Dissipated Power		P_S	1	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

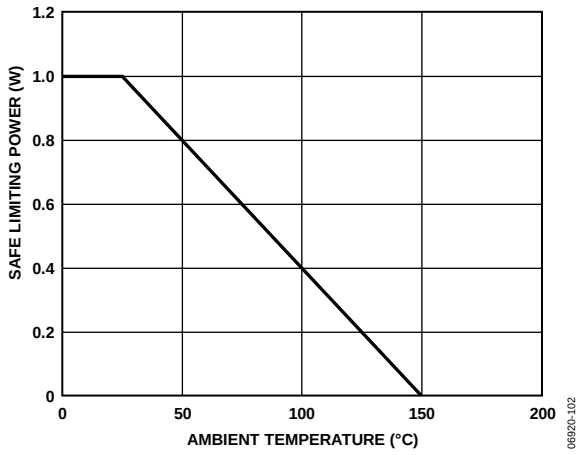

Figure 2. Thermal Derating Curve, Dependence of Safety-Limiting Values on Case Temperature, per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 6.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	−40	+105	°C
Input Supply Voltage[1]	V_{DD1}	4.5	5.5	V
Output Supply Voltages[1]	V_{DDA}, V_{DDB}	12	18	V
Input Signal Rise and Fall Times			100	ns
Common-Mode Transient Immunity				
Input-to-Output[2]		−75	+75	kV/µs
Between Outputs[2]		−75	+75	kV/µs
Transient Immunity, Supply Voltages[2]		−75	+75	kV/µs

[1] All voltages are relative to their respective grounds.
[2] See the Common-Mode Transient Immunity section for more information.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
Storage Temperature (T_{ST})	−55°C to +150°C
Ambient Operating Temperature (T_A)	−40°C to +105°C
Input Supply Voltage[1] (V_{DD1})	−0.5 V to +7.0 V
Output Supply Voltage[1] (V_{DDA}, V_{DDB})	−0.5 V to +27 V
Input Voltage[1] (V_{IA}, V_{IB})	−0.5 V to V_{DD1} + 0.5 V
Output Voltage[1]	
V_{OA}	−0.5 V to V_{DDA} + 0.5 V
V_{OB}	−0.5 V to V_{DDB} + 0.5 V
Input-to-Output Voltage[2]	−700 V peak to +700 V peak
Output Differential Voltage[3]	700 V peak
Output DC Current (I_{OA}, I_{OB})	−20 mA to +20 mA
Common-Mode Transients[4]	−100 kV/µs to +100 kV/µs

[1] All voltages are relative to their respective grounds.
[2] Input-to-output voltage is defined as GND_A – GND_1 or GND_B – GND_1.
[3] Output differential voltage is defined as GND_A – GND_B.
[4] Refers to common-mode transients across any insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 8. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	560	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform			
Basic Insulation	700	V peak	Analog Devices recommended maximum working voltage
DC Voltage			
Basic Insulation	700	V peak	Analog Devices recommended maximum working voltage

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more information.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

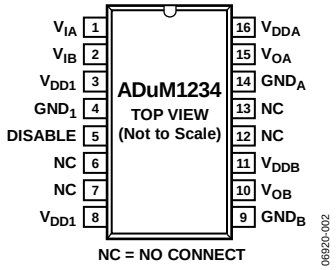

Figure 3. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{IA}	Logic Input A.
2	V_{IB}	Logic Input B.
3, 8	V_{DD1}	Input Supply Voltage, 4.5 V to 5.5 V. Pin 3 and Pin 8 are internally connected. Connecting both pins to V_{DD1} is recommended.
4	GND_1	Ground Reference for Input Logic Signals.
5	DISABLE	Input Disable. Disables the isolator inputs and refresh circuits. Outputs take on default low state.
6, 7, 12, 13	NC	No Connect. Pin 12 and Pin 13 are floating and should be left unconnected.
9	GND_B	Ground Reference for Output B.
10	V_{OB}	Output B.
11	V_{DDB}	Output B Supply Voltage, 12 V to 18 V.
14	GND_A	Ground Reference for Output A.
15	V_{OA}	Output A.
16	V_{DDA}	Output A Supply Voltage, 12 V to 18 V.

Table 10. Truth Table (Positive Logic)

V_{IA}/V_{IB} Input	V_{DD1} State	DISABLE	V_{OA}/V_{OB} Output	Notes
High	Powered	Low	High	
Low	Powered	Low	Low	
X[1]	Unpowered	X[1]	Low	Output returns to input state within 1 µs of V_{DD1} power restoration.
X[1]	Powered	High	Low	

[1] X is don't care.

TYPICAL PERFOMANCE CHARACTERISTICS

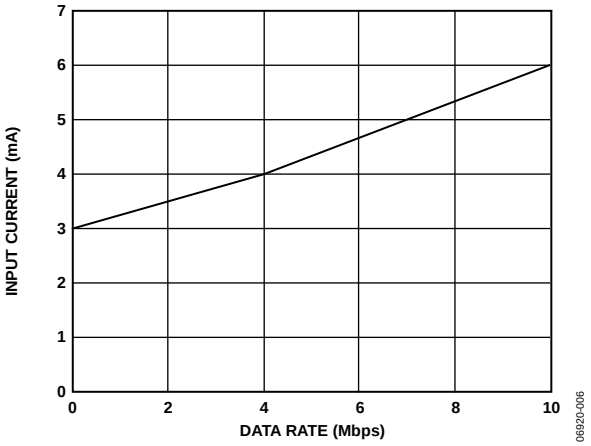

Figure 4. Typical Input Supply Current Variation with Data Rate

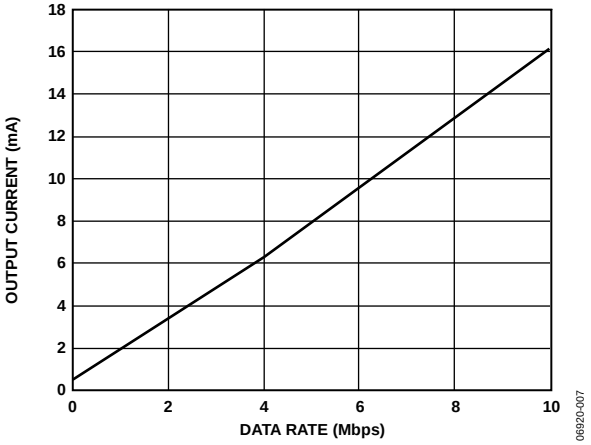

Figure 5. Typical Output Supply Current Variation with Data Rate

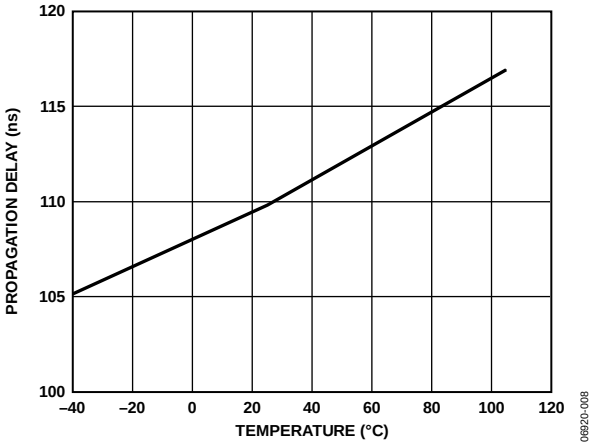

Figure 6. Typical Propagation Delay Variation with Temperature

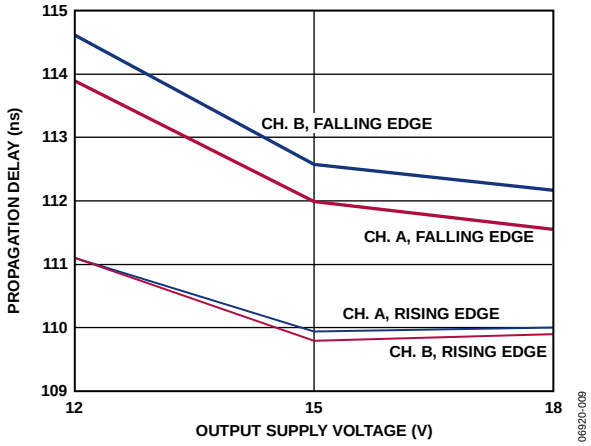

Figure 7. Typical Propagation Delay Variation with Output Supply Voltage (Input Supply Voltage = 5.0 V)

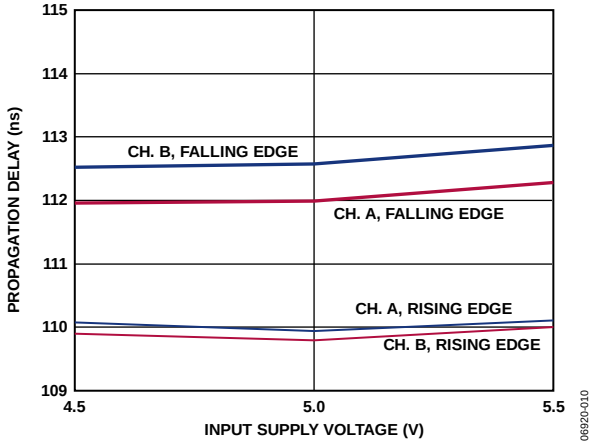

Figure 8. Typical Propagation Delay Variation with Input Supply Voltage (Output Supply Voltage = 15.0 V)

APPLICATIONS INFORMATION

COMMON-MODE TRANSIENT IMMUNITY

In general, common-mode transients consist of linear and sinusoidal components. The linear component of a common-mode transient is given by

$$V_{CM,\,linear} = (\Delta V/\Delta t)t$$

where $\Delta V/\Delta t$ is the slope of the transient shown in Figure 12 and Figure 13.

The transient of the linear component is given by

$$dV_{CM}/dt = \Delta V/\Delta t$$

Figure 9 characterizes the ability of the ADuM1234 to operate correctly in the presence of linear transients. The data is based on design simulation and is the maximum linear transient magnitude that the ADuM1234 can tolerate without an operational error. This data shows a higher level of robustness than the values listed in Table 6 because the transient immunity values obtained in Table 6 use measured data and apply allowances for measurement error and margin.

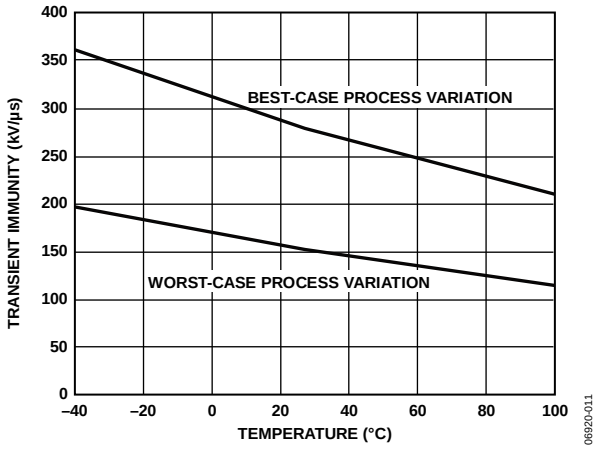

Figure 9. Transient Immunity (Linear Transients) vs. Temperature

The sinusoidal component (at a given frequency) is given by

$$V_{CM,\,sinusoidal} = V_0 \sin(2\pi ft)$$

where:
V_0 is the magnitude of the sinusoidal.
f is the frequency of the sinusoidal.

The transient magnitude of the sinusoidal component is given by

$$dV_{CM}/dt = 2\pi f\, V_0$$

Figure 10 and Figure 11 characterize the ability of the ADuM1234 to operate correctly in the presence of sinusoidal transients. The data is based on design simulation and is the maximum sinusoidal transient magnitude ($2\pi f\, V_0$) that the ADuM1234 can tolerate without an operational error. Values for immunity against sinusoidal transients are not included in Table 6 because measurements to obtain such values have not been possible.

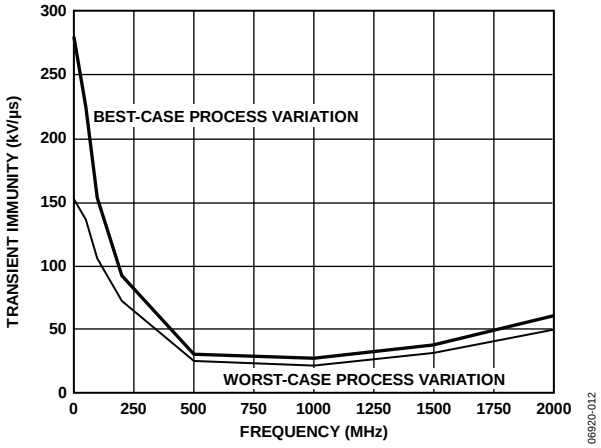

Figure 10. Transient Immunity (Sinusoidal Transients), 27°C Ambient Temperature

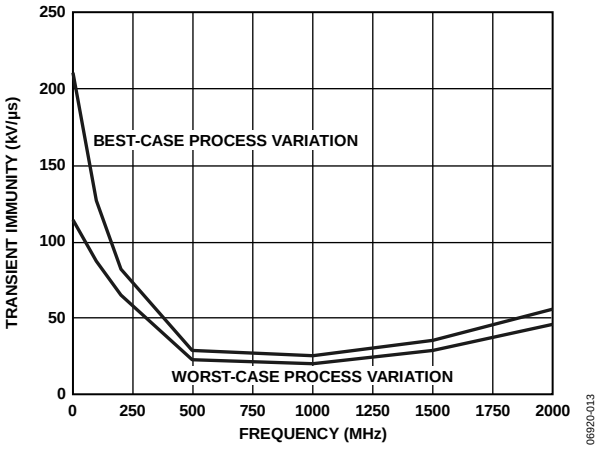

Figure 11. Transient Immunity (Sinusoidal Transients), 100°C Ambient Temperature

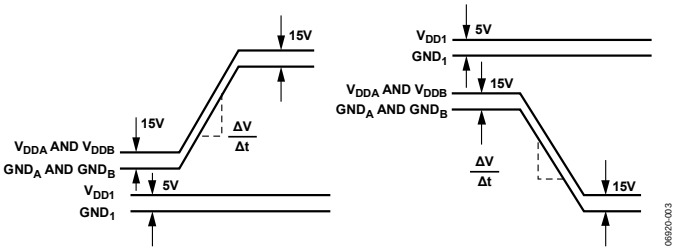

Figure 12. Common-Mode Transient Immunity Waveforms, Input to Output

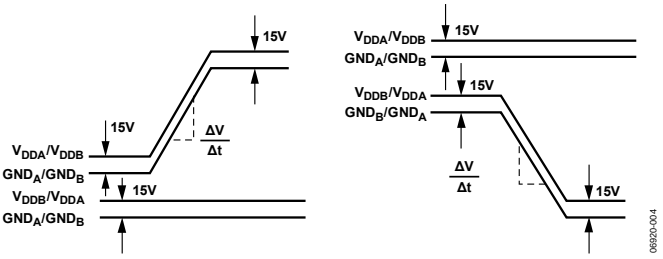

Figure 13. Common-Mode Transient Immunity Waveforms, Between Outputs

Figure 14. Transient Immunity Waveforms, Output Supplies

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation depends on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices conducts an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM1234.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

Table 8 lists the peak voltages for 50 years of service life for a bipolar ac operating condition and the maximum working voltages recommended by Analog Devices. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM1234 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 15, Figure 16, and Figure 17 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the bipolar ac condition determines the maximum working voltage recommended by Analog Devices.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 8 can be applied while maintaining the 50-year minimum lifetime, provided that the voltage conforms to either the unipolar ac or dc voltage cases.

Any cross-insulation voltage waveform that does not conform to Figure 16 or Figure 17 should be treated as a bipolar ac waveform and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 8.

Note that the voltage presented in Figure 16 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

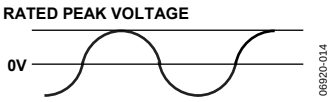

Figure 15. Bipolar AC Waveform

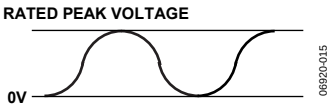

Figure 16. Unipolar AC Waveform

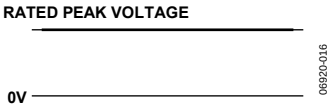

Figure 17. DC Waveform

OUTLINE DIMENSIONS

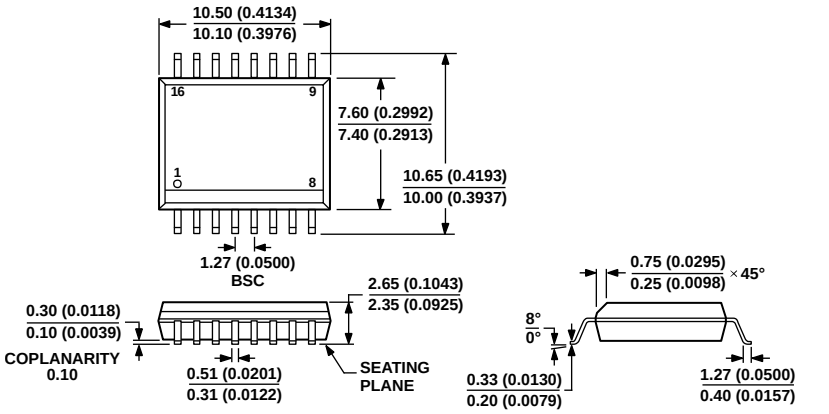

Figure 18. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	No. of Channels	Output Peak Current (A)	Output Voltage (V)	Temperature Range	Package Description	Package Option
ADuM1234BRWZ	2	0.1	15	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1234BRWZ-RL	2	0.1	15	−40°C to +105°C	16-Lead SOIC_W, 13-Inch Tape and Reel Option (1,000 Units)	RW-16

[1] Z = RoHS Compliant Part.

NOTES

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