Setup Instructions for the ISL6271A Evaluation Kit

READ ALL INSTRUCTIONS BEFORE APPLYING POWER OR CONNECTING CABLES

The **ISL6271A** is a power management integrated circuit (PMIC) designed to provide the low-voltage requirements for the Bulverde XScale processor. There are three(3) such voltages generated by the PMIC:

1) .85V-1.6V core voltage under DVM or VID control
2) 1.3V PLL voltage, and
3) 1.1V SRAM voltage.

All three outputs are enabled/disabled simultaneously by a common Power Enable (EN) signal from the processor. Various control and diagnostic functions attend to the orderly sequencing and dynamic control of the PMIC. A complete functional description of the PMIC can be found in the **ISL6271A** data sheet (provided).

The **ISL6271A** evaluation board provides a means to explore and validate the functional capabilities of the **ISL6271A** XScale Regulator. The board was designed to have an intuitive layout flow with strapping options to aid in ease of instrumenting and testing. There is a left-to-right flow of input-to-output, with external inputs coming onto the board from the left side and the outputs on the right side. LED indicator functions are to the top side of the layout and the transient load-generator option is in the lower right corner of the board with various strapping options. The core regulator output can be controlled by either an externally connected I2C interface module (provided) or on-board static VID switches. Appropriate cabling is provided to make the necessary connections with external testing equipment.

The following instructions are not intended to effect an exhaustive evaluation of the **ISL6271A**. They are intended as a guide into an introductory suite of tests with which the evaluator can gain enough confidence and skill to go deeper in functional exploration/validation.

Test Equipment Required:

- Multi-channel Storage Oscilloscope (with appropriate probes)
- Digital Multi-meters (up to 3)
- Dual Low-Voltage Adjustable Power Supply
- Load - electronic or resistors (0-1A)
- PC with available USB port
- USB cable
- USB/I2C interface module and I2C cable (provided with eval kit)
- USB/I2C Software (downloadable from www.intersil.com)

Initial Set-Up

Position the **ISL6271A** eval board so that the **Intersil** logo is in the upper right corner, relative to testers perspective.

All switch positions on S1 should be to the 'left' to Enable the device for static VID input.

Place shunts as follows, **(see Figure 1)**:

- H1 to 'enable'
- H2 no shunt (if external LVCC being supplied, left two pins should never be shorted)
- H3 no shunt
- H4 no shunt

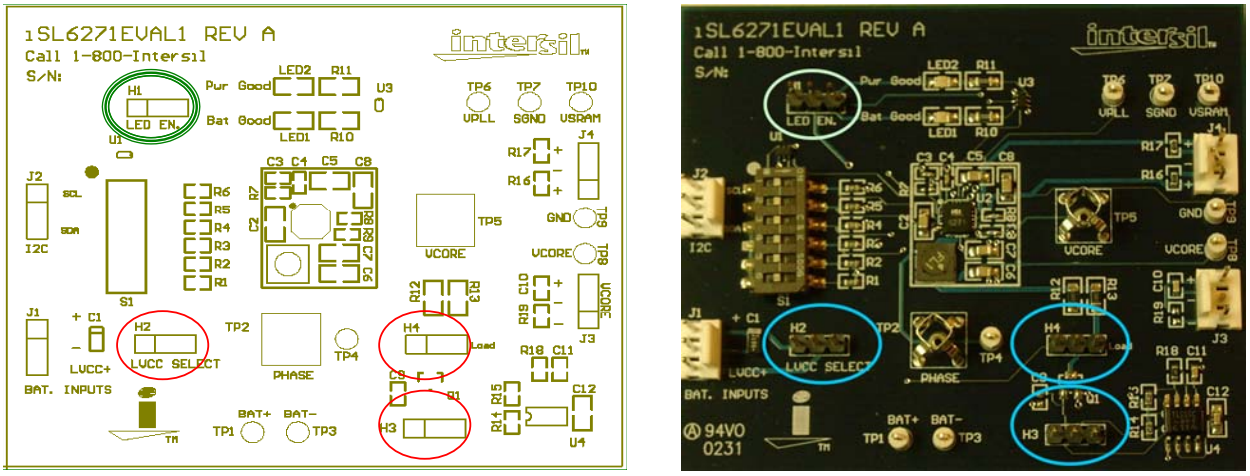


FIGURE 1. SHUNT PLACEMENT ON H1 TO ENABLE, AND NO SHUNT ON H2, H3 AND H4

Adjust the External Power Supplies to **3.7V** and **2.5V** respectively, and turn off.

NOTE: (Under NO circumstances should the voltage on either supply be allowed to exceed 6.0V)

Adjust the external electronic load for a constant current of 200mA (**Do not interconnect**).

Connect J1 on the eval board to the dual power supply, with the (LVCC+) pin to 2.5V (supply to the 2 LDO's), the (+) pin to 3.7V (supply to the swiching regulator), and the (-) pin to the supply common (gnd), **Figure 2.**

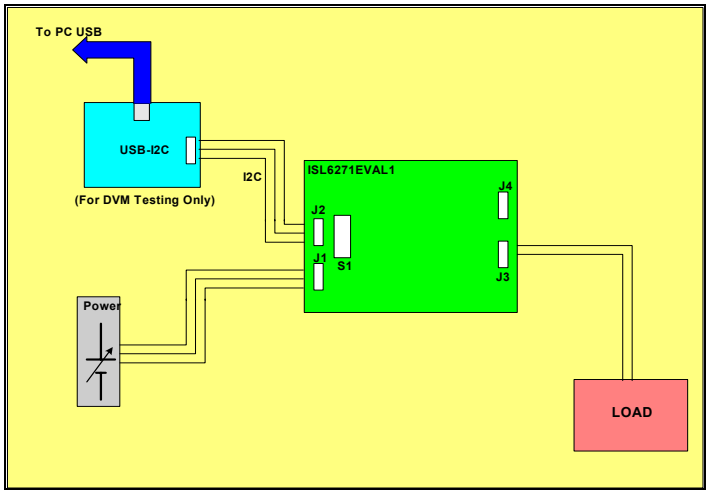


FIGURE 2. CONNECT J1 TO THE DUAL POWER SUPPLY

Connect the test leads of **DVM#1** between **TP1**(+) and **TP3**(-) and set to measure VDC.

Connect the test leads of **DVM#2** between **TP8**(+) and **TP9**(-) and set to measure VDC.

Connect the test leads of **DVM#3** between **TP6**(+) and **TP7**(-) and set to measure VDC.

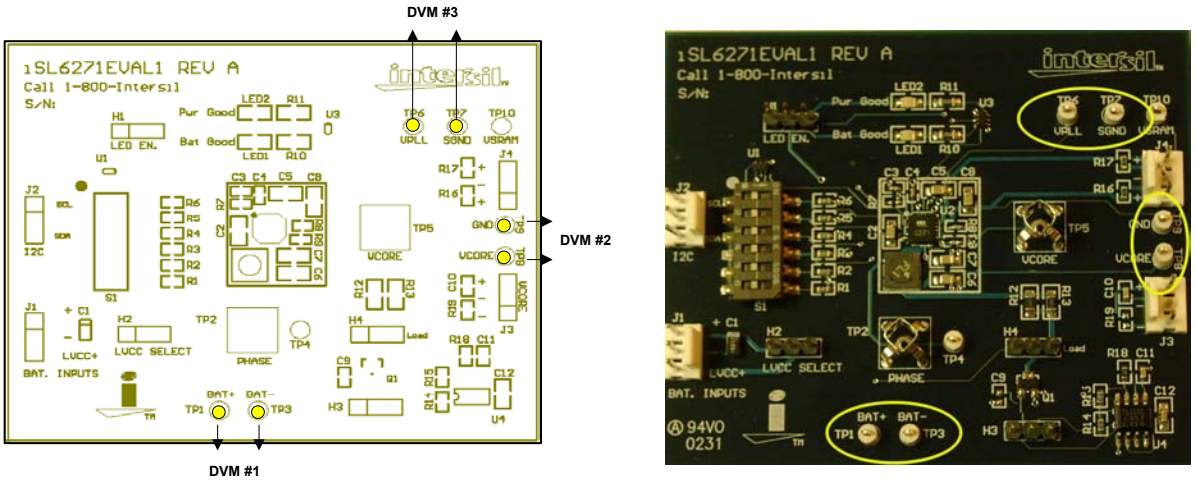


FIGURE 3. CONNECT THE TEST LEADS BETWEEN TP1, TP3, TP8, TP9, TP6, TP7

Initial Power-Up

With all the switches of S1 on the eval board at “off” positions and the external supplies adjusted to 3.7V and 2.5V, turn both power supplies ‘on’.

- Observe that both LEDs (LED1, LED2) are illuminated, see **Figure 4.**
- Confirm DVM#2 indicates 1.6V (+-25mV) for V_{Core}
- Confirm DVM#1 indicates 3.7V (+-50mV) — this voltage will vary with the load current
- Confirm DVM#3 indicates 1.3V (+-25mV) for VPLL
- Move DVM#3 (+) lead to TP10 and confirm 1.1V(+-25mV) for VSRAM

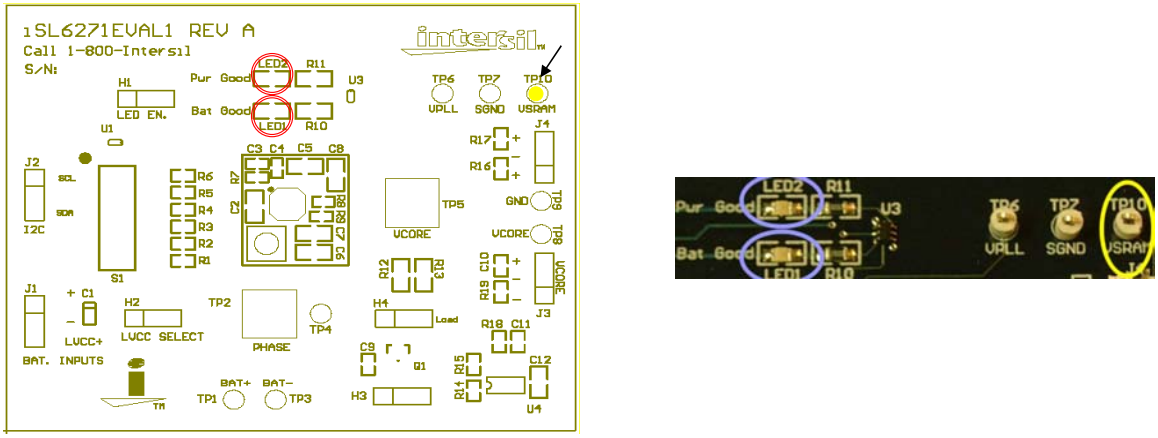


FIGURE 4. OBSERVE LED1, LED2 AND CONFIRM VOLTAGES

With the board still powered, slide switch (S1) positions 1- 4 to the right and confirm **DVM#2** indicates .85V(+-25V). Return switches to left position, and verify 1.6V is restored (**Figure 5**). Slide S1 position 6 to the right (on), Vcore should be 1.3V. This confirms static **4-bit VID** management capability of the core voltage (see the datasheet for the various VID codes which can be set).

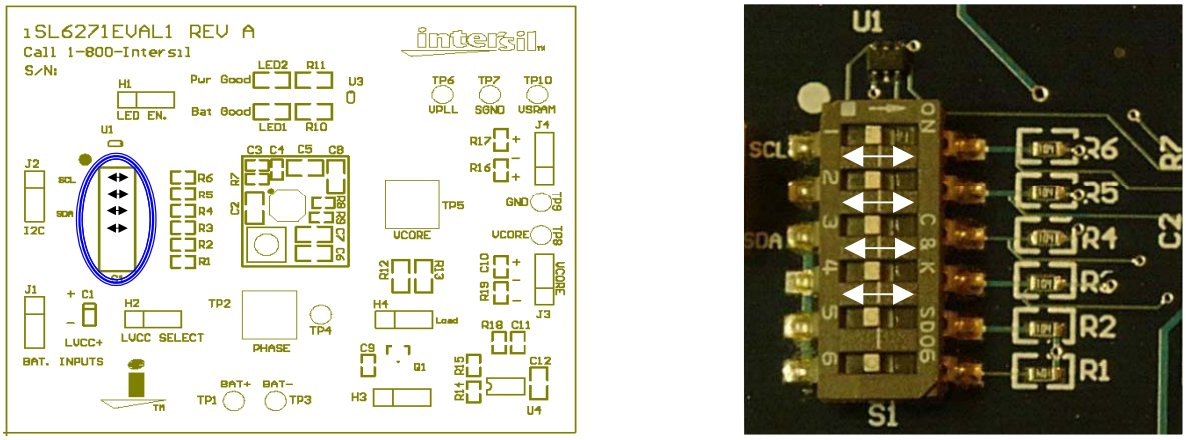


FIGURE 5. SLIDE SWITCH POSITIONS 1-4 ON S1 TO CONFIRM 4-BIT VID

Slide switch(S1) position 5 to the ‘right’ **(Figure 6)** and confirm DVM#2/3 registers low outputs. Return S1pos 5 to the ‘left’ position; confirm that the outputs are restored. This confirms the **Enable** function.

Turn the external power supplies ‘off’.

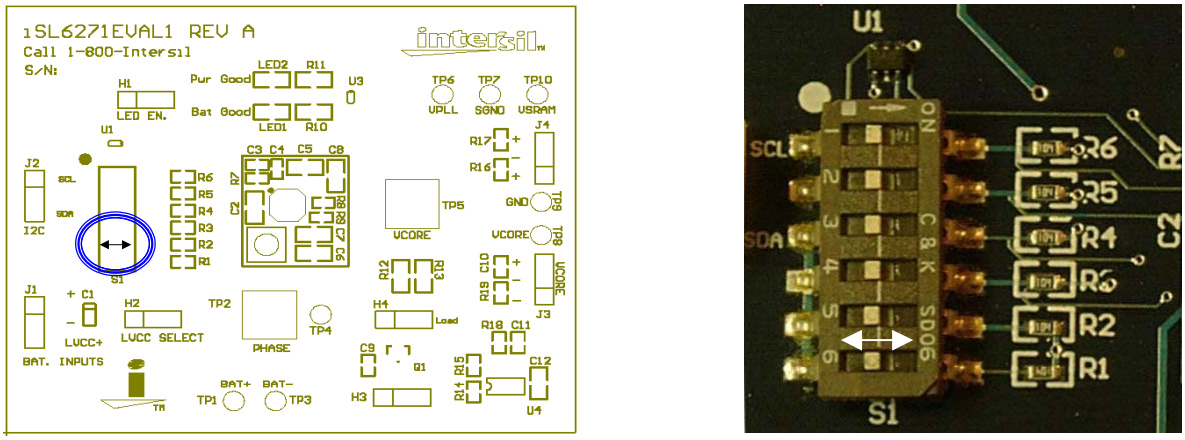


FIGURE 6. SLIDE SW1 POSITION 5 TO THE RIGHT TO CONFIRM REGISTERS

Connect J3 on evaluation board to the electronic load, (**Figure 7**), observing proper polarities.

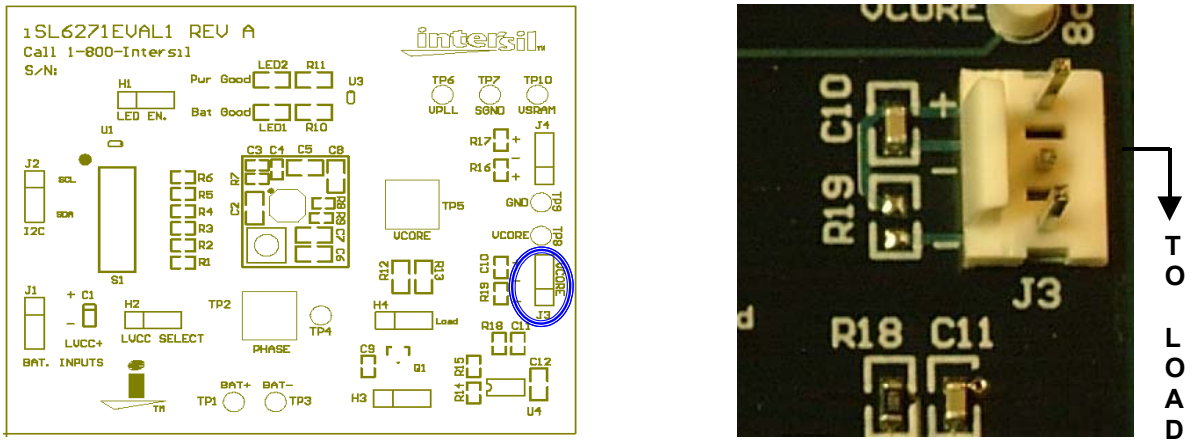


FIGURE 7. CONNECT THE J3 ON THE EVALUATION BOARD TO THE ELECTRONIC LOAD

NOTE: (Fixed resistive loads of 1Kohm each are connected across the VPLL and VSRAM outputs onboard. If variable loading is desired, such a load can be connected via J4)

Reapply power and observe **DVM#2** indicating 1.3V and that the load is sinking 200mA.

Basic functionality is confirmed and thorough testing/characterization can begin.

TP5 and **TP2** will accommodate low-noise Tek scope probe tips for monitoring the AC characteristics of Vcore and Phase, respectively.

The phase node is a good signal point from which to trigger and observe cycle-by-cycle switching behavior of the V_{core} regulator. Connect the trigger channel to the TP2 probe point to trigger on the phase signal. See **Figure 8** for a typical scope shot of the Vcore voltage(AC) when triggered from the phase node.

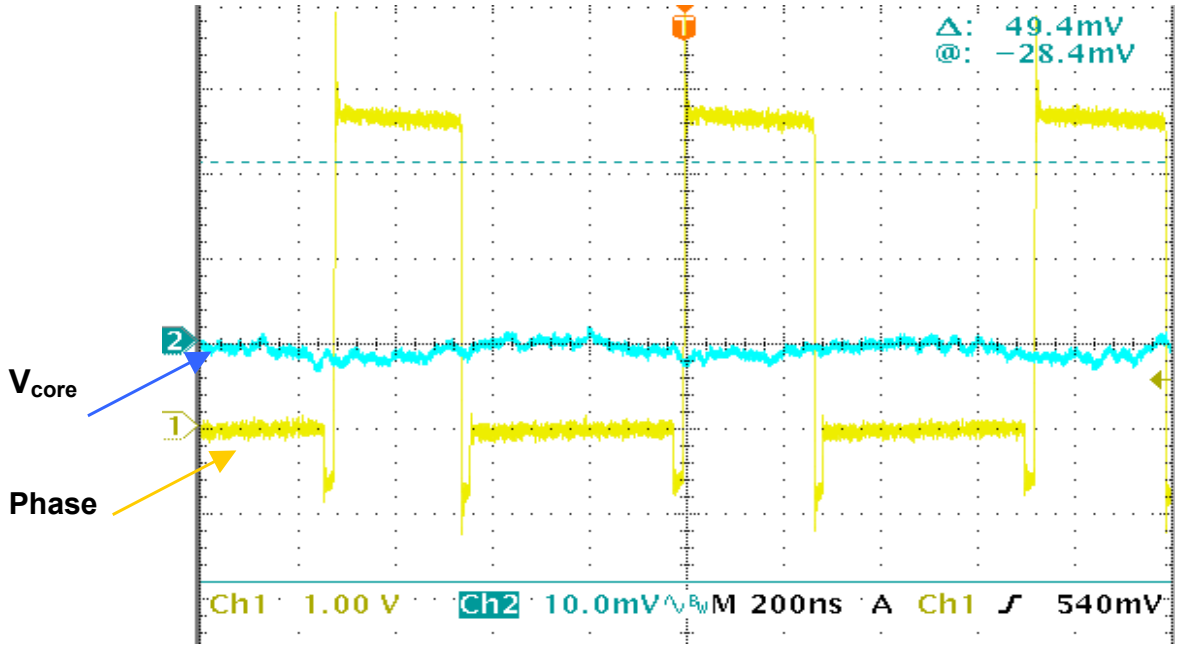


FIGURE 8. V_{CORE} AND PHASE

Transient Load Testing w/onboard Transient Generator

The onboard transient generator function permits dynamically changing the load current on Vcore and is enabled by placing a shunt across H4 pins 2-3 (while H1 is enabled), see **Figure 1**. This periodically connects and disconnects a 5 ohm load across the Vcore output at about a 1 second interval, corresponding to about a 250mA pulse load on the output at 1.3V. H4 pin 2 can then be used to trigger the scope and observe the effect on Vcore each time this load switches in either the positive or negative direction, thus observing the transient response of the Vcore regulator. This is illustrated below in **Figure 9** with a 10mA external load bias applied. (Note: The output load can be biased to some DC level by an external load connected through J3) . A programmable external load may provide more versatility for transient load testing, but this on-board capability gives an excellent read on the regulators response characteristic.

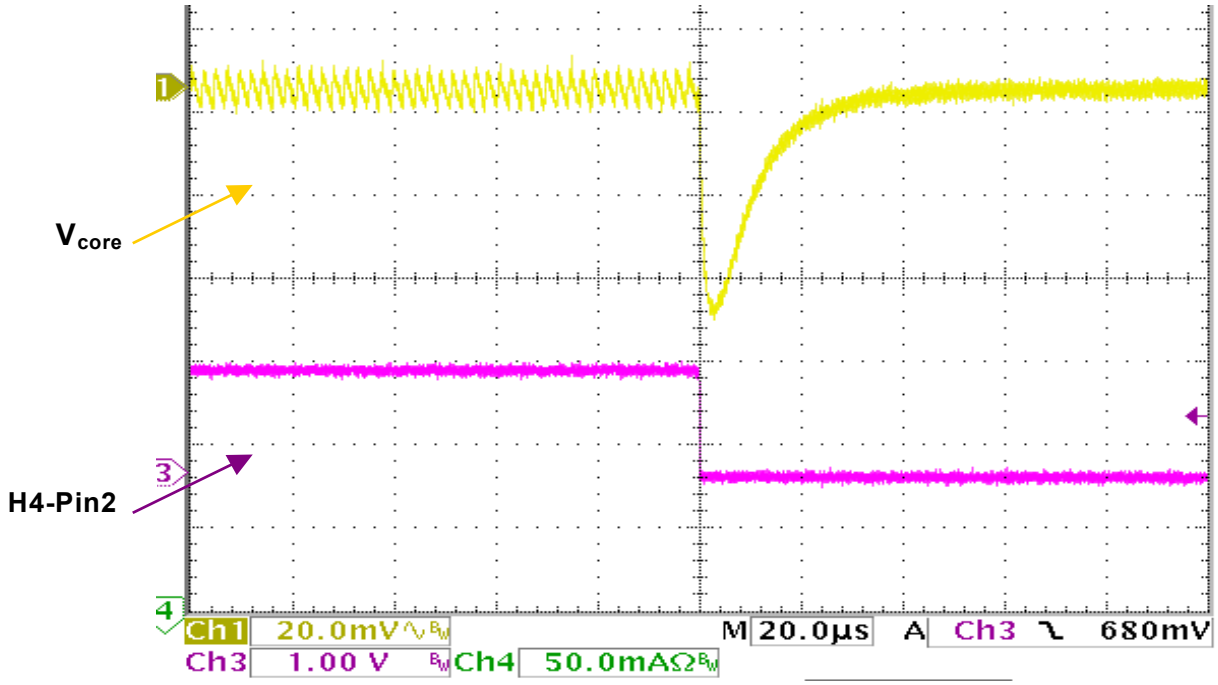


FIGURE 9. V_{CORE} TRANSIENT RESPONSE (10MA – 250MA)

Efficiency Measurement Considerations

Since the **ISL6271A** is a multi-regulator PMIC, it is important to segregate the regulators as much as possible when attempting accurate efficiency measurements on the core regulator. The power input to the LDOs (LVCC) can be tied to the main PVCC input by a strap on H2, but should be separated from the core regulator input voltage (PVCC) during efficiency measurements. All other extraneous draw from PVCC should be removed, such as the LED power and the transient generator circuitry. Removing the shunt from H1 effectively removes power from both the LED and transient-generator circuits, and prepares the circuit for core regulator efficiency measurements.

Another drain to take into consideration, if efficiency testing is being done under static VID control, is the 100K pull-up resistors for the switches in S1, which will drain 30-40uA each from PVCC when in the ‘right’ position. If testing is being done at an output voltage of less than 1.3V (all ‘left’), then the number of switches in the ‘right’ position should be factored into the efficiency calculation. This should be a relatively insignificant factor at higher output current levels, but it is a factor to be cognizant of.

Dynamic Voltage Management(DVM) via I²C

The following steps will guide the evaluator through the set-up required to control both the voltage level and slew rate of Vcore dynamically from a PC over a USB-to-I2C interface. The user will be able to easily set the core voltage at any one of 16 discrete levels between 0.85V and 1.3V, and the slew rate to one of 4 discrete levels from .1mV/uS to 5mV/uS (see data sheet) simply by selecting the desired level(s) and commanding a 'writeI2C' to the device.

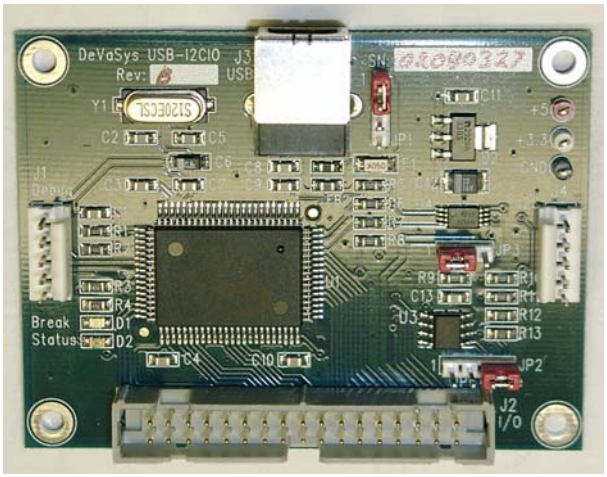


FIGURE 10. THE USB I²C INTERFACE MODULE

Load Driver Software

The first step is to connect the USB-I²C interface module to the PC USB port with the supplied cable **(Figure 10)** .

Next install the driver software for the I2C interface, provided on the same evaluation kit CD as this document (see Appendix B), and by following the installation instructions provided in Appendix B.

The screen below will appear after the application software is installed and the testing application is executed.

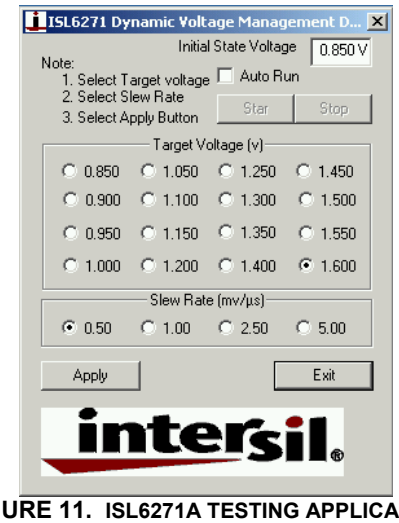


FIGURE 11. ISL6271A TESTING APPLICATION WINDOW

Hardware Module(s) Interconnect

Once the SW is loaded and the DVM-choice screen is displayed **(Figure 11),** the two boards should be connected together **(Figure 12).** Before connecting the cable between the eval board and the USB-I2C module (**Figure 2**), apply input power (3.7V) to the eval board and then connect the interconnecting cable to J2 on the eval board. *Switch S1 position 6 should be switched to the 'right' for I2C testing.*

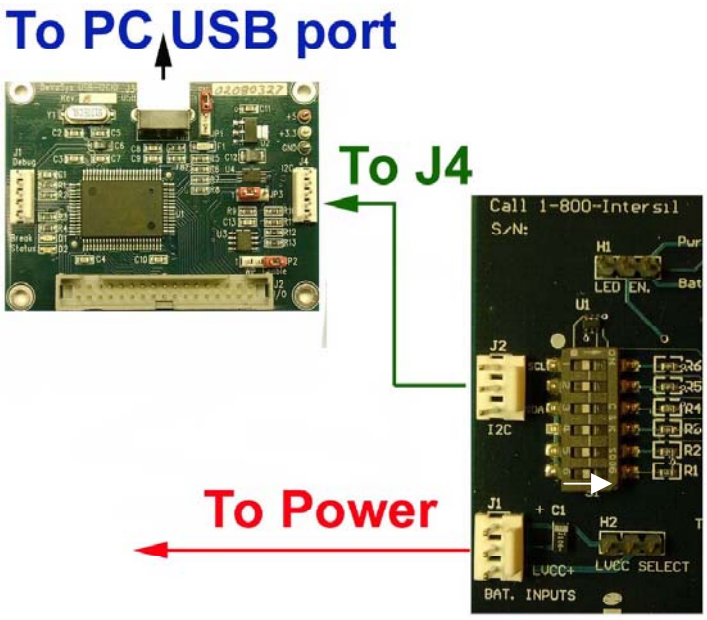


FIGURE 12. CONNECT THE INTERCONNECTING CABLE TO J2 ON THE EVALUATION BOARD

DVM Testing

Monitor Vcore DC voltage (TP8-TP9), while varying the voltage set-point using the I2C commands from the drop-down voltage palate on the PC screen. The variable slew rate command-set can be verified by monitoring Vcore at TP5 with a scope set on AC coupling and 200mV/Div sensitivity. The scope could be set to one-shot trigger off the change in Vcore voltage, commanded by the user adjusting the trigger level about 50mV from the '0'V level in the commanded direction. A more reliable, and repeatable, one-shot trigger is the incoming I2C clock signal. This signal can be easily accessed on either end of the red conductor in the I2C interconnect cable. Now, when the 'Write I2C' command is given, the scope will trigger on the clock burst, and the Vcore voltage slew rate to the new voltage level can be observed. This is illustrated below in **Figure 13** for both a positive and negative slew command.

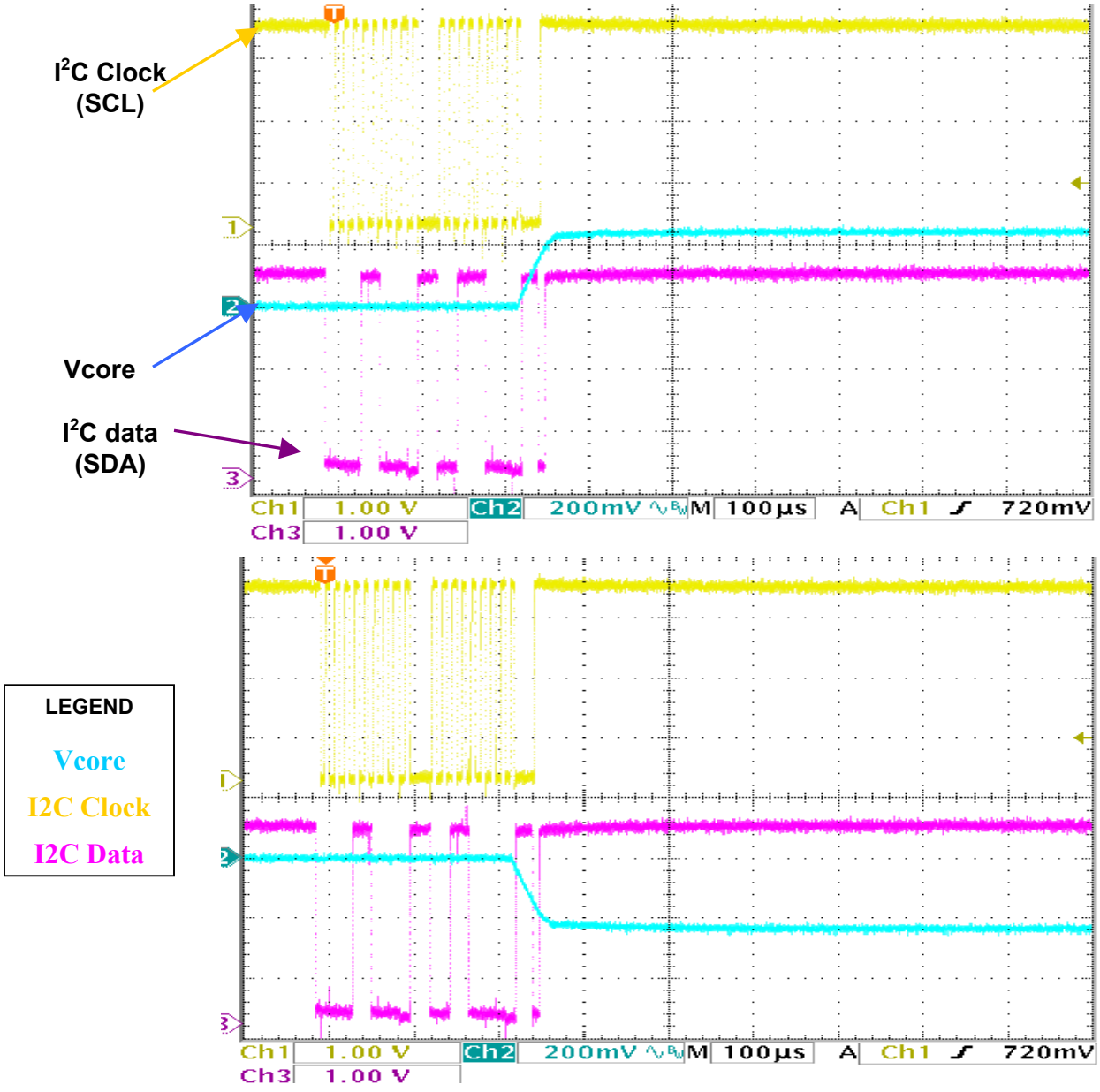
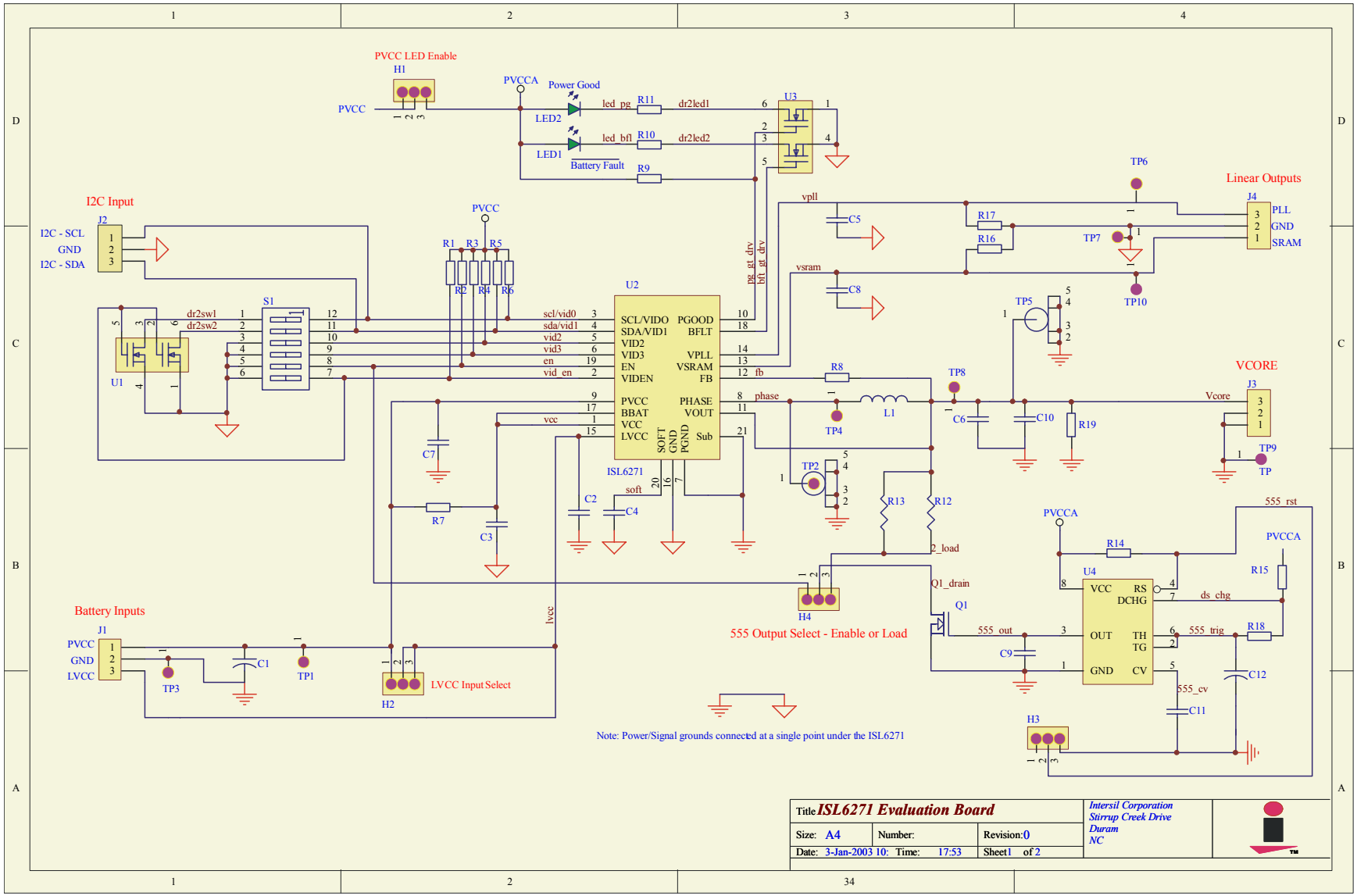


FIGURE 13. VCORE SLEW RATE

Appendix A

Schematics and Bill of Materials



ISL6271A Evaluation Board Bill-of-Materials

Item	Qty	Ref Des	Description	Footprint	Vendor	PN
1	3	C2,C5,C8	2.2uF/6.3V cer cap	0805		DK- PCC2176CT
2	1	C7	10uF/6.3V cer cap	0805		C2010X5R0J106K DK- PCC1923CT
3		C3	.1uF cer cap	0402		DK- PCC2146CT
4		C9,C10,C11	.1uF cer cap	0603		DK- PCC1762CT
5		C4	.01uF cer cap	0402		PCC103BQCT
6		C12	.47uF cer cap	0603		PCC1911CT
7		C1	10uF/10V tant cap	'A' Case 3.2x1.6x1.6	Sprague	
8		C6	10uF/6.3V cer	0805		
9	2	R10,R11	200	0805		
10	9	R1,R2,R3,R4,R5,R6,R14,R15	100K	0603		
11		R8	49.9K	0402		
12	1	R7	10	0402		
13	3	R16, R17, R19	1K	0603		
14	2	R12, R13	10	0805		
15		R9	100K	0402		
16		R18	1Meg	0603		
17	1	S1	6 pos switch		C&K	SD06H0SK
18	2	U1,U3	Dual n-fet	SC-70	Vishay Siliconix	TN0205AD
19	2	LED1,LED2	Green led	0805	Lumex	SML-LXT0805GW-TR
20	1	Q1	n-FET	SOT-23	Vishay Siliconix	Si2302ADS
21	1	L1	Inductor, 4.7uH	5.2x5.2x1mm	Cooper	SD20-4R7

ISL6271A Evaluation Board Bill-of-Materials

Item	Qty	Ref Des	Description	Footprint	Vendor	PN
22	4	J1,J2,J3,J4	Header/3ckt		DigiKey	A19430-ND
23	4	H1,H2,H3,H4	Jumper/3ckt			
24	2	TP2,TP5	Probe Socket		Tektronix	
25	8	TP1,3,4,6,7,8,9,10	testpoints			
26	1	U4	Timer IC	SO-8	Intersil	ICM7555
27	1	U2	Controller	4x4 mm QFN	Intersil	**ISL6271A**
28	1		PCB	2.5x3 inch		

Appendix B

Driver Installation Instructions

1. Go to www.intersil.com and search for ISL6271A;
2. Down load the software driver ISL6271A-installer.zip to your computer;
3. Expand the zip file into C:\ISL6271A
4. After the USB-I2C evaluation hardware been connected to the USB cable of the PC, the OS (Windows 2000/XP/98) will prompt you for the directory path of the hardware device driver. Point to the directory path to C:\ISL6271A, the OS will automatically install the device driver for you.
5. After you have successfully installed the USBI2CIO device driver, install the **ISL6271A** software tool. Run SETUP.EXE from the C:\ISL6271A subdirectory, and follow the on-screen instructions.
6. Click the “ISL6271A Demo” icon on your desk top to run the software. If you receive “Error in setting the initial stage” message, check your cable connections. Figure 11 window will pop up on your desktop. You will be able to adjust the ISL6271A output voltage and slew rate through the software.

Contact your local Intersil Field Application Engineer for technical assistance:

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Authorized Distribution Brand :

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