April 2015

FDB082N15A

N-Channel PowerTrench® MOSFET

150 V, 117 A, 8.2 mΩ

Features

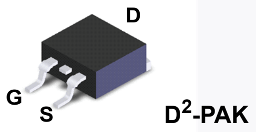
- $R_{DS(on)}$ = 6.7 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 75 A
- Fast Switching Speed
- Low Gate Charge, Q_G = 64.5 nC (Typ.)
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

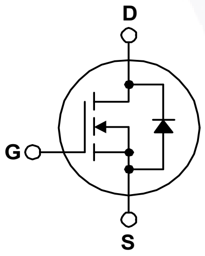
Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advance PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor drives and Uninterruptible Power Supplies
- Micro Solar Inverter





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FDB082N15A	Unit
V_{DSS}	Drain to Source Voltage		150	V
V_{GSS}	Gate to Source Voltage	- DC	±20	V
		- AC (f > 1 Hz)	±30	
I_D	Drain Current	- Continuous (T_C = 25°C, Silicon Limited)	117	A
		- Continuous (T_C = 100°C, Silicon Limited)	83	
I_{DM}	Drain Current	- Pulsed (Note 1)	468	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		542	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		6	V/ns
P_D	Power Dissipation	(T_C = 25°C)	294	W
		- Derate Sbove 25°C	1.96	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FDB082N15A	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.51	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDB082N15A	FDB082N15A	D^2-PAK	Tape and Reel	330 mm	24 mm	800 units

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit

Off Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu A$, $V_{GS} = 0\ V$, $T_C = 25^oC$	150	-	-	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu A$, Referenced to 25^oC	-	0.08	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 120\ V$, $V_{GS} = 0\ V$	-	-	1	μA
		$V_{DS} = 120\ V$, $T_C = 150^oC$	-	-	500	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm20\ V$, $V_{DS} = 0\ V$	-	-	±100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu A$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ V$, $I_D = 75\ A$	-	6.7	8.20	mΩ
g_{FS}	Forward Transconductance	$V_{DS} = 10\ V$, $I_D = 75\ A$	-	139	-	S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input Capacitance	$V_{DS} = 25\ V$, $V_{GS} = 0\ V$, f = 1 MHz	-	4645	6040	pF
C_{oss}	Output Capacitance		-	1445	1880	pF
C_{rss}	Reverse Transfer Capacitance		-	100	-	pF
C_{iss}	Input Capacitance	$V_{DS} = 75\ V$, $V_{GS} = 0\ V$, f = 1 MHz	-	4570	6040	pF
C_{oss}	Output Capacitance		-	460	1880	pF
C_{rss}	Reverse Transfer Capacitance		-	20	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 120\ V$, $I_D = 75\ A$, $V_{GS} = 10\ V$ (Note4)	-	64.5	84	nC
Q_{gs}	Gate to Source Gate Charge		-	19.1	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	8.7	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	13.5	-	nC
ESR	Equivalent Series Resistance (G-S)	f = 1 MHz	-	2.5	-	Ω

Switching Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75\ V$, $I_D = 75\ A$, $V_{GS} = 10\ V$, $R_G = 4.7\ \Omega$ (Note4)	-	22	54	ns
t_r	Turn-On Rise Time		-	58	126	ns
$t_{d(off)}$	Turn-Off Delay Time		-	61	132	ns
t_f	Turn-Off Fall Time		-	26	62	ns

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	117	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	468	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\ V$, $I_{SD} = 75\ A$	-	-	1.25	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\ V$, $I_{SD} = 75\ A$, $dI_F/dt = 100\ A/\mu s$	-	96	-	ns
Q_{rr}	Reverse Recovery Charge		-	268	-	nC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. Starting $T_J = 25°C$, L = 3 mH, $I_{SD} = 19\ A$.
3. $I_{SD} \leq 75\ A$, $di/dt \leq 200\ A/\mu s$, $V_{DD} \leq BV_{DSS}$, starting $T_J = 25°C$.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

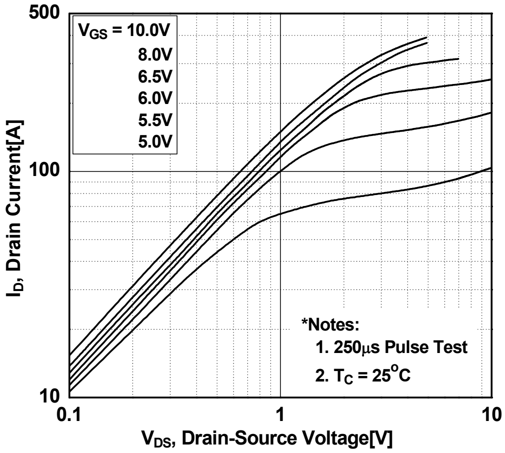


Figure 2. Transfer Characteristics

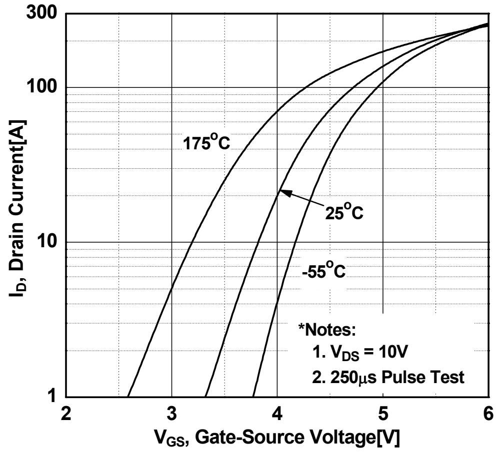


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

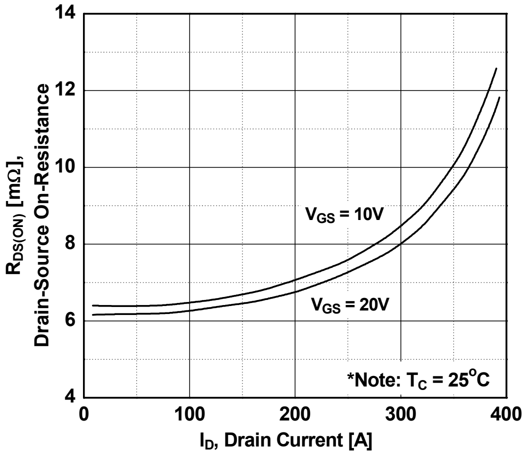


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

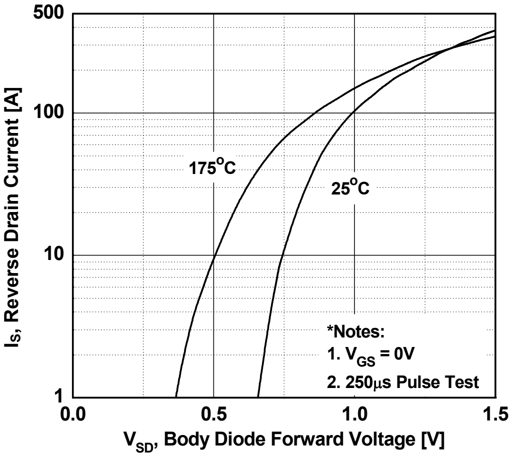


Figure 5. Capacitance Characteristics

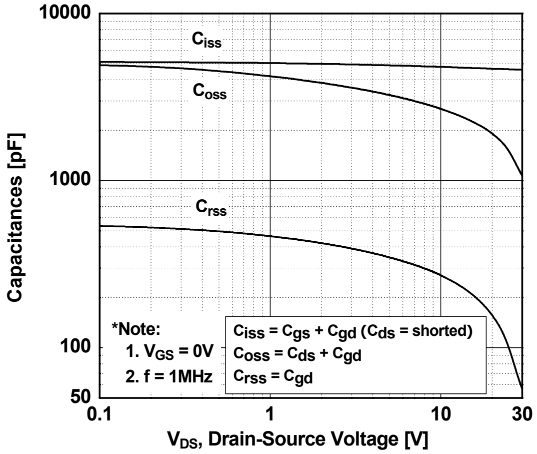
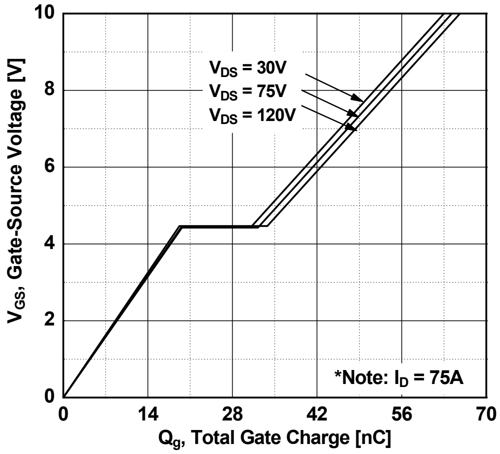


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

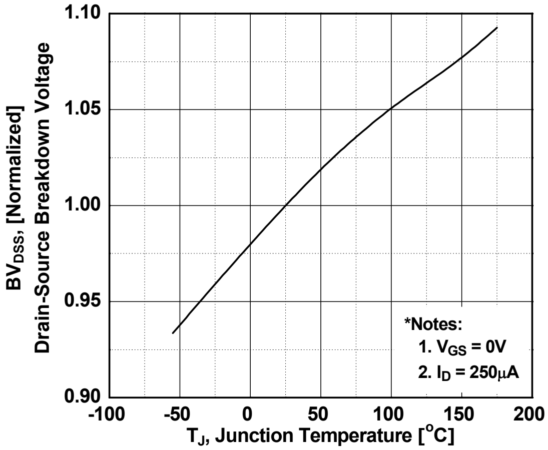


Figure 7. Breakdown Voltage Variation vs. Temperature

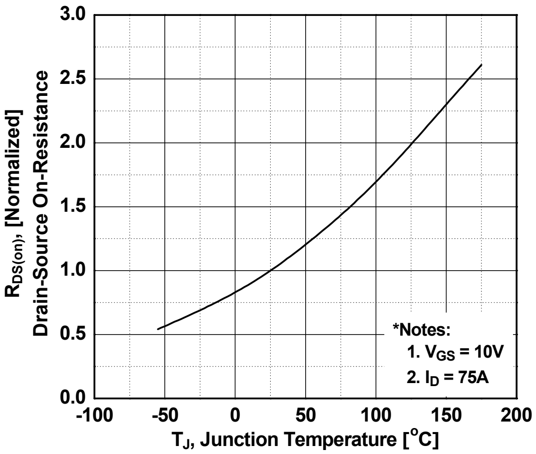


Figure 8. On-Resistance Variation vs. Temperature

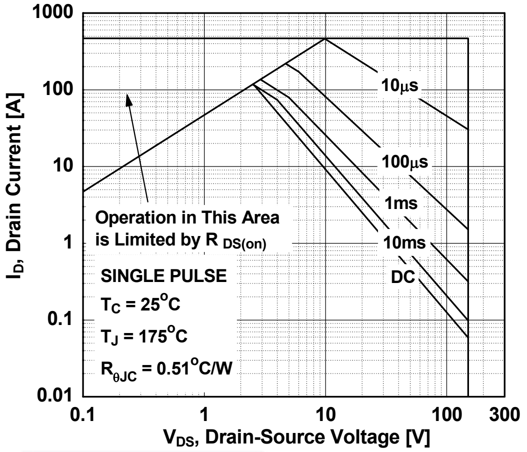


Figure 9. Maximum Safe Operating Area

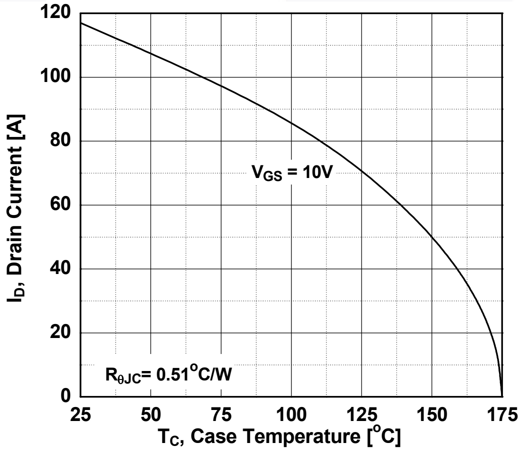


Figure 10. Maximum Drain Current vs. Case Temperature

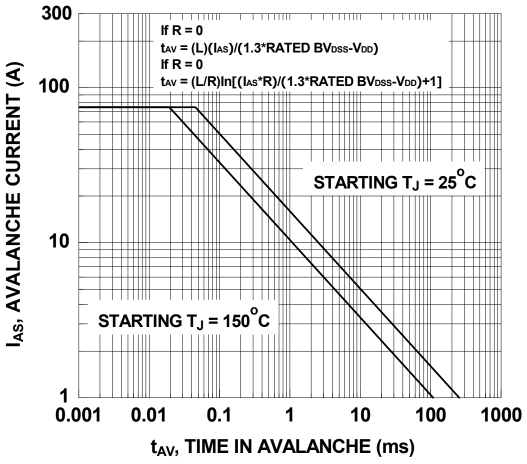
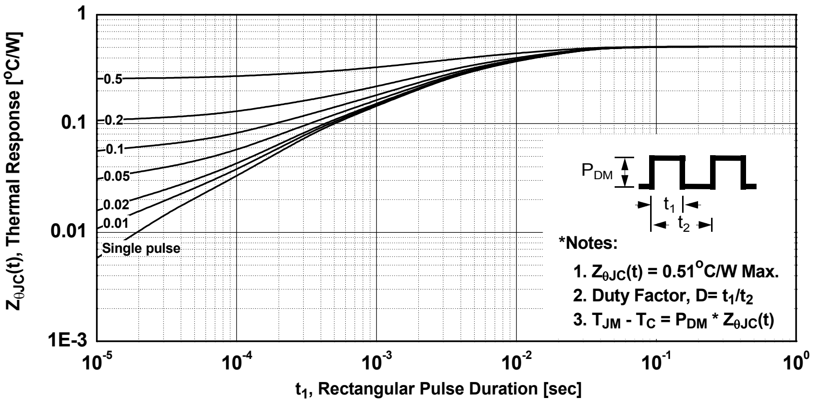


Figure 11. Unclamped Inductive Switching Capability

Typical Performance Characteristics

Figure 12. Transient Thermal Response Curve



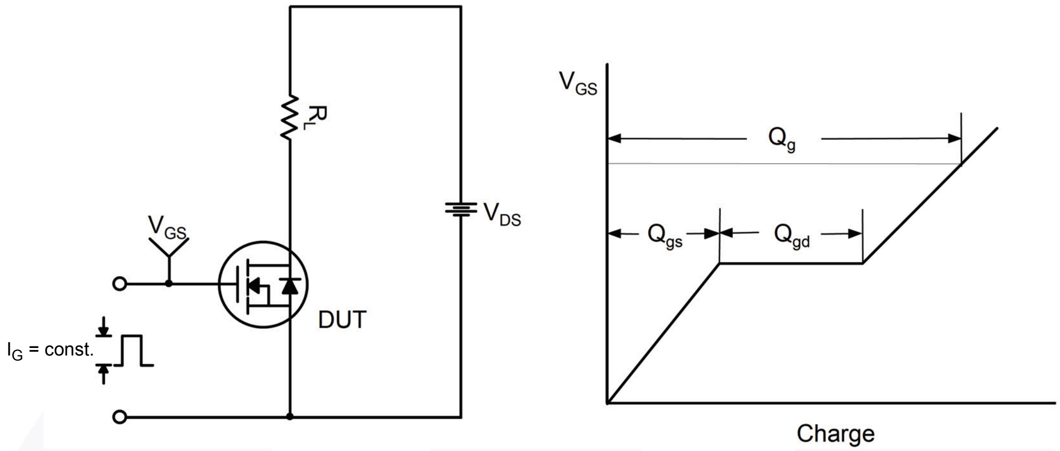


Figure 13. Gate Charge Test Circuit & Waveform

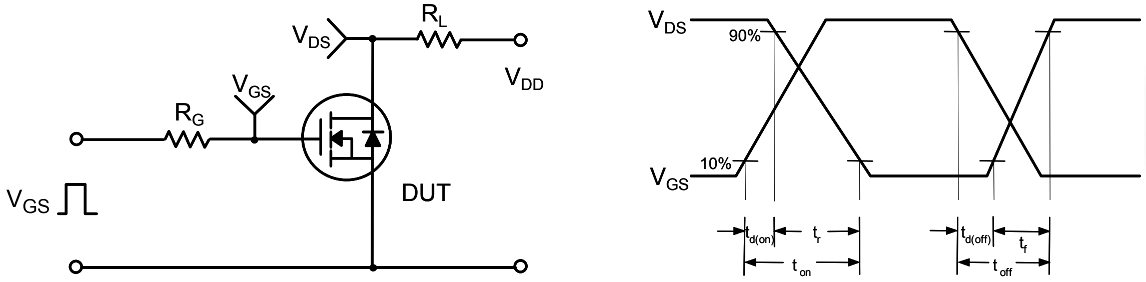


Figure 14. Resistive Switching Test Circuit & Waveforms

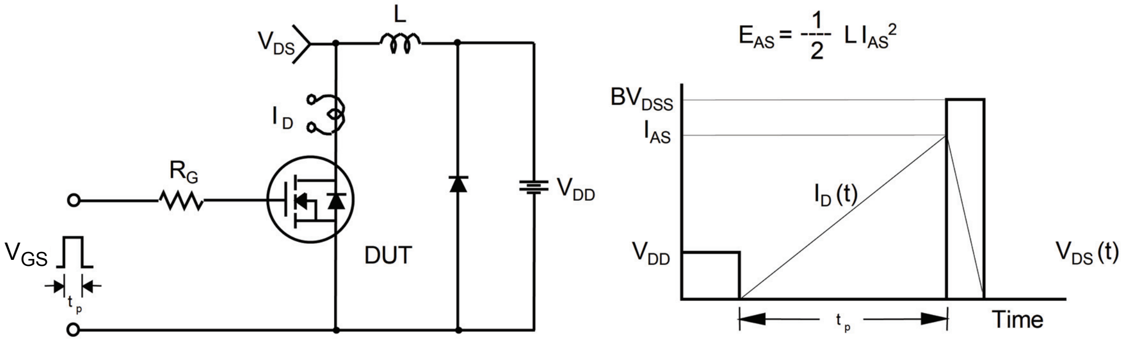


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

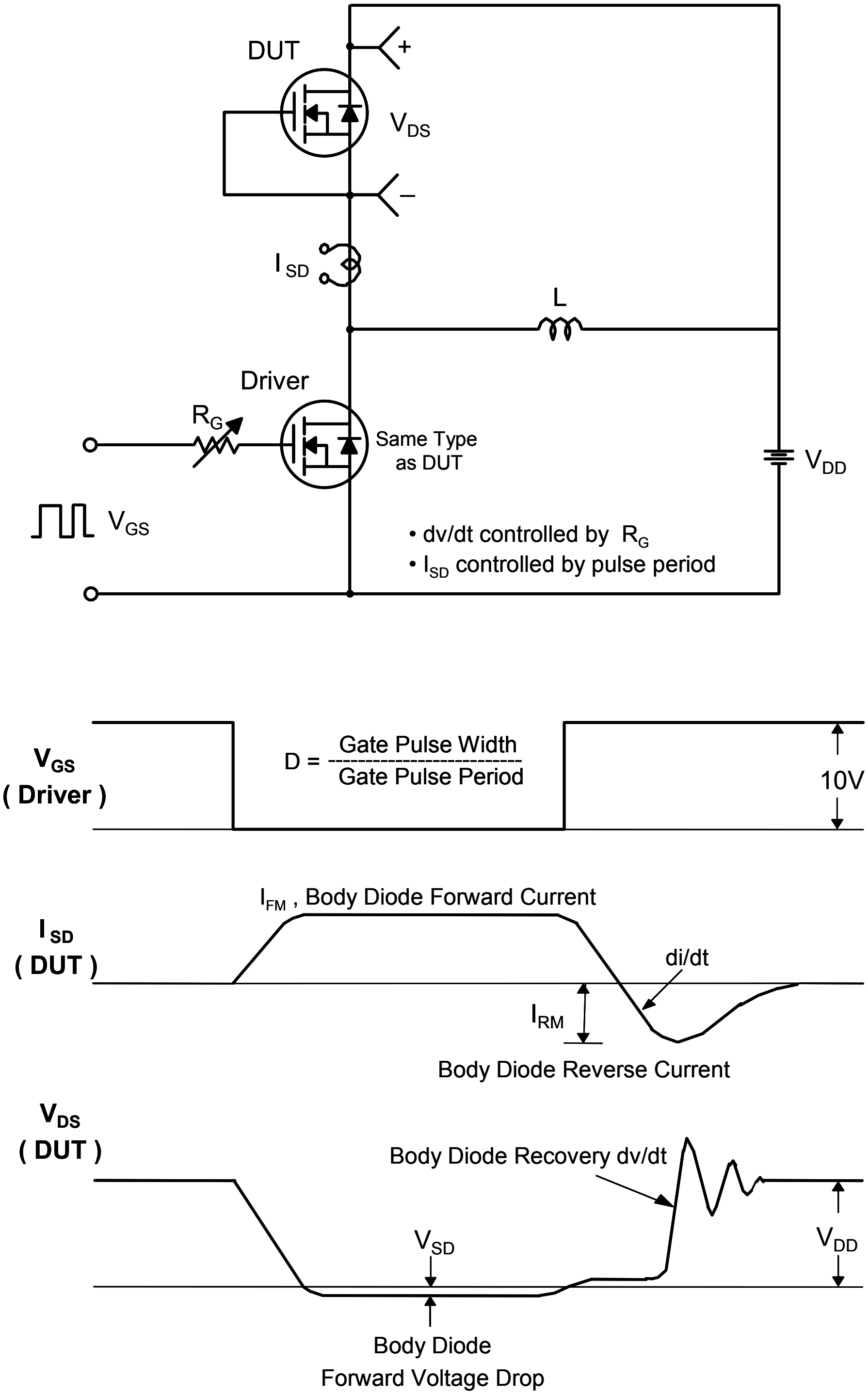
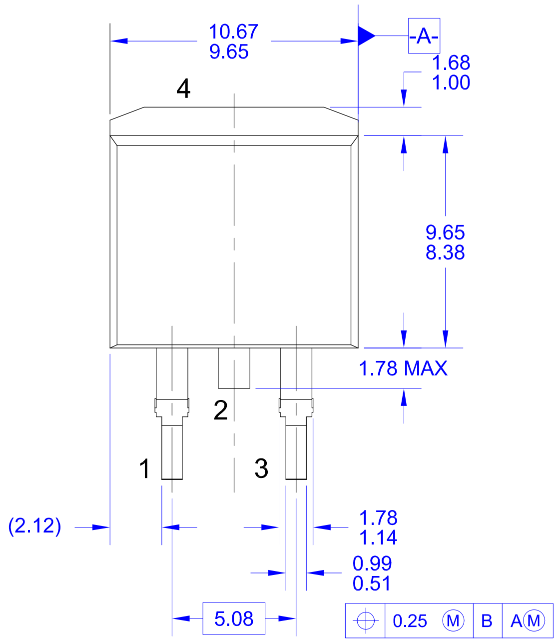
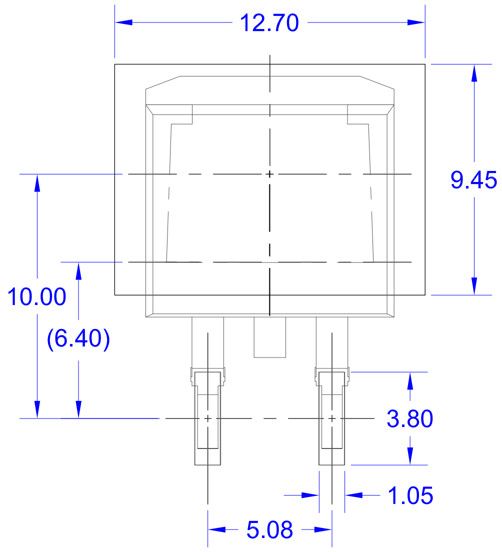
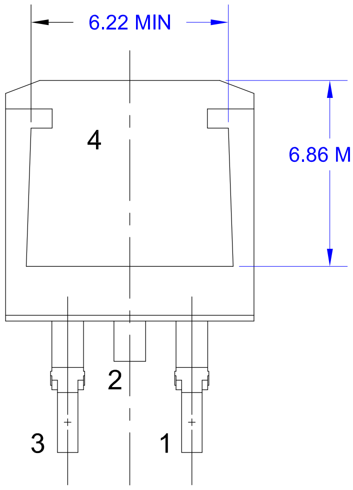


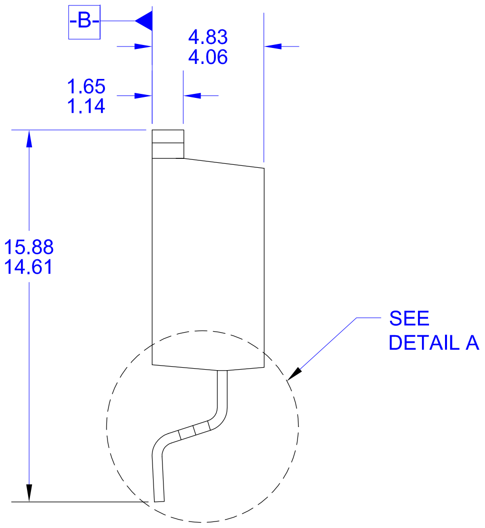
Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms



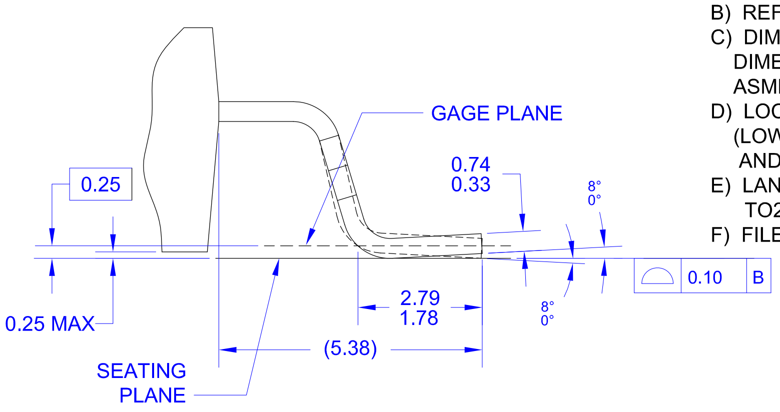


LAND PATTERN RECOMMENDATION
UNLESS NOTED, ALL DIMS TYPICAL





NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) REFERENCE JEDEC, TO-263, VARIATION AB.
- C) DIMENSIONING AND TOLERANCING PER DIMENSIONING AND TOLERANCING PER ASME Y14.5 - 2009.
- D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE).
- E) LANDPATTERN RECOMMENDATION PER IPC TO254P1524X482-3N
- F) FILENAME: TO263A02REV7



DETAIL A, ROTATED 90°
SCALE: 2X

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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