TEXAS INSTRUMENTS

TMP302A, **TMP302B**, **TMP302C**, **TMP302D**

SBOS488B –JUNE 2009–REVISED DECEMBER 2014

TMP302x Easy-to-Use, Low-Power, Low-Supply Temperature Switch in Micropackage

1 Features

- Low Power: 15 µA (maximum)
- SOT563 Package: 1.6-mm × 1.6-mm × 0.6 mm
- Trip-Point Accuracy: ±0.2°C (typical) From +40°C to +125°C
- Pin-Selectable Trip Points
- Open-Drain Output
- Pin-Selectable Hysteresis: 5°C and 10°C
- Low Supply Voltage Range: 1.4 V to 3.6 V

2 Applications

- Cell Phone Handsets
- Portable Media Players
- Consumer Electronics
- Servers
- Power-Supply Systems
- DC-DC Modules
- Thermal Monitoring
- Electronic Protection Systems

3 Description

The TMP302x is a temperature switch in a micropackage (SOT563). The TMP302x offers low power (15 µA maximum) and ease-of-use through pin-selectable trip points and hysteresis.

These devices require no additional components for operation; they can function independent of microprocessors or microcontrollers.

The TMP302x is available in several different versions. For additional trip points, contact a TI representative.

Device Information[1]

PART NUMBER	PACKAGE	SELECTABLE TRIP POINTS (ºC)[2]
TMP302A	SOT (6)	50, 55, 60, 65
TMP302B	SOT (6)	70, 75, 80, 85
TMP302C	SOT (6)	90, 95, 100, 105
TMP302D	SOT (6)	110, 115, 120, 125

(1) For all available packages, see the orderable addendum at the end of the datasheet.

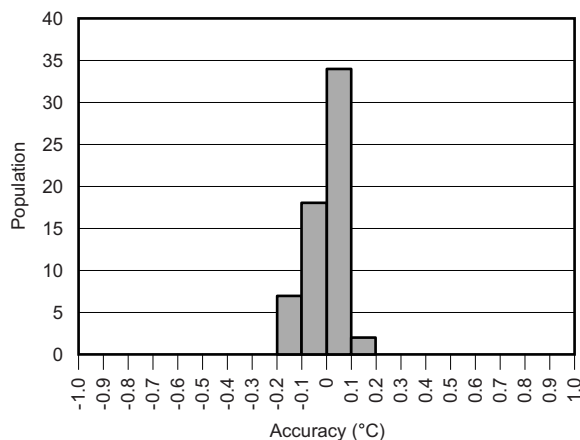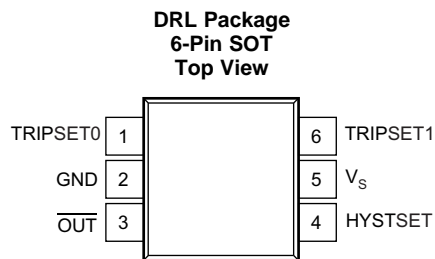(2) For other available trip points, contact a TI representative.

Trip Threshold Accuracy

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4 Revision History

Changes from Revision A (September 2009) to Revision B   **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 4

Product Folder Links: *TMP302A TMP302B TMP302C TMP302D*

5 Pin Configuration and Functions

DRL Package
6-Pin SOT
Top View

```
TRIPSET0   1 |        | 6   TRIPSET1
   GND     2 |        | 5   V_S
   OUT     3 |        | 4   HYSTSET
```

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	TRIPSET0	Digital Input	Used in combination with TRIPSET1 to select the temperature at which the device trips
2	GND	Ground	Ground
3	$\overline{\text{OUT}}$	Digital Output	Open drain, active-low output
4	HYSTSET	Digital Input	Used to set amount of thermal hysteresis
5	V_S	Power Supply	Power supply
6	TRIPSET1	Digital Input	Used in combination with TRIPSET0 to select the temperature at which the device trips

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [(1)]

		MIN	MAX	UNIT
Supply voltage			3.6	V
Input pin voltage	TRIPSET0, TRIPSET1, HYSTSET	−0.5	V_S + 0.5	V
Output pin voltage	$\overline{OUT}$	−0.5	3.6	V
Output pin current	$\overline{OUT}$		10	mA
Operating temperature		−55	130	°C
Junction temperature			150	°C
T_{stg}	Storage temperature	−60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	±1000	
		Machine Model (MM)	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Power supply voltage	1.4	3.3	3.6	V
R_{pullup}	Pullup resistor connected from $\overline{OUT}$ to V_S	10		100	kΩ

6.4 Thermal Information

		TMP302x	
	THERMAL METRIC[(1)]	**DRL**	**UNIT**
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	200	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	34.4	
ψ_{JT}	Junction-to-top characterization parameter	3.1	
ψ_{JB}	Junction-to-board characterization parameter	34.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

Product Folder Links: *TMP302A TMP302B TMP302C TMP302D*

6.5 Electrical Characteristics

At T_A = –40°C to 125°C, and V_S = 1.4 to 3.6 V, unless otherwise noted. 100% of all units are production tested at T_A = 25°C. Over temperature specifications are specified by design.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE MEASUREMENT						
	Trip point accuracy	T_A = 40°C to 125°C		±0.2	±2	°C
	Trip point accuracy versus supply			±0.2	±0.5	°C/V
	Trip point hysteresis	HYSTSET = GND		5		°C
		HYSTSET = V_S		10		°C
TEMPERATURE TRIP POINT SET						
	Temperature trip point set	TRIPSET1 = GND, TRIPSET0 = GND		Default		°C
		TRIPSET1 = GND, TRIPSET0 = V_S		Default + 5		°C
		TRIPSET1 = V_S, TRIPSET0 = GND		Default + 10		°C
		TRIPSET1 = V_S, TRIPSET0 = V_S		Default + 15		°C
HYSTERESIS SET INPUT						
V_{IH}	Input logic level high		$0.7 \times V_S$		V_S	V
V_{IL}	Input logic level low		–0.5		$0.3 \times V_S$	V
I_I	Input current	0 < V_I < 3.6 V			1	µA
DIGITAL OUTPUT						
V_{OL}	Output logic level low	V_S > 2 V, I_{OL} = 3 mA	0		0.4	V
		V_S < 2 V, I_{OL} = 3 mA	0		$0.2 \times V_S$	V
POWER SUPPLY						
	Operating Supply Range		1.4		3.6	V
I_Q	Quiescent Current			8	15	µA
		V_S = 3.3V, T_A = 50°C		7		µA
TEMPERATURE RANGE						
	Specified Range		–40		125	°C
	Operating Range		–55		130	°C

6.6 Typical Characteristics

At T_A = 25°C and V_S = 3.3 V, unless otherwise noted.
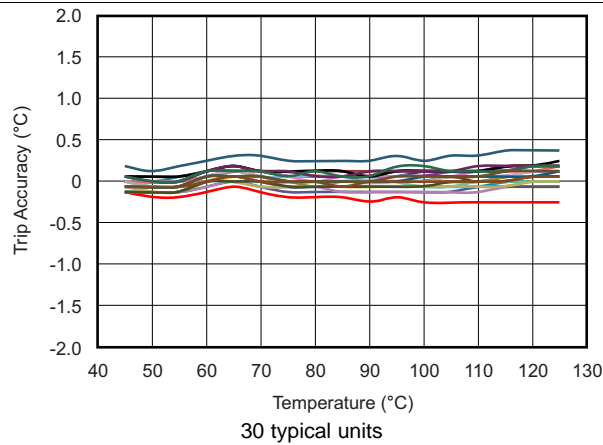

30 typical units

Figure 1. Trip Accuracy Error vs Temperature
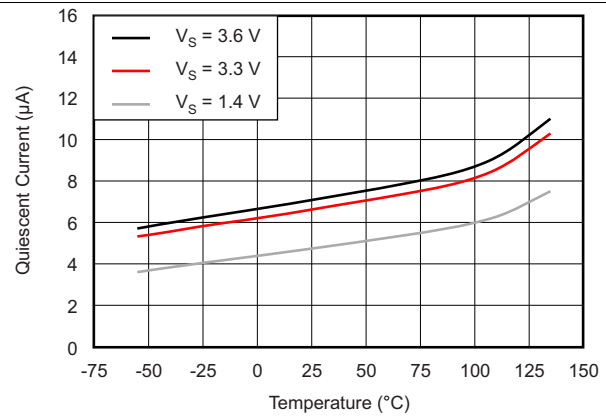

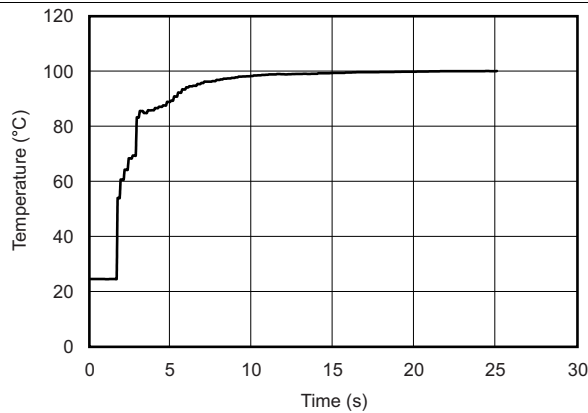**Figure 2. Quiescent Current vs Temperature**

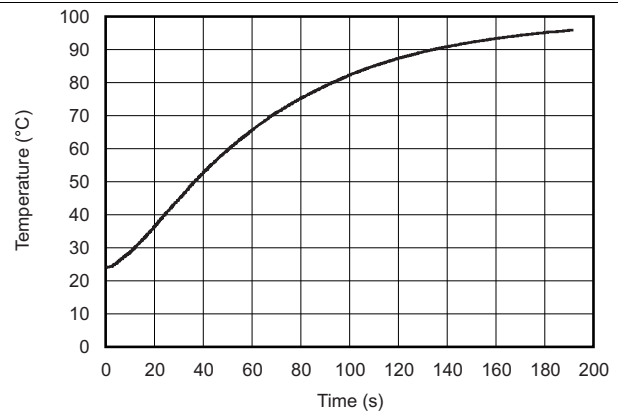**Figure 3. Temperature Step Response In Perfluorinated Fluid at 100°C vs Time**
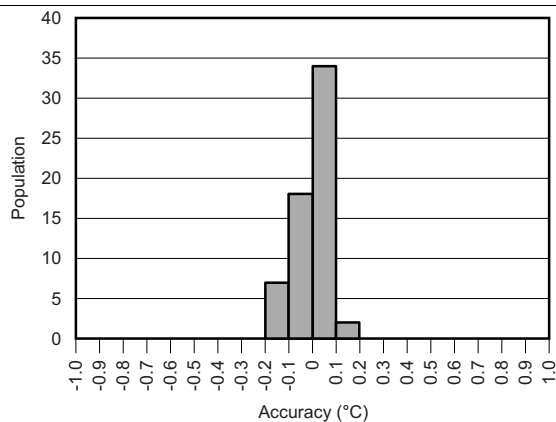

Figure 4. Thermal Step Response in Air at 100°C vs Time
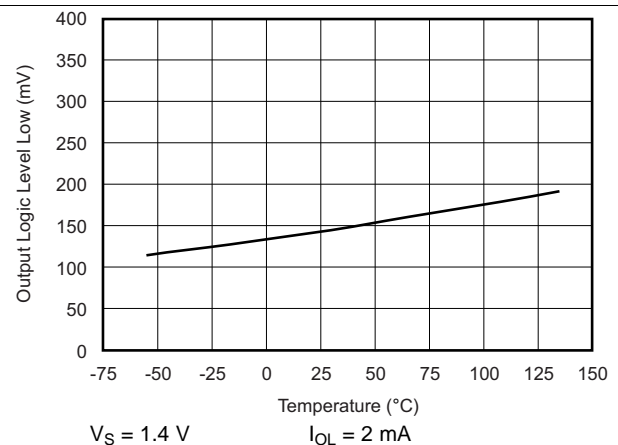

Figure 5. Trip Threshold Accuracy

V_S = 1.4 V I_{OL} = 2 mA

Figure 6. Output Logic-Level Low V_{OL} vs Temperature

Product Folder Links: *TMP302A   TMP302B   TMP302C   TMP302D*

Typical Characteristics (continued)

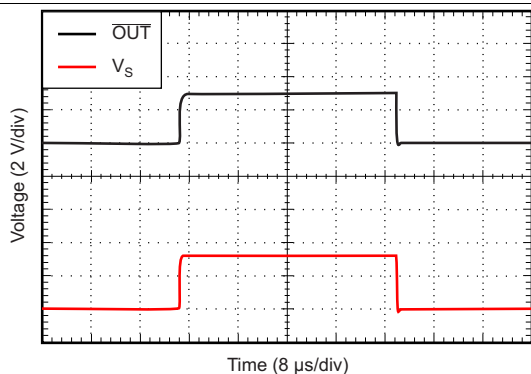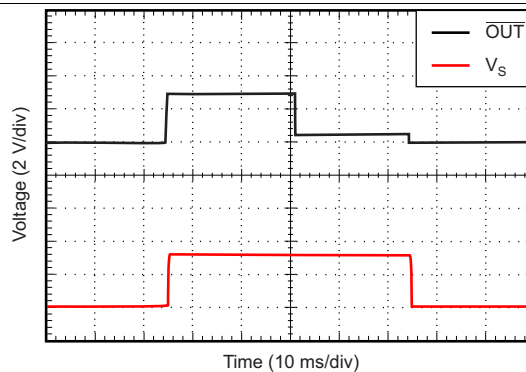At T_A = 25°C and V_S = 3.3 V, unless otherwise noted.

Figure 7. Power-Up and Power-Down Response

TMP302A-Q1, T_A = 55°C   TRIPSET1 = TRIPSET0 = GND

Figure 8. Power-Up, Trip, and Power-Down Response

Submit Documentation Feedback   7

Product Folder Links: *TMP302A   TMP302B   TMP302C   TMP302D*

7 Detailed Description

7.1 Overview

The TMP302 temperature switch is optimal for ultra low-power applications that require accurate trip thresholds. A temperature switch is a device that issues an alert response when a temperature threshold is reached or exceeded. The trip thresholds are programmable to four different settings using the TRIPSET1 and TRIPSET0 pins. Table 1 lists the pin settings versus trip points.

Table 1. Trip Point versus TRIPSET1 and TRIPSET0

TRIPSET1	TRIPSET0	TMP302A	TMP302B	TMP302C	TMP302D
GND	GND	50°C	70°C	90°C	110°C
GND	V_S	55°C	75°C	95°C	115°C
V_S	GND	60°C	80°C	100°C	120°C
V_S	V_S	65°C	85°C	105°C	125°C

7.2 Functional Block Diagram

Product Folder Links: *TMP302A TMP302B TMP302C TMP302D*
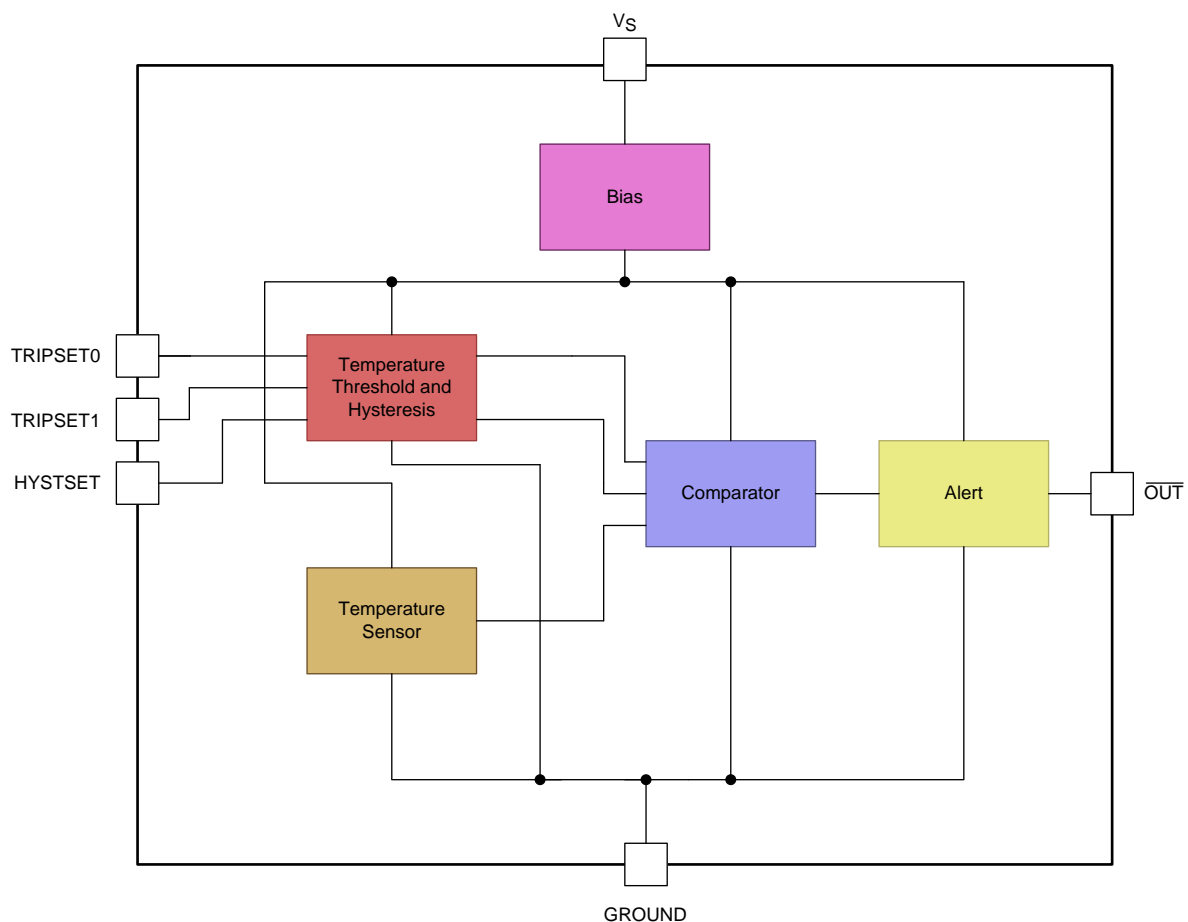
7.3 Feature Description

7.3.1 HYSTSET

If the temperature trip threshold is crossed, the open-drain, active low output ($\overline{\text{OUT}}$) goes low and does not return to the original high state (that is, V_S) until the temperature returns to a value within a hysteresis window set by the HYSTSET pin. The HYSTSET pin allows the user to choose between a 5°C and a 10°C hysteresis window. Table 2 lists the hysteresis window that corresponds to the HYSTSET setting.

Table 2. HYSTSET Window

HYSTSET	THRESHOLD HYSTERESIS
GND	5°C
V_S	10°C

For the specific case of the TMP302A device, if the HYSTSET pin is set to 10°C (that is, connected to V_S) and the device is configured with a 60°C trip point (TRIPSET1 = V_S, TRIPSET0 = GND), when this threshold is exceeded the output does not return to the original high state until it reaches 50°C. This case is more clearly shown in Figure 9.
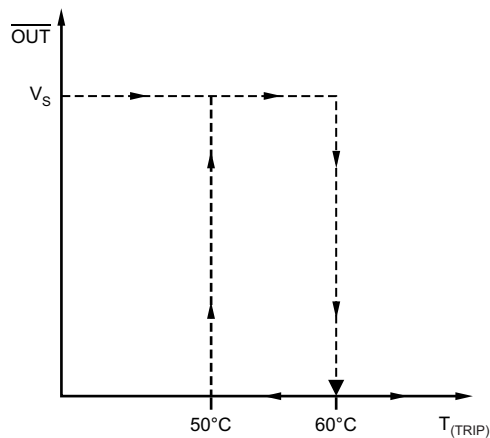

Figure 9. TMP302A: HYSTSET = V_S, TRIPSET1 = V_S, TRIPSET0 = GND

7.4 Device Functional Modes

The TMP302 family of devices has a single functional mode. Normal operation for the TMP302 family of devices occurs when the power-supply voltage applied between the V_S pin and GND is within the specified operating range of 1.4 to 3.6 V. The temperature threshold is selected by connecting the TRIPSET0 and TRIPSET1 pins to either the GND or V_S pins (see Table 1). Hysteresis is selected by connecting the HYSTSET pin to either the GND or V_S pins (see Table 2). The output pin, $\overline{\text{OUT}}$, remains high when the temperature is below the selected temperature threshold. The $\overline{\text{OUT}}$ pin remains low when the temperature is at or above the selected temperature threshold. The $\overline{\text{OUT}}$ pin returns from a low state back to the high state based upon the amount of selected hysteresis (see the *HYSTSET* section).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Configuring the TMP302

The TMP302 family of devices is simple to configure. The only external components that the device requires are a bypass capacitor and pullup resistor. Power-supply bypassing is strongly recommended. Use a 0.1-µF capacitor placed as close as possible to the supply pin. To minimize the internal power dissipation of the TMP302 family of devices, use a pullup resistor value greater than 10 kΩ from the $\overline{\text{OUT}}$ pin to the V_S pin. Refer to Table 1 for trip-point temperature configuration. The TRIPSET pins can be toggled dynamically; however, the voltage of these pins must not exceed V_S. To ensure a proper logic high, the voltage must not drop below 0.7 V × V_S.

8.2 Typical Application

Figure 10 shows the typical circuit configuration for the TMP302 family of devices. The TMP302 family of devices is configured for the default temperature threshold by connecting the TRIPSET0 and TRIPSET1 pins directly to ground. Connecting the HYSTSET pin to ground configures the device for 5°C of hysteresis. Place a 10-kΩ pullup resistor between the $\overline{\text{OUT}}$ and V_S pins. Place a 0.1-µF bypass capacitor between the V_S pin and ground, close to the TMP302x-Q1 device.
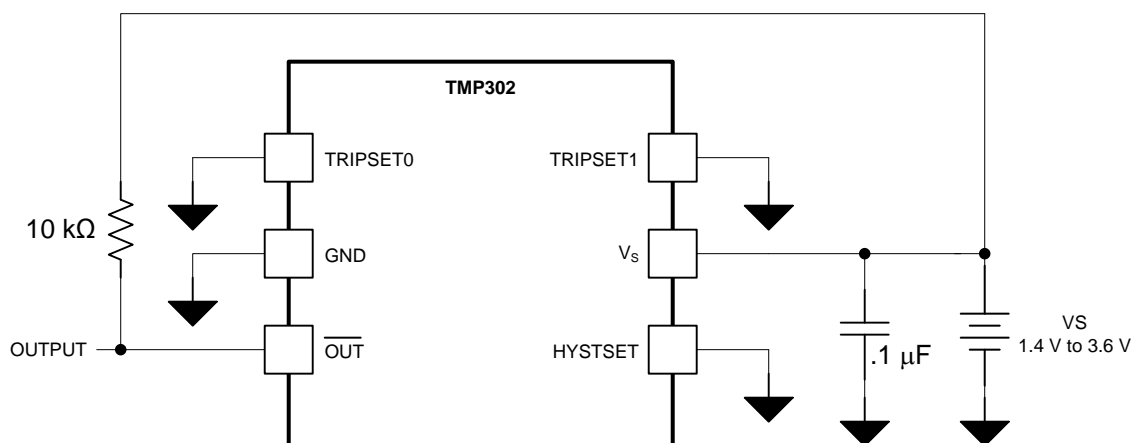

Figure 10. TMP302 Typical Application Schematic

Figure 11 shows the most generic implementation of the TMP302 family of devices. Switches are shown connecting the TMPSET0, TMPSET1, and HYSTSET pins to either V_S or ground. The use of switches is not strictly required; the switches are shown only to illustrate the various pin connection combinations. In practice, connecting the TMPSET0, TMPSET1, and HYSTSET pins to ground or directly to the V_S pin is sufficient and minimizes space and cost. If additional flexibility is desired, connections from the TMPSET0, TMPSET1, and HYSTSET pins can be made through 0-Ω resistors which can be either populated or not populated depending upon the desired connection.

Product Folder Links: *TMP302A TMP302B TMP302C TMP302D*

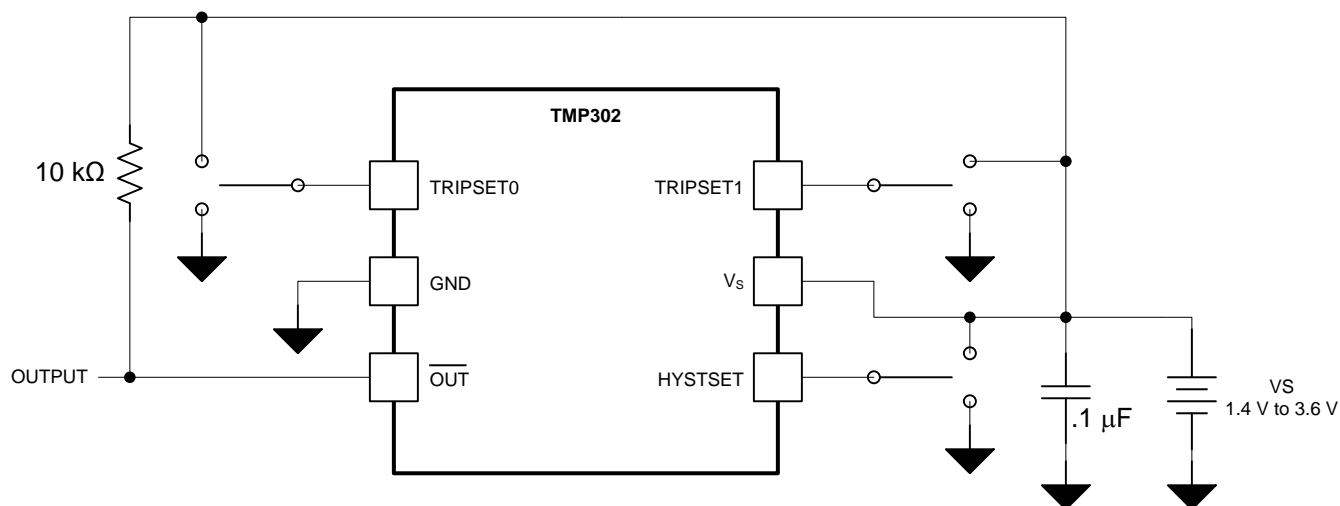## Typical Application (continued)

Figure 11. TMP302 Generic Application Schematic

8.2.1 Design Requirements

Designing with the TMP302 family of devices is simple. The TMP302 is a temperature switch commonly used to signal a microprocessor in the event of an over temperature condition. The temperature at which the TMP302 issues an active low alert is determined by the configuration of the TRIPSET0 and TRIPSET1 pins. These two pins are digital inputs and must be tied either high or low, according to Table 1. The TMP302 will issue an active low alert when the temperature threshold is exceeded. To avoid the TMP302 signaling the microprocessor as soon as the temperature drops below the temperature threshold the TMP302 has built-in hysteresis. The amount of hysteresis is determined by the Hystest pin. This pin is a digital input and must be tied either high or low, according to Table 2.

See Figure 10 and Figure 11 for typical circuit configurations.

8.2.2 Detailed Design Procedure

Determine the threshold temperature and hysteresis required for the application. Connect the TMPSET0, TMPSET1, and HYSTSET pins according to the application requirements. Refer to Table 1 and Table 2. Use a 10-kΩ pullup resistor from the $\overline{\text{OUT}}$ pin to the V_S pin. To minimize power, a larger-value pullup resistor can be used but must not exceed 100 kΩ. Place a 0.1-µF bypass capacitor close to the TMP302 device to reduce noise coupled from the power supply.

Typical Application (continued)

8.2.3 Application Curves

Figure 12 and Figure 13 show the TMP302A power on response with the ambient temperature less than 50°C and greater than 50°C respectively. The TMP302A was configured with trip point set to 50°C. TMP302B, C and D parts behave similarly with regards to power on response with T_A below or above the trip point. Note that the $\overline{OUT}$ signal typically requires 35 ms following power on to become valid.
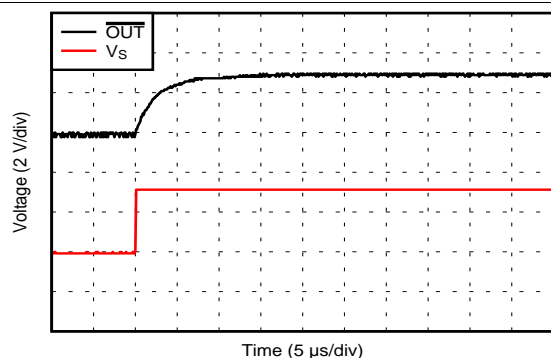

Figure 12. TMP302A Power-On Response, T_A Less than 50°C
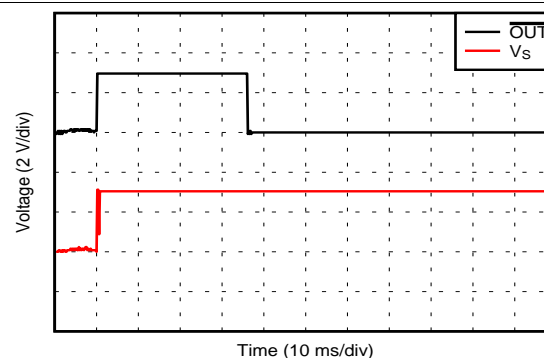
Figure 13. TMP302A Power-On Response, T_A Greater than 50°C

Product Folder Links: *TMP302A   TMP302B   TMP302C   TMP302D*

9 Power Supply Recommendations

The TMP302 family of devices is designed to operate from a single power supply within the range 1.4 and 3.6 V. No specific power supply sequencing with respect to any of the input or output pins is required. The TMP302 family of devices is fully functional within 35 ms of the voltage at the V_S pin reaching or exceeding 1.4 V.

10 Layout

10.1 Layout Guidelines

Place the power supply bypass capacitor as close as possible to the V_S and GND pins. The recommended value for this bypass capacitor is 0.1-µF. Additional bypass capacitance can be added to compensate for noisy or high-impedance power supplies. Place a 10-kΩ pullup resistor from the open drain $\overline{OUT}$ pin to the power supply pin V_S.
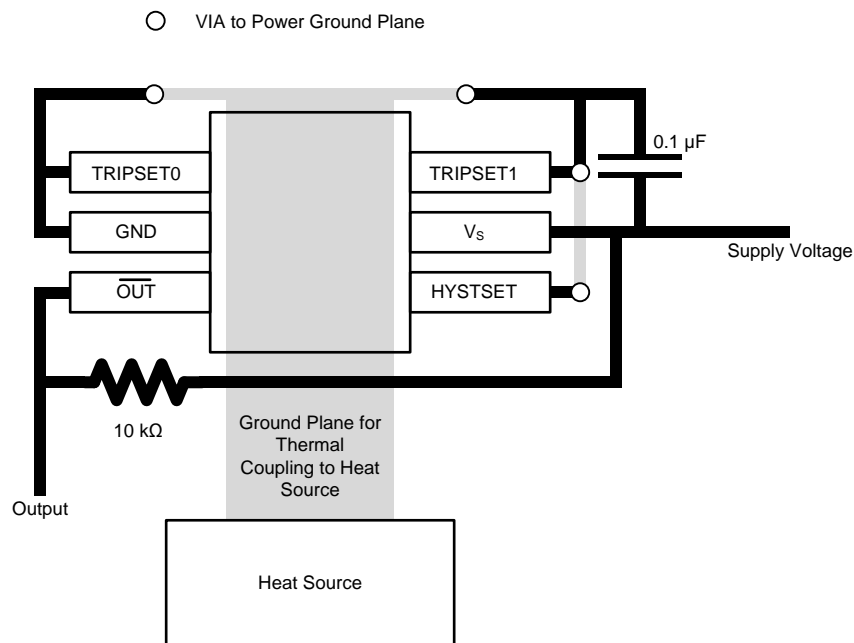
10.2 Layout Example

Figure 14. PCB Layout Example

Product Folder Links: *TMP302A TMP302B TMP302C TMP302D*

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TMP302A	Click here	Click here	Click here	Click here	Click here
TMP302B	Click here	Click here	Click here	Click here	Click here
TMP302C	Click here	Click here	Click here	Click here	Click here
TMP302D	Click here	Click here	Click here	Click here	Click here

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP302ADRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCP	Samples
TMP302ADRLT	ACTIVE	SOT	DRL	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCP	Samples
TMP302BDRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCT	Samples
TMP302BDRLT	ACTIVE	SOT	DRL	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCT	Samples
TMP302CDRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCR	Samples
TMP302CDRLT	ACTIVE	SOT	DRL	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCR	Samples
TMP302DDRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCS	Samples
TMP302DDRLT	ACTIVE	SOT	DRL	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCS	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

Cavity

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP302ADRLR	SOT	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP302ADRLT	SOT	DRL	6	250	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP302BDRLR	SOT	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP302BDRLR	SOT	DRL	6	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
TMP302BDRLT	SOT	DRL	6	250	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
TMP302BDRLT	SOT	DRL	6	250	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP302CDRLR	SOT	DRL	6	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
TMP302CDRLR	SOT	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP302CDRLT	SOT	DRL	6	250	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
TMP302DDRLR	SOT	DRL	6	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
TMP302DDRLR	SOT	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP302DDRLT	SOT	DRL	6	250	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP302DDRLT	SOT	DRL	6	250	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP302ADRLR	SOT	DRL	6	4000	202.0	201.0	28.0
TMP302ADRLT	SOT	DRL	6	250	202.0	201.0	28.0
TMP302BDRLR	SOT	DRL	6	4000	202.0	201.0	28.0
TMP302BDRLR	SOT	DRL	6	4000	184.0	184.0	19.0
TMP302BDRLT	SOT	DRL	6	250	184.0	184.0	19.0
TMP302BDRLT	SOT	DRL	6	250	202.0	201.0	28.0
TMP302CDRLR	SOT	DRL	6	4000	184.0	184.0	19.0
TMP302CDRLR	SOT	DRL	6	4000	202.0	201.0	28.0
TMP302CDRLT	SOT	DRL	6	250	184.0	184.0	19.0
TMP302DDRLR	SOT	DRL	6	4000	184.0	184.0	19.0
TMP302DDRLR	SOT	DRL	6	4000	202.0	201.0	28.0
TMP302DDRLT	SOT	DRL	6	250	202.0	201.0	28.0
TMP302DDRLT	SOT	DRL	6	250	184.0	184.0	19.0

A
1,70 / 1,50
C
6X 0,27 / 0,13
B
6 5 4
C 1,30 / 1,10
1,70 / 1,50
Pin 1 Index Area
1 2 3
0,50
6X 0,25 / 0,15

| ⊕ | 0,10 Ⓜ | C | A | B |
| | 0,05 Ⓜ | C | | |

0,60 / 0,50
0,05 C
Seating Plane
C
0,05 / 0,00
0,18 / 0,08

1 2 3
6X 0,40 / 0,20
6 5 4

Bottom View

4205622−3/D 08/2007
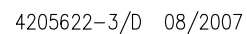
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs.
Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

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