

OMAP-L137

Evaluation Module

***Technical
Reference***

OMAP-L137 Evaluation Module Technical Reference

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About This Manual

This document describes the board level operations of the OMAP-L137 Evaluation Module (EVM). The EVM is based on the Texas Instruments OMAP-L137 Processor.

The OMAP-L137 Evaluation Module is a table top card that allows engineers and software developers to evaluate certain characteristics of the OMAP-L137 processor to determine if the processor meets the designers application requirements. Evaluators can create software to execute on board or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The OMAP-L137 Evaluation Module will sometimes be referred to as the OMAP-L137 EVM or EVM.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

```
equations  
!rd = !strobe&rw;
```

Information About Cautions

This book may contain cautions.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents, Application Notes and User Guides

Information regarding the OMAP-L137 can be found at the following Texas Instruments website:

<http://www.ti.com>

Table 1: Manual History

Revision	History
A	Beta

Table 2: Board History

PWB Revision	History
D	Beta Release

Chapter 1

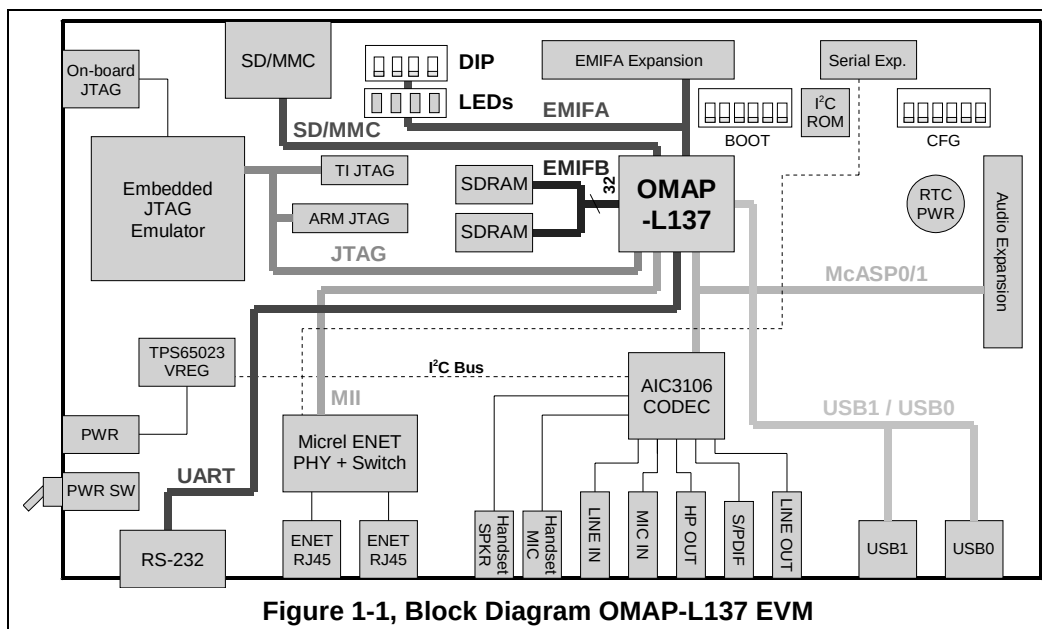
Introduction to the OMAP-L137 EVM

Chapter One provides a description of the OMAP-L137 EVM along with the key features and a block diagram of the circuit board.

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1.1 Key Features

The OMAP-L137 EVM is a standalone development platform that enables users to evaluate and develop applications for the OMAP-L137 processor. Schematics and application notes are available to ease hardware development and reduce time to market.



The EVM comes with a full complement of on board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments OMAP-L137 device with a C674x VLIW DSP floating point processor and an ARM926EJ-S processor operating up to 300 Mhz.
- 64 Megabytes SDRAM
- SPI Boot EEPROM
- 2 Port Ethernet Phy/switch
- SD/MMC/MMC Plus media card interfaces
- TLV320AIC3106 Stereo Codec
- USB 1.1 High speed interface
- USB2 2.0 Full speed interface
- RS-232 Interface

- On chip real time clock
- Configurable boot load options
- 4 user LEDs/4 position user DIP switch
- Single voltage power supply (+5V)
- Expansion connectors for daughter card use
- Embedded JTAG Emulation
- 14 Pin TI JTAG/20 Pin ARM JTAG Interfaces

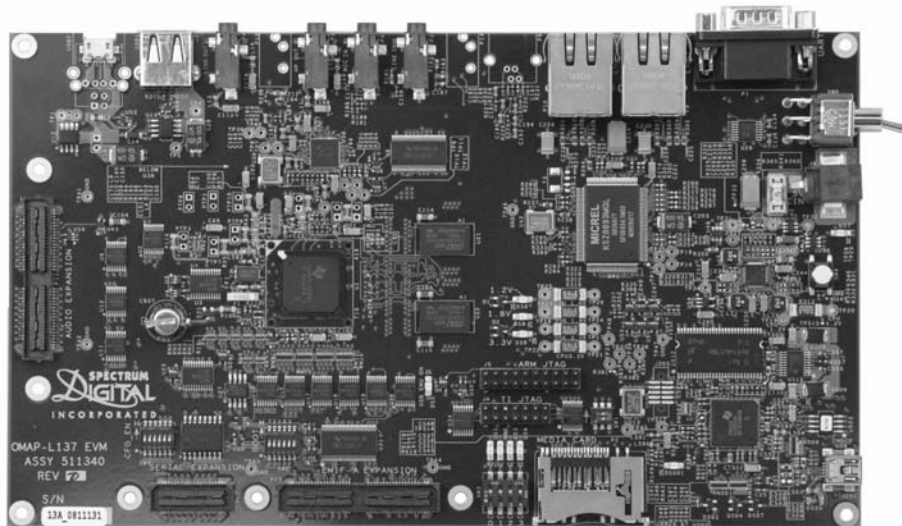


Figure 1-2, OMAP-L137 EVM

1.2 Functional Overview of the OMAP-L137 EVM

The OMAP-L137 on the EVM interfaces to on-board peripherals through the 16-bit wide multiplexed EMIF interface pins. The SDRAM memory is connected to its own dedicated 32 bit wide bus.

An on-board AIC3106 codec allows the DSP to transmit and receive analog audio signals. The I²C bus is used for the codec control interface, while the McASP controls the audio stream. Signal interfacing is done through 3.5mm audio jacks that correspond to microphone input, headphone output, line input, and line output.

The EVM includes 4 user LEDs, a 4 position user DIP switch, and on chip real time clock. On board multi-plexing allows ease of interfacing to the daughter cards.

An included +5V external power supply is used to power the board. On-board switching voltage regulators provide the CPU core voltage, +3.3V, +1.8V for peripheral interfacing. The board is held in reset by the on board power controller until these supplies are within operating specifications.

Code Composer Studio communicates with the EVM through an embedded emulator or via the TI 14 pin or ARM 20 pin external JTAG connectors.

1.3 Basic Operation

The EVM is designed to work with TI's Code Composer Studio IDE™, or MontaVista tool environments. Code Composer communicates with the board through an on board JTAG emulator. This EVM is shipped with an EVM specific Code Composer Studio environment. To start, follow the instructions in the Quick Start Guide to install Code Composer. This process will install all of the necessary development tools, documentation and drivers.

1.4 Memory Map

The OMAP-L137 processor has a byte addressable address space. However, there are some limitations to byte addressing determined by peripheral interconnection to the OMAP-L137 device. Program code and data can be placed anywhere in the unified address space. Addresses are multiple sizes depending on hardware implementation. Refer to the appropriate device data sheets for more details.

The memory map shows the address space of a generic OMAP-L137 processor on the left with specific details of how each region is used on the right. By default, the internal memory sits at the beginning of the address space. Portions of memory can be remapped in software as L2 cache rather than fixed RAM.

The part incorporates a dual EMIF interface. One dedicated EMIF, EMIF-B, directly interfaces to the SDRAM memory. EMIF-A has 3 separate addressable regions called chip enable spaces (CE0, CS2, CS3), however the EVM uses this interface as a peripheral interface to daughter card connectors. The memory map of the OMAP-L137 EVM is shown in the table below.

Table 1: OMAP-L137 EVM Memory Map

Start Address	End Address	ARM Mem Map	DSP Mem Map
0x0080 0000	0x0083 FFFF		DSP L2 RAM
0x00E0 0000	0x00f0 7FFFF		DSP L1P RAM
0x00F0 0000	0x00F0 8000		DSP L1D RAM
0x0184 0000	0x0184 FFFF		DSP Memory System
0x1180 0000	0x1183 FFFF		DSP L2 RAM
0x11E0 0000	0x11E0 7FFF		DSP L1P RAM
0x1FF0 0000	0x11F0 7FFF		DSP L1D RAM
0x8000 0000	0x8001 FFFF		Shared RAM
0xB000 0000	0xB000 7FFF		EMIFB control regs
0xC000 0000	0xDFFF FFFF		EMIFB SDRAM Data
0xFFFFE E000	0xFFFFE FFFF	ARM Interrupt Controller	
0xFFFF 0000	0xFFFF 1FFF	ARM Local RAM	

1.5 Boot Switch Settings

The EVM has a 5 position switch that allow users to configure the operational state of the processor when it is released from reset and determine the source for processor booting. Switch SW2 configures the boot mode that will be used when the DSP starts executing. By default the switches are configured to serial EEPROM boot. The table below shows the boot mode sources and their respective switch positions.

Table 2: SW2, Boot Mode Select

Pos 1 Boot[7]	Pos 2 Boot[2]	Pos 3 Boot[1]	Pos 4 Boot[0]	Pos 5 Boot[3]	Boot Pin BTMODE[7,2,1,0,3]	Boot Mode
OFF	OFF	OFF	ON	NA	0 0 0 1 x	NOR
OFF	OFF	ON	OFF	NA	0 0 1 0 x	HPI
OFF	ON	OFF	ON	NA	0 1 0 1 x	SPI0 Flash
OFF	ON	ON	OFF	NA	0 1 1 0 x	SPI1 Flash
OFF	ON	ON	ON	NA	0 1 1 1 x	NAND 8-bit
OFF	OFF	OFF	OFF	OFF	0 0 0 0 0	I ² C0 Master
OFF	OFF	OFF	OFF	ON	0 0 0 0 1	I ² C0 Slave
OFF	OFF	ON	ON	OFF	0 0 1 1 0	I ² C1 Master
OFF	OFF	ON	ON	ON	0 0 1 1 1	I ² C1 Slave
OFF	ON	OFF	OFF	OFF	0 1 0 0 0	SPI0 EEPROM *
OFF	ON	OFF	OFF	ON	0 1 0 0 1	SPI1 EEPROM
ON	OFF	OFF	ON	OFF	1 0 0 1 0	SPI0 Slave
ON	OFF	OFF	ON	ON	1 0 0 1 1	SPI1 Slave
ON	OFF	ON	ON	OFF	1 0 1 1 0	UART0
ON	OFF	ON	ON	ON	1 0 1 1 1	UART1
ON	OFF	ON	OFF	OFF	1 0 1 0 0	UART2 *
ON	ON	ON	ON	OFF	1 1 1 1 0	Emulation Debug *

* Supported on Standalone EVM

1.6 Power Supply

The EVM operates from a single +5V external power supply connected to the main power input (J6), a 2.5 MM. barrel-type plug. Internally, the +5V input is converted into core voltage, +1.8V and +3.3V using Texas Instruments TPS65023 Power Management Unit. The +3.3V and +1.8V supply are used for the DSP's I/O buffers and other chips on the board.

Chapter 2

Board Components

This chapter describes the operation of the major board components on the OMAP-L137 EVM.

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2.1 EMIF-A Interfaces

A separate 16 bit EMIF with three chip enables divide up the address space and allow for asynchronous accesses on the EVM. The EVM uses this interface for peripheral interfaces to the daughter card.

2.1.1 EMIF-B SDRAM Memory Interface

The OMAP-L137 device incorporates a dedicated 32 bit wide SDRAM memory bus. The EVM uses two 256 Megabit, 16 bit wide memories on this bus, for a total of 64 megabytes of memory for program, data, and video storage. The internal SDRAM controller uses a PLL to control the SDRAM memory timing. Memory refresh for SDRAM is handled automatically by the OMAP-L137 internal SDRAM controller.

2.1.2 Memory Card Interface

The EVM supports SD/MMC/MMC PLUS media card interfaces. This interface is multiplexed with other function the EMIFA bus.

2.1.3 UART Interface

The internal UART2 on the OMAP-L137 device is driven to connector P1. The UART's interface is routed to the RS-232 line drivers prior to being brought out to a DB-9 connector, P1.

2.1.4 USB Interface

The OMAP-L137 incorporates two on chip USB controllers. The USB 2.0 interface is brought out to a micro A/B connector. A jumper is provided to make a flexible host, peripheral, and USB on the go interface. The second USB 1.1 interface is brought out to an A type host interface connector.

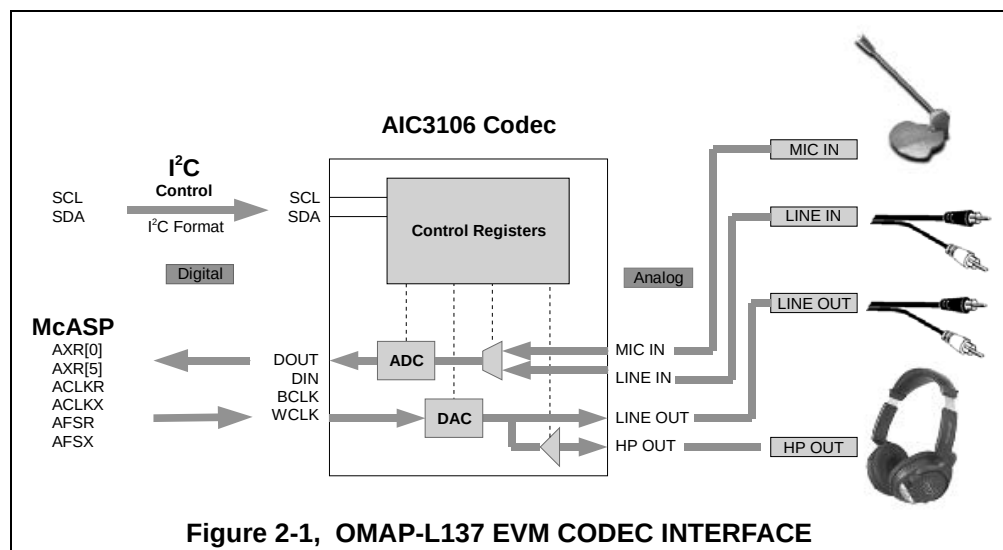
2.2 AIC3106 Interface

The EVM incorporates a Texas Instruments TLV320AIC3106 stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the DSP. When the DSP is finished with the data it uses the codec to convert the samples back into analog signals on the line output so the user can hear the output.

The codec communicates using two serial channels, one to control the codec's internal configuration registers and one to send and receive digital audio samples. The I²C bus is used as the AIC3106's control channel. The control channel is generally only used when configuring the codec, it is typically idle when audio data is being transmitted,

McASP1 is used as the bi-directional data channel. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source and serial data format. The EVM examples generally use a 16-bit sample width with the codec in master mode so it generates the frame sync and bit clocks at the correct sample rate without effort on the DSP side.

The codec is clocked via a 24.576 Mhz oscillator. The internal sample rate generator subdivides the default system clock to generate common audio frequencies. The sample rate is set by a codec register. The figure below shows the codec interface on the OMAP-L137 EVM.



2.3 Ethernet Interface

The OMAP-L137 incorporates an ethernet MAC which interfaces to a Micrel KSZ8893MQL ethernet switch. The multi-port 10/100 Mbit interface is isolated and brought out to two RJ-45 standard ethernet connectors, P9, P10. The ethernet addresses is stored in the on board I²C EEPROM. The 2 ethernet addresses stored in the EEPROM are the first address and the address + 1. The first address should always be an even number. The I²C bus is also used to control configuration registers in the switch that are not accessible via the MDIO module.

Two ports provide the ability to input and pass data for Voice Over IP (VOIP) or other daisy chained applications. Connector P9 is the primary port for normal operation.

The RJ-45 jacks have 2 LEDs integrated into their connector. The LEDs are green and yellow and provide link and transmit status from the ethernet controller.

The MAC address for each EVM is also written on a label on the bottom of the board. The figure below shows an examples of this.

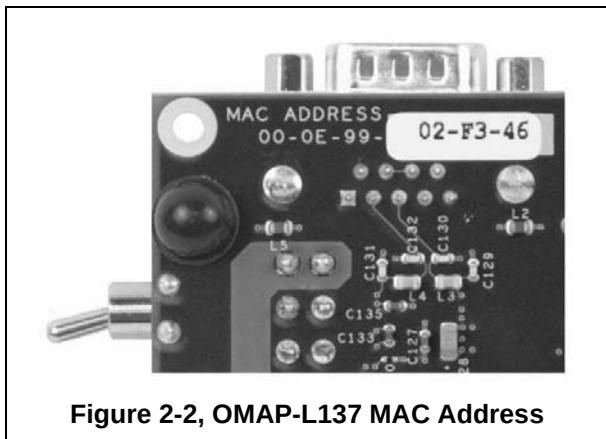
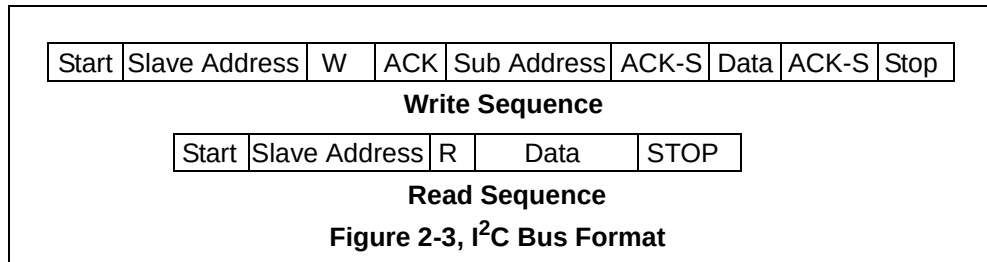


Figure 2-2, OMAP-L137 MAC Address

2.4 I²C0 Interface

The I²C0 bus on the OMAP-L137 is ideal for interfacing to the control registers of many devices. On the OMAP-L137 EVM the I²C0 bus is used to configure the ethernet phy and Codec. An I²C ROM is also interfaced via the serial bus. The format of the bus is shown in the figure below.



The addresses of the on board peripherals are shown in the table below.

Table 1: I²C0 Memory Map

Device	Address	R/W	Function
KSZ8893MQL	0x5D	R/W	Ethernet Switch
TLV320AIC3106	0x1B	R/W	CODEC
I ² C EEPROM	0x25	R/W	I ² C EEPROM

2.5 Daughter Card Interfaces

The EVM provides expansion connectors that can be used to accept plug-in daughter cards. The daughter card allows users to build on their EVM platform to extend its capabilities and provide customer and application specific I/O. The expansion connectors are interfaces which include McASP, and serial I/O expansion. The EMIF-A signals are brought out as LCD, peripheral, or EMIF signals.

The daughter card connectors used on the EVM are shown in the table below.

Table 2: Daughter Card Connectors

Reference Designator	Part Numbers Used On EVM	Manufacturer
P11	QSE-040-01-L-D-A-K	Samtec
P12	QSE-020-01-L-D-A-K	Samtec
P13	QSE-040-01-L-D-A-K	Samtec

One of the compatible mating daughter card connectors used to interface to the EVM are shown in the table below (other heights are available).

Table 3: Mating Daughter Card Connectors

Reference Designator	Part Numbers Used On EVM	Manufacturer
XP11	QTE-040-02-L-D-A-K	Samtec
XP12	QTE-020-02-L-D-A-K	Samtec
XP13	QTE-040-02-L-D-A-K	Samtec

Chapter 3

Physical Description

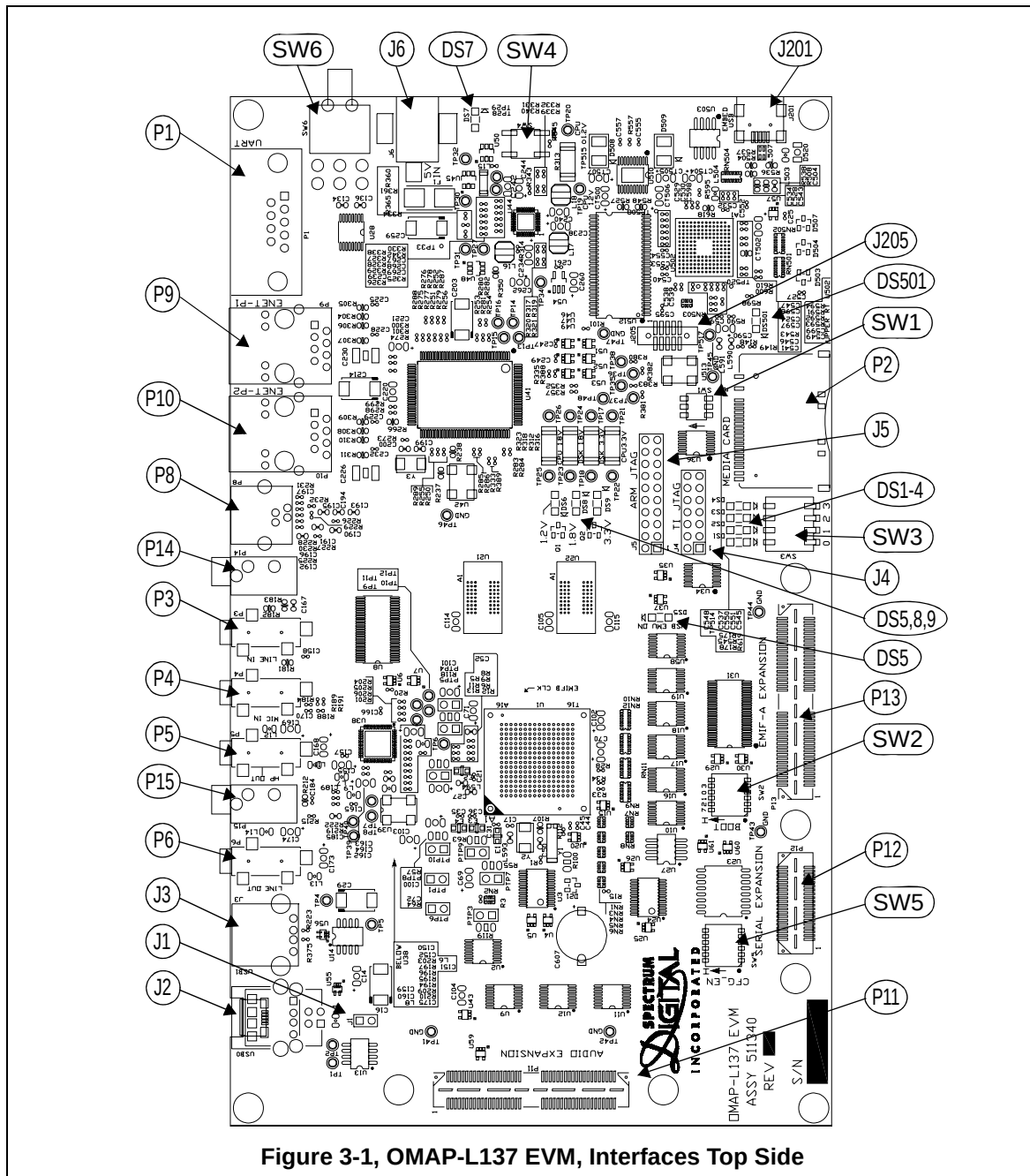
This chapter describes the physical layout of the OMAP-L137 EVM and its interfaces.

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3.1 Board Layout

The OMAP-L137 EVM is a 5.0 x 8.55 inch (127 x 217 mm.) ten (10) layer printed circuit board which is powered by an external +5 volt only power supply. Figure 3-1 shows the layout of the top side of the OMAP-L137 EVM.



3.2 Connectors

The EVM has numerous connectors and option jumpers to control and provide connections to various peripherals. These connectors and jumpers are described in the following sections.

Table 1: Connectors

Connector	Size	Function
J1	1 x 2	USB Capacitance Select
J2	2	USB Interface
J3	6	USB Interface
J4	2 x 7	TI 14 Pin JTAG
J5	2 x 8	ARM JTAG Emulation Header
J6	2	+5V In
P1	9	RS-232 UART
P2	28	SD/MMC Connector
P3	4	Line In
P4	4	Microphone In
P5	4	Headphone Out
P6	4	Line Out
P8	4	RJ9 Connector
P9	12	Ethernet
P10	12	Ethernet
P11	2 x 45	Audio Expansion Connector
P12	2 x 22	Expansion 2
P13	2 x 45	Expansion 3
P14	3	Phono Jack
P15	3	Phono Jack
J201		Embedded JTAG Interface
J205	2 x 5	Not populated, factory use only

3.2.1 J1, USB Capacitance Select

Connector J1 is a jumper is used to provide more capacitance when the USB connector is used in the host mode. When the jumper is shorted the extra capacitance is provided. These open and shorted position are shown below.

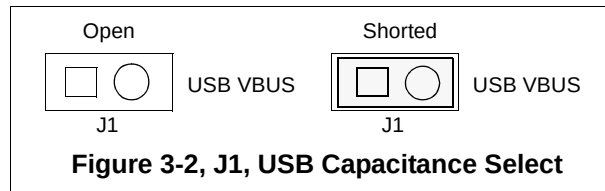


Table 2: J1, USB Capacitance Select

Position	Function
Open	6.8 uF Capacitance
Shorted	106.8 uF Capacitance

3.2.2 J2, USB 2.0 Connector and Jumpers

Connector J2 is a micro A/B USB connector. The pinout for the J2 connector is shown in the table below.

Table 3: J2, USB Connector

Pins	Signal
1	USB_VBUS
2	USB_DM
3	USB_DP
4	USB_ID
5-9	USB_SHIELD

* Use internal register to swap DM/DP pair. This feature was used to improve printed circuit board routing.

The EVM supplies up to 500 ma of current to the USB_VBUS via a TPS2065. This is enabled via the OMAP-L137's DRV_VBUS pin. J1 supplies extra capacitance for host mode operations. Remove J1 for "USB On The Go" operations.

3.2.3 J3, USB 1.1 Connector

Connector J3 is a USB-A connector. This connector is connected directly to the OMAP L137 processor. A TPS2065 switches on host power via the L137 GPIO[15]. The pinout for the J3 connector is shown in the table below.

Table 4: J3, USB Connector

Pins	Signal
1	VBUS
2	D-, USB1_DM
3	D+, USB1_DP
4	GND, Ground
5	USB_Shield
6	USB_Shield

3.2.4 J4, 14 Pin External JTAG Connector

Connector J4 is a 2 x 7 double row male header. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs. The pinout for the connector is shown in the figure below.

TMS	1	2	TRST-	Header Dimensions Pin-to-Pin spacing, 0.100 in. (X,Y) Pin width, 0.025-in. square post Pin length, 0.235-in. nominal
TDI	3	4	GND	
PD (+3.3V)	5	6	no pin (key)	
TDO	7	8	GND	
TCK-RET	9	10	GND	
TCK	11	12	GND	
EMU0	13	14	EMU1	

Figure 3-3, 14 Pin External JTAG Connector

3.2.5 J5, ARM JTAG Emulation Header

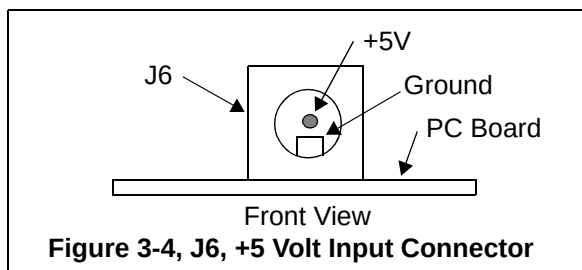
The J5 emulation header is located on the top side of the board and is used to provide an interface to ARM compatible JTAG emulators. The pinout for this connector is shown in the table below.

Table 5: J5, ARM JTAG Emulation Header

Pin #	Signal	Pin #	Signal
1	VCC_3V3	2	VCC_3V3
3	ARM_TRSTn	4	Ground
5	ARM_TDI	6	Ground
7	ARM_TMS	8	Ground
9	ARM_TCK	10	Ground
11	ARM_TCKRET	12	Ground
13	ARM_TDO	14	Ground
15	ARM_RSTn	16	Ground
17	NC	18	Ground
19	NC	20	Ground

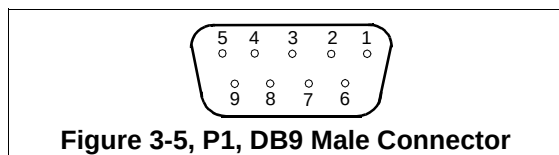
3.2.6 J6, +5V Input

Connector J6 is the input power connector. This connector brings in +5 volts to the EVM. This is a 2.5mm. jack. The inside of the jack is tied to through a fuse to VCC_5V. The other side is tied to ground and LED DS7. The figure below shows this connector as viewed from the card edge.



3.2.7 P1, RS-232 UART

The P1 connector is a 9 pin male D-connector which provides a UART interface to the EVM. This connector interfaces to the MAX 3221 RS-232 line driver (U28) and is located on the top side of the board. A view of the connector from the card edge is shown in the figure below. The signals present on this connector are defined in the following table.



The pin numbers and their corresponding signals are shown in the table below. This corresponds to a standard dual row to DB-9 connector interface used on personal computers.

Table 6: P1, RS-232 Pinout

Pin #	Signal Name
1	NC
2	R_IN, Rx Data
3	T_OUT, Tx Data
4	NC
5	GND
6	NC
7	Pin 8
8	Pin 7
9	NC

3.2.8 P2, MMC/SD Connector

The P2 MMC/SD connector is located on the top side of the board and is used to provide an interface to the following interfaces: MMC+, SD, and MMC. The pinout for the P2 connector is shown in the table below.

Table 7: P2, MMC/SD Connector

Pin #	Signal
1	MMC_SD_DATA3 - #1_MMC+/MMC/SD
2	MMC_SD_CMD - #2_MMC+/MMC/SD
3	GND - #3_MMC+/MMC/SD
4	DSK_3V3 - #4_MMC+/MMC/SD
5	MMC_SD_CLK - #5_MMC+/MMC/SD
6	GND - #6_MMC+/MMC/SD
7	MMC_SD_DATA0 - #7_MMC+/MMC/SD
8	MMC_SD_DATA1 - #8_MMC+/SD
9	MMC_SD_DATA2 - #9_MMC+/SD
10	MMC_SD_DATA4 - #10_MMC+
11	MMC_SD_DATA5 - #11_MMC+
12	MMC_SD_DATA6 - #12_MMC+
13	MMC_SD_DATA7 - #13_MMC+/
14	MMC_SD_WP - SD_WP
15	MMC_SD_INS - CD
16	Reserved
17	Reserved
18	GND
19	DSK_3V3
20	Reserved
21	GND
22	Reserved
23	Reserved
24	Reserved
25	NC -
26	NC -
27	GND
28	GND

3.2.9 P3, Line In

Connector P3 is an stereo audio line input. The input connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

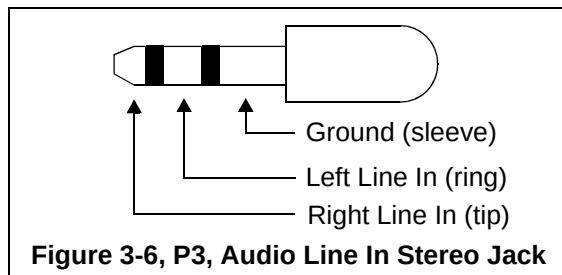


Table 8: P3, Line In Interface

Pin #	AIC3106 Signal
1 (sleeve)	GND_AC
2 (ring)	LINE1L+
3 (tip)	LINE1R+
4 (sleeve)	GND_AC

3.2.10 P4, Microphone In

Connector P4 is an stereo microphone line input. The input connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

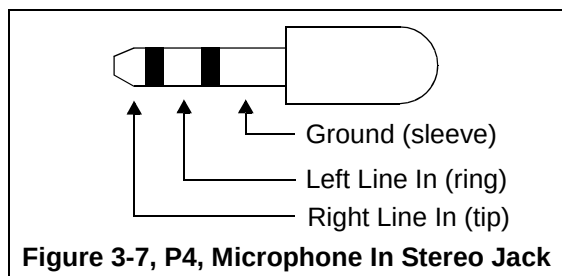


Table 9: P4, Microphone In Interface

Pin #	AIC3106 Signal
1 (sleeve)	GND_AC
2 (ring)	MIC3L/MIC3R
3 (tip)	MIC3L/MIC3R
4 (sleeve)	GND_AC

3.2.11 P5, Headphone Out

The P5 connector is a 3.5 mm. stereo headphone output from the TVL320AIC3106 on the EVM. The signals on the mating plug are shown in the figure below. The signals present on this connector are defined in the following table.

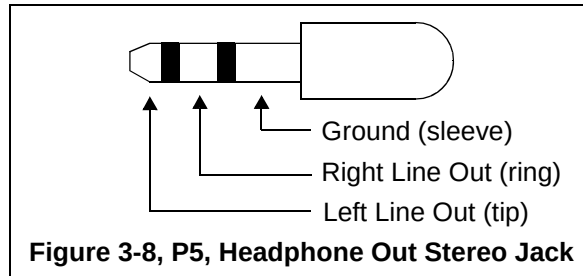


Table 10: P5, Headphone Out Interface

Pin #	AIC3106 Signal
1(sleeve)	GND_AC
2(ring)	HPLOUT
3(tip)	HPROUT
4	NC

3.2.12 P6, Line Out

The audio line out connector P6, is a stereo output. The output connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

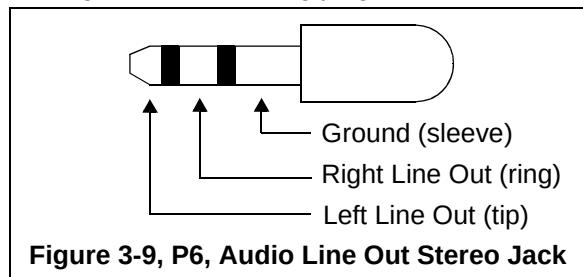


Table 11: P6, Audio Line Out Stereo Jack

Pin #	AIC33 Signal
1 (sleeve)	GND_AC
2 (ring)	LEFT_LO+
3 (tip)	RIGHT_LO+
4 (sleeve)	NC

3.2.13 P8, RJ9 Connector

The headset interface, P8, is a standard RJ9-4 connector which is not populated as shipped.

3.2.14 P9, Ethernet Interface

The P9 connector is located on the top side of the board and is used to provide an Ethernet interface. P9 integrates the magnetics and standard RJ-45 connector. The two tables below show the signals present on the magnetics interface and the connector side.

Table 12: P9, Magnetics/LEDs Interface Signals

Pin #	Signal	Pin #	Signal
1	TXP1 (TXD+)	2	TXM1 (TXD-)
3	RXP1 (RXD+)	4	ENET_VDDATR (TXD-CT)
5	ENET_VDDATR (RXD-CT)	6	RXM1 (RXD-)
7	NC1	8	GND
9	VCC_3V3(LED1+)	10	P1LED2(LED1-)
11	DSK_3V3(LED2+)	12	P1LED3(LED2-)

The ethernet connector incorporates 2 LEDs which give link and transmit status from the ethernet controller.

Table 13: P9, RJ-45 Connector

Pin #	Signal	Pin #	Signal
1	TX_DATA+	2	TX_DATA-
3	RX_DATA+	4	NC
5	NC	6	RX_DATA-
7	NC	8	NC

3.2.15 P10, Ethernet Interface

The P10 connector is located on the top side of the board and is used to provide an Ethernet interface. P10 integrates the magnetics and standard RJ-45 connector. The two tables below show the signals present on the magnetics interface and the connector side.

Table 14: P10, Magnetics/LEDs Interface Signals

Pin #	Signal	Pin #	Signal
1	TXP2 (TXD+)	2	TXM2 (TXD-)
3	RXP2 (RXD+)	4	ENET_VDDATR (TXD-CT)
5	ENET_VDDATR (RXD-CT)	6	RXM2 (RXD-)
7	NC1	8	GND
9	VCC_3V3(LED1+)	10	P2LED2(LED1-)
11	DSK_3V3(LED2+)	12	P2LED3(LED2-)

The ethernet connector incorporates 2 LEDs which give link and transmit status from the ethernet controller.

Table 15: P10, RJ-45 Connector

Pin #	Signal	Pin #	Signal
1	TX_DATA+	2	TX_DATA-
3	RX_DATA+	4	NC
5	NC	6	RX_DATA-
7	NC	8	NC

3.2.16 Expansion Connector Overview

The EVM has three expansion connectors which allow the user to interface to other logic which is unique to his application

Some of the signals on the EVM are multiplexed with an on board resource or they have multiple options on the L137 device. To enable these signals there are several control lines on the expansion connector. Pulling the control lines high enables the functions marked in the Mux_Ctl column tables. The number in the Mux_Ctl column indicates which pins it controls. An 'N' in front of the column indicates the pin is available when the control line is not pulled high. Each control line is pulled down on the EVM, therefore a pull-up resistor of approximately 500 ohms is required to enable the control line to a logic '1'. A '*' in the Mux_Ctl column indicates this is a control line on the expansion connectors.

The next 3 tables indicate the interface signal and the appropriate control line on the pins of the expansion connectors.

3.2.16.1 P11, Audio / Expansion Connector

Table 16: P11, Audio / Expansion Connector

Pin	Signal	Mux_Ctl	Pin	Signal	Mux_Ctl
2	VCC_5V		1	VCC_5V	
4	VCC_5V		3	VCC_5V	
6	NC		5	I2C0_SDA	
8	SEL_ENETn_MCASP0	* 1	7	I2C0_SCL	
10	T_AMUTE0		9	EXP_ACHLKR0	1
12	Ground		11	Ground	
14	EXP1_AFSX0		13	T_AFSR0	
16	Ground		15	Ground	
18	T_ACLKX0		17	T_ACLKR0	
20	Ground		19	Ground	
22	EXP_AXR0[0]	1	21	EXP_AXR[8]	1
24	EXP_AXR0[1]	1	23	EXP_AXR0_9	N7
26	EXP_AXR0[2]	1	25	EXP_AXR0_10	N7
28	EXP_AXR0[3]	1	27	EXP1_AXR0_12	N11
30	EXP_AXR0[4]	1	29	EXP1_AXR0_13	N11
32	EXP_AXR0[5]	1	31	EXP1_AXR0_14	N11
34	EXP_AXR0[6]	1	33	EXP1_AXR0_15	N11
36	EXP_AXR0[7]	1	35	T_AXR0_11/AXR2_0/GPIO3_11	
38	Ground		37	Ground	
40	AHCLKR2		39	EXP1_AMUTE2_8	N12
42	EXP1_SPI1_SCSn	3	41	EXP1_SPI1_ENAn	3
44	EXP1_SPI1_CLK		43	EXP1_SPI1_SIMO	
46	EXP_RESETh		45	EXP1_SPI1_SOMI	
48	Ground		47	Ground	
50	T_AMUTE1		49	EXP_AHCLKX1	2
52	Ground		51	Ground	
54	EXP_AFSX1	2	53	T_AFSR1	
56	Ground		55	Ground	
58	EXP_ACLKX1	2	57	T_ACLKR1	
60	Ground		59	Ground	
62	EXP_AXR1[0]	2	61	T_AXR1[6]	
64	EXP_AXR1[1]		63	T_AXR1[7]	
66	EXP_AXR1[2]		65	T_AXR1[8]	
68	EXP_AXR1[3]	N5	67	T_AXR1[9]	
70	EXP_AXR1[4]	N5	69	T_AXR1[10]	
72	EXP_AXR1[5]	2	71	T_AXR1[11]	
74	EXP1_SEL_MCASP1	* 2	73	SEL_SPI1_EXP1	* 3
76	NC		75	NC	
78	VCC_5V		77	VCC_5V	
80	VCC_5V		79	VCC_5V	
82	Ground		81	Ground	
84	Ground		83	Ground	
86	Ground		85	Ground	
88	Ground		87	Ground	
90	NC		89	NC	

* 1 Control line for Mux_Ctl 1 signals,

* 3 Control line for Mux_Ctl 3 signals,

* N7 is not control signal 7 (default),

* N12 is not control signal 12 (default)

* 2 Control line for Mux_Ctl 2 signals

* N5 is not control signal 5 (default)

* N11 is not control signal 11 (default)

3.2.16.2 P12, Expansion 2 Connector

Table 17: P12, Expansion 2 Connector

Pin	Signal	Mux_Ctl	Pin	Signal	Mux_Ctl
2	VCC_5V		1	VCC_5V	
4	VCC_5V		3	VCC_5V	
6	Ground		5	Ground	
8	EXP_SPI1_SOMI	9	7	EXP2_SPI0_SOMI	6
10	EXP2_SPI1_SIMO	9	9	EXP2_SPI0_SOMO	6
12	EXP_SPI1_CLK	9	11	EXP2_SPI0_CLK	6
14	EXP2_SPI1_SCSn	4	13	EQEP0A	6
16	EXP2_SPI1_ENAn	4	15	EQEP0B	6
18	Ground		17	Ground	
20	SEL_SPI1_EXP2	* 4	19	IC20_SCL	
22	EXP_EQEP1A	5	21	IC20_SDA	
24	EXP_EQE1B	5	23	NC	
26	SEL_EXP2_QEP1	* 5	25	SEL_EXP2_QEP0	* 6
28	EXP2_UART1_RXD	7	27	EXP2_TMP640_OUT12	9
30	EXP2_UART1_TXD	7	29	EXP2_TMP640_IN12	9
32	Ground		31	Ground	
34	SEL_EXP2_UART1	* 7	33	SEL_SPI1_EXP2_B	* 8
36	EXP_RESETh		35	SEL_EXP2_TIMER	* 9
38	VCC_5V		37	VCC_5V	
40	VCC_5V		39	VCC_5V	
42	Ground		41	Ground	
44	Ground		43	Ground	

* 4 Control line for Mux_Ctl 4 signals

* 5 Control line for Mux_Ctl 5 signals

* 6 Control line for Mux_Ctl 6 signals

* 7 Control line for Mux_Ctl 7 signals

* 8 Control line for Mux_Ctl 8 signals

* 9 Control line for Mux_Ctl 9 signals

3.2.16.3 P13, Expansion 3 Connector

Table 18: P13, Expansion 3 Connector

Pin	Signal	Mux_Ctl	Pin	Signal	Mux_Ctl
2	VCC_5V		1	VCC_5V	
4	VCC_5V		3	VCC_5V	
6	EXP3_SEL_MEMD0_7	* 10	5	NC	
8	EXP3_SEL_MEM	* 11	7	EXP3_SEL_MEM_CTL	* 12
10	Ground		9	Ground	
12	EXP_EMIFA_D0	10	11	EXP_EMIFA_D1	10
14	EXP_EMIFA_D2	10	13	EXP_EMIFA_D3	10
16	EXP_EMIFA_D4	10	15	EXP_EMIFA_D5	10
18	EXP_EMIFA_D6	10	17	EXP_EMIFA_D7	10
20	Ground		19	Ground	
22	EXP_EMIFA_D8	13	21	EXP_EMIFA_D9	13
24	EXP_EMIFA_D10	13	23	EXP_EMIFA_D11	13
26	EXP_EMIFA_D12	14	25	EXP_EMIFA_D13	14
28	EXP_EMIFA_D14	14	27	EXP_EMIFA_D15	14
30	Ground		29	Ground	
32	EXP3_SEL_MEMD8_D11	* 13	31	EXP_EMIFA_WEn_DQM0	11
34	EXP3_SEL_MEMD12_D16	* 14	33	EXP_EMIFA_WEn_DQM1	11
36	Ground		35	Ground	
38	EXP3_EMIFA_CLK		37	EMIFA_SDCKE	
40	Ground		39	Ground	
42	Ground		41	Ground	
44	EXP3_EMIFA_OEn	11	43	EMIFA_CS4n	10
46	EXP3_EMIFA_WEn	11	45	EMIFA_CS5n	10
48	Ground		47	NC	
50	EMIFA_WAIT0		49	EMIFA_CS2n	
52	EMIFA_CS0n		51	EXP3_EMIFA_CS3n	12
54	NC		53	NC	
56	EMIFA_BA0		55	EMIFA_BA1	
58	EMIFA_A0		57	EXP_EMIFA_A1	10
60	EXP_EMIFA_A2	10	59	EMIFA_A4	
62	EMIFA_A3		61	EMIFA_A6	
64	EMIFA_A5		63	EMIFA_A8	
66	EMIFA_A7		65	EMIFA_A10	
68	EMIFA_A9		67	EMIFA_A12	
70	EMIFA_A11		69	NC	
72	Ground		71	Ground	
74	EXP_RESETn		73	NC	
76	NC		75	NC	
78	VCC_5V		77	VCC_5V	
80	VCC_5V		79	VCC_5V	
82	Ground		81	Ground	
84	Ground		83	Ground	
86	Ground		85	Ground	
88	Ground		87	Ground	
90	NC		89	NC	

* 10 Control line for Mux_Ctl 10 signals

* 11 Control line for Mux_Ctl 11 signals

* 12 Control line for Mux_Ctl 12 signals

* 13 Control line for Mux_Ctl 13 signals

* 14 Control line for Mux_Ctl 14 signals

3.2.17 P14, Phono Jack In

Connector P14 is a phono jack input. This connector is not populated as shipped.

3.2.18 P15, Phono Jack In

Connector P15 is a phono jack input. This connector is not populated as shipped.

3.2.21 J201, Embedded JTAG Emulation Interface

Connector J201 is a USB interface providing JTAG access to the processor. This allows the user to develop and debug using Code Composer Studio on a PC.

3.3 LEDs

The EVM has ten (10) LEDs which are located on the top side of the board. Information regarding the LEDs are shown in the table below.

Table 19: LEDs

LED #	Use	Color
DS1	User control, EMIFA D12	Green
DS2	User control, EMIFA D13	Green
DS3	User control, EMIFA D14	Green
DS4	User control, EMIFA D15	Green
DS5	USB-EMU ON/OFF	Green
DS6	VCC_1V2	Green
DS7	VCC_5V	Green
DS8	VCC_1V8	Green
DS9	VCC_3V3	Green
DS501	On board EMU status	Green

3.4 Switches

The EVM has six (6) switches. The function of these switches are shown in the table below.

Table 20: Switches

Switch	Function	Type
SW1	EMU0/EMU1 Control	4 Position DIP
SW2	Boot Mode Select	6 Position DIP
SW3	User Readable	4 Position DIP
SW4	RESET Switch	Push Button/Momentary
SW5	Pull Up Select	6 Position DIP
SW6	On/Off Power Switch	Toggle

3.4.1 SW1, EMU0/1 Select Switch

SW1 is a 2 position DIP switch providing 4 options in selecting the state of the EMU0 and EMU1 pins on the OMAP-L137 processor. This switch is not needed for the OMAP-L137 processor.

The default is to select pull ups on the EMU0 and EMU1.

3.4.2 SW2, Boot Mode Select Switch

Switch SW2 is a 6 position DIP switch. Only 5 of the positions are used. Note that only 5 combinations provide valid options. The boot mode options are described in the table below.

Table 21: SW2, Boot Mode Select DIP Switch

Position	Pins	Signal
1	1-12	BOOTMODE[7]
2	2-11	BOOTMODE[2]
3	3-10	BOOTMODE[1]
4	4-9	BOOTMODE[0]
5	5-8	BOOTMODE[3]
6	6-7	NC

The figure below shows the SW2 switch.

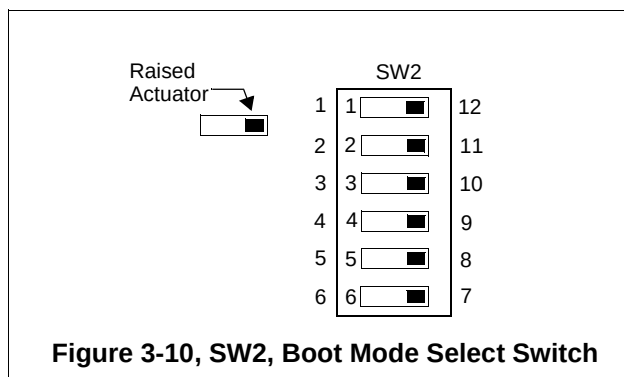


Figure 3-10, SW2, Boot Mode Select Switch

The table below shows the position settings which select the various boot modes.

Table 22: SW2, Boot Mode Select

Pos 1 Boot[7]	Pos 2 Boot[2]	Pos 3 Boot[1]	Pos 4 Boot[0]	Pos 5 Boot[3]	Boot Pin BTMODE[7,2,1,0,3]	Boot Mode
OFF	OFF	OFF	ON	NA	0 0 0 1 x	NOR
OFF	OFF	ON	OFF	NA	0 0 1 0 x	HPI
OFF	ON	OFF	ON	NA	0 1 0 1 x	SPI0 Flash
OFF	ON	ON	OFF	NA	0 1 1 0 x	SPI1 Flash
OFF	ON	ON	ON	NA	0 1 1 1 x	NAND 8-bit
OFF	OFF	OFF	OFF	OFF	0 0 0 0 0	I ² C0 Master
OFF	OFF	OFF	OFF	ON	0 0 0 0 1	I ² C0 Slave
OFF	OFF	ON	ON	OFF	0 0 1 1 0	I ² C1 Master
OFF	OFF	ON	ON	ON	0 0 1 1 1	I ² C1 Slave
OFF	ON	OFF	OFF	OFF	0 1 0 0 0	SPI0 EEPROM *
OFF	ON	OFF	OFF	ON	0 1 0 0 1	SPI1 EEPROM
ON	OFF	OFF	ON	OFF	1 0 0 1 0	SPI0 Slave
ON	OFF	OFF	ON	ON	1 0 0 1 1	SPI1 Slave
ON	OFF	ON	ON	OFF	1 0 1 1 0	UART0
ON	OFF	ON	ON	ON	1 0 1 1 1	UART1
ON	OFF	ON	OFF	OFF	1 0 1 0 0	UART2 *
ON	ON	ON	ON	OFF	1 1 1 1 0	Emulation Debug *

* Supported in standalone EVM

3.4.3 SW3, User Readable 4 Position DIP Switch

Switch SW6 is a 4 position DIP switch mapped to EMIFA data bus lines D8-D11 via a multiplexer. The table below shows what signal each position appears on.

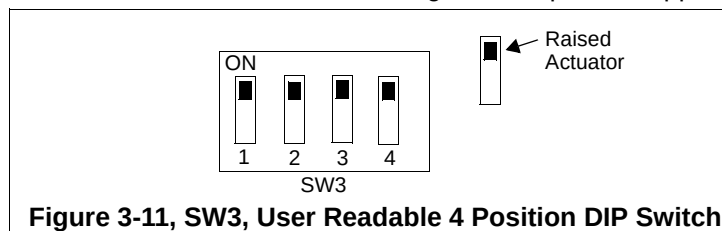


Table 23: SW3, User Readable 4 Position DIP Switch

Position	Signal
1	SW_DIP0, EMIFA - D8
2	SW_DIP1, EMIFA - D9
3	SW_DIP2, EMIFA - D10
4	SW_DIP3, EMIFA - D11

3.4.4 SW4, RESET Switch

Switch SW4 is a push button reset switch that will RESET the board.

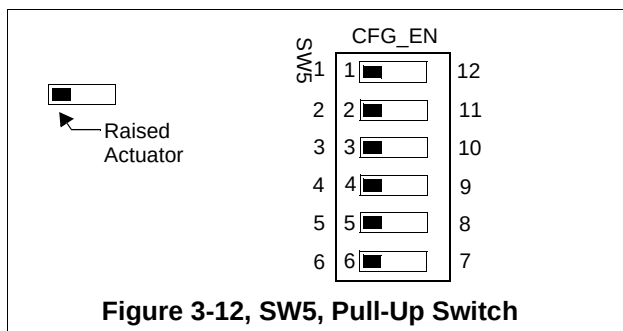
3.4.5 SW5, Mux Control Switch

Switch SW5 is a 6 position DIP switch that allows mux control signals to be pulled up to +3.3 volts. This switch allows enabling on mux control signals. The six signals that can be pulled up are shown in the table below. Alternatively the multiplexer control lines can be enabled via daughter card connectors. Additional control lines are mapped to the daughter card connectors. Refer to the expansion connector sections 3.2.16.1 to 3.2.16.2 for more information.

Table 24: SW5, Pull-Up Switch

Position	Signal	Mux_Ctl
SW5-1	SEL_ENETn_MCASP0	* 1
SW5-2	SEL_EXP2_TIMER	* 9
SW5-3	SEL_EXP2_UART1	* 7
SW5-4	ON_BD_OFF_BD	U19 control for USB
SW5-5	EXP3_SEL_MEMD8-D11	* 13
SW5-6	EXP3_SEL_MEMD12-D15	* 14

The figure below shows the SW5 switch.



3.4.6 SW6, On/Off Switch

Switch SW6 is an on/off toggle switch that allows +5 volts from the J6 connector to be applied to the board.

3.5 Test Points

The EVM has 49 test points. All test points appear on the top of the board. The following figure identifies the position of each test point. The next table lists each test point and the signal appearing on that test point.

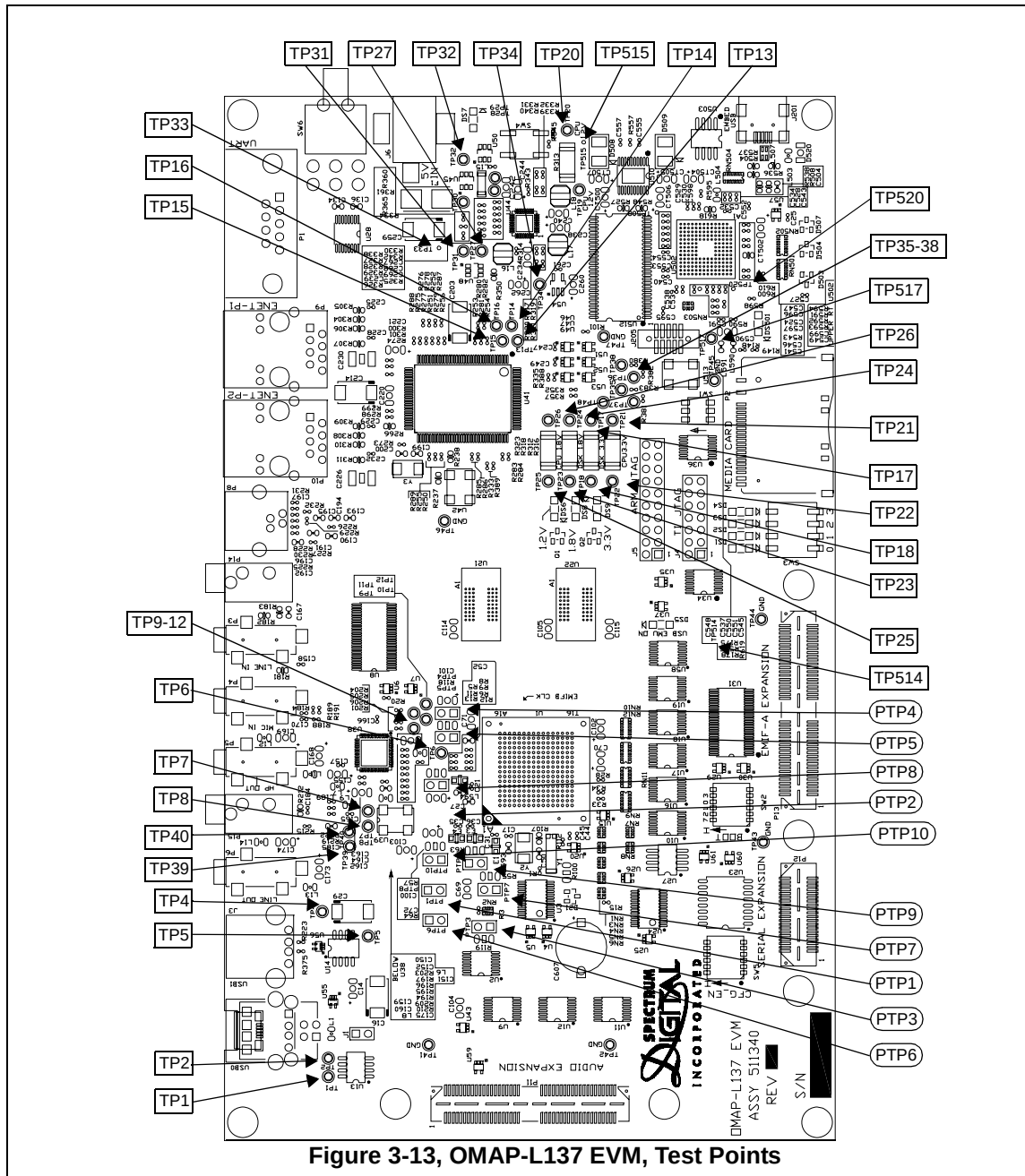


Table 25: OMAP-L137 EVM Test Points

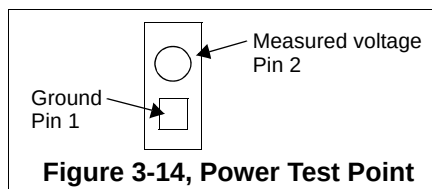
Test Point #	Signal	Test Point #	Signal
TP1	U13, Pin 6,7,8, VBUS From J2	TP16	U41, Pin 6, P2LED0
TP2	DSK_3V3, U13, Pin 5, OCn	TP27	U44, Pin 28, INTn
TP4	U14, Pin 6,7,8, VBUS from J3	TP28	U44, Pin 20, VLDO1
TP5	DSK_3V3, U14, Pin 5, OCn	TP29	U44, Pin 18, VLDO2
TP6	U1, F7, RSV1	TP33	VCC_5V
TP7	U38, Pin 35, GPIO1	TP34	U54, Pin 5, ALT_CPU_1V2
TP8	U38, Pin 35, GPIO2	TP35	USB1, TAIN0
TP9	U38, Pin 45, MFP0	TP36	USB1, TAIN1
TP10	U38, Pin 46, MFP1	TP37	USB1, TAIN2
TP11	U38, Pin 47, MFP2	TP38	USB1, TAIN3
TP12	U38, Pin 48, MFP3	TP39	U38, Pin 27, MONO_LO+
TP13	U41, Pin 2, P1LED1	TP40	U38, Pin 28, MONO_LO-
TP14	U41, Pin 3, P1LED0	TP515	Factory Use
TP15	U41, Pin 5, P2LED1	TP517	Factory Use
		TP520	Factory Use

There are 10 power test point pairs for major power domains on the EVM. These test points provide a convenient mechanism to check the EVM's multiple power supplies. The table below shows the voltages for each test point and what the supply is used for.

Table 26: Power Test Points

Access Test Points	Voltage	Shunt	Comments
TP17, TP18	DSK_3V3	0.025 ohms	All EVM 3.3V supplies except CPU
TP19, TP20	CPU_1V2	0.025 ohms	All CPU 1.2V supplies
TP21, TP22	CPU_3V3	0.025 ohms	All CPU 3.3V supplies
TP23, TP24	DSK_1V8	0.025 ohms	All EVM 1.8V supplies except CPU
TP25, TP26	CPU_1V8	0.025 ohms	All CPU 1.8V supplies

Furthermore the EVM has ten 2 pin power test points for specific power domains on the L137 device. These voltages are measured across a resistor which is why there are two points to each test position. The square pad is the ground. The round pad is the measured voltage. The figure below shows what a typical power test point looks like.



The table below shows the power test points and the voltage measured.

Table 27: Power Test Points

Power Test Point	Voltage Measured
PTP1	CPU_3V3
PTP2	CPU_1V2
PTP3	CPU_1V2
PTP4	CPU_1V2
PTP5	CPU_1V2
PTP6	CPU_1V2
PTP7	CPU_3V3
PTP8	CPU_1V8
PTP9	CPU_3V3
PTP10	CPU_1V8

Appendix A

Schematics

This appendix contains the schematics for the OMAP-L137 EVM.

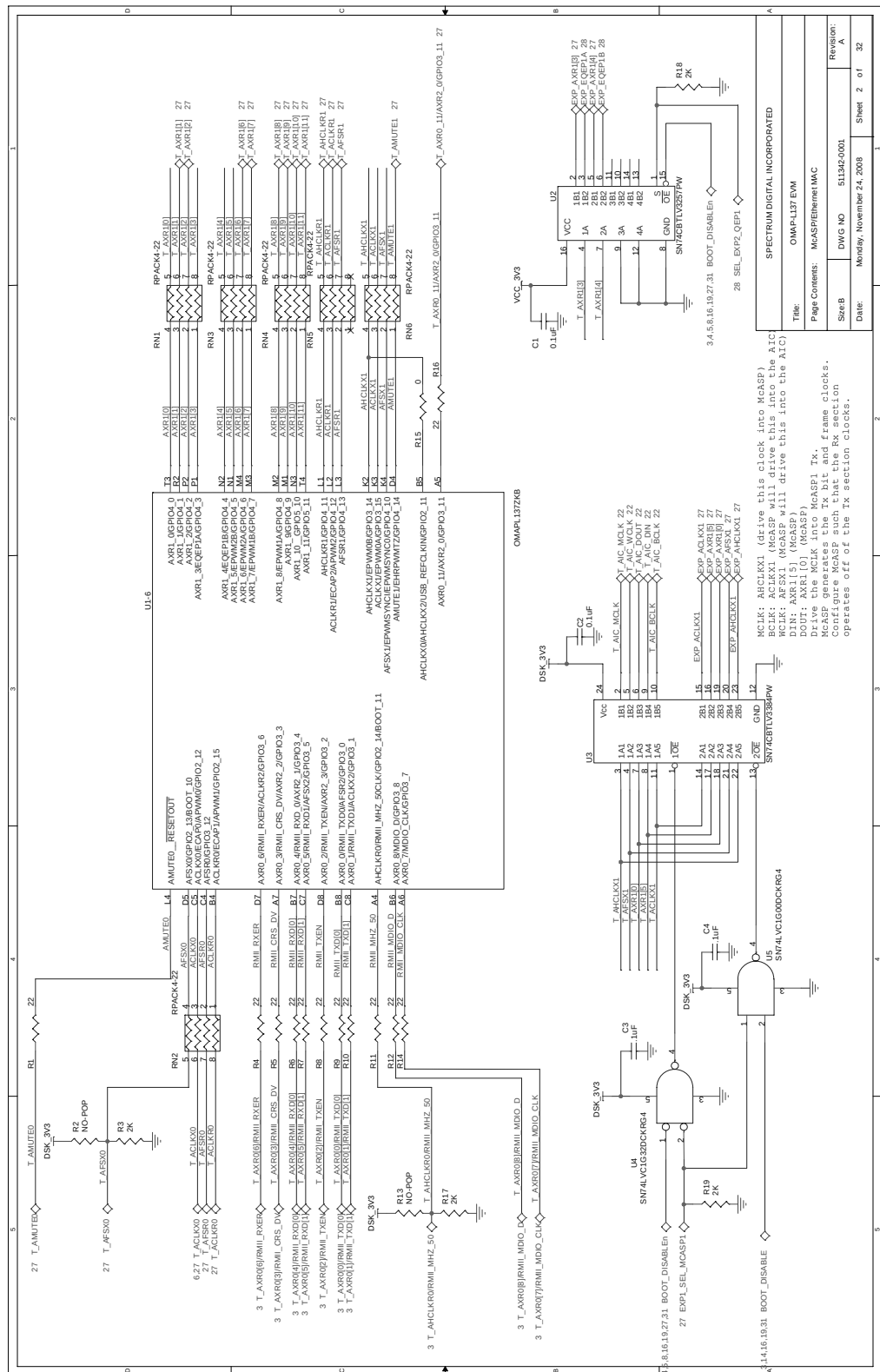
SCHEMATIC CONTENTS

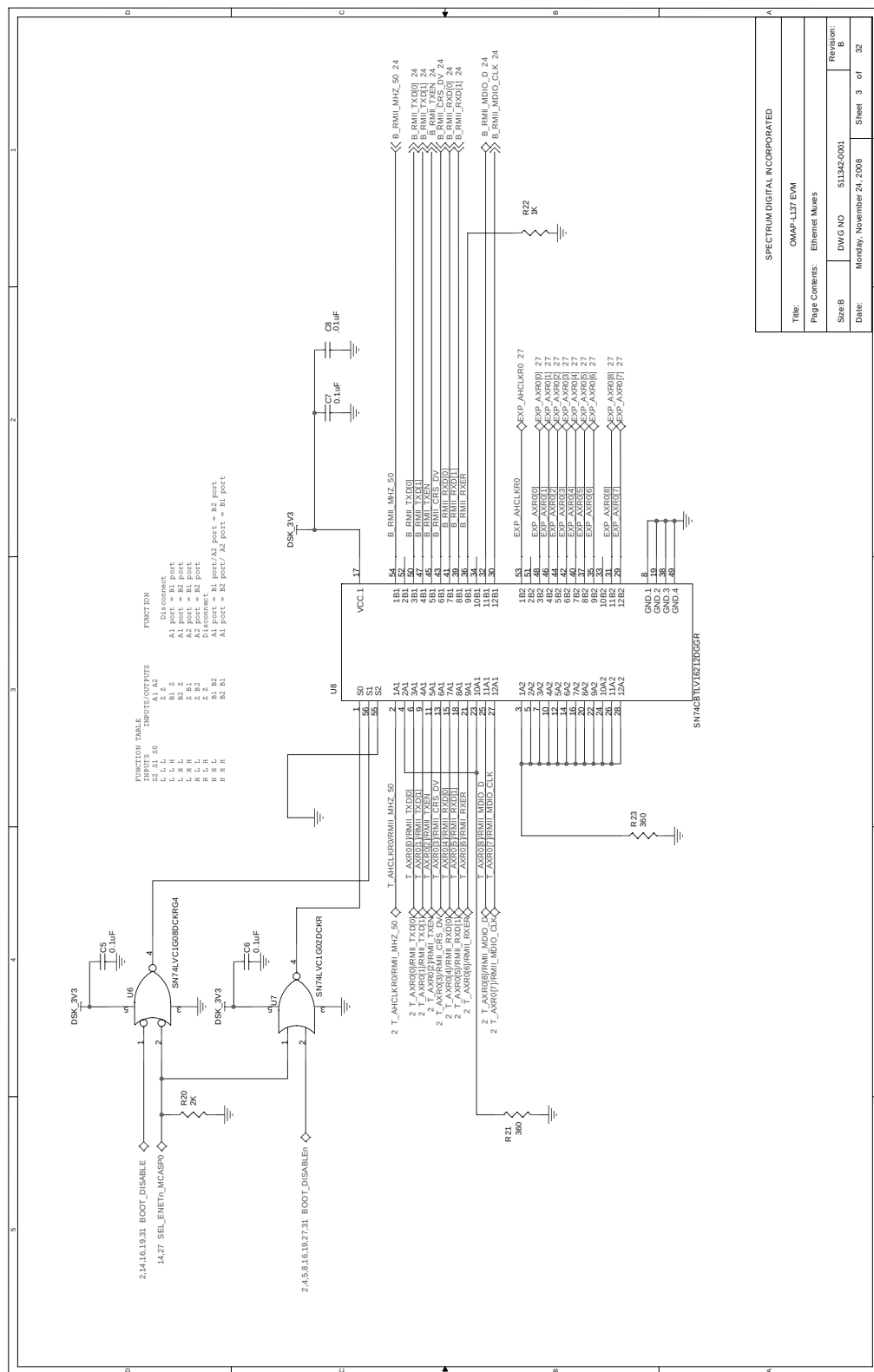
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SHEET03	ETHERNET/MCASP MUX
SHEET04	L137 SERIAL I/O
SHEET05	SPI MUXING
SHEET06	L137 USB 2.0 PORT
SHEET07	L137 USB 1.0 PORT
SHEET08	L137 EMIF A
SHEET09	L137 EMIF B
SHEET10	L137 JTAG/CLOCKS
SHEET11	L137 POWER PINS
SHEET12	L137 GROUND PINS
SHEET13	L137 DECOUPLING CAPACITORS
SHEET14	BOOT MODE SWITCHES
SHEET15	EMIFB DSDRAM
SHEET16	SPI ROM
SHEET17	USER SWITCHES/LEDS
SHEET18	RS32 INTERFACE
SHEET19	SD/MMC MUXING
SHEET20	SD/MMC/MMC PLUS CARD INTERFACE
SHEET21	JTAG/CONNECTOR INTERFACE
SHEET22	AIC3106 AUDIO CODEC
SHEET23	AIC PHONE/AUDIO JACK
SHEET24	ETHERNET PHY/SWITCH
SHEET25	ETHERNET POWER
SHEET26	ETHER NET PORTS
SHEET27	EXPANSION CONNECTOR 1
SHEET28	EXPANSION CONNECTOR 2
SHEET29	EXPANSION CONNECTOR 3
SHEET30	POWER
SHEET31	POWER I1
SHEET32	POWER IN

DIVISION STATUS OF SHARES					
	REV'	B	B		
SR	31	32			
REV	A	B	A	A	A
B	B	B	B	A	A
SR	21	22	23	24	25
REV	A	D	A	A	A
B	A	D	A	A	A
SR	11	12	13	14	15
REV	A	B	C	D	E
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SR	1	2	3	4	5
REV	A	B	C	D	E
B	B	B	B	B	B

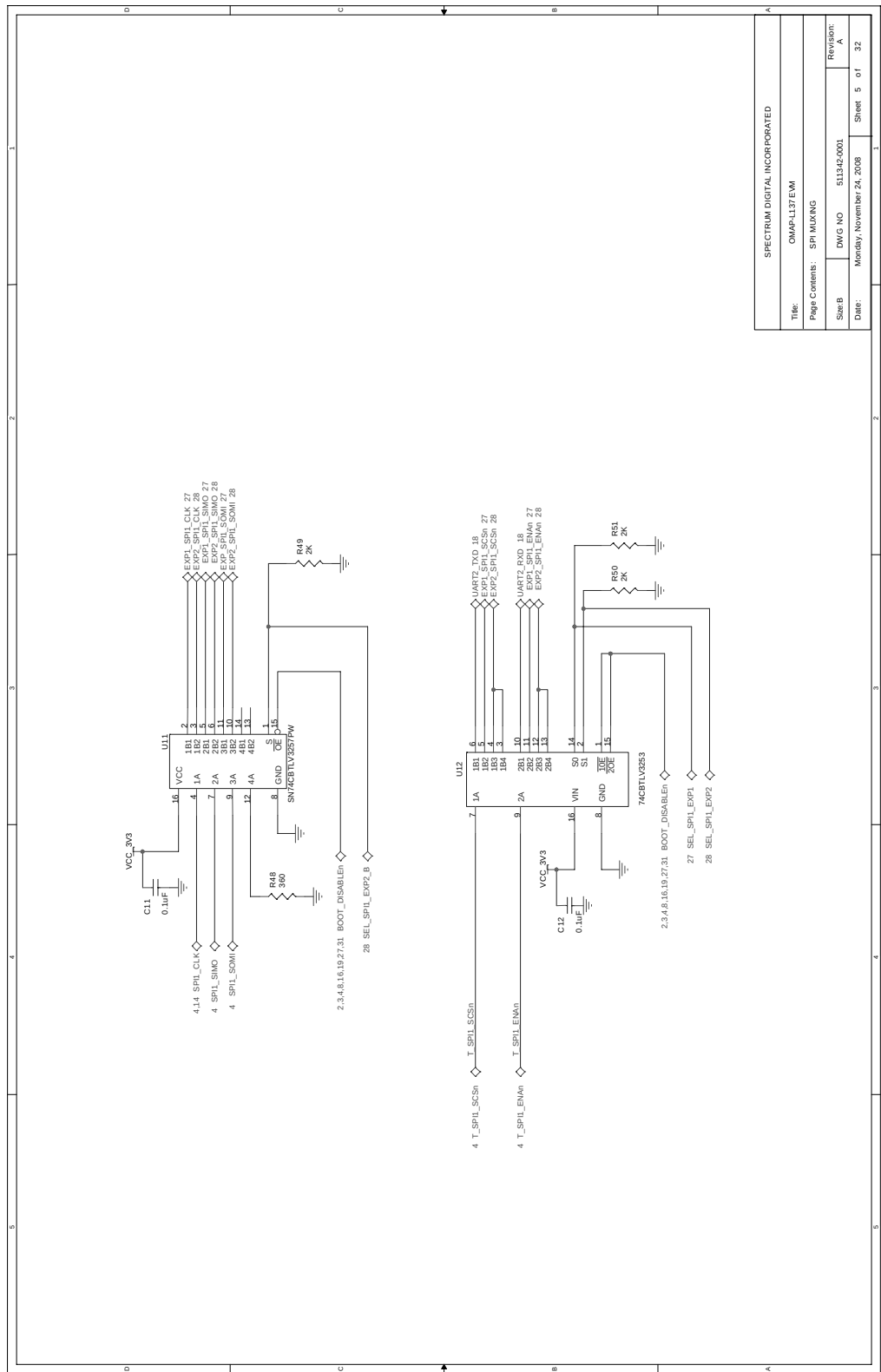
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TRK		DATE
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SEGR	R.R.P.	DATE
SEGR-SEGR		DATE
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SPG	C.M.D.	DATE
SESE	R.R.P.	DATE
	R.R.P.	DATE

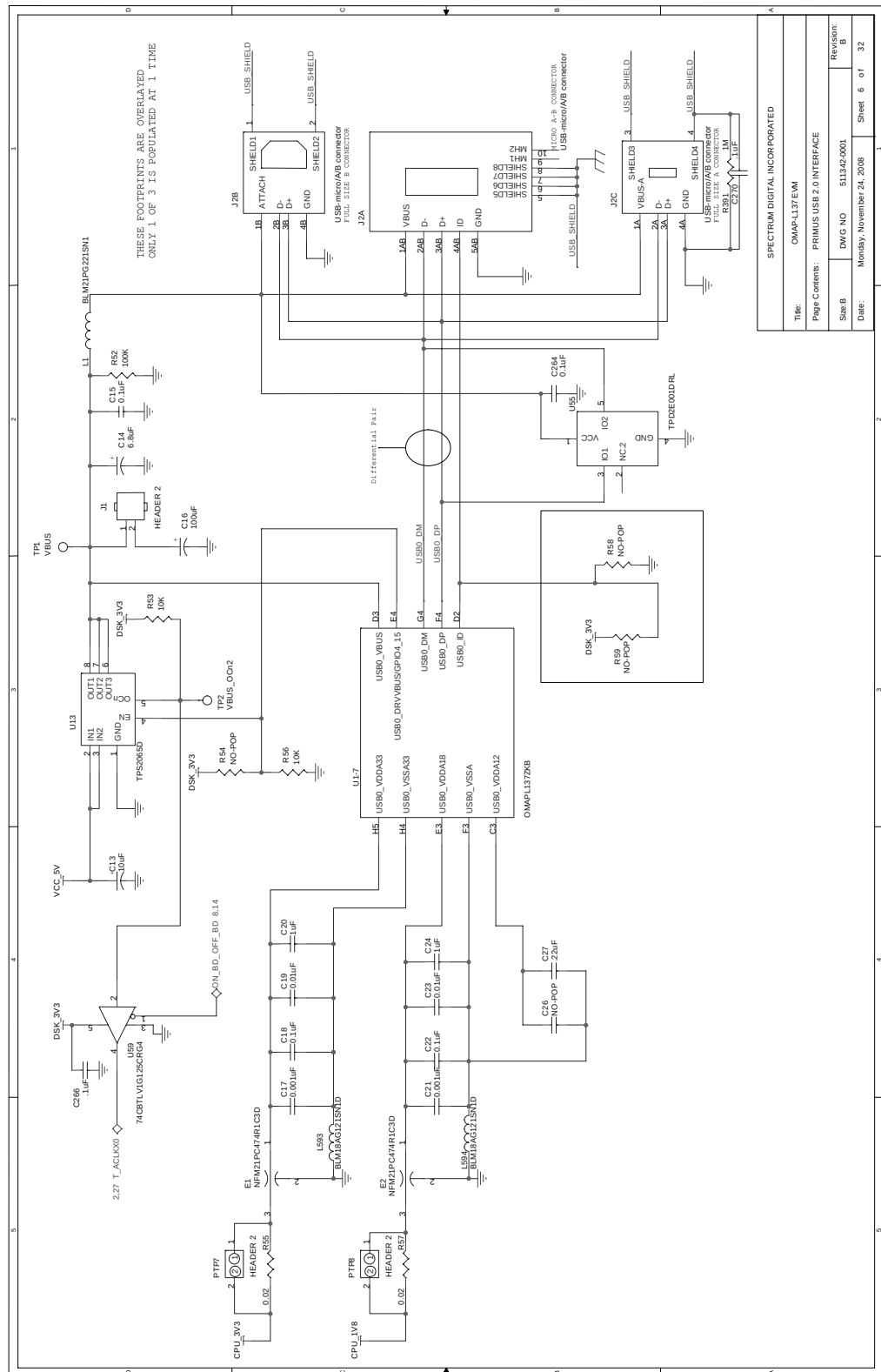
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Date:	Monday, November 24, 2008		Sheet 1 of 32

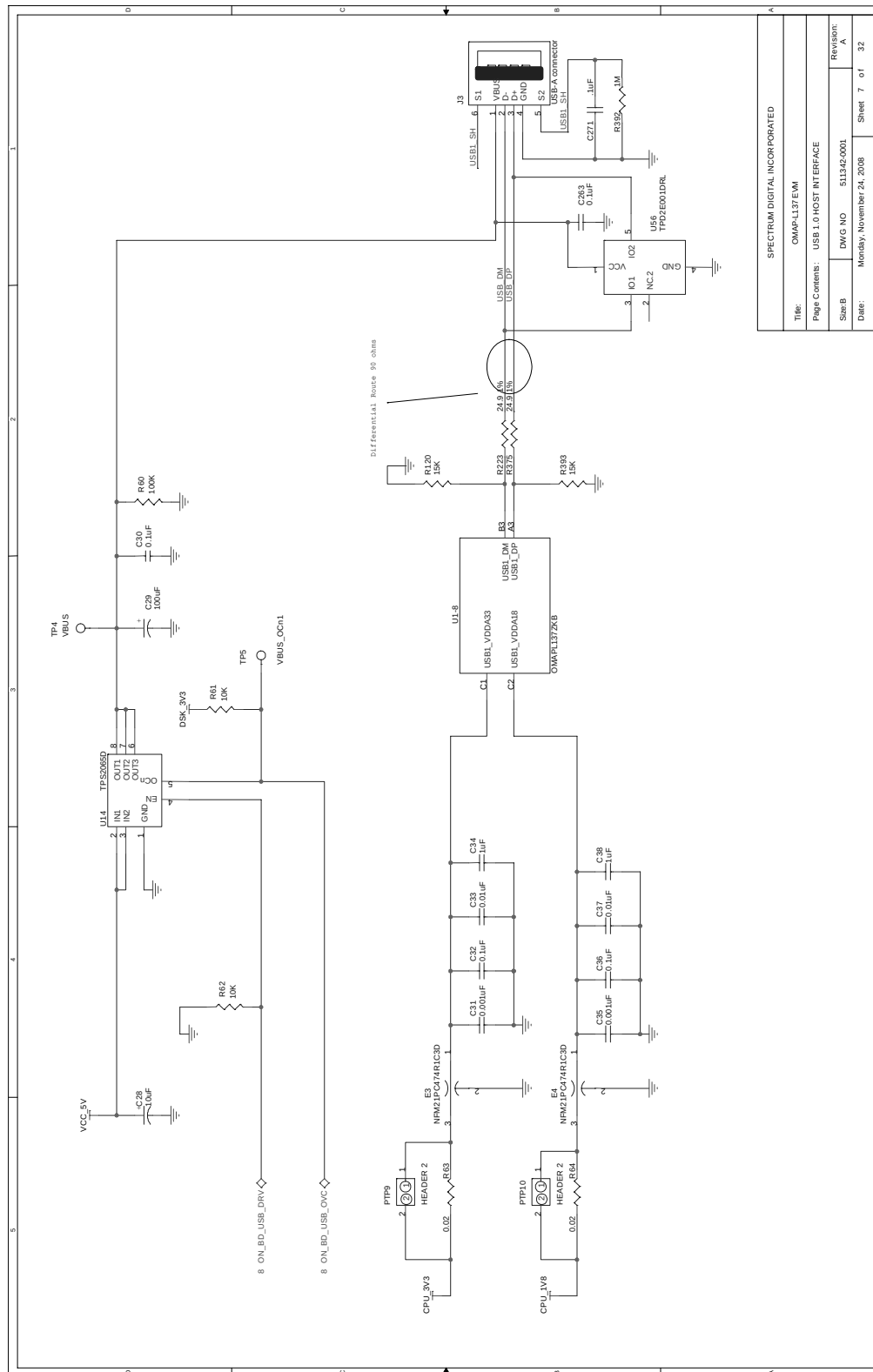




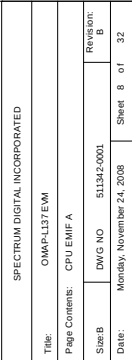


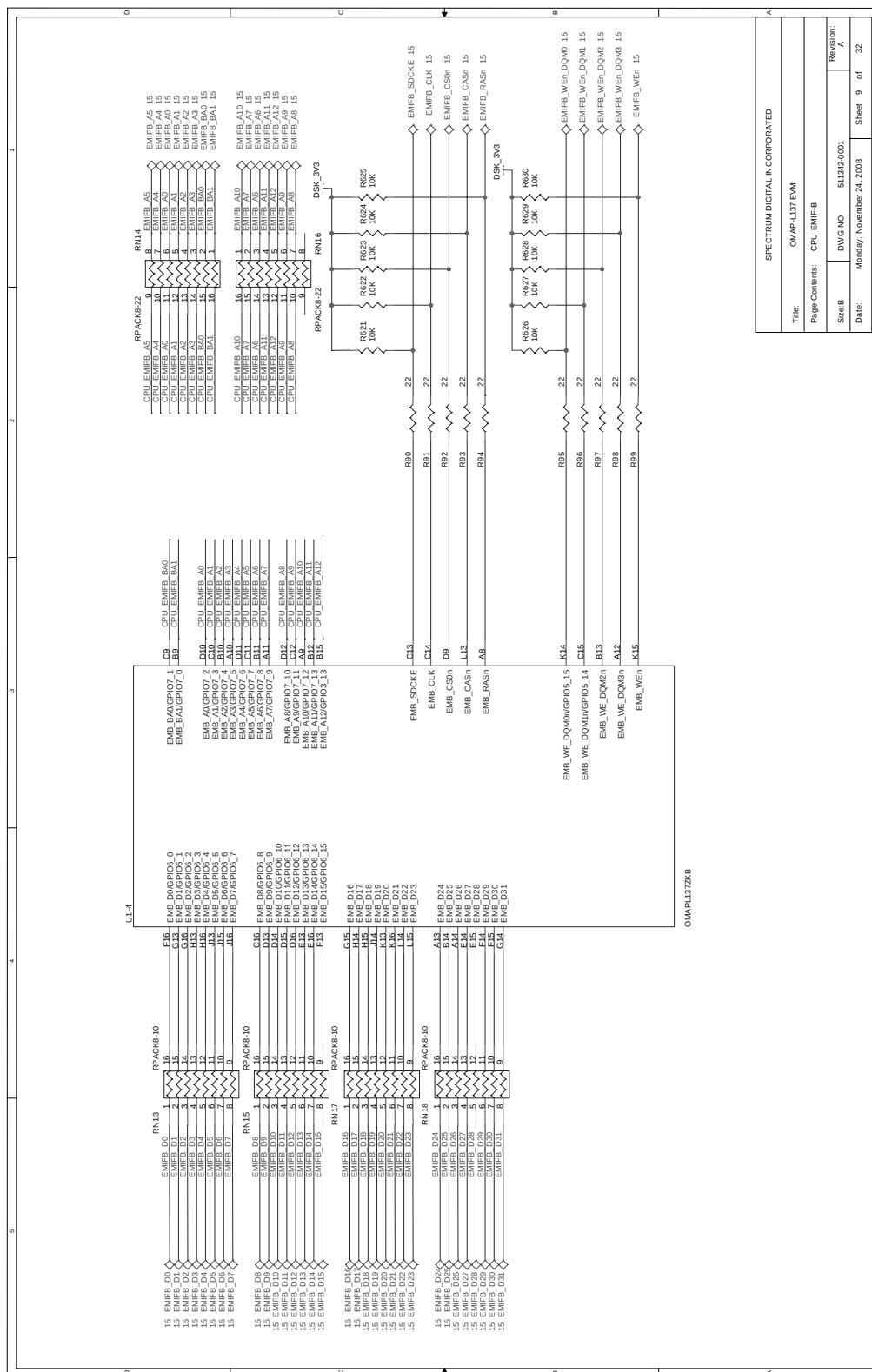


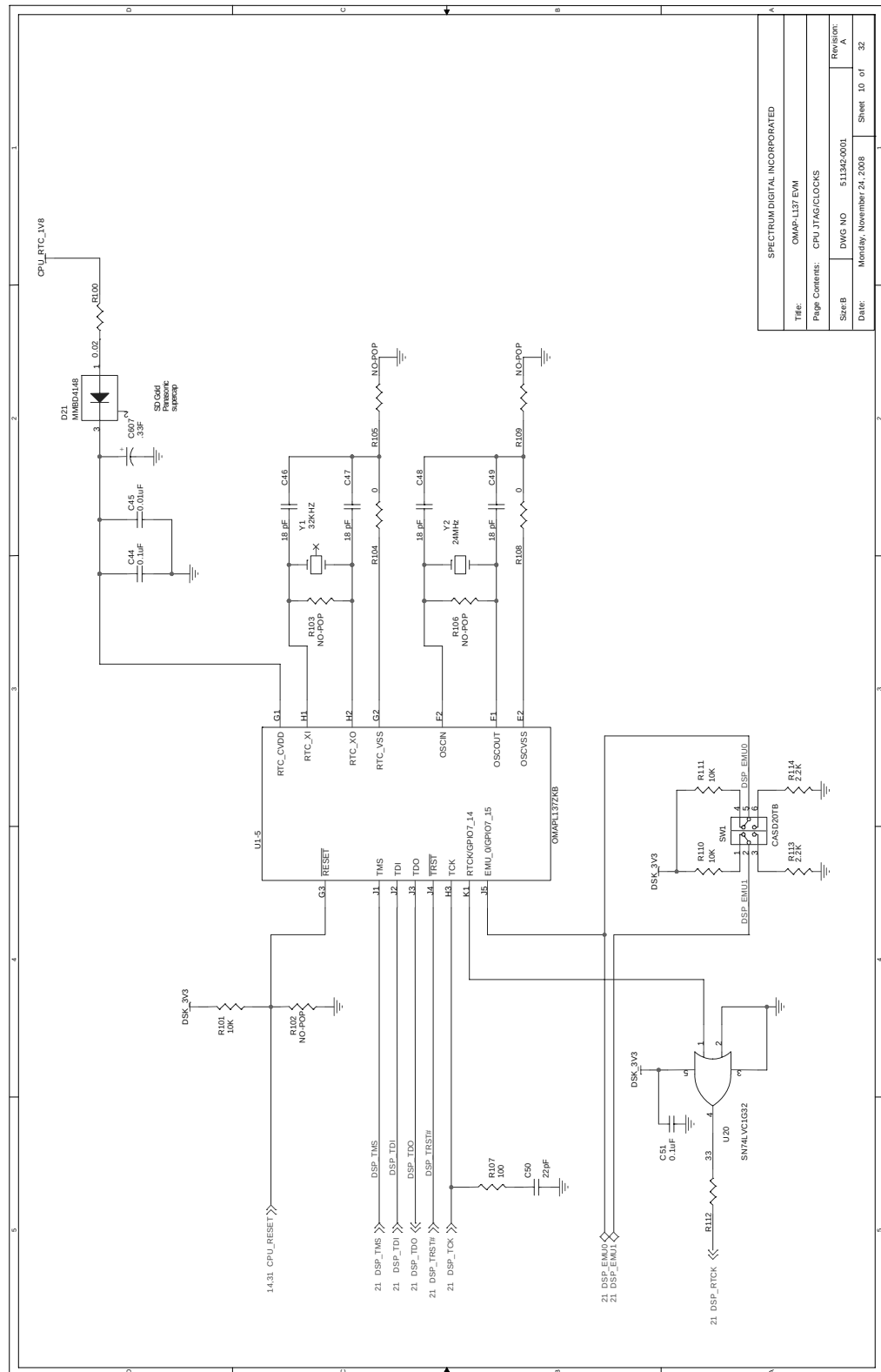


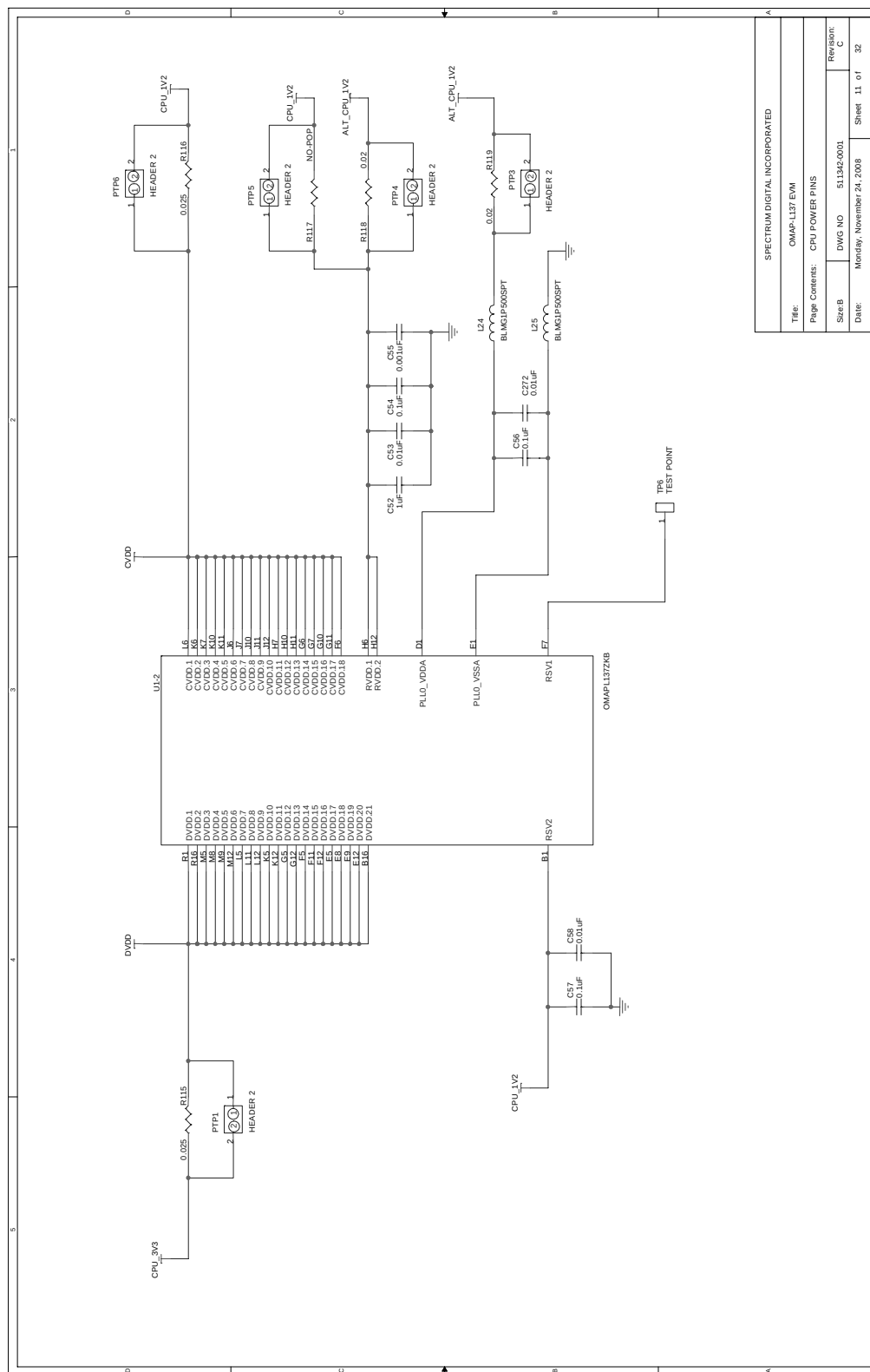


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Sheet:	DWG NO	511342-0001	Revision:
Date:	Monday, November 24, 2008	Sheet	7 of 32

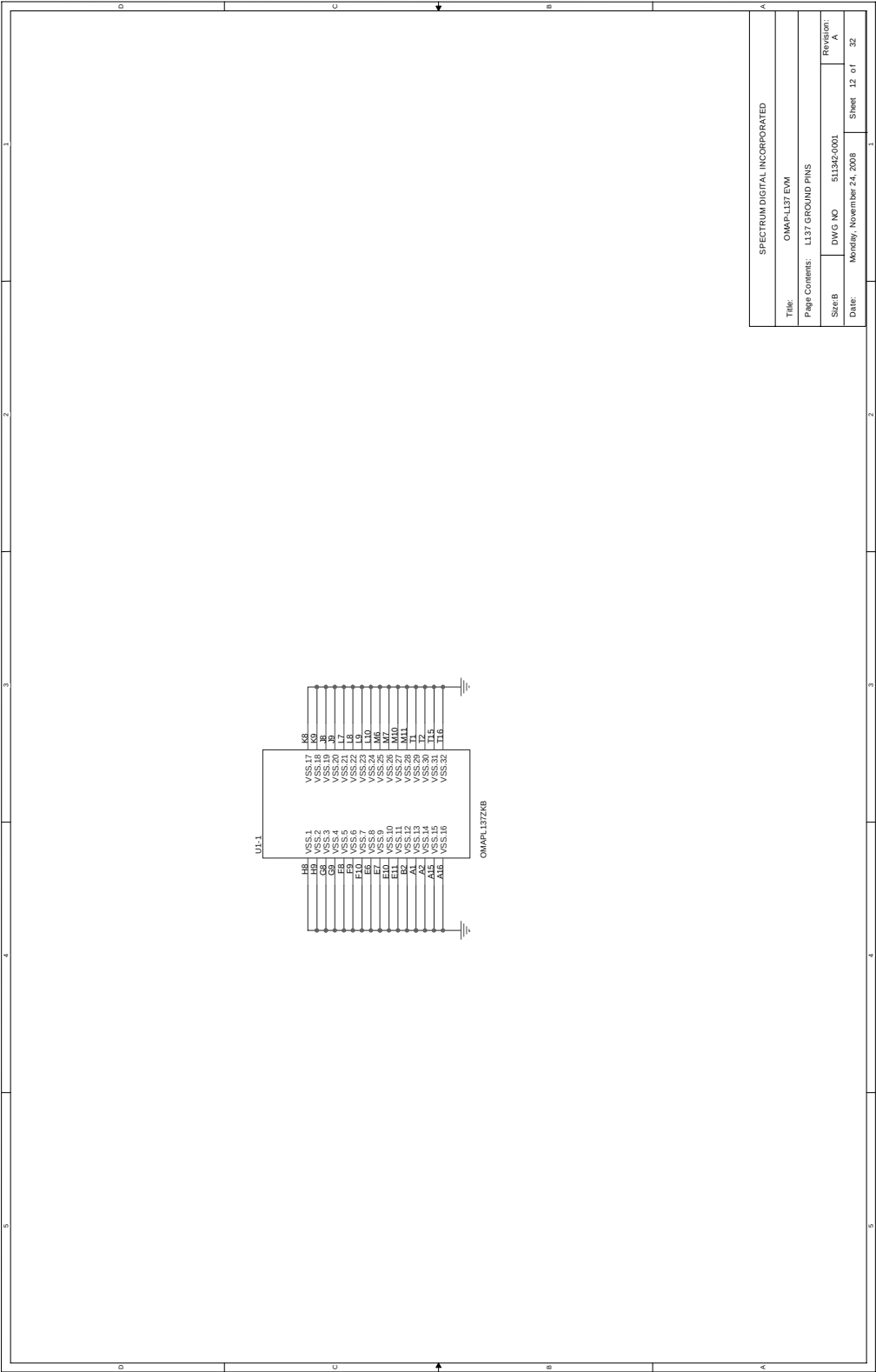




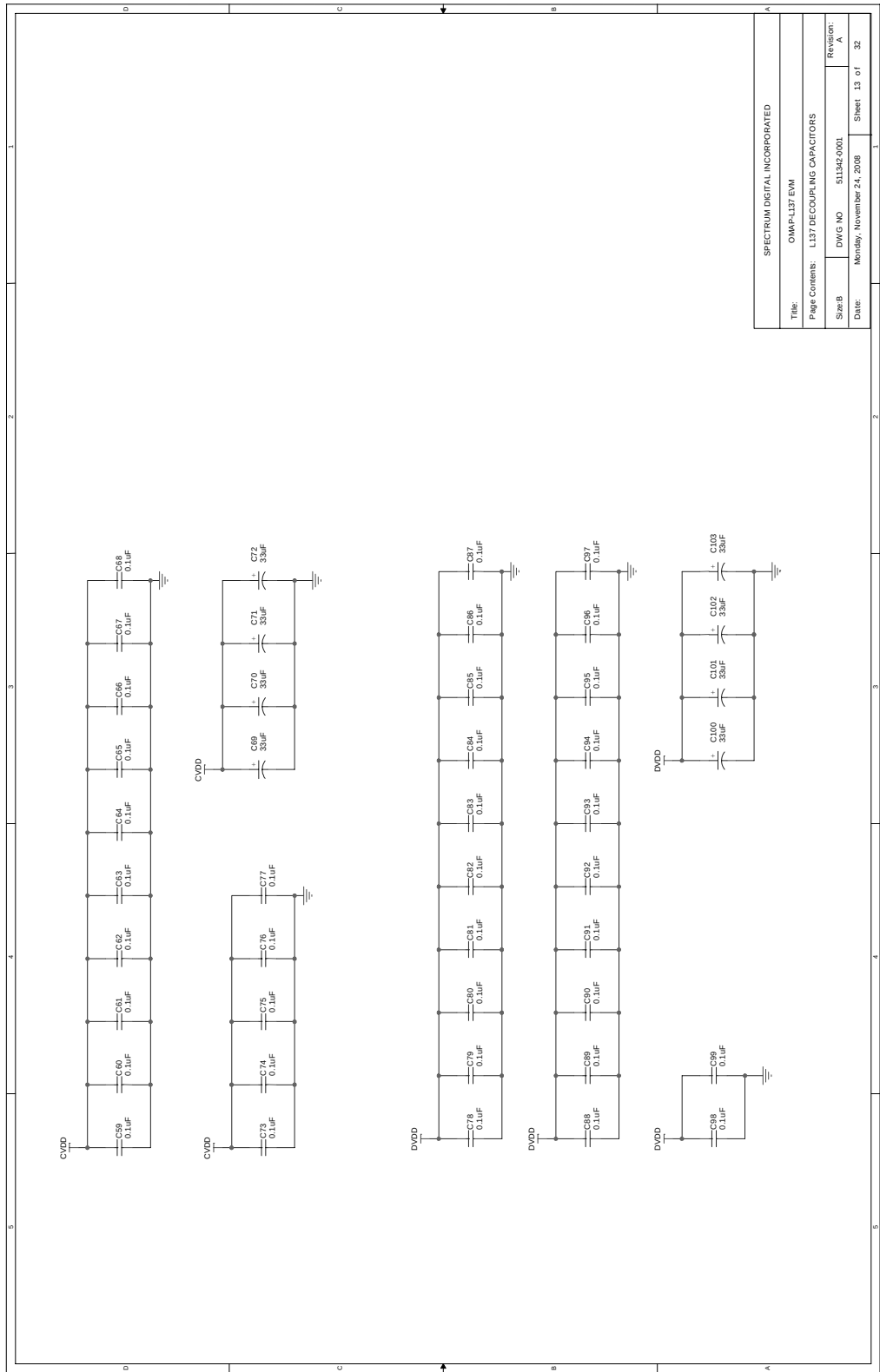




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Page Comments:	CPU POWER PINS		
Size:	B	DWG NO	511342-0001
Revision:	C		
Date:	Monday, November 24, 2008		
Sheet	11	of	32

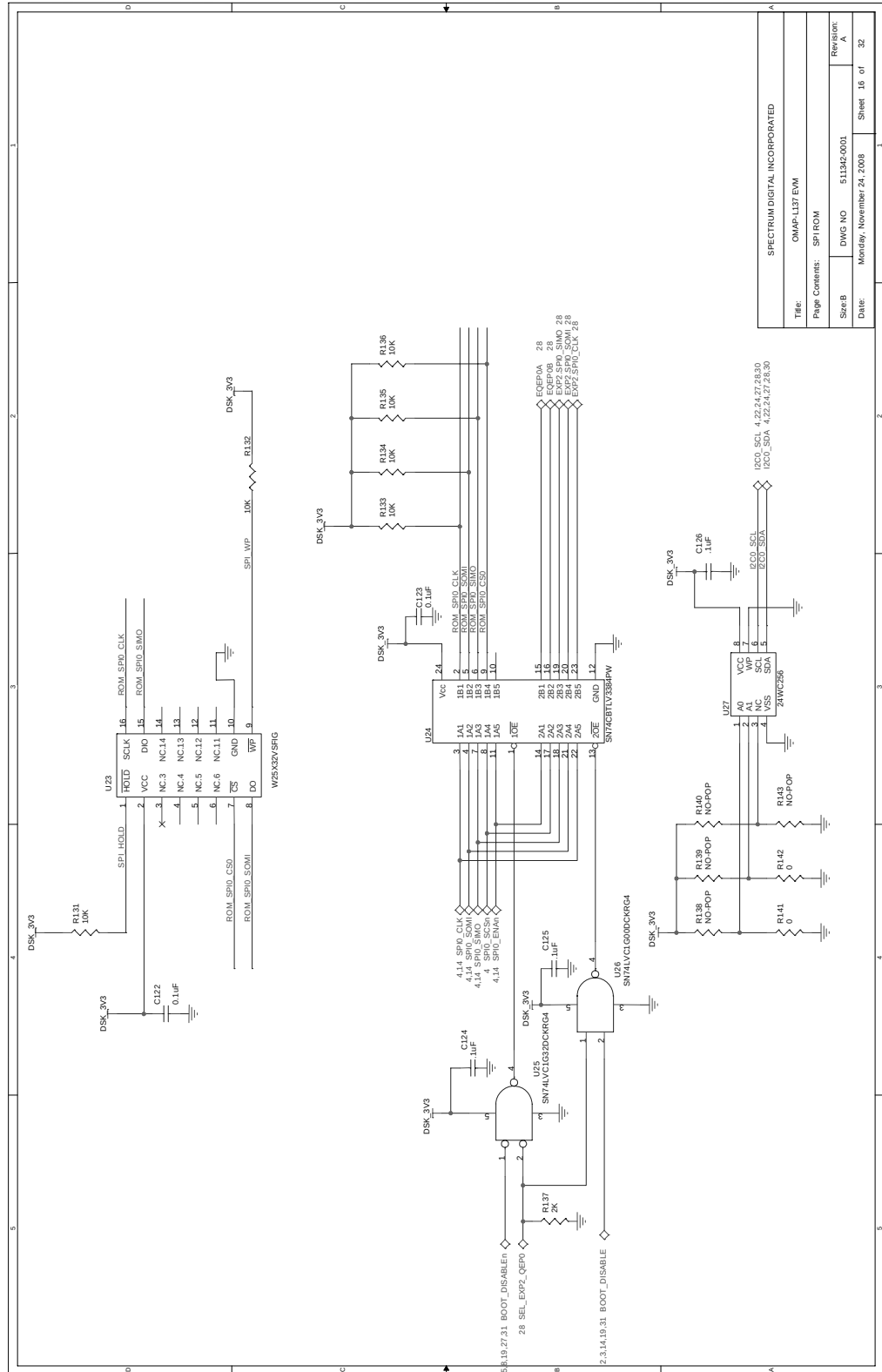


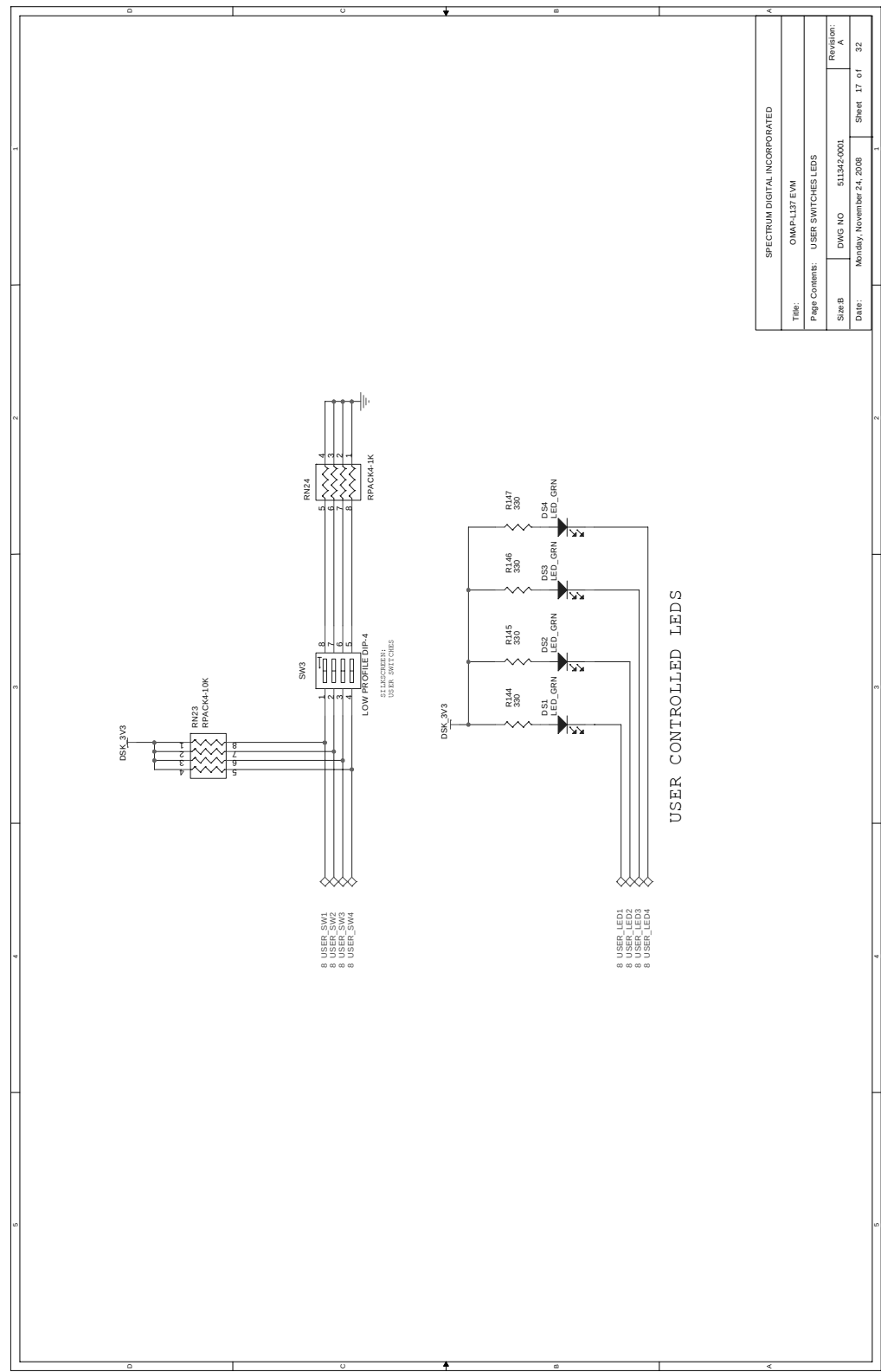
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Date:	Monday, November 24, 2008	Sheet	12 of 32



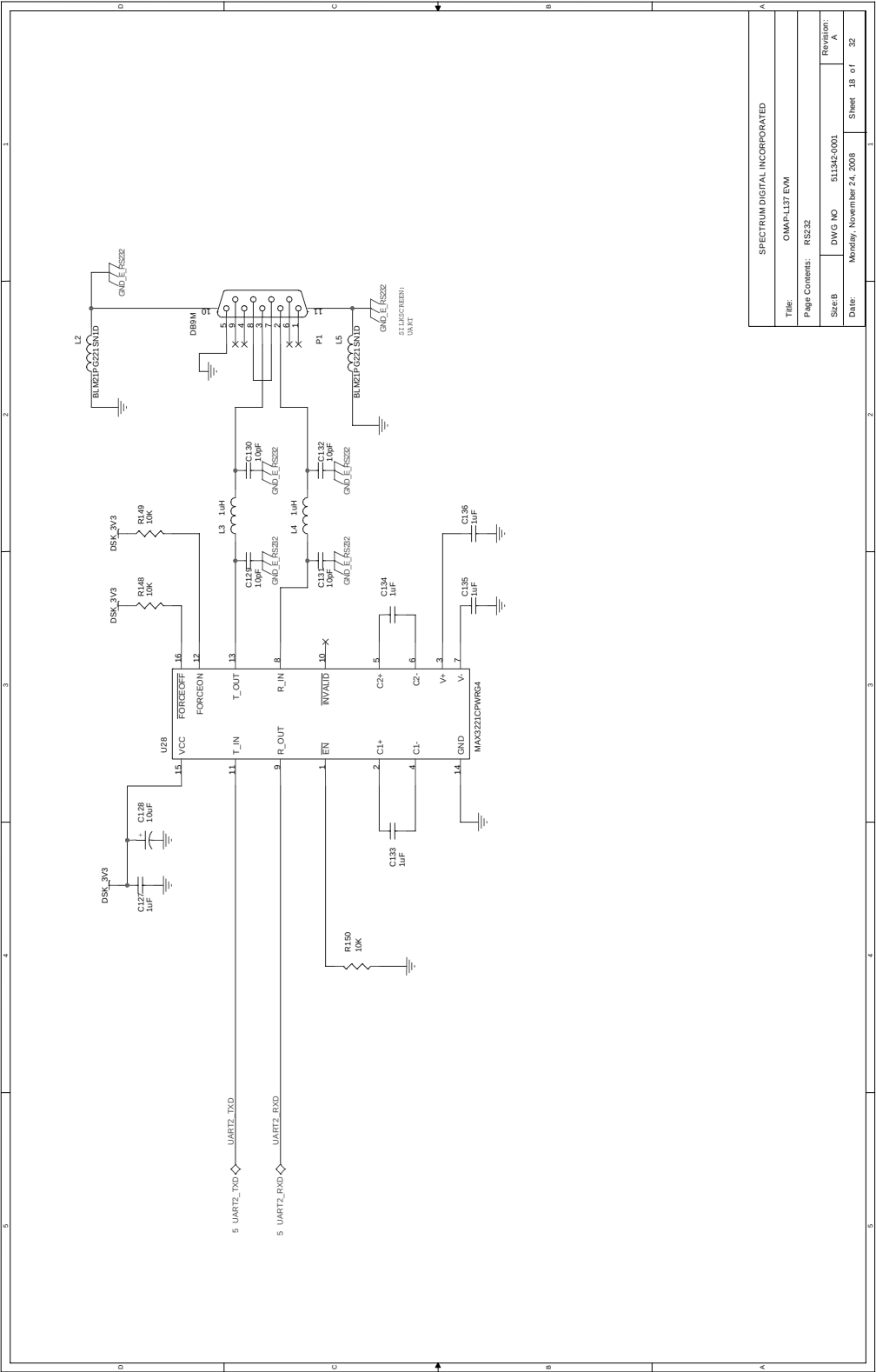


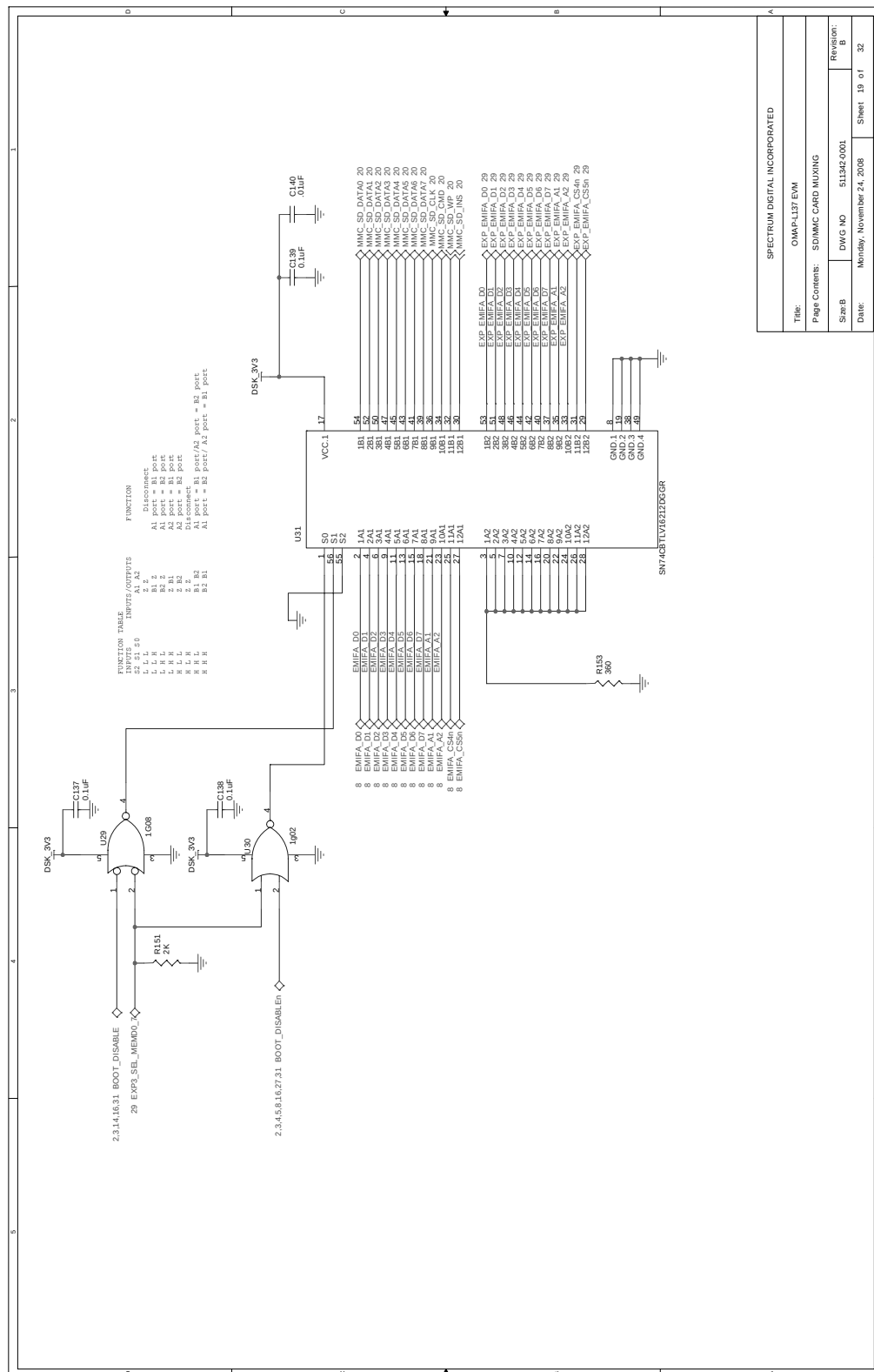


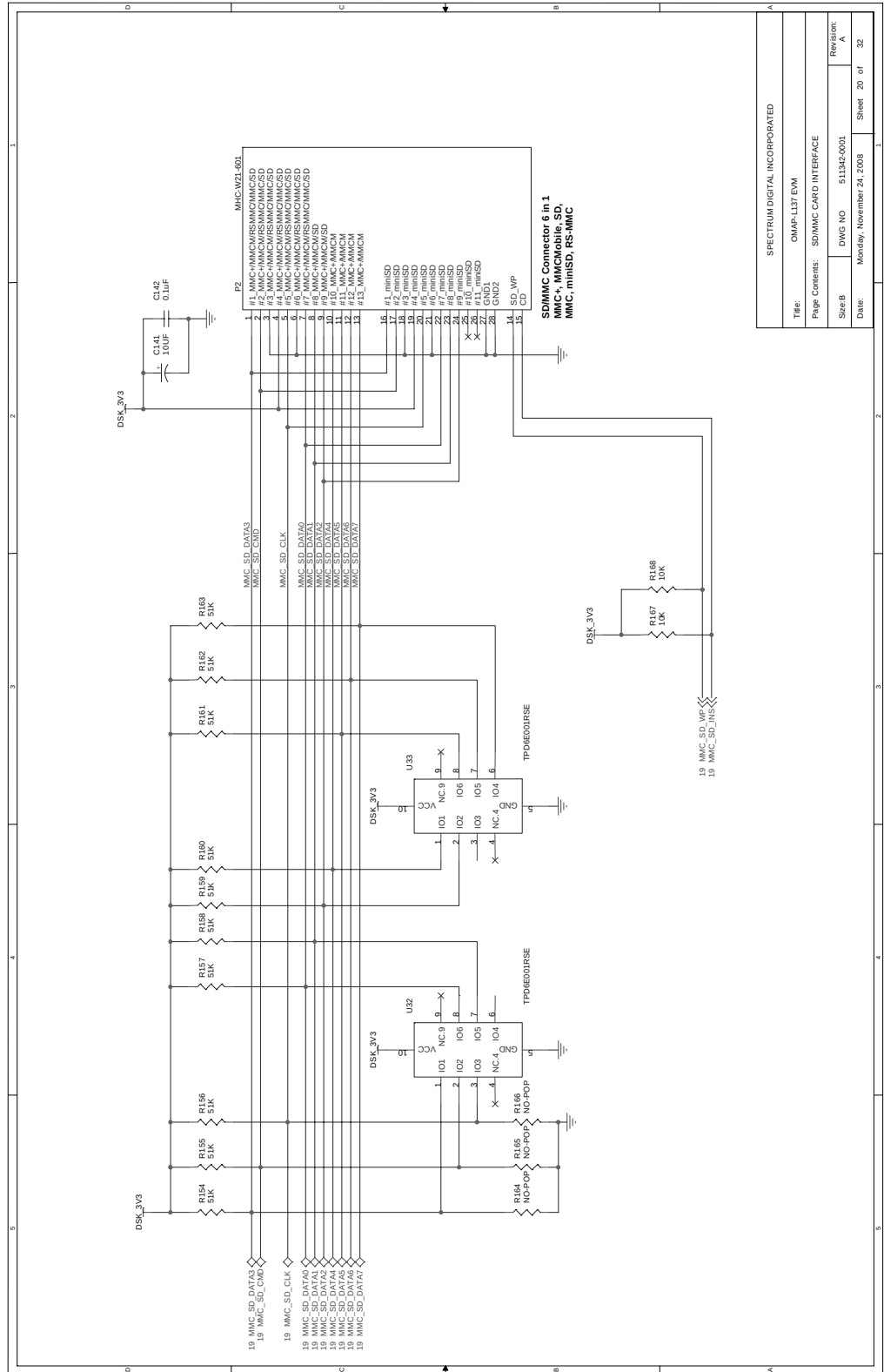




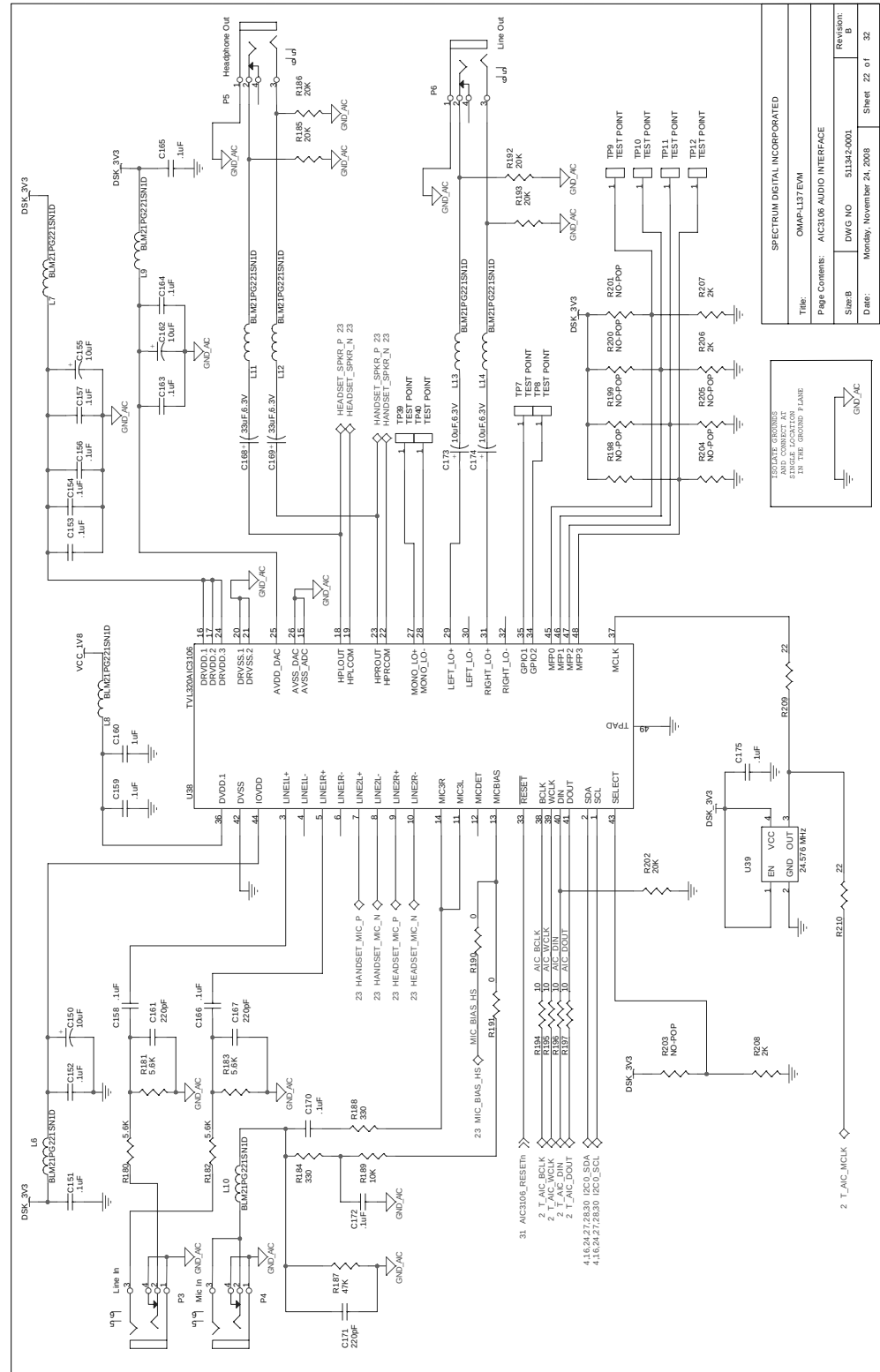
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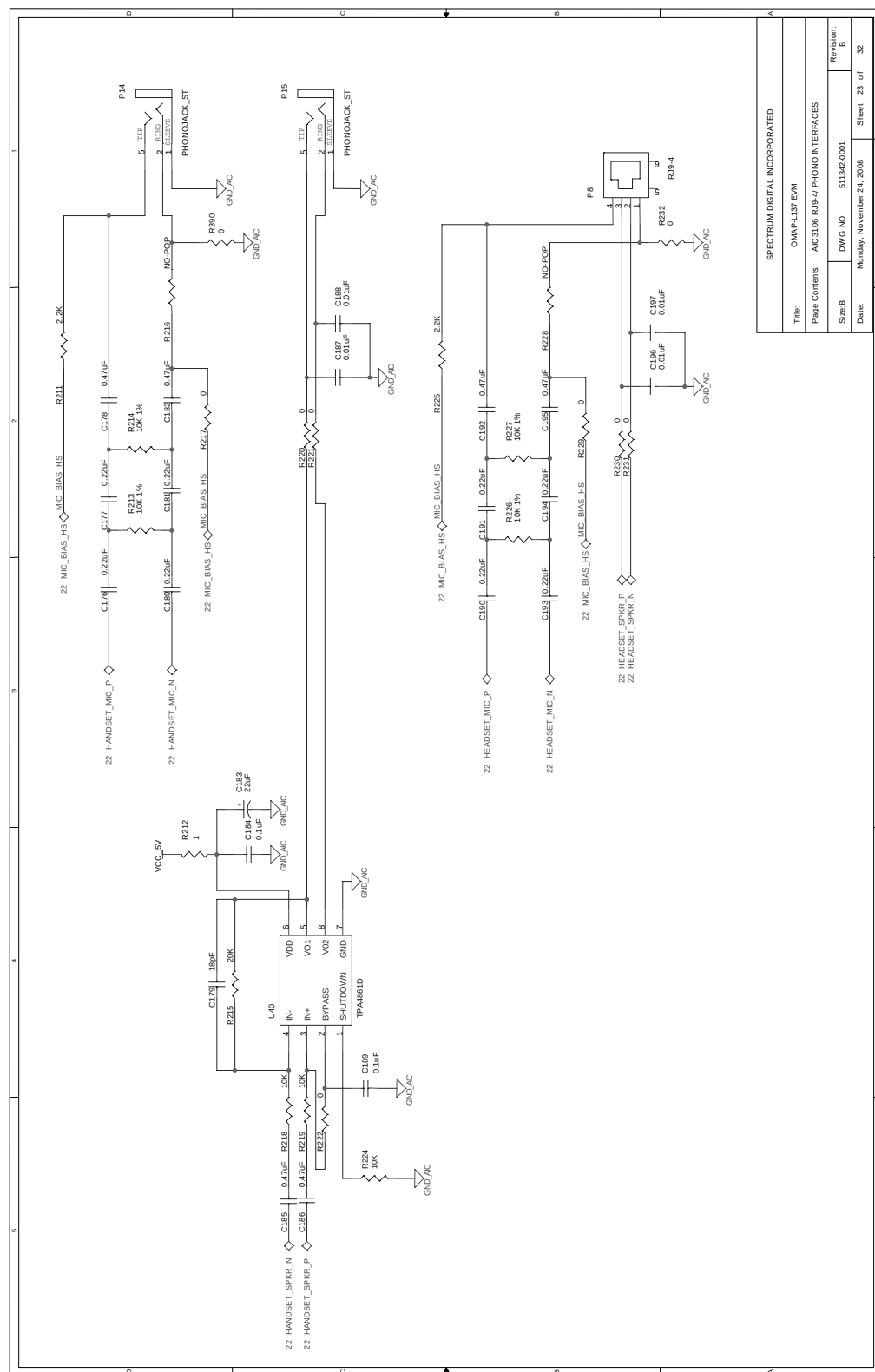




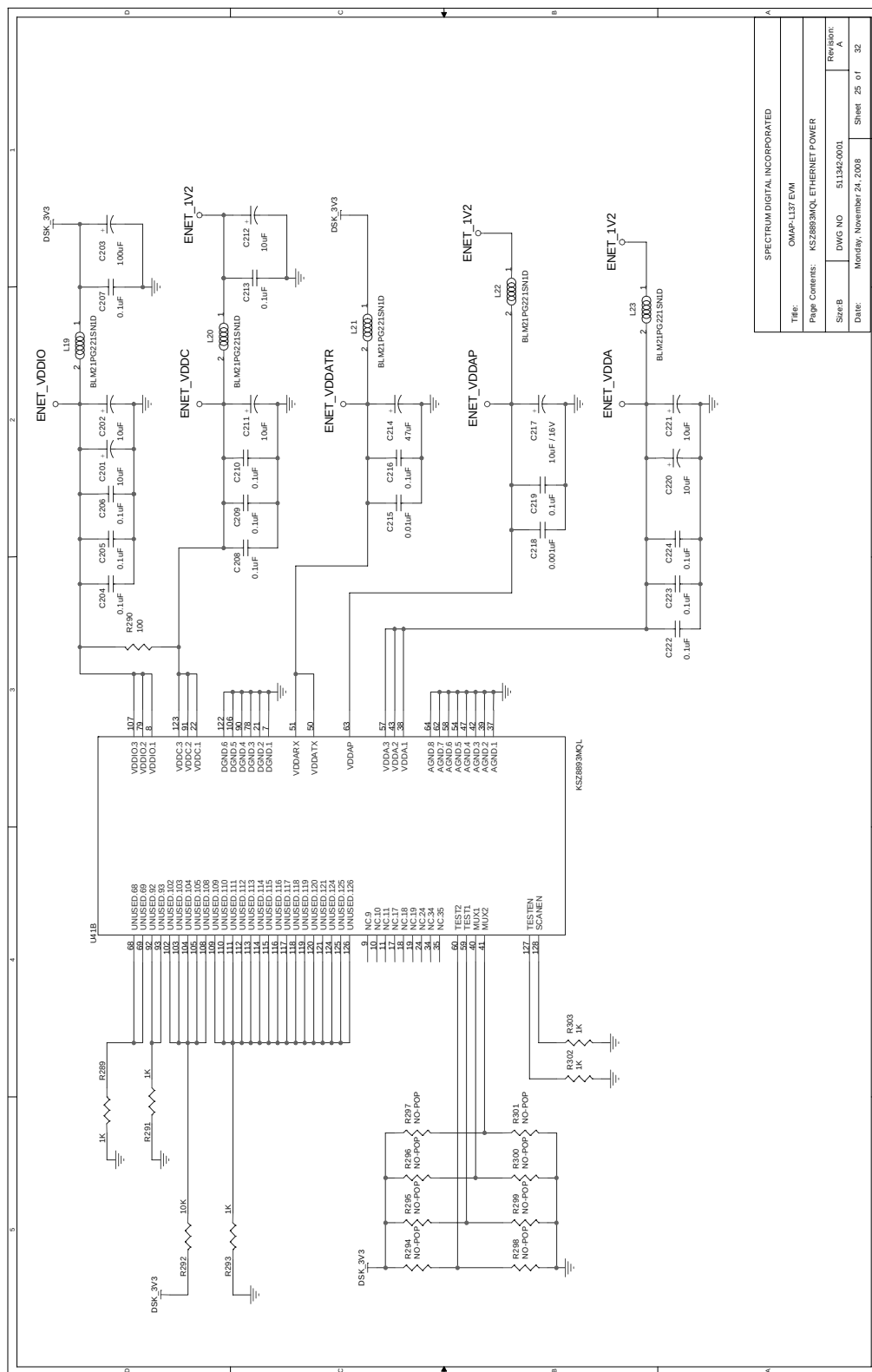


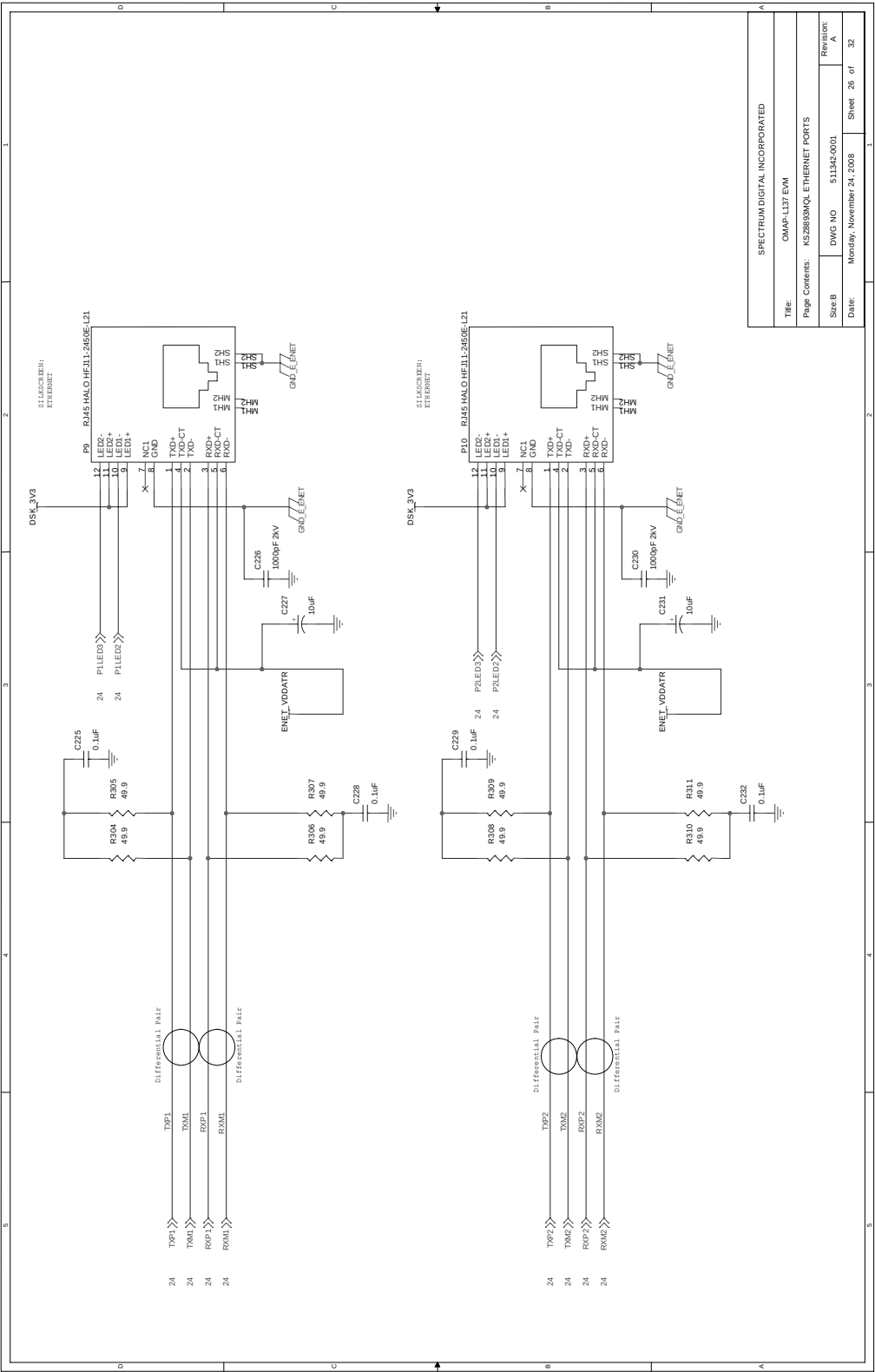




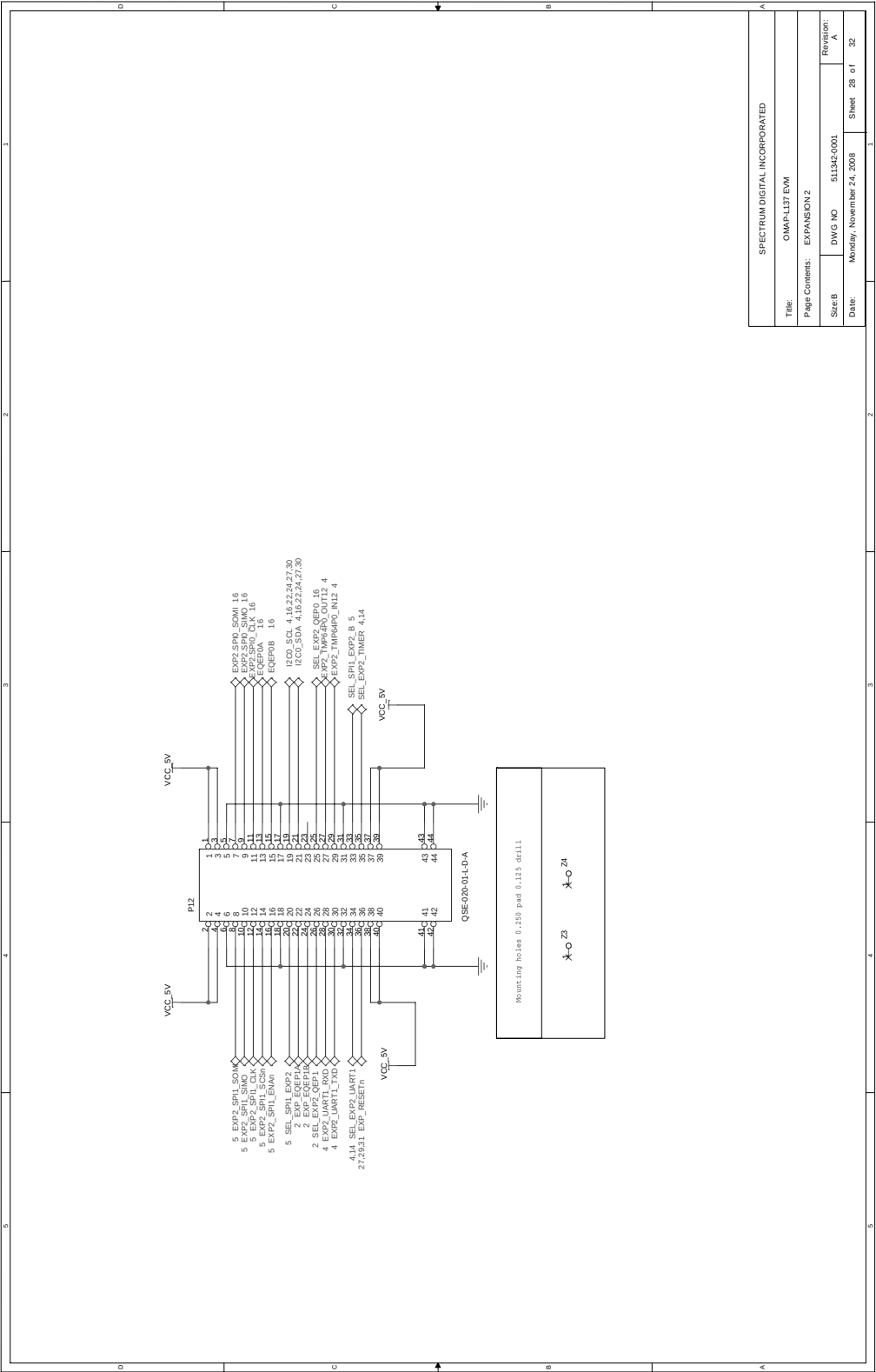


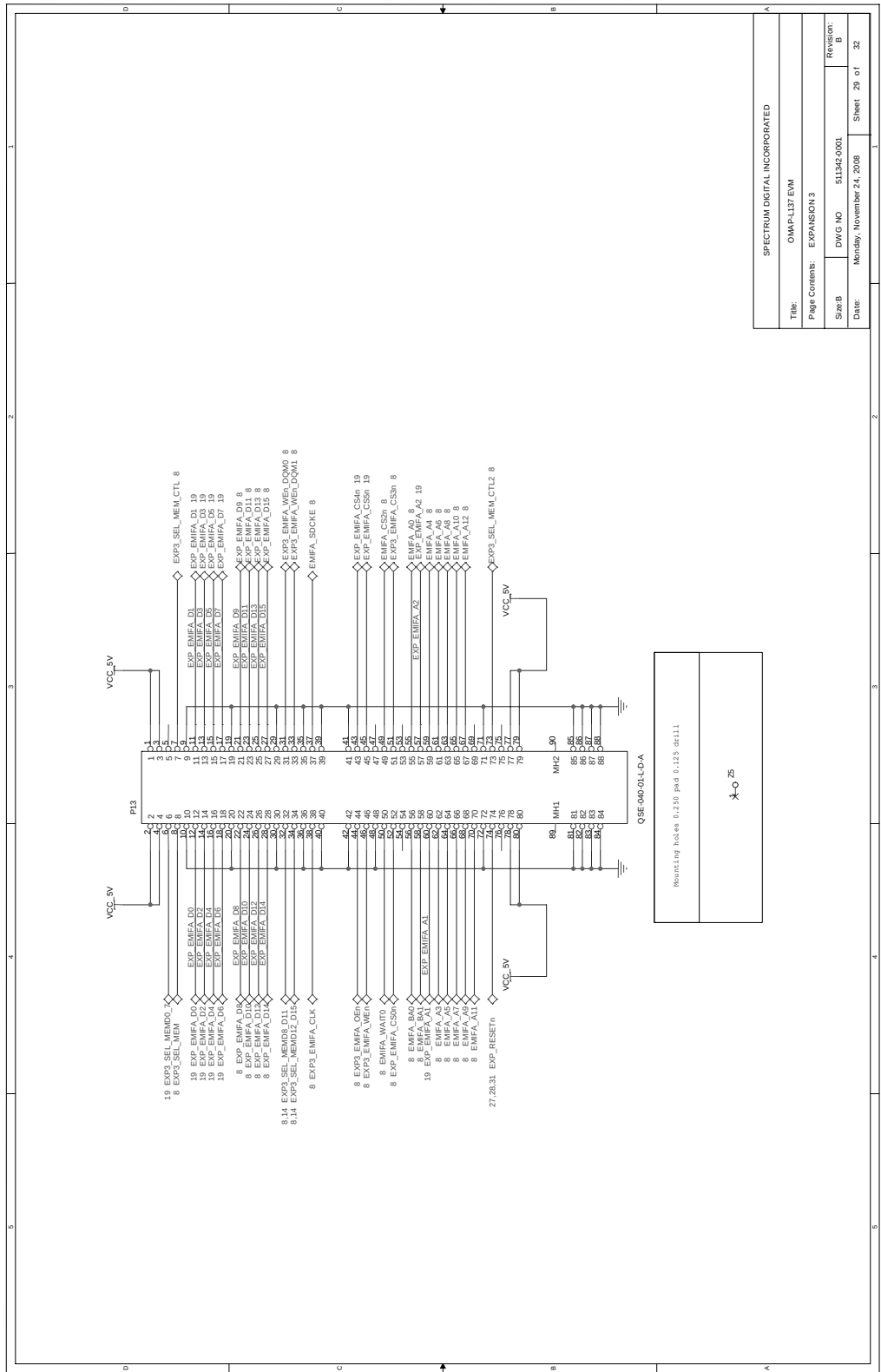


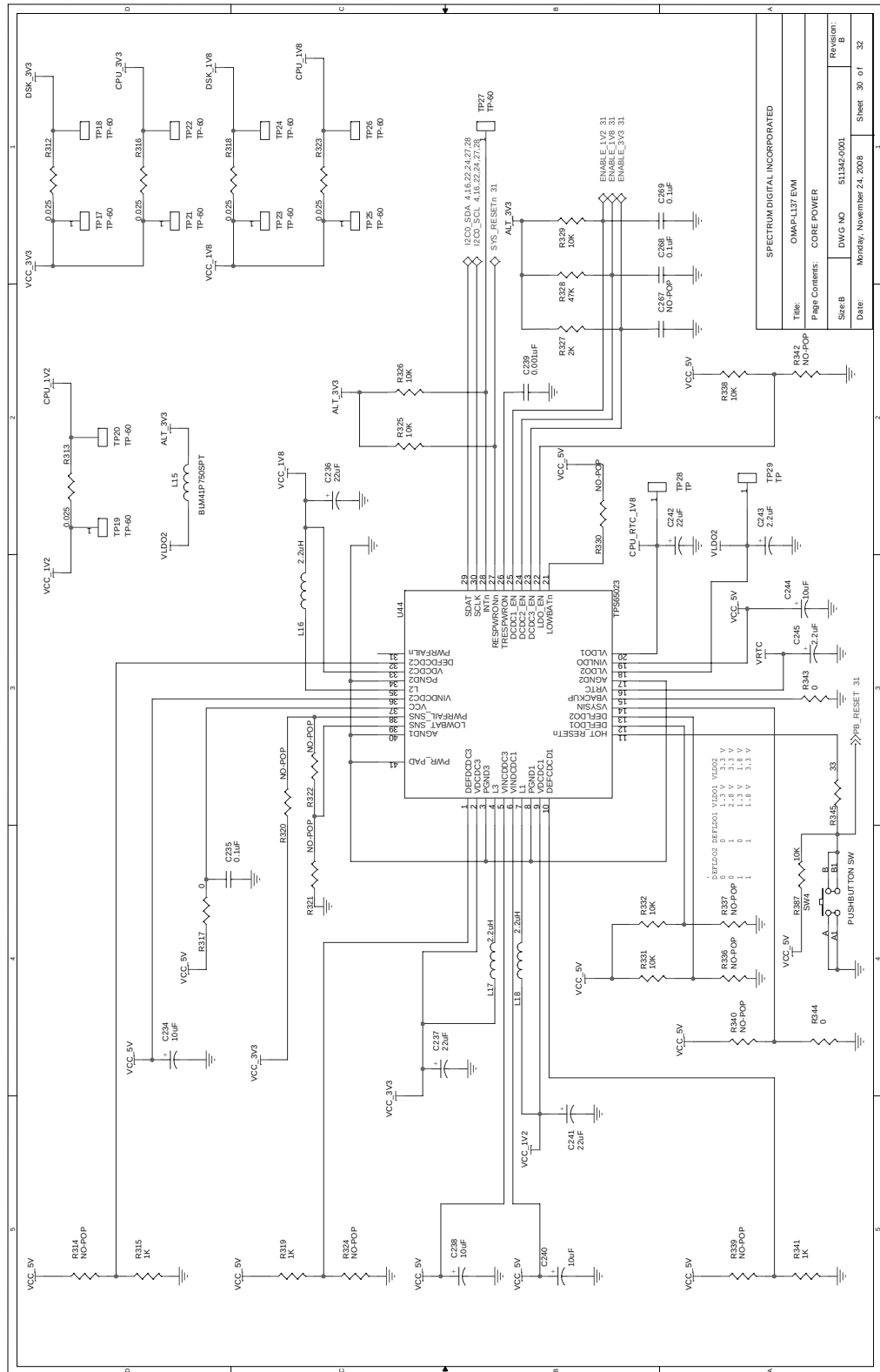


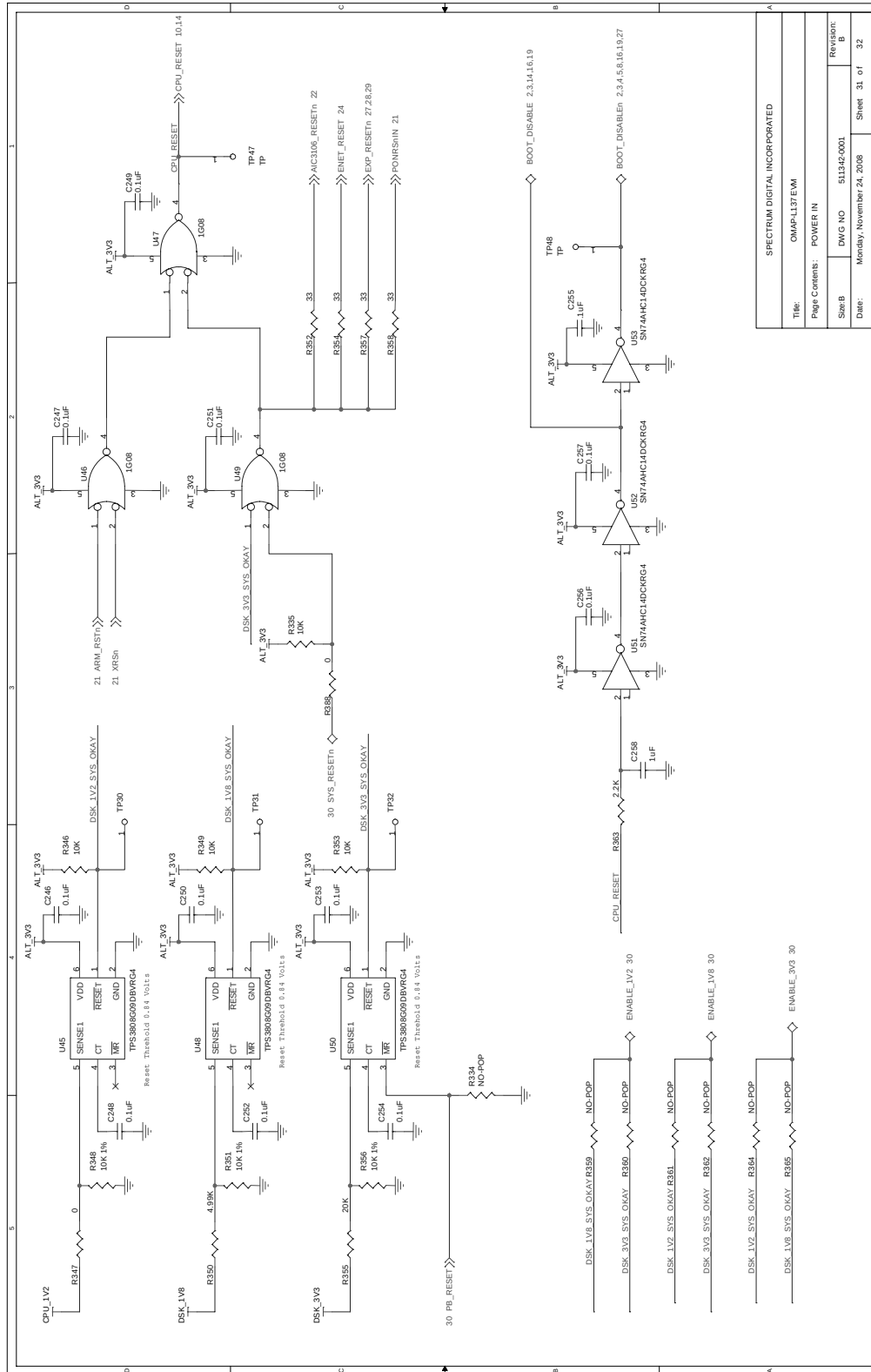




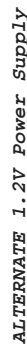








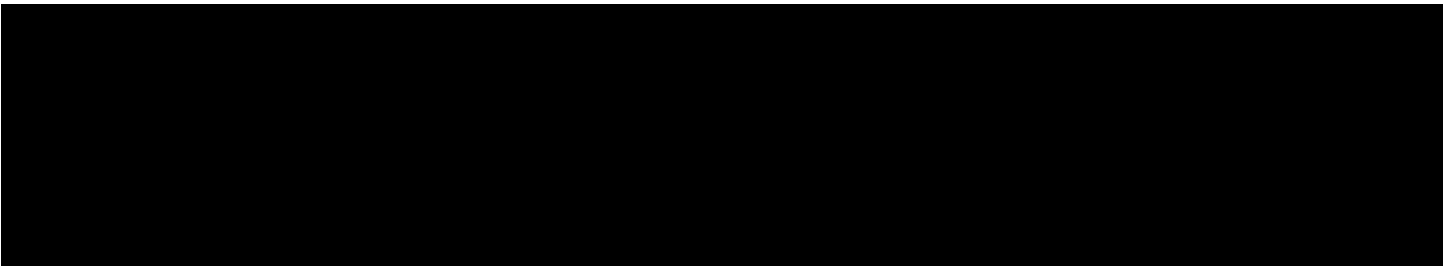
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Page Contents:	POWER IN		
Size:	B	DWG NO	511342-0001
Date:	Monday, November 24, 2008	Sheet	31 of 32



Appendix B

Mechanical Information

This appendix contains the mechanical information about the OMAP-L137 EVM produced by Spectrum Digital.



AMEYA360

Components Supply Platform

Authorized Distribution Brand :



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