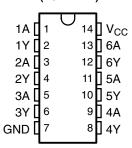
- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- 2-V to 6-V V<sub>CC</sub> Operation
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20-μA Max I<sub>CC</sub>

#### description/ordering information

This Schmitt-trigger device contains six independent inverters. It performs the Boolean function  $Y = \overline{A}$  in positive logic.

- Typical t<sub>pd</sub> = 11 ns
- ±4-mA Output Drive at 5 V
- Low Input Current of 1 μA Max

#### D OR PW PACKAGE (TOP VIEW)



#### ORDERING INFORMATION<sup>†</sup>

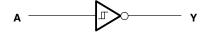
T <sub>A</sub>	T <sub>A</sub> PACKAGE <sup>‡</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
40°C to 105°C	SOIC - D	Tape and reel	SN74HC14QDRQ1	HC14QQ1
-40°C to 125°C	TSSOP - PW	Tape and reel	SN74HC14QPWRQ1	HC14QQ1

<sup>&</sup>lt;sup>†</sup> For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

# FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
Н	L
L	Н

#### logic diagram (positive logic)





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



<sup>&</sup>lt;sup>‡</sup> Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	±20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> ) (see Note 1)	±20 mA
Continuous output current, I <sub>O</sub> (V <sub>O</sub> = 0 to V <sub>CC</sub> )	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	86°C/W
PW package	113°C/W
Storage temperature range, T <sub>stg</sub>	. –65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	5	6	V
V <sub>IL</sub>	Low-level input voltage V <sub>CC</sub> = 6 V			1.8	V
VI	Input voltage	0		$V_{CC}$	V
Vo	Output voltage	0		$V_{CC}$	V
T <sub>A</sub>	Operating free-air temperature	-40		125	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEGT COMPLET	FIGNO	1 ,,	Т	A = 25°C	;	MAINI	MAY	
PARAMETER	TEST CONDIT	IIONS	v <sub>cc</sub>	MIN	TYP	MAX	MIN	MAX	UNIT
					1.2	1.5	0.7	1.5	
$V_{T+}$		4.5 V	1.55	2.5	3.15	1.55	3.15	V	
			6 V	2.1	3.3	4.2	2.1	4.2	
			2 V	0.3	0.6	1	0.3	1	
$V_{T-}$			4.5 V	0.9	1.6	2.45	0.9	2.45	V
			6 V	1.2	2	3.2	1.2	3.2	
			2 V	0.2	0.6	1.2	0.2	1.2	
$V_{T+} - V_{T-}$			4.5 V	0.4	0.9	2.1	0.4	2.1	V
		6 V	0.5	1.3	2.5	0.5	2.5		
	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>		2 V	1.9	1.998		1.9		
		$I_{OH} = -20 \mu A$	4.5 V	4.4	4.499		4.4		
V <sub>OH</sub>			6 V	5.9	5.999		5.9		V
		$I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.3		3.7		
		$I_{OH} = -5.2 \text{ mA}$	6 V	5.48	5.8		5.2		
			2 V		0.002	0.1		0.1	
		$I_{OL} = 20 \mu A$	4.5 V		0.001	0.1		0.1	]
$V_{OL}$	$V_i = V_{iH}$ or $V_{iL}$		6 V		0.001	0.1		0.1	V
		$I_{OL} = 4 \text{ mA}$	4.5 V		0.17	0.26		0.4	
		$I_{OL} = 5.2 \text{ mA}$	6 V		0.15	0.26		0.4	
l <sub>l</sub>	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000	nA
I <sub>CC</sub>	$V_I = V_{CC}$ or 0,	I <sub>O</sub> = 0	6 V			2		40	μΑ
C <sub>i</sub>			2 V to 6 V		3	10		10	pF

# switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

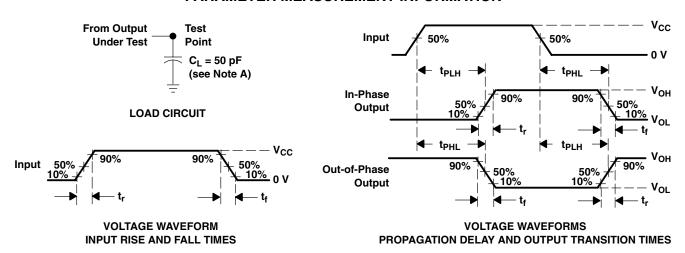
DADAMETED	FROM	то	v <sub>cc</sub>	T	չ = 25°C	;	BAINI	MAY	LINUT		
PARAMETER	(INPUT)	(OUTPUT)		(INPUT) (OUTPUT)		MIN	TYP	MAX	MIN	MAX	UNIT
			2 V		55	125		190			
t <sub>pd</sub>	Α	Υ	4.5 V		12	25		38	ns		
·			6 V		11	21		32			
			2 V		38	75		110			
t <sub>t</sub>		Y	4.5 V		8	15		22	ns		
			6 V		6	13		19			

### operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per inverter	No load	20	pF



#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and test-fixture capacitance.

- B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns.  $t_f = 6$  ns.
- C. The outputs are measured one at a time with one input transition per measurement.
- D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms







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#### PACKAGING INFORMATION

Orderable Device	Status	Package Type	_	Pins	•	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
	(1)		Drawing		Qty	(2)		(3)		(4)	
SN74HC14QDRG4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC14QQ1	Samples
SN74HC14QDRQ1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC14QQ1	Samples
SN74HC14QPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC14QQ1	Samples
SN74HC14QPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC14QQ1	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.





11-Apr-2013

#### OTHER QUALIFIED VERSIONS OF SN74HC14-Q1:

Catalog: SN74HC14

• Military: SN54HC14

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

#### PACKAGE MATERIALS INFORMATION

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#### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC14QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC14QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

# **PACKAGE MATERIALS INFORMATION**

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#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC14QPWRG4Q1	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74HC14QPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0

# D (R-PDSO-G14)

#### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



# D (R-PDSO-G14)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

#### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
  - Sody length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



# PW (R-PDSO-G14)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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