

## LM2724A High Speed 3A Synchronous MOSFET Driver

Check for Samples: [LM2724A](#)

### FEATURES

- Shoot-Through Protection
- Input Under-Voltage-Lock-Out
- 3A Peak Driving Current
- 195 $\mu$ A Quiescent Current
- 28V Input Voltage in Buck Configuration
- SOIC-8 and WSON Packages

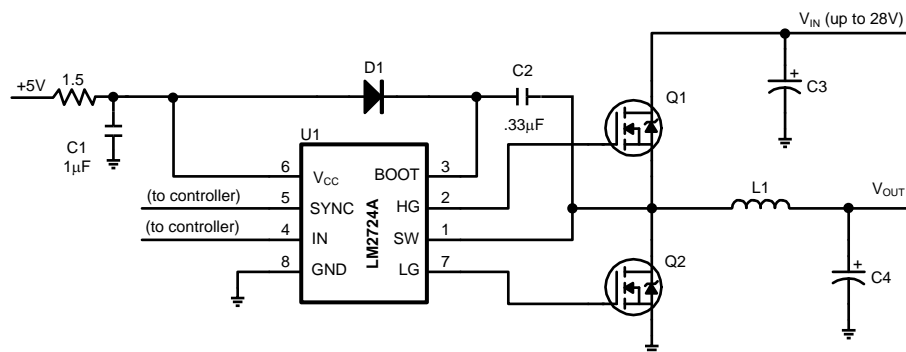
### APPLICATIONS

- High Current DC/DC Power Supplies
- High Input Voltage Switching Regulators
- Fast Transient Microprocessors
- Notebook Computers

### DESCRIPTION

The LM2724A is a dual N-channel MOSFET driver which can drive both the top and bottom MOSFETs in a push-pull structure simultaneously. The LM2724A takes a logic input and splits it into two complimentary signals with a typical 20ns dead time in between. The built-in cross-conduction protection circuitry prevents the top and bottom MOSFETs from turning on simultaneously. With a bias voltage of 5V, the peak sourcing and sinking current for each driver of the LM2724A is about 3A. Input UVLO (Under-Voltage-Lock-Out) ensures that all the driver outputs stay low until the supply rail exceeds the power-on threshold, or after the supply rail drops below power-on threshold by a specified hysteresis during system power down. The cross-conduction protection circuitry detects both driver outputs and will not turn on a driver until the other driver output is low. The top gate voltage needed by the top MOSFET is obtained through an external boot-strap structure. When not switching, the LM2724A only draws up to 195 $\mu$ A from the 5V rail. The synchronization operation of the bottom MOSFET can be disabled by pulling the SYNC pin to ground.

### TYPICAL APPLICATION



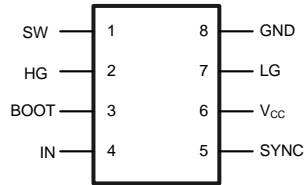
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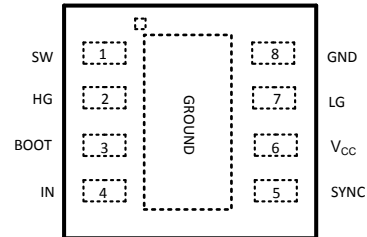


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## CONNECTION DIAGRAM



**Figure 1. 8-Lead SOIC**  
See Package Number D

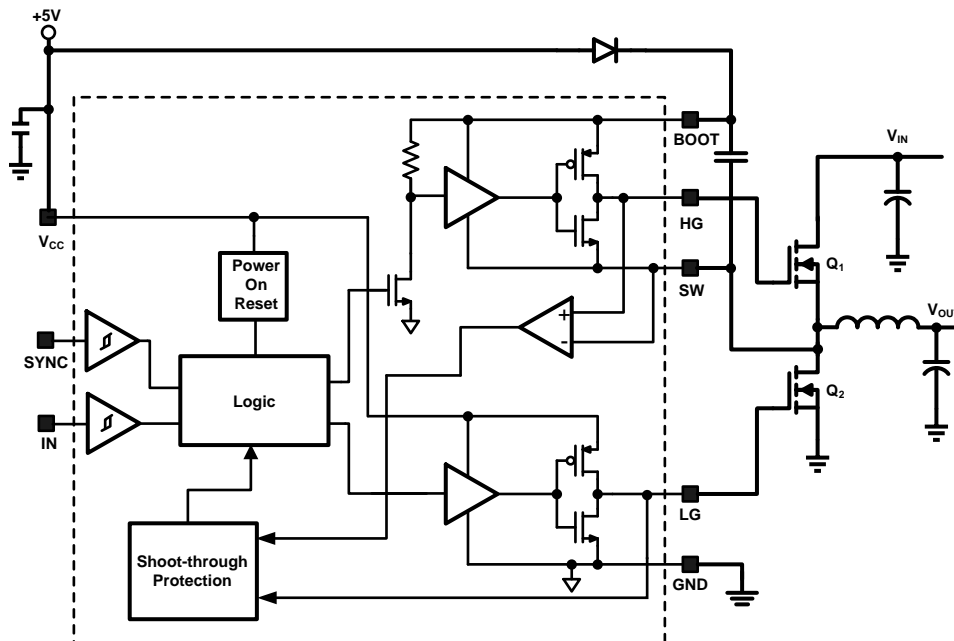


**Figure 2. 8-Lead WSON**  
See Package Number NGN

## PIN DESCRIPTIONS

| Pin | Name            | Function   |
|-----|-----------------|--|
| 1   | SW              | Top driver return. Should be connected to the common node of top and bottom FETs |
| 2   | HG              | Top gate drive output. Should be connected to the top FET gate.                  |
| 3   | BOOT            | Bootstrap. Accepts a bootstrap voltage for powering the high-side driver         |
| 4   | IN              | Accepts a logic control signal   |
| 5   | SYNC            | Bottom gate enable   |
| 6   | V <sub>CC</sub> | Connect to +5V supply  |
| 7   | LG              | Bottom gate drive output. Should be connected to the bottom FET gate.            |
| 8   | GND             | Ground   |

## BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)</sup>**

|                                  |                                 | VALUE / UNITS                   |
|----------------------------------|---------------------------------|---------------------------------|
| $V_{CC}$                         |                                 | 7V                              |
| BOOT to SW                       |                                 | 7V                              |
| BOOT to GND <sup>(3)</sup>       |                                 | 35V                             |
| SW to GND <sup>(4)</sup>         |                                 | -2V to 30V                      |
| Junction Temperature             |                                 | +150°C                          |
| Power Dissipation <sup>(5)</sup> |                                 | 720mW (SOIC-8)<br>3.2W (WSON-8) |
| Storage Temperature              |                                 | -65°C to 150°C                  |
| ESD Susceptibility               | Human Body Model <sup>(6)</sup> | 2.0 kV                          |
| Soldering Time, Temperature      |                                 | 10sec., 300°C                   |

- (1) **Absolute Maximum Ratings** are limits beyond which damage to the device may occur. **Operating ratings** are conditions under which the device operates correctly. The ensured specifications apply only for the listed test conditions. Some performance characteristics may degrade when the part is not operated under listed conditions.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) If BOOT voltage exceeds this value, the ESD structure will degrade.
- (4) The SW pin can have -2V to -0.5V applied for a maximum duty cycle of 10% with a maximum period of 1 second. There is no duty cycle or maximum period limitation for a SW pin voltage range of -0.5V to 30V.
- (5) Maximum allowable power dissipation is a function of the maximum junction temperature,  $T_{JMAX}$ , the junction-to-ambient thermal resistance,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable power dissipation at any ambient temperature is calculated using:  $P_{MAX} = (T_{JMAX} - T_A) / \theta_{JA}$ . The junction-to-ambient thermal resistance,  $\theta_{JA}$ , for LM2724A is 172°C/W. For a  $T_{JMAX}$  of 150°C and  $T_A$  of 25°C, the maximum allowable power dissipation is 0.7W. The  $\theta_{JA}$ , for LM2724A WSON package is 39°C/W. For a  $T_{JMAX}$  of 150°C and  $T_A$  of 25°C, the maximum allowable power dissipation is 3.2W.
- (6) ESD machine model susceptibility is 200V.

**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

|                            |  | VALUE / UNITS  |
|----------------------------|--|----------------|
| $V_{CC}$                   |  | 4.3V to 6.8V   |
| Junction Temperature Range |  | -40°C to 125°C |

- (1) **Absolute Maximum Ratings** are limits beyond which damage to the device may occur. **Operating ratings** are conditions under which the device operates correctly. The ensured specifications apply only for the listed test conditions. Some performance characteristics may degrade when the part is not operated under listed conditions.

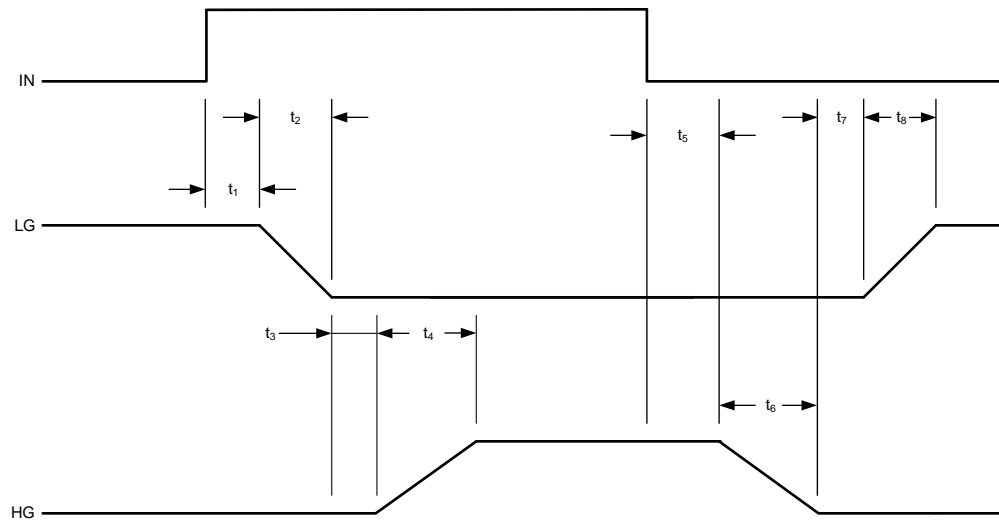
## Electrical Characteristics — LM2724A

$V_{CC} = \text{BOOT} = \text{SYNC} = 5\text{V}$ ,  $\text{SW} = \text{GND} = 0\text{V}$ , unless otherwise specified. Typicals and limits appearing in plain type apply for  $T_A = T_J = +25^\circ\text{C}$ . Limits appearing in **boldface** type apply over the entire operating temperature range.

| Symbol               | Parameter   | Condition                                 | Min        | Typ  | Max        | Units         |
|----------------------|---|---|------------|------|------------|---------------|
| <b>POWER SUPPLY</b>  |   |   |            |      |            |               |
| $I_{q\_op}$          | Operating Quiescent Current   | $\text{IN} = 0\text{V}$                   |            | 145  | <b>195</b> | $\mu\text{A}$ |
| <b>TOP DRIVER</b>    |   |   |            |      |            |               |
|                      | Peak Pull-Up Current  |   |            | 3.0  |            | A             |
|                      | Pull-Up $R_{ds\_on}$  | $I_{BOOT} = I_{HG} = 0.3\text{A}$         |            | 1.2  |            | $\Omega$      |
|                      | Peak Pull-down Current  |   |            | -3.2 |            | A             |
|                      | Pull-down $R_{ds\_on}$  | $I_{SW} = I_{HG} = 0.3\text{A}$           |            | 0.5  |            | $\Omega$      |
| $t_4$                | Rise Time   | Timing Diagram, $C_{LOAD} = 3.3\text{nF}$ |            | 17   |            | ns            |
| $t_6$                | Fall Time   |   |            | 12   |            | ns            |
| $t_3$                | Pull-Up Dead Time   | Timing Diagram                            |            | 19   |            | ns            |
| $t_5$                | Pull-Down Delay   | Timing Diagram, from IN Falling Edge      |            | 27   |            | ns            |
| <b>BOTTOM DRIVER</b> |   |   |            |      |            |               |
|                      | Peak Pull-Up Current  |   |            | 3.2  |            | A             |
|                      | Pull-up $R_{ds\_on}$  | $I_{VCC} = I_{LG} = 0.3\text{A}$          |            | 1.1  |            | $\Omega$      |
|                      | Peak Pull-down Current  |   |            | 3.2  |            | A             |
|                      | Pull-down $R_{ds\_on}$  | $I_{GND} = I_{LG} = 0.3\text{A}$          |            | 0.6  |            | $\Omega$      |
| $t_8$                | Rise Time   | Timing Diagram, $C_{LOAD} = 3.3\text{nF}$ |            | 17   |            | ns            |
| $t_2$                | Fall Time   |   |            | 14   |            | ns            |
| $t_7$                | Pull-up Dead Time   | Timing Diagram                            |            | 22   |            | ns            |
| $t_1$                | Pull-down Delay   | Timing Diagram                            |            | 13   |            | ns            |
| <b>LOGIC</b>         |   |   |            |      |            |               |
| $V_{uvlo\_up}$       | $V_{CC}$ Under-Voltage-Lock-Out Upper Threshold                         | $V_{CC}$ rises from 0V toward 5V          |            |      | <b>4</b>   | V             |
| $V_{uvlo\_dn}$       | $V_{CC}$ Under-Voltage-Lock-Out Lower Threshold                         | $V_{CC}$ falls from 5V toward 0V          | <b>2.5</b> |      |            | V             |
| $V_{uvlo\_hys}$      | $V_{CC}$ Under-Voltage-Lock-Out Hysteresis                              | $V_{CC}$ falls from 5V toward 0V          |            | 0.8  |            | V             |
| $V_{IH\_SYNC}$       | SYNC Pin High Input   |   | <b>55%</b> |      |            | $V_{CC}$      |
| $V_{IL\_SYNC}$       | SYNC Pin Low Input  |   |            |      | <b>25%</b> |               |
| $I_{leak\_SYNC}$     | SYNC Pin Leakage Current  | SYNC = 5V, Sink Current                   |            |      | <b>2</b>   | $\mu\text{A}$ |
|                      |   | SYNC = 0V, Source Current                 |            |      | <b>10</b>  |               |
| $I_{leak\_IN}$       | IN Pin Leakage Current  | IN = 0V, Source Current                   |            |      | <b>2</b>   | $\mu\text{A}$ |
|                      |   | IN = 5V, Sink Current                     |            |      | <b>10</b>  |               |
| $t_{on\_min1}$       | Minimum Positive Pulse Width at IN Pin <sup>(1)</sup>                   |   |            | 160  |            | ns            |
| $t_{on\_min2}$       | Minimum Positive Pulse Width at IN Pin for HG to Respond <sup>(2)</sup> |   |            | 45   |            |               |
| $t_{on\_min3}$       | Minimum Positive Pulse Width at IN Pin for LG to Respond <sup>(3)</sup> |   |            | 10   |            |               |
| $t_{off\_min1}$      | Minimum Negative Pulse Width at IN Pin for LG to Respond <sup>(4)</sup> |   |            | 40   |            |               |
| $t_{off\_min2}$      | Minimum Negative Pulse Width at IN Pin for HG to Respond <sup>(5)</sup> |   |            | 5    |            |               |
| $V_{IH\_IN}$         | IN High Level Input Voltage   | When IN pin goes high from 0V             | <b>55%</b> |      |            | $V_{CC}$      |
| $V_{IL\_IN}$         | IN Low Level Input Voltage  | When IN pin goes low from 5V              |            |      | <b>25%</b> |               |

- (1) If the positive pulse width at IN pin is below this value but above  $t_{on\_min2}$ , the pulse is internally stretched to  $t_{on\_min1}$ , so the HG width will be a constant value.
- (2) If the positive pulse width at IN pin is below this value but above  $t_{on\_min3}$ , then HG stops responding while LG still responds to the pulse.
- (3) If the positive pulse width at IN pin is below this value, the pulse will be completely ignored. Neither HG or LG will respond to it.
- (4) If the negative pulse width at IN pin is below this value but above  $t_{off\_min2}$ , then LG stops responding while HG still responds.
- (5) If the negative pulse width at IN pin is below this value, the pulse will be completely ignored. Neither HG or LG will respond to it.

## TIMING DIAGRAM



## REVISION HISTORY

### Changes from Revision B (March 2013) to Revision C

### Page

- Changed layout of National Data Sheet to TI format ..... [5](#)

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|------------------|----------------------|--------------|--------------------------|---------|
| LM2724AMX        | NRND          | SOIC         | D                  | 8    | 2500           | TBD                        | Call TI          | Call TI              |              | 2724<br>AM               |         |
| LM2724AMX/NOPB   | NRND          | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | CU SN            | Level-1-260C-UNLIM   |              | 2724<br>AM               |         |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LM2724AMX      | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.5     | 5.4     | 2.0     | 8.0     | 12.0   | Q1            |
| LM2724AMX/NOPB | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.5     | 5.4     | 2.0     | 8.0     | 12.0   | Q1            |



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LM2724AMX      | SOIC         | D               | 8    | 2500 | 367.0       | 367.0      | 35.0        |
| LM2724AMX/NOPB | SOIC         | D               | 8    | 2500 | 367.0       | 367.0      | 35.0        |

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

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|                               |  |
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