

Low-Voltage 1:10 LVPECL/HSTL With Selectable Input Clock Driver

Check for Samples: [CDCLVP110](#)

FEATURES

- Distributes One Differential Clock Input Pair LVPECL/HSTL to 10 Differential LVPECL Clock Outputs
- Fully Compatible With LVECL/LVPECL/HSTL
- Single Supply Voltage Required, $\pm 3.3\text{-V}$ or $\pm 2.5\text{-V}$ Supply
- Selectable Clock Input Through CLK_SEL
- Low-Output Skew (Typ 15 ps) for Clock-Distribution Applications
- VBB Reference Voltage Output for Single-Ended Clocking
- Available in a 32-Pin LQFP Package
- Frequency Range From DC to 3.5 GHz
- Pin-to-Pin Compatible With MC100 Series EP111, ES6111, LVEP111, PTN1111

DESCRIPTION

The CDCLVP110 clock driver distributes one differential clock pair of either LVPECL or HSTL (selectable) input, (CLK0, CLK1) to ten pairs of differential LVPECL clock (Q0, Q9) outputs with minimum skew for clock distribution. The CDCLVP110 can accept two clock sources into an input multiplexer. The CLK0 input accepts either LVECL/LVPECL input signals, while CLK1 accepts an HSTL input signal when operated under LVPECL conditions. The CDCLVP110 is specifically designed for driving 50- Ω transmission lines.

The VBB reference voltage output is used if single-ended input operation is required. In this case the VBB pin should be connected to $\overline{\text{CLK0}}$ and bypassed to GND via a 10-nF capacitor.

However, for high-speed performance up to 3.5 GHz, the differential mode is strongly recommended.

The CDCLVP110 is characterized for operation from -40°C to 85°C .

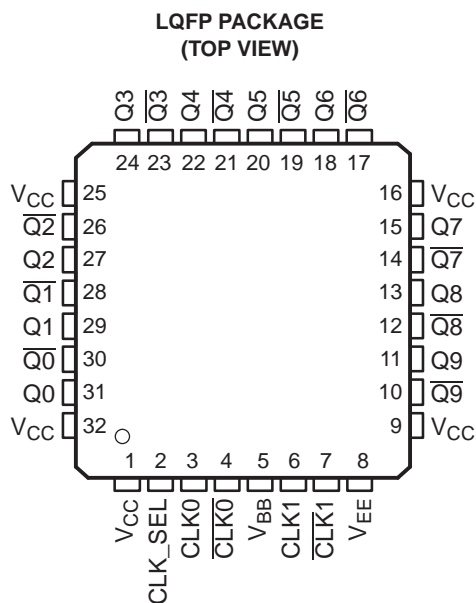


Table 1. FUNCTION TABLE

| CLK_SEL | ACTIVE CLOCK INPUT |
|---------|--------------------------------|
| 0 | CLK0, $\overline{\text{CLK0}}$ |
| 1 | CLK1, $\overline{\text{CLK1}}$ |



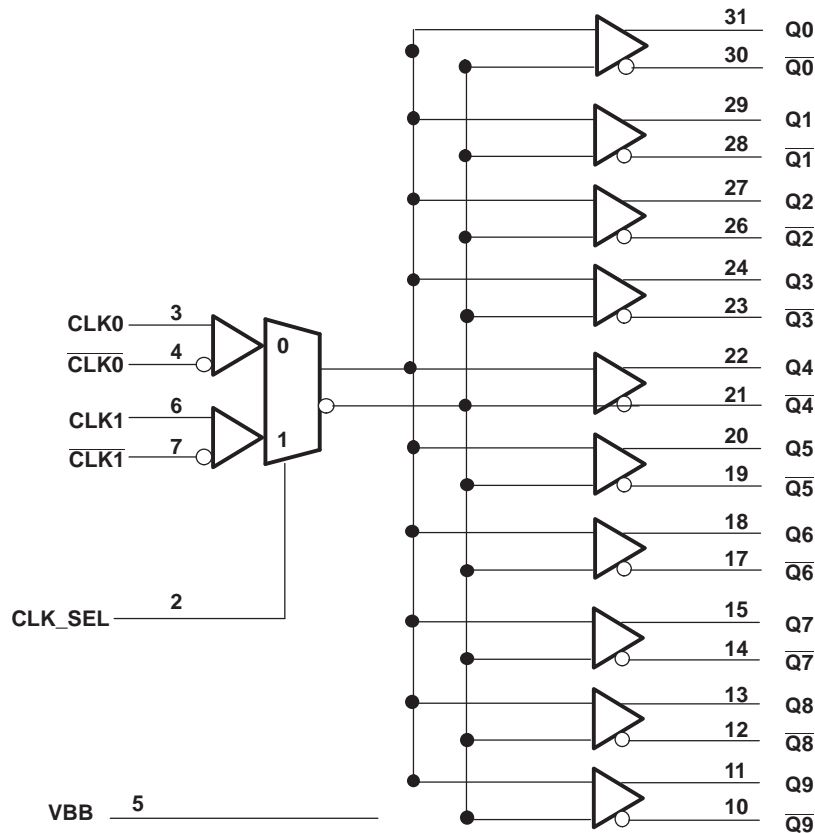
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



TERMINAL FUNCTIONS

| TERMINAL | | DESCRIPTION |
|--------------------------------|--|--|
| NAME | NO. | |
| CLK_SEL | 2 | Clock select. Used to select between CLK0 and CLK1 input pairs. |
| CLK0, $\overline{\text{CLK0}}$ | 3, 4 | Differential LVECL/LVPECL input pair |
| CLK1, $\overline{\text{CLK1}}$ | 6, 7 | Differential HSTL input pair |
| Q [9:0] | 11, 13, 15, 18, 20, 22, 24, 27, 29, 31 | LVECL/LVPECL clock outputs, these outputs provide low-skew copies of CLKn. |
| $\overline{\text{Q}}$ [9:0] | 10, 12, 14, 17, 19, 21, 23, 26, 28, 30 | LVECL/LVPECL complementary clock outputs, these outputs provide copies of $\overline{\text{CLKn}}$. |
| V _{BB} | 5 | Reference voltage output for single-ended input operation |
| V _{CC} | 1, 9, 16, 25, 32 | Supply voltage |
| V _{EE} | 8 | Device ground or negative supply voltage in ECL mode |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | | VALUE | UNIT |
|------------------|---------------------------|-------------------------------|------|
| V _{CC} | Supply voltage | –0.3 to 4.6 | V |
| V _I | Input voltage | –0.3 to V _{CC} + 0.5 | V |
| V _O | Output voltage | –0.3 to V _{CC} + 0.5 | V |
| I _{IN} | Input current | ±20 | mA |
| V _{EE} | Negative supply voltage | –0.3 to 4.6 | V |
| I _{BB} | Sink/source current | –1 to 1 | mA |
| I _O | DC output current | –50 | mA |
| T _{stg} | Storage temperature range | –65 to 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|-------------------------------|---|-------|---------|-----|------|
| V _{CC} | Supply voltage (relative to V _{EE}) | 2.375 | 2.5/3.3 | 3.8 | V |
| T _A ⁽¹⁾ | Operating free-air temperature | –40 | | 85 | °C |

- (1) Operating junction temperature affects device lifetime. The continuous operation junction temperature is recommended to be at max 110°C. The device ac and dc parameters are specified up to 85°C ambient temperature. See the *PCB Layout Guidelines for CDCLVP110* application note, literature number SCAA057 for more details.

PACKAGE THERMAL IMPEDANCE

| | | TEST CONDITIONS | MIN | MAX | UNIT |
|-----------------|---|-----------------|-----|-----|------|
| Θ _{JA} | Thermal resistance junction to ambient ⁽¹⁾ | 0 LFM | | 74 | °C/W |
| | | 150 LFM | | 66 | °C/W |
| | | 250 LFM | | 64 | °C/W |
| | | 500 LFM | | 61 | °C/W |
| Θ _{JC} | Thermal resistance junction to case | | | 39 | °C/W |

- (1) According to JESD 51-7 standard.

LVECL DC ELECTRICAL CHARACTERISTICS

V_{supply}: V_{CC} = 0 V, V_{EE} = –2.375 V to –3.8 V

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | | |
|-------------------|--|--|-------------------|----------------------------|--------|-------|---|
| I _{EE} | Supply internal current Absolute value of current | –40°C | | 78 | mA | | |
| | | 25°C | | 82 | | | |
| | | 85°C | | 85 | | | |
| I _{CC} | Output and internal supply current All outputs terminated 50 Ω to V _{CC} – 2 V | –40°C | | 343 | mA | | |
| | | 25°C | | 370 | | | |
| | | 85°C | | 380 | | | |
| I _{IN} | Input current | –40°C, 25°C, 85°C | | 150 | μA | | |
| V _{BB} | Internally generated bias voltage | For V _{EE} = –3 to –3.8 V, I _{BB} = –0.2 mA | –40°C, 25°C, 85°C | –1.45 | –1.3 | –1.15 | V |
| | | V _{EE} = –2.375 to –2.75 V, I _{BB} = –0.2 mA | –40°C, 25°C, 85°C | –1.4 | –1.25 | –1.1 | |
| V _{IH} | High-level input voltage (CLK_SEL) | –40°C, 25°C, 85°C | –1.165 | | –0.88 | V | |
| V _{IL} | Low-level input voltage (CLK_SEL) | –40°C, 25°C, 85°C | –1.81 | | –1.475 | V | |
| V _{INPP} | Input amplitude (CLK0, $\overline{\text{CLK0}}$) | Difference of input 9 V _{IH} –V _{IL} , See Note ⁽¹⁾ | –40°C, 25°C, 85°C | 0.5 | | 1.3 | V |
| V _{CM} | Common-mode voltage (CLK0, $\overline{\text{CLK0}}$) | Cross point of input 9 average (V _{IH} , V _{IL}) | –40°C, 25°C, 85°C | V _{EE} + 0.975 | | –0.3 | V |
| V _{OH} | High-level output voltage | I _{OH} = –21 mA | –40°C | –1.26 | | –0.9 | V |
| | | 25°C | –1.2 | | –0.9 | | |
| | | 85°C | –1.15 | | –0.9 | | |

- (1) V_{INPP} minimum and maximum is required to maintain ac specifications, actual device function tolerates a minimum V_{INPP} of 100 mV.

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LVECL DC ELECTRICAL CHARACTERISTICS (continued)

Vsupply: $V_{CC} = 0\text{ V}$, $V_{EE} = -2.375\text{ V}$ to -3.8 V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|-----------------------------------|---|-------------------|-------|-------|------|
| V _{OL} | Low-level output voltage | I _{OL} = -5 mA | -40°C | -1.85 | -1.5 | V |
| | | | 25°C | -1.85 | -1.45 | |
| | | | 85°C | -1.85 | -1.4 | |
| V _{OD} | Differential output voltage swing | Terminated with 50 Ω to V _{CC} - 2 V, See Figure 3 | -40°C, 25°C, 85°C | 600 | | V |

LVPECL/HSTL DC ELECTRICAL CHARACTERISTICS

Vsupply: $V_{CC} = 2.375\text{ V}$ to 3.8 V , $V_{EE} = 0\text{ V}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|-------------------|---|--|-------------------|-------------------------|-------------------------|------------------------|---|
| I _{EE} | Supply internal current | Absolute value of current | -40°C | 40 | 78 | mA | |
| | | | 25°C | 45 | 82 | | |
| | | | 85°C | 48 | 85 | | |
| I _{CC} | Output and internal supply current | All outputs terminated 50 Ω to V _{CC} - 2 V | -40°C | | 343 | mA | |
| | | | 25°C | | 370 | | |
| | | | 85°C | | 380 | | |
| I _{IN} | Input current | | -40°C, 25°C, 85°C | | 150 | μA | |
| V _{BB} | Internally generated bias voltage | V _{EE} = -3 to -3.8 V, I _{BB} = -0.2 mA | -40°C, 25°C, 85°C | V _{CC} - 1.45 | V _{CC} - 1.3 | V _{CC} - 1.15 | V |
| | | V _{EE} = -2.375 to -2.75 V, I _{BB} = -0.2 mA | -40°C, 25°C, 85°C | V _{CC} - 1.4 | V _{CC} - 1.25 | V _{CC} - 1.1 | |
| V _{IH} | High-level input voltage (CLK_SEL) | | -40°C, 25°C, 85°C | V _{CC} - 1.165 | V _{CC} - 0.88 | V | |
| V _{IL} | Low-level input voltage (CLK_SEL) | | -40°C, 25°C, 85°C | V _{CC} - 1.81 | V _{CC} - 1.475 | V | |
| V _{INPP} | Input amplitude (CLK0, CLK0) | Difference of input 9 V _{IH} -V _{IL} , see Note ⁽¹⁾ | -40°C, 25°C, 85°C | 0.5 | 1.3 | V | |
| V _{IC} | Common-mode voltage (CLK0, CLK0) | Cross point of input 9 average (V _{IH} , V _{IL}) | -40°C, 25°C, 85°C | 0.975 | V _{CC} - 0.3 | V | |
| V _{ID} | Differential input voltage (CLK1, CLK1) | Difference of input V _{IH} -V _{IL} , See Note ⁽¹⁾ | -40°C, 25°C, 85°C | 0.4 | 1.9 | V | |
| V _{I(x)} | Input crossover voltage (CLK1, CLK1) | Cross point of input 9 average (V _{IH} , V _{IL}) | -40°C, 25°C, 85°C | 0.68 | 0.9 | V | |
| V _{OH} | High-level output voltage | I _{OH} = -21 mA | -40°C | V _{CC} - 1.26 | V _{CC} - 0.9 | V | |
| | | | 25°C | V _{CC} - 1.2 | V _{CC} - 0.9 | | |
| | | | 85°C | V _{CC} - 1.15 | V _{CC} - 0.9 | | |
| V _{OL} | Low-level output voltage | I _{OL} = -5 mA | -40°C | V _{CC} - 1.85 | V _{CC} - 1.5 | V | |
| | | | 25°C | V _{CC} - 1.85 | V _{CC} - 1.45 | | |
| | | | 85°C | V _{CC} - 1.85 | V _{CC} - 1.4 | | |
| V _{OD} | Differential output voltage swing | Terminated with 50 Ω to V _{CC} - 2 V, See Figure 4 | -40°C, 25°C, 85°C | 600 | | mV | |

(1) V_{INPP} minimum and maximum is required to maintain ac specifications, actual device function tolerates a minimum V_{INPP} of 100 mV.

AC ELECTRICAL CHARACTERISTICS

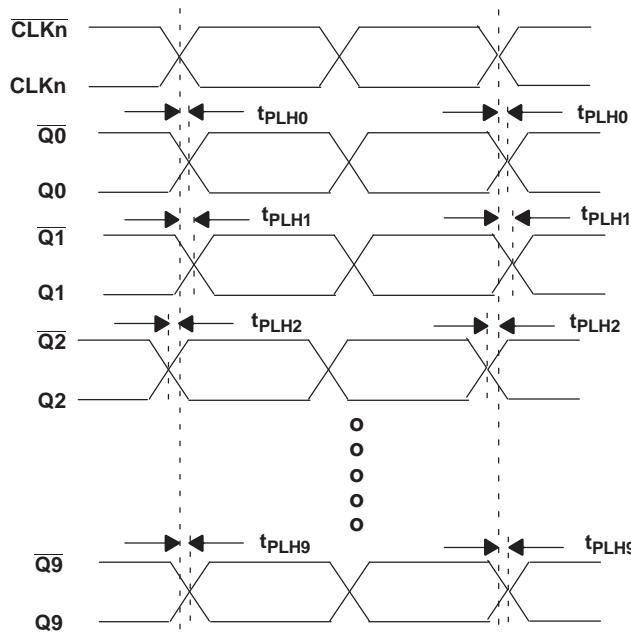
Vsupply: $V_{CC} = 2.375\text{ V to }3.8\text{ V}$, $V_{EE} = 0\text{ V}$ or LVECL/LVPECL input $V_{CC} = 0\text{ V}$, $V_{EE} = -2.375\text{ V to }-3.8\text{ V}$

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|----------------|---|--|-------------------|-----|-----|------|------|
| t_{pd} | Differential propagation delay CLK0, CLK0 to all Q0, Q0... Q9, Q9 | Input condition: $V_{CM} = 1\text{ V}$, $V_{PP} = 0.5\text{ V}$ | -40°C, 25°C, 85°C | 230 | | 350 | ps |
| $t_{sk(pp)}$ | Part-to-part skew | See Note B and Figure 1 | -40°C, 25°C, 85°C | | | 70 | ps |
| $t_{sk(o)}$ | Output-to-output skew | See Note A and Figure 1 | -40°C, 25°C, 85°C | | 15 | 30 | ps |
| $t_{(JITTER)}$ | Cycle-to-cycle RMS jitter | | -40°C, 25°C, 85°C | | | < 1 | ps |
| $f_{(max)}$ | Maximum frequency | Functional up to 3.5 GHz, timing specifications apply at 1 GHz, see Figure 3 | -40°C, 25°C, 85°C | | | 3500 | MHz |
| t_r/t_f | Output rise and fall time (20%, 80%) | | -40°C, 25°C, 85°C | 100 | | 200 | ps |

HSTL INPUT

Vsupply: $V_{CC} = 2.375\text{ V to }3.8\text{ V}$, $V_{EE} = 0\text{ V}$

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|----------------|---|--|-------------------|-----|-----|------|------|
| t_{pd} | Differential propagation delay CLK0, CLK0 to all Q0, Q0... Q9, Q9 | Input condition: $V_x = 0.68\text{ V}$, $V_{dif} = 0.4\text{ V}$ | -40°C, 25°C, 85°C | 290 | | 370 | ps |
| $t_{sk(pp)}$ | Part-to-part skew | See Note B and Figure 1 | -40°C, 25°C, 85°C | | | 70 | ps |
| $t_{sk(o)}$ | Output to output skew | See Note A and Figure 1 | -40°C, 25°C, 85°C | | 10 | 30 | ps |
| $t_{(JITTER)}$ | Cycle-to-cycle RMS jitter | | -40°C, 25°C, 85°C | | | < 1 | ps |
| $f_{(max)}$ | Maximum frequency | Functional up to 3.5 GHz, timing specifications apply at 1 GHz, See Figure 4 | -40°C, 25°C, 85°C | | | 3500 | MHz |
| t_r/t_f | Output rise and fall time (20%, 80%) | | -40°C, 25°C, 85°C | 100 | | 200 | ps |



- A. Output skew is calculated as the greater of: The difference between the fastest and the slowest t_{PLHn} ($n = 0, 1, \dots, 9$) or the difference between the fastest and the slowest t_{PHLn} ($n = 0, 1, \dots, 9$).
- B. Part-to-part skew, is calculated as the greater of: The difference between the fastest and the slowest t_{PLHn} ($n = 0, 1, \dots, 9$) across multiple devices or the difference between the fastest and the slowest t_{PHLn} ($n = 0, 1, \dots, 9$) across multiple devices.

Figure 1. Waveform for Calculating Both Output and Part-to-Part Skew

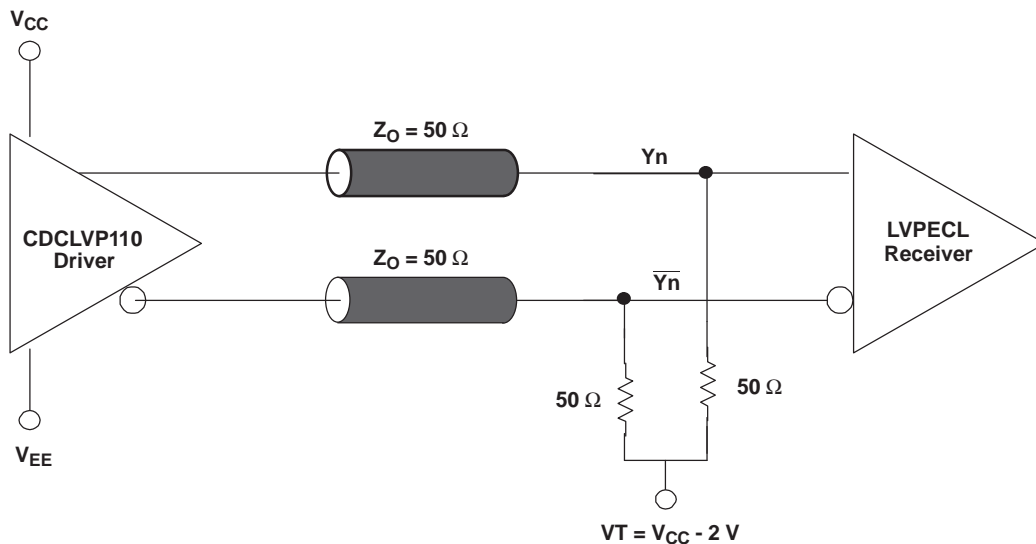


Figure 2. Typical Termination for Output Driver (See the Interfacing Between LVPECL, LVDS, and CML Application Note, Literature Number SCAA056)

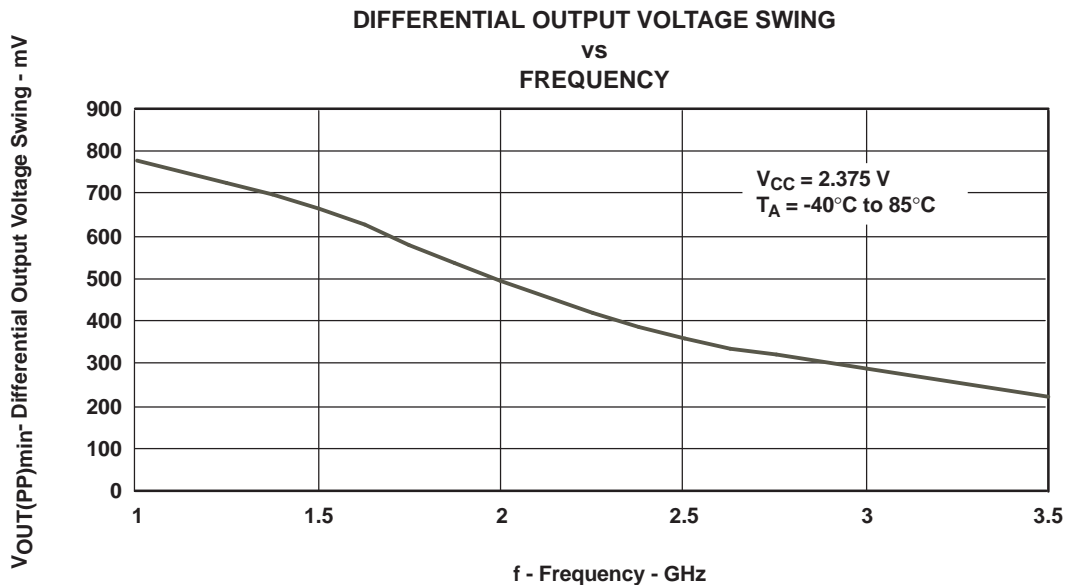


Figure 3. LVPECL Input Using CLK0 Pair, VCM = 1 V, VIN_{diff} = 0.5 V

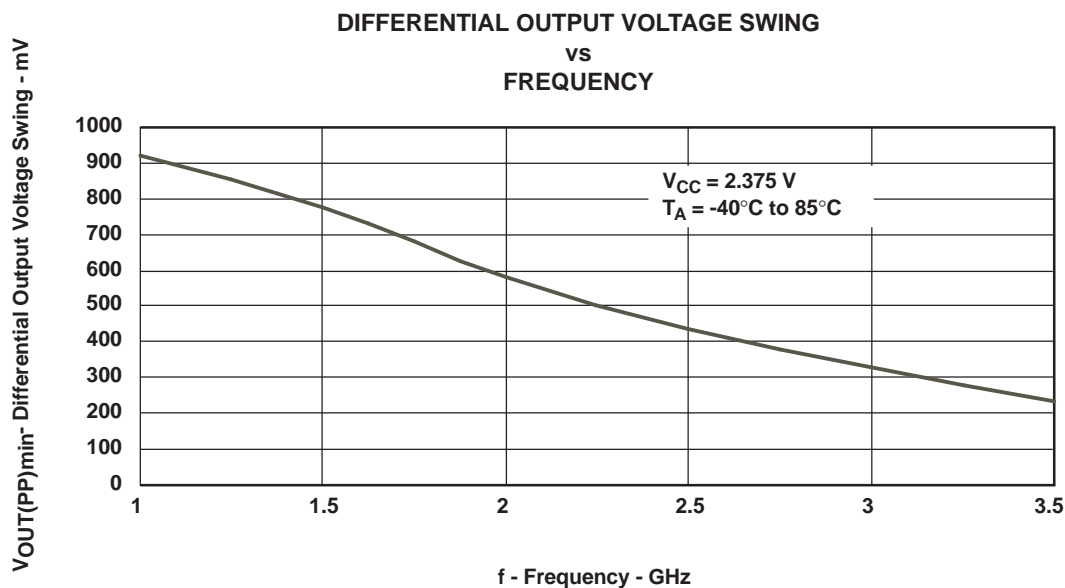


Figure 4. HSTL Input Using CLK1 Pair, VCM = 0.68 V, VIN_{diff} = 0.4 V

REVISION HISTORY

| Changes from Revision A (August 2002) to Revision B | Page |
|--|-------------|
| • Changed PACKAGE THERMAL IMPEDANCE max values | 3 |
| • Deleted I_{IN} test condition | 3 |
| • Deleted I_{IN} test condition | 4 |
| Changes from Revision B (January 2010) to Revision C | Page |
| • Changed LVECL DC spec for V_{BB} ($V_{EE} = -3$ to -3.8 V) from 3 rows to 1 row and added TYP value. | 3 |
| • Changed LVECL DC spec for V_{BB} ($V_{EE} = -2.375$ to -2.75 V); MIN value from -1.38 V to -1.4 V, MAX from -1.16 V to -1.1 V, and added TYP value of -1.25 V | 3 |
| • Changed LVECL/HSTL DC spec for V_{BB} ($V_{EE} = -3$ to -3.8 V) from 3 rows to 1 row and added TYP value. | 4 |
| • Changed LVECL/HSTL DC spec for V_{BB} ($V_{EE} = -2.375$ to -2.75 V); MIN value from $V_{CC} -1.38$ V to $V_{CC} -1.4$ V; MAX from $V_{CC} -1.16$ V to $V_{CC} -1.1$ V; and added TYP value of $V_{CC} -1.25$ V | 4 |
| Changes from Revision C (January 2011) to Revision D | Page |
| • Changed V_{CM} spec from $V_{EE}+1$ to $V_{EE}+0.975$ | 3 |
| • Changed V_{IC} spec from 1 to 0.975 | 4 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| CDCLVP110MVFR | ACTIVE | LQFP | VF | 32 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CDCLVP110 | Samples |
| CDCLVP110MVFRG4 | ACTIVE | LQFP | VF | 32 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CDCLVP110 | Samples |
| CDCLVP110VF | ACTIVE | LQFP | VF | 32 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CDCLVP110 | Samples |
| CDCLVP110VFG4 | ACTIVE | LQFP | VF | 32 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CDCLVP110 | Samples |
| CDCLVP110VFR | ACTIVE | LQFP | VF | 32 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CDCLVP110 | Samples |
| CDCLVP110VFRG4 | ACTIVE | LQFP | VF | 32 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CDCLVP110 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CDCLVP110MVFR | LQFP | VF | 32 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.9 | 12.0 | 16.0 | Q1 |
| CDCLVP110VFR | LQFP | VF | 32 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.9 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

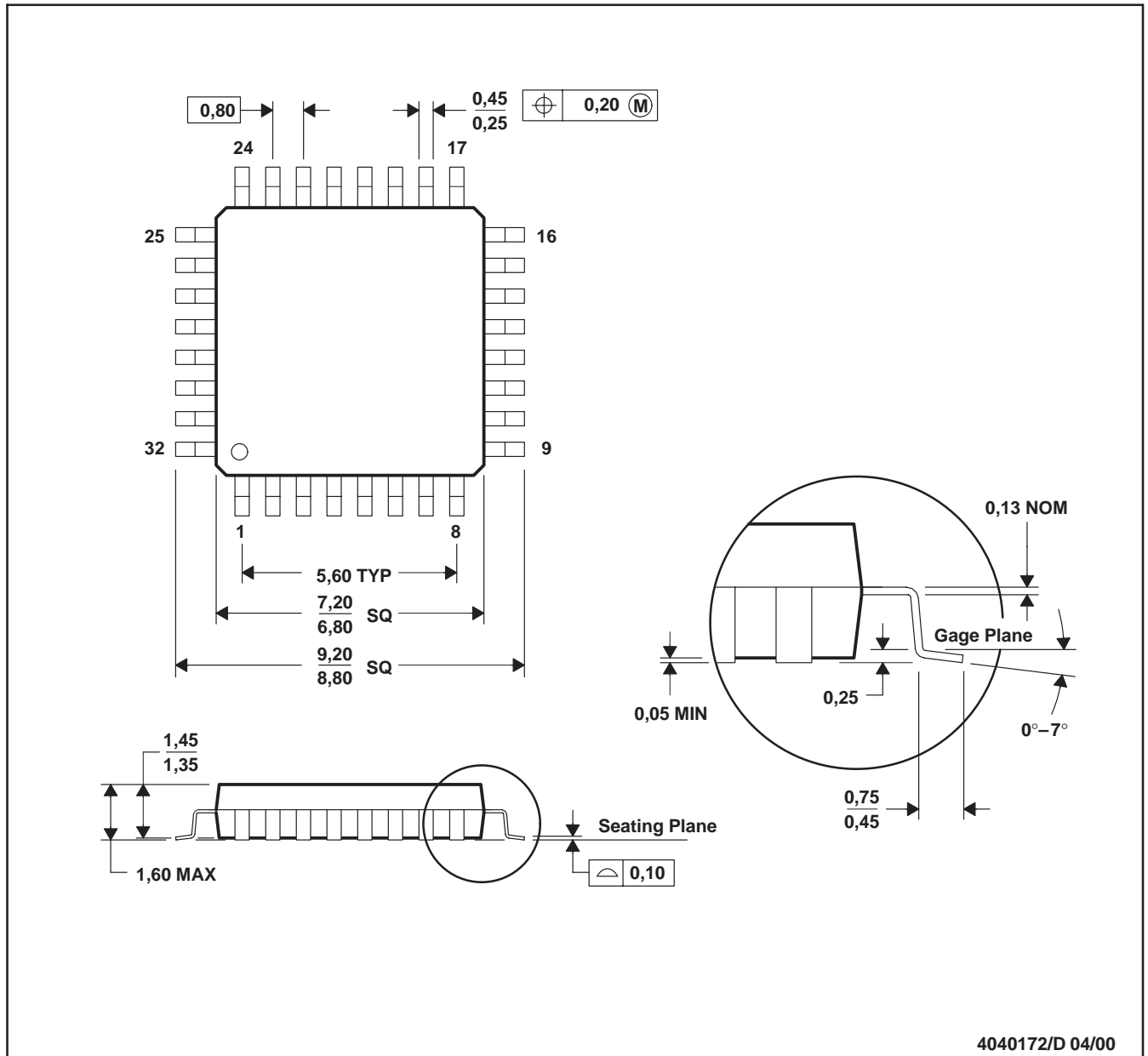


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CDCLVP110MVFR | LQFP | VF | 32 | 1000 | 341.0 | 159.0 | 123.5 |
| CDCLVP110VFR | LQFP | VF | 32 | 1000 | 367.0 | 367.0 | 38.0 |

VF (S-PQFP-G32)

PLASTIC QUAD FLATPACK



4040172/D 04/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.

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Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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