MJD200 (NPN), MJD210 (PNP)

Complementary Plastic Power Transistors

NPN/PNP Silicon DPAK For Surface Mount Applications

Designed for low voltage, low–power, high–gain audio amplifier applications.

Features

- High DC Current Gain
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Low Collector–Emitter Saturation Voltage
- High Current–Gain – Bandwidth Product
- Annular Construction for Low Leakage
- Epoxy Meets UL 94 V–0 @ 0.125 in
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q101 Qualified and PPAP Capable
- These Devices are Pb–Free and are RoHS Compliant

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector–Base Voltage	V_{CB}	40	Vdc
Collector–Emitter Voltage	V_{CEO}	25	Vdc
Emitter–Base Voltage	V_{EB}	8.0	Vdc
Collector Current – Continuous	I_C	5.0	Adc
Collector Current – Peak	I_{CM}	10	Adc
Base Current	I_B	1.0	Adc

Total Power Dissipation
    @ T_C = 25°C
    Derate above 25°C
	P_D	12.5
		0.1
			W
			W/°C

Total Power Dissipation (Note 1)
    @ T_A = 25°C
    Derate above 25°C
	P_D	1.4
		0.011
			W
			W/°C

Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C
ESD – Human Body Model	HBM	3B	V
ESD – Machine Model	MM	C	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
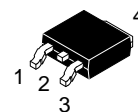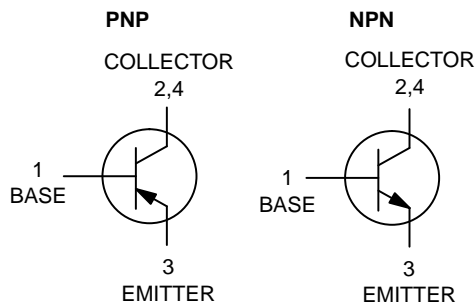
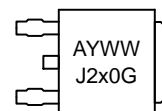1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

SILICON POWER TRANSISTORS
5 AMPERES
25 VOLTS, 12.5 WATTS

PNP
COLLECTOR 2,4
1 BASE
3 EMITTER

NPN
COLLECTOR 2,4
1 BASE
3 EMITTER

DPAK
CASE 369C
STYLE 1

MARKING DIAGRAM

AYWW
J2x0G

A	= Assembly Location
Y	= Year
WW	= Work Week
x	= 1 or 0
G	= Pb–Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	10	°C/W
Thermal Resistance, Junction−to−Ambient (Note 2)	$R_{\theta JA}$	89.3	°C/W

2. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 3) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	25	–	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 40 Vdc, I_E = 0, T_J = 125°C)	V_{CBO}	– –	100 100	nAdc μAdc
Emitter Cutoff Current (V_{BE} = 8 Vdc, I_C = 0)	V_{EBO}	–	100	nAdc
ON CHARACTERISTICS				
C Current Gain (Note 3), (I_C = 500 mAdc, V_{CE} = 1 Vdc) (I_C = 2 Adc, V_{CE} = 1 Vdc) (I_C = 5 Adc, V_{CE} = 2 Vdc)	h_{FE}	70 45 10	– 180 –	–
Collector−Emitter Saturation Voltage (Note 3) (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 2 Adc, I_B = 200 mAdc) (I_C = 5 Adc, I_B = 1 Adc)	$V_{CE(sat)}$	– – –	0.3 0.75 1.8	Vdc
Base−Emitter Saturation Voltage (Note 3) (I_C = 5 Adc, I_B = 1 Adc)	$V_{BE(sat)}$	–	2.5	Vdc
Base−Emitter On Voltage (Note 3) (I_C = 2 Adc, V_{CE} = 1 Vdc)	$V_{BE(on)}$	–	1.6	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain − Bandwidth Product (Note 4) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	65	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJD200 MJD210, NJVMJD210T4G	C_{ob}	 – –	 80 120	pF

3. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≈ 2%.
4. $f_T = |h_{fe}| \cdot f_{test}$.

MJD200 (NPN), MJD210 (PNP)

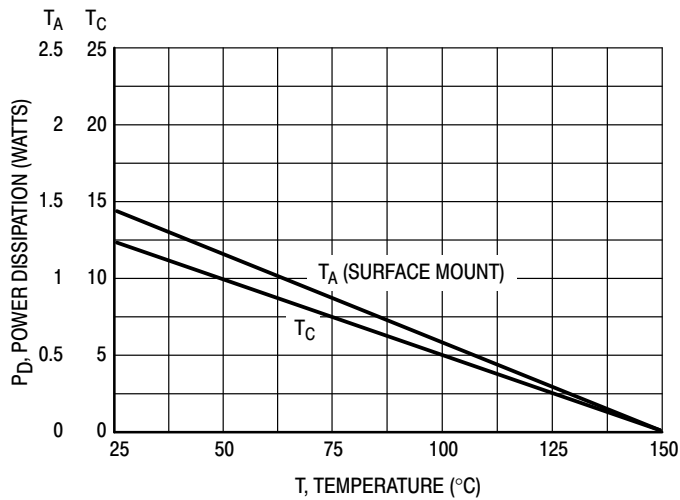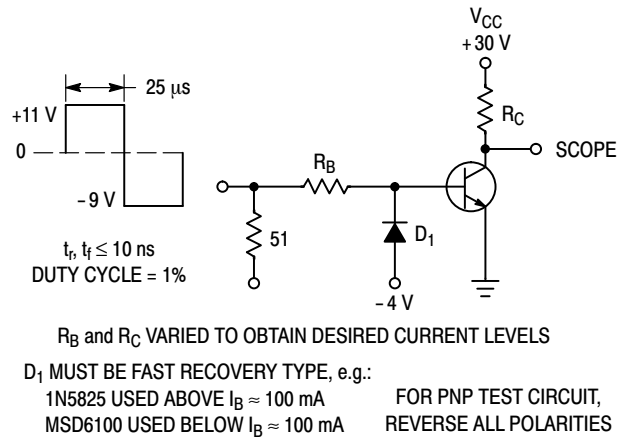**Figure 1. Power Derating**

$t_r, t_f \leq 10$ ns
DUTY CYCLE = 1%

R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, e.g.:
 1N5825 USED ABOVE $I_B \approx 100$ mA
 MSD6100 USED BELOW $I_B \approx 100$ mA

FOR PNP TEST CIRCUIT,
REVERSE ALL POLARITIES

Figure 2. Switching Time Test Circuit

$V_{CC} = 30$ V
$I_C/I_B = 10$
$T_J = 25°C$

MJD200 ———
MJD210 – – –

Figure 3. Turn–On Time

$V_{CC} = 30$ V
$I_C/I_B = 10$
$I_{B1} = I_{B2}$
$T_J = 25°C$
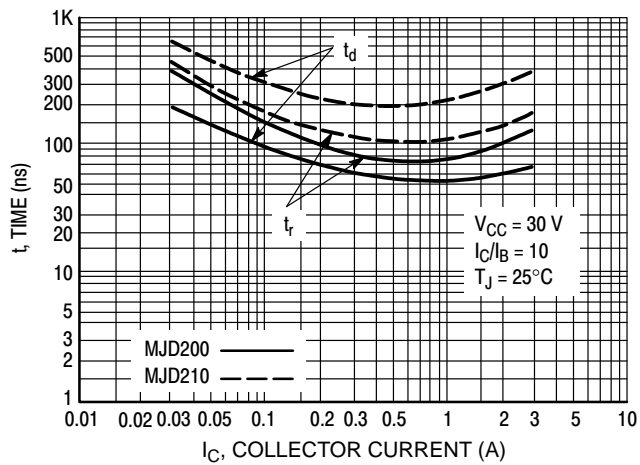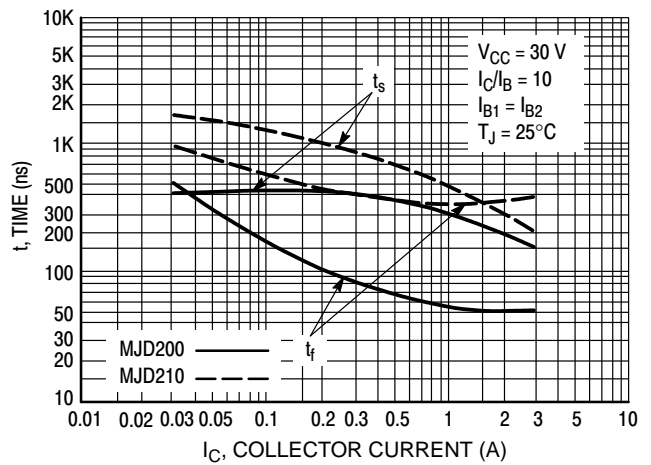
MJD200 ———
MJD210 – – –

Figure 4. Turn–Off Time

MJD200 (NPN), MJD210 (PNP)

NPN
MJD200

PNP
MJD210
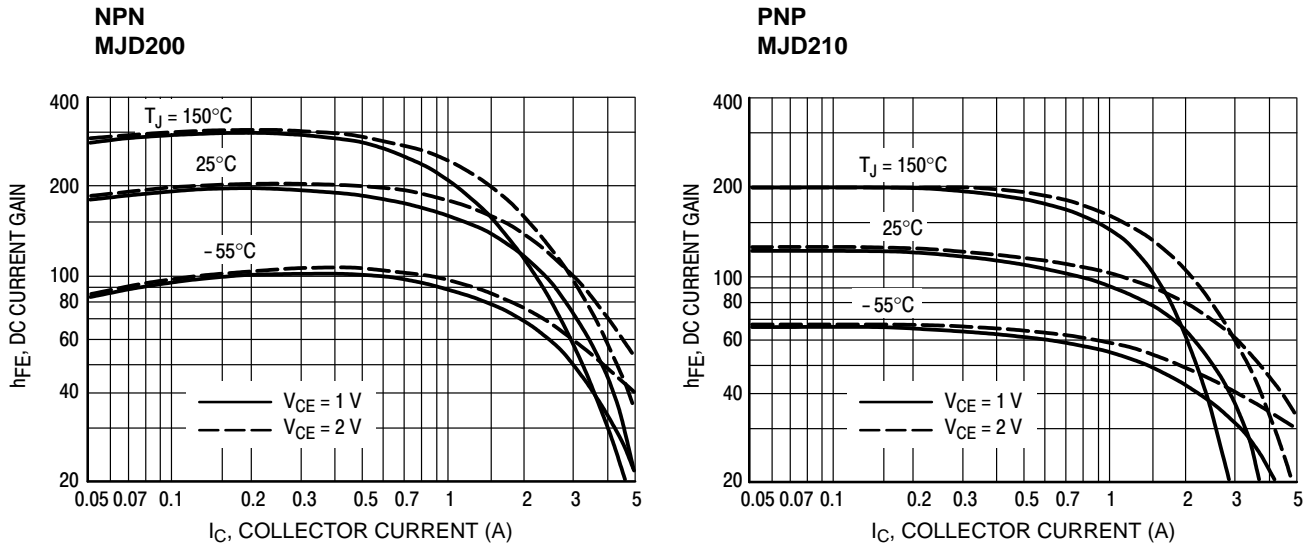
Figure 5. DC Current Gain
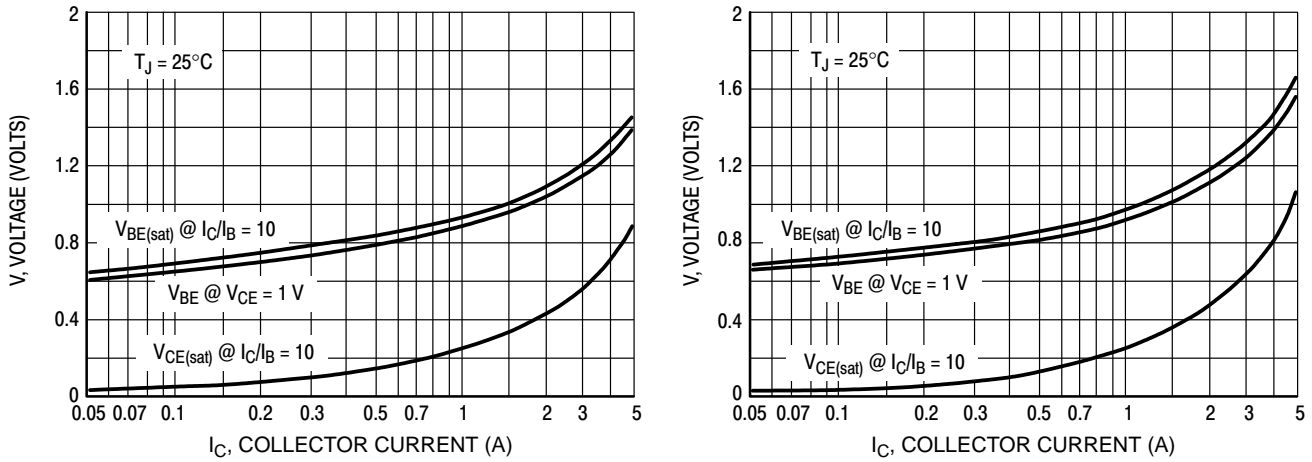
Figure 6. "On" Voltage
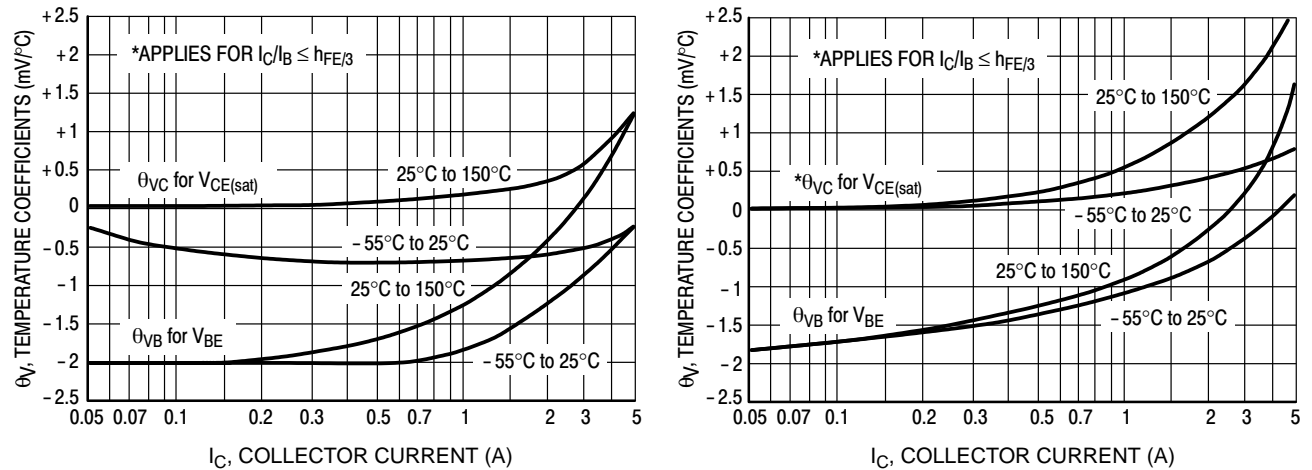
Figure 7. Temperature Coefficients

MJD200 (NPN), MJD210 (PNP)
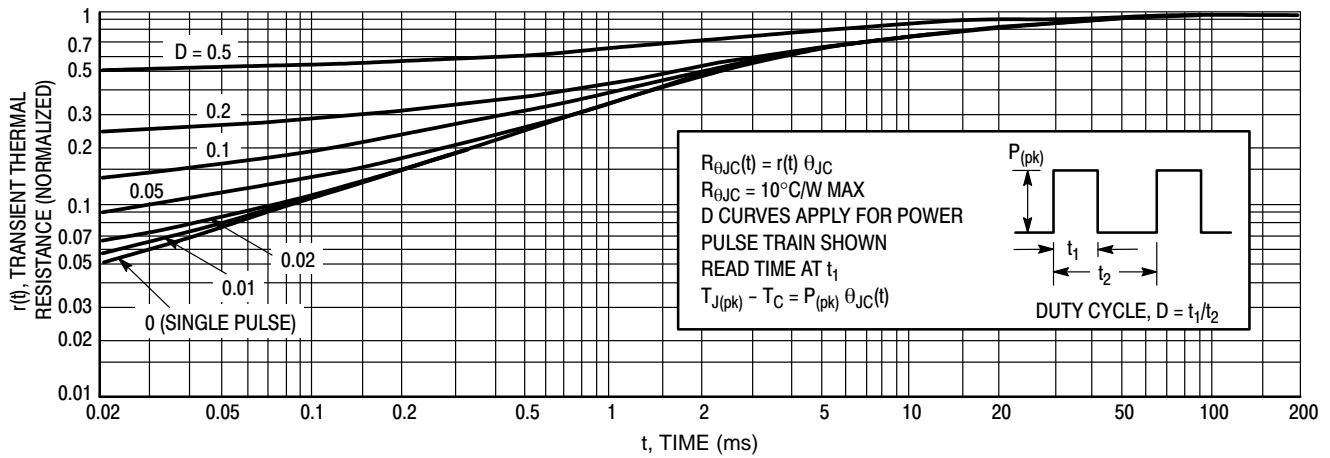
Figure 8. Thermal Response
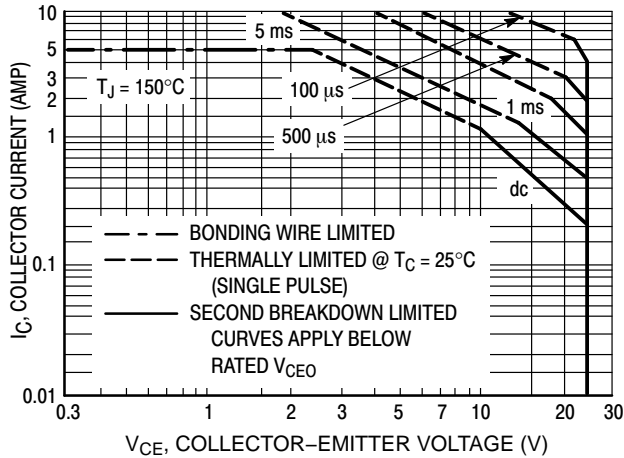
Figure 9. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 9 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 8. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.
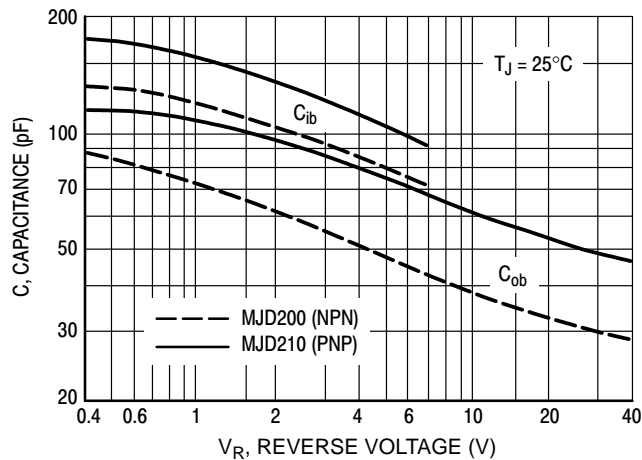
Figure 10. Capacitance

MJD200 (NPN), MJD210 (PNP)

ORDERING INFORMATION

Device	Package Type	Shipping†
MJD200G	DPAK (Pb−Free)	75 Units / Rail
MJD200RLG	DPAK (Pb−Free)	1,800 / Tape & Reel
MJD200T4G	DPAK (Pb−Free)	2,500 / Tape & Reel
MJD210G	DPAK (Pb−Free)	75 Units / Rail
MJD210RLG	DPAK (Pb−Free)	1,800 / Tape & Reel
MJD210T4G	DPAK (Pb−Free)	2,500 / Tape & Reel
NJVMJD210T4G*	DPAK (Pb−Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable

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PACKAGE DIMENSIONS

DPAK
CASE 369C
ISSUE D
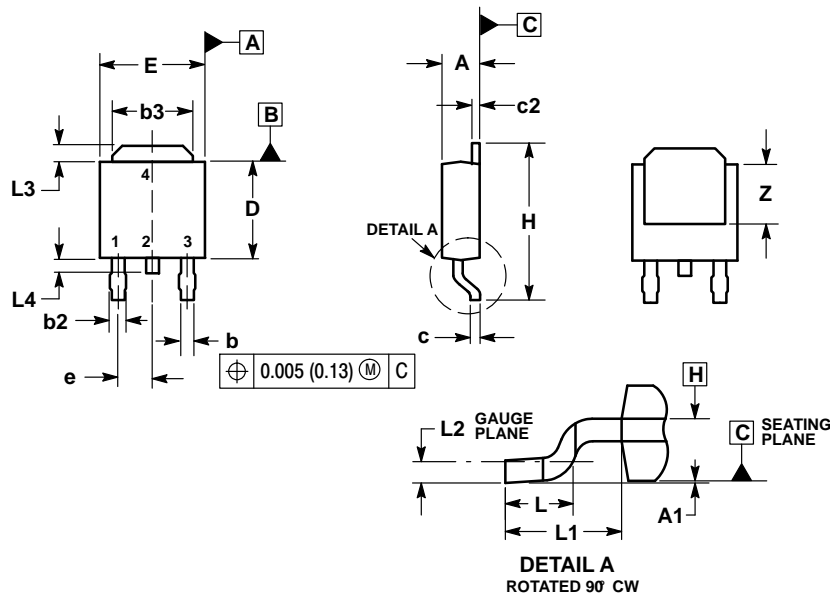
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

⊕ | 0.005 (0.13) Ⓜ | C

DETAIL A
ROTATED 90° CW

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	–––	0.040	–––	1.01
Z	0.155	–––	3.93	–––
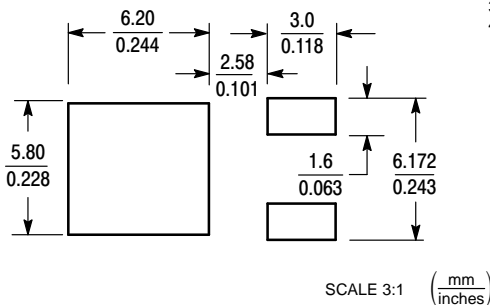
STYLE 1:
PIN 1. BASE
    2. COLLECTOR
    3. EMITTER
    4. COLLECTOR

SOLDERING FOOTPRINT*

$\frac{6.20}{0.244}$ $\frac{3.0}{0.118}$

$\frac{2.58}{0.101}$

$\frac{5.80}{0.228}$ $\frac{1.6}{0.063}$ $\frac{6.172}{0.243}$

SCALE 3:1 $\left(\frac{mm}{inches}\right)$

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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