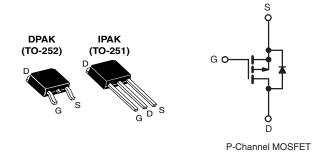


Vishay Siliconix

Power MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	- 50				
$R_{DS(on)}(\Omega)$	V _{GS} = - 10 V 0.28				
Q _g (Max.) (nC)	14				
Q _{gs} (nC)	6.5				
Q _{gd} (nC)	6.5				
Configuration	Single				



FEATURES

 Surface Mountable (Order As IRFR9020, SiHFR9020)



COMPLIANT

HALOGEN

FREE Available

 Straight Lead Option (Order As IRFU9020, SiHFU9020)

Repetitive Avalanche Ratings

Dynamic dV/dt Rating

Simple Drive Requirements

Ease of Paralleling

 Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

DESCRIPTION

The power MOSFET technology is the key to Vishay's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dV/dt.

The power MOSFET transistors also feature all of the well established advantages of MOSFET'S such as voltage control, very fast switching, ease of paralleling and

temperature stability of the electrical parameters. Surface mount packages enhance circuit performance by reducing stray inductances and capacitance. The TO-252 surface mount package brings the advantages of power MOSFET's to high volume applications where PC board surface mounting is desirable. The surface mount option IRFR9020, SiHFR9020 is provided on 16mm tape. The straight lead option IRFU9020, SiHFU9020 of the device is called the IRAK (TO 251) called the IPAK (TO-251).

They are well suited for applications where limited heat dissipation is required such as, computers and peripherals, telecommunication equipment, DC/DC converters, and a wide range of consumer products.

ORDERING INFORMATION							
Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)			
Lead (Pb)-free and Halogen-free	SiHFR9020-GE3	SiHFR9020TR-GE3a	SiHFR9020TRL-GE3a	SiHFU9020-GE3			
Lead (Pb)-free	IRFR9020PbF	IRFR9020TRPbFa	IRFR9020TRLPbFa	IRFU9020PbF			
Lead (PD)-lifee	SiHFR9020-E3	SiHFR9020T-E3a	SiHFR9020TL-E3a	SiHFU9020-E3			

Note

See device orientation.

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	LIMIT	UNIT				
Drain-Source Voltage			V_{DS}	- 50	V		
Gate-Source Voltage			V_{GS}	± 20	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \		
Continuous Drain Current	\/ ot 10.\/	$T_{\rm C} = 25 ^{\circ}{\rm C}$ $T_{\rm C} = 100 ^{\circ}{\rm C}$	-	- 9.9			
Continuous Drain Current	V _{GS} at - 10 V	T _C = 100 °C	I _D	- 6.3	Α		
Pulsed Drain Current ^a			I _{DM}	- 40			
Linear Derating Factor				0.33	W/°C		
Single Pulse Avalanche Energy ^b			E _{AS}	250	mJ		
Repetitive Avalanche Current ^a			I _{AR}	- 9.9	Α		
Repetitive Avalanche Energy ^a			E _{AR}	4.2	mJ		
Maximum Power Dissipation $T_C = 25 ^{\circ}C$			P_{D}	42	W		
Peak Diode Recovery dV/dt ^c			dV/dt	5.8	V/ns		
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	00		
Soldering Recommendations (Peak Temperature) ^d for 10 s			•	300	°C		

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 16). b. $V_{DD} = -25$ V, Starting $T_J = 25$ °C, L = 5.1 mH, $R_g = 25 \Omega$, Peak $I_L = -9.9$ A c. $I_{SD} \le -9.9$ A, $dI/dt \le -120$ A/µs, $V_{DD} \le 40$ V, $T_J \le 150$ °C. d. 0.063" (1.6 mm) from case.

- When mounted on 1" square PCB (FR-4 or G-10 material).



IRFR9020, IRFU9020, SiHFR9020, SiHFU9020

Vishay Siliconix

THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R _{thJA}	-	-	110		
Case-to-Sink	R _{thCS}	-	1.7	-	°C/W	
Maximum Junction-to-Case (Drain)	R _{4b,10}	_	_	3.0		

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static		•			L	L	
Drain-Source Breakdown Voltage	V _{DS}	V _G	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$		-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS}	_S = V _{GS} , I _D = - 250 μA	- 2.0	-	- 4.0	V
Gate-Source Leakage	I _{GSS}		V _{GS} = ± 20 V	-	-	± 500	nA
Zava Cata Valtaga Dvain Cuwant		V _{DS} =	max. rating, V _{GS} = 0 V	-	-	250	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 0.8 \text{ x m}$	ax. rating, V _{GS} = 0 V, T _J = 125 °C	-	-	1000	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = - 10 V	I _D = 5.7 A ^b	-	0.20	0.28	Ω
Forward Transconductance	9 _{fs}	V _{DS}	≤ - 50 V, I _{DS} = - 5.7 A	2.3	3.5	-	S
Dynamic							
Input Capacitance	C _{iss}		$V_{GS} = 0 V$	-	490	-	
Output Capacitance	C _{oss}		$V_{DS} = -25 V$,	-	320	-	pF
Reverse Transfer Capacitance	C _{rss}	f =	f = 1.0 MHz, see fig. 9		70	-	
Total Gate Charge	Qg	$I_D = -9.7 \text{ A}, V_{DS} = 0.8 \text{ x max}.$		-	9.4	14	nC
Gate-Source Charge	Q _{gs}	V _{GS} = - 10 V	V _{GS} = -10 V rating, see fig. 18		4.3	6.5	
Gate-Drain Charge	Q _{gd}	(Independent operating temperature)		-	4.3	6.5	
Turn-On Delay Time	t _{d(on)}			-	8.2	12	ns
Rise Time	t _r		$V_{DD} = -25 \text{ V}, I_D = -9.7 \text{ A},$		57	66	
Turn-Off Delay Time	t _{d(off)}	$R_g = 18 \Omega$, $R_D = 2.4 \Omega$, see fig. 17 (Independent operating temperature)		-	12	18	
Fall Time	t _f			-	25	38	
Internal Drain Inductance	L _D	Between lead,		-	4.5	-	
Internal Source Inductance	L _S	package an	6 mm (0.25") from package and center of die contact.		7.5	-	nH
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	Is	,	MOSFET symbol		-	- 9.9	
Pulsed Diode Forward Current ^a	I _{SM}	showing the integral reverse p - n junction diode		-	-	- 40	А
Body Diode Voltage	V _{SD}	T _J = 25 °	°C, I _S = - 9.9 A, V _{GS} = 0 V ^b	-	-	- 6.3	V
Body Diode Reverse Recovery Time	t _{rr}	T 05.00	I 07 A dl/d± 400 A/ -b	56	110	280	ns
Body Diode Reverse Recovery Charge	Q _{rr}	$T_J = 25 ^{\circ}\text{C}, I_F = -9.7 \text{A}, \text{dI/dt} = 100 \text{A/}\mu\text{s}^b$		0.17	0.34	0.85	nC
Forward Turn-On Time	t _{on}	Intrinsic	turn-on time is negligible (turn-	on is don	ninated b	y L _S and	L _D)

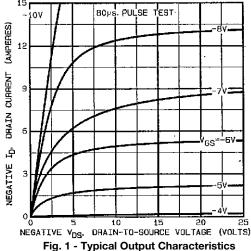
Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 16).

b. Pulse width \leq 300 µs; duty cycle \leq 2 %.

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





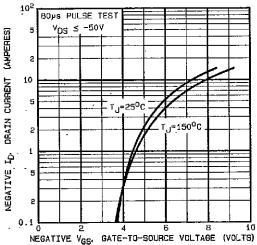
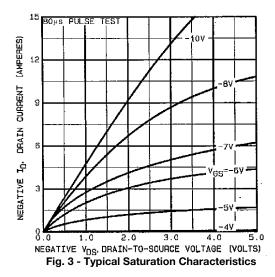
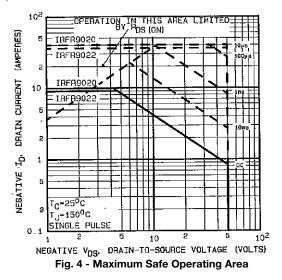


Fig. 2 - Typical Transfer Characteristics





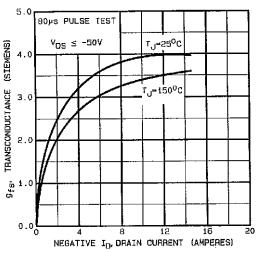


Fig. 5 - Typical Transconductance vs. Drain Current

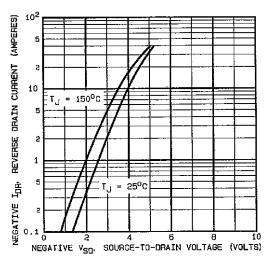


Fig. 6 - Typical Source-Drain Diode Forward Voltage

1000

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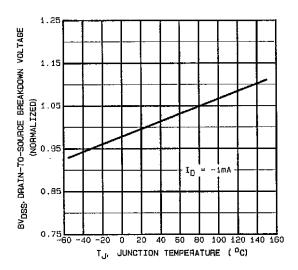
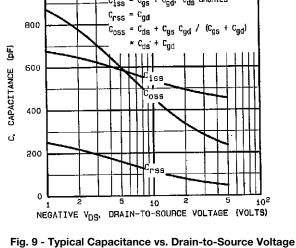


Fig. 7 - Breakdown Voltage vs. Temperature



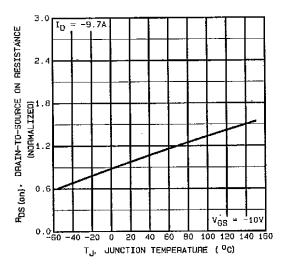


Fig. 8 - Normalized On-Resistance vs. Temperature

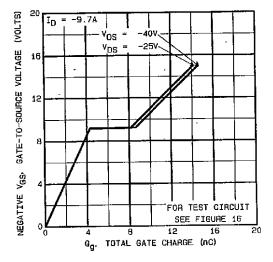


Fig. 10 - Typical Gate Charge vs. Gate-to-Source Voltage

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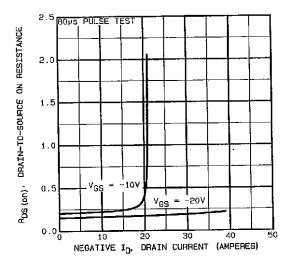


Fig. 11 - Typical On-Resistance vs. Drain Current

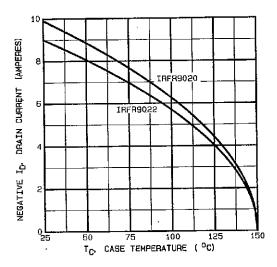


Fig. 12 - Maximum Drain Current vs. Case Temperature

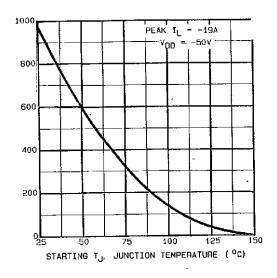


Fig. 13 - Maximum Avalanche vs. Starting Junction Temperature

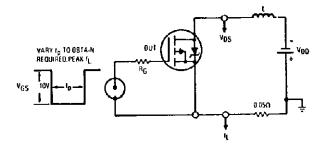


Fig. 14 - Unclamped Inductive Test Circuit

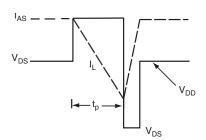


Fig. 15 - Unclamped Inductive Waveforms



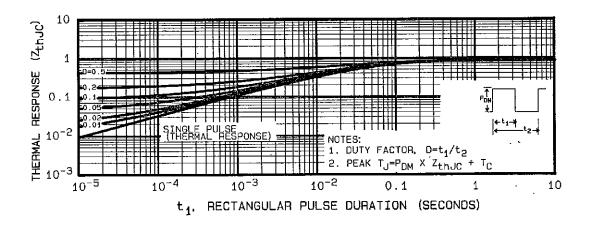


Fig. 16 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration

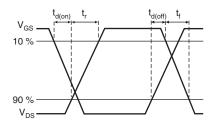


Fig. 17 - Switching Time Waveforms

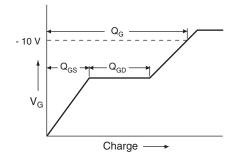


Fig. 19 - Basic Gate Charge Waveform

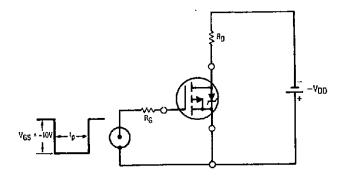


Fig. 18 - Switching Time Test Circuit

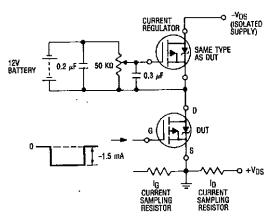
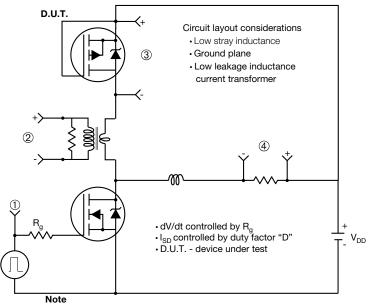


Fig. 20 - Gate Charge Test Circuit

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Peak Diode Recovery dV/dt Test Circuit



· Compliment N-Channel of D.U.T. for driver

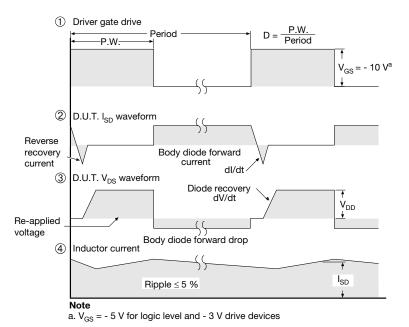
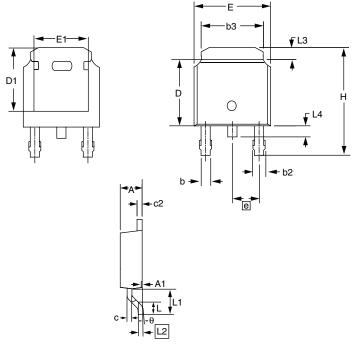


Fig. 21 - For P-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?90350.



TO-252AA (HIGH VOLTAGE)



MILLIMETERS		METERS	INC	HES	
DIM.	MIN.	MAX.	MIN.	MAX.	
Е	6.40	6.73	0.252	0.265	
L	1.40	1.77	0.055	0.070	
L1	2.74	3 REF	0.108	REF	
L2	0.50	8 BSC	0.020) BSC	
L3	0.89	1.27	0.035	0.050	
L4	0.64	1.01	0.025	0.040	
D	6.00	6.22	0.236	0.245	
Н	9.40	10.40	0.370	0.409	
b	0.64	0.88	0.025	0.035	
b2	0.77	1.14	0.030	0.045	
b3	5.21	5.46	0.205	0.215	
е	2.28	2.286 BSC		0.090 BSC	
Α	2.20	2.38	0.087	0.094	
A1	0.00	0.13	0.000	0.005	
С	0.45	0.60	0.018	0.024	
c2	0.45	0.58	0.018	0.023	
D1	5.30	-	0.209	-	
E1	4.40	-	0.173	-	
θ	0'	10'	0'	10'	

ECN: S-81965-Rev. A, 15-Sep-08

DWG: 5973

Notes

- 1. Package body sizes exclude mold flash, protrusion or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 0.10 mm per side.
- 2. Package body sizes determined at the outermost extremes of the plastic body exclusive of mold flash, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
- 3. The package top may be smaller than the package bottom.
- 4. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10 mm total in excess of "b" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.

Document Number: 91344 www.vishay.com Revision: 15-Sep-08



TO-251AA (HIGH VOLTAGE)



Section B - B and C - C

	MILLIN	METERS	INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.
Α	2.18	2.39	0.086	0.094
A1	0.89	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b1	0.65	0.79	0.026	0.031
b2	0.76	1.14	0.030	0.045
b3	0.76	1.04	0.030	0.041
b4	4.95	5.46	0.195	0.215
С	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.86	0.018	0.034
D	5.97	6.22	0.235	0.245

	MILLIN	IETERS	INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.
D1	5.21	-	0.205	-
Е	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
е	2.29	2.29 BSC		BSC
L	8.89	9.65	0.350	0.380
L1	1.91	2.29	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.14	1.52	0.045	0.060
θ1	0'	15'	0'	15'
θ2	25'	35'	25'	35'

ECN: S-82111-Rev. A, 15-Sep-08

DWG: 5968

Notes

- 1. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 2. Dimension are shown in inches and millimeters.
- 3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
- 4. Thermal pad contour optional with dimensions b4, L2, E1 and D1.
- 5. Lead dimension uncontrolled in L3.
- 6. Dimension b1, b3 and c1 apply to base metal only.
- 7. Outline conforms to JEDEC outline TO-251AA.

Document Number: 91362 Revision: 15-Sep-08



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index

APPLICATION NOTE



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Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.

Revision: 02-Oct-12 Document Number: 91000

AMEYA360 Components Supply Platform

Authorized Distribution Brand:

























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