Secondary power supply series for automotive

2.69 to 5.5V, 1.2V Output, 2.25MHz Synchronous Step-Down Converter

BD90571EFJ-C

●General Description

The BD90571EFJ-C is a synchronous rectification type step-down DC/DC converter with a 2.25MHz fixed frequency that operates in with an input voltage range of 2.69V-5.5V. It has an integrated feedback resistor that supplies a fixed output voltage of 1.2V and a phase compensation constant. Applications can be created with a minimum of three external components. Moreover, the integrated Pch and Nch output MOSFET can supply a maximum output current of 1A.

●Features

- Thanks to the integrated output feedback resistor and phase compensation, applications can be created with a minimum of external components
- Excellent load response through current mode control
- Integrated Pch and Nch output MOSFET
- Integrated overcurrent protection with auto-reset
- Integrated output overvoltage detection/ short-circuit detection
- Integrated TSD and UVLO
- Light load mode/PWM fixation operation selection terminal

●Applications

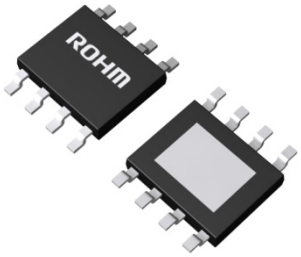
- Automotive equipment
- Car audio and navigation
- TV
- Other electronic equipment

●Key Specifications

■ Input voltage range	2.69V～5.5[V]
■ Output voltage	1.2 [V] (Typ.)
■ Output voltage accuracy	±2.0[%](-40～+125°C)
■ Operating frequency	2.25 [MHz] (Typ.)
■ Maximum output current	1.0 [A] (Max.)
■ Circuit current at standby	0[μA](Typ., 25°C)
■ Operational temperature range	-40～+125[°C]

●Package

HTSOP-J8 4.90 ㎜×6.00 ㎜×1.00 ㎜



●Typical application circuit

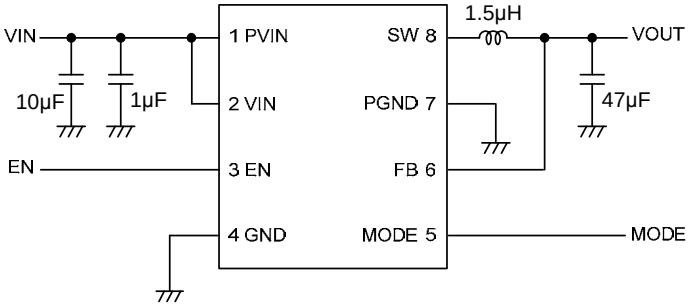


Figure 1. Typical application circuit
(VIN=5V, VOUT=1.2V, IOUT=1A)

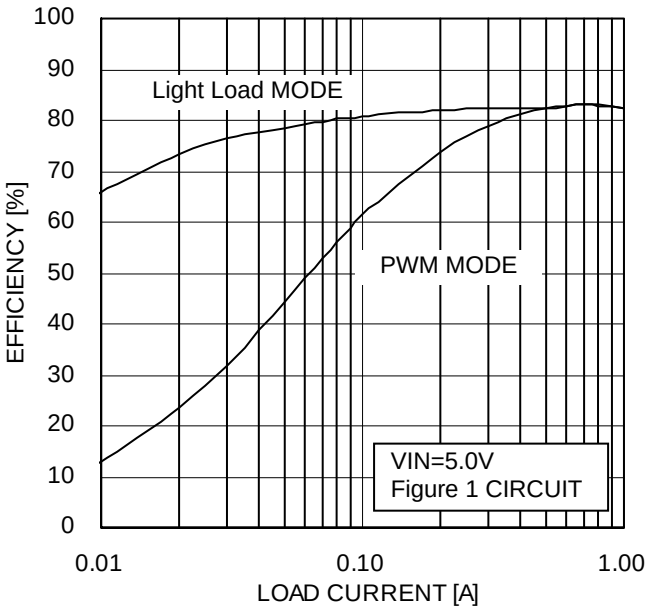


Figure 2. Efficiency(VIN=5V)

●Pin Configuration [TOP VIEW]

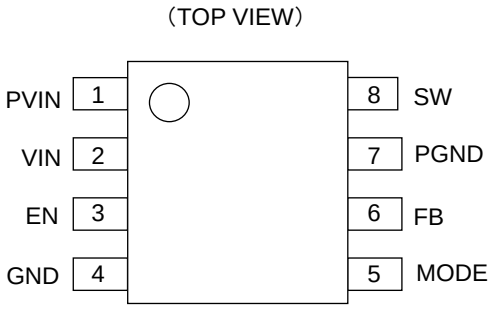


Figure 3. Pin arrangement diagram

●Pin Description

Pin	Symbol	Function
1	PVIN	Power supply pin for output FET
2	VIN	Power supply pin
3	EN	Enable pin
4	GND	GND pin
5	MODE	Light load mode/Fixed PWM mode select pin
6	FB	Output feedback pin
7	PGND	GND pin for output FET
8	SW	SW pin

●Block diagram

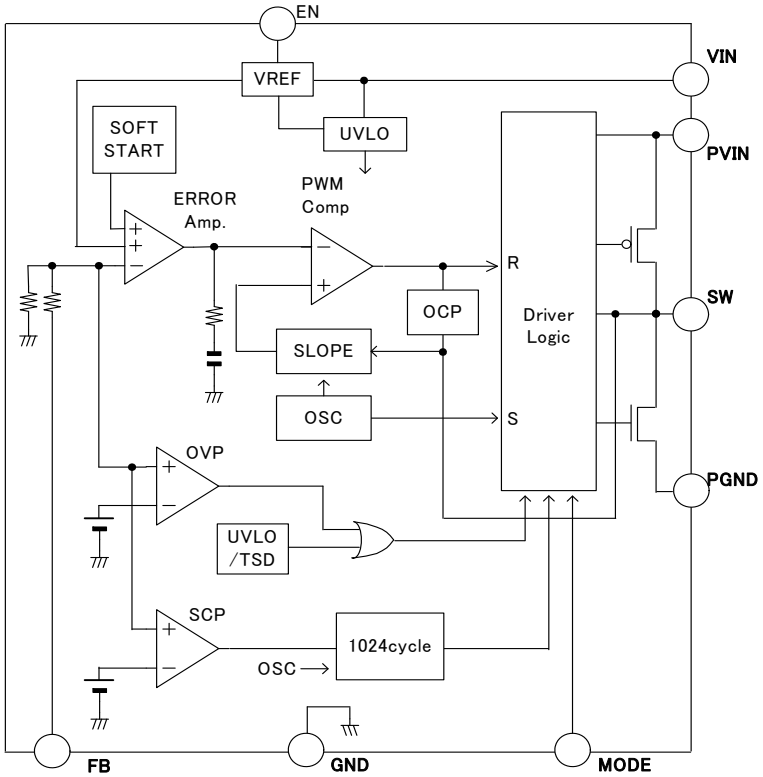


Figure 4. Block diagram

●Block operation descriptions

■ Standby
The circuit enters the state of standby when the terminal EN is set to 0.7V or less. All the circuits, such as internal reference voltage VREF, oscillators OSC, and drivers are turned off during standby, and current consumption of the power supply becomes 0μA(25℃, Typ.). Via the FB terminal, the output capacitor is discharged at a resistance of 1kΩ.

■ Start operation
The circuit starts operating when terminal EN is set to 2.1V or more. A soft start circuit (SOFT START) is integrated to prevent inrush current to the capacitor when starting. The output voltage reaches a set voltage with 1ms(Typ.) while following the startup of the soft start circuit. There is a delay of about 200μsec up to the beginning of soft start after the terminal EN is turned on and the internal logic operation is started. In order to prevent a defective start, the short-circuit protection is not active during startup.

■ Error amplifier and phase compensation
The voltage of the output feedback terminal (FB) is compared with an internal reference voltage, the voltage corresponding to the difference is generated, and send to the PWM comparator which determines the duty ratio of the output. The feedback resistor which determines the output voltage, resistance for compensations, and the capacitor are integrated into the BD90571EFJ-C.

■ Oscillator
The 2.25MHz(Typ.) internally fixed clock is generated and send to the slope generation circuit (SLOPE) and to the driver.

■ Light load mode and PWM fixation mode
BD90571EFJ-C operates in the light load mode when the terminal MODE is set to 0.7V or less. When the output load current is small, the switching operation automatically becomes intermittent in the light load mode. The efficiency at light load improves compared to the PWM fixation mode because the switching loss is suppressed by operating intermittently. The intermittently operating load current level changes depending on the input voltage, inductor value, etc.
If the terminal MODE is set to 2.1V or more the chip operates in PWM fixation mode. In the PWM fixation mode, the efficiency at a light load decreases compared with the light load mode. However, because of the fixed frequency switching through the entire load range, noise is more easily countered.

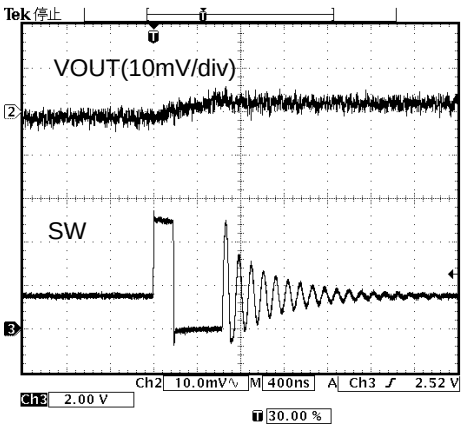


Figure 5. Switching operation at light load mode

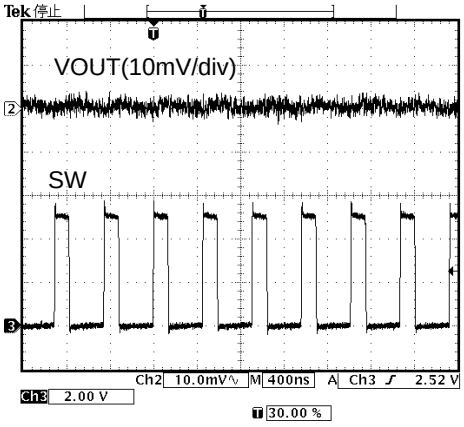


Figure 6. Switching operation at PWM mode

■ Overcurrent detection
When in the output stage the current flowing to the Pch FET is 1.0A(Min.) or more, the Pch FET is turned off and the power supply to the output is intercepted. The overcurrent detection is operated every cycle, limits the switching duty, and returns at the next clock cycle.

■ Output short-circuit detection
The output short-circuit detection circuit (SCP) detects a short-circuit of the output when output voltage falls below 70% of a set value during 1024 cycles of the frequency. In this case, the Pch FET and Nch FET of the output are turned off, and the power supply is intercepted. The count is reset when the output voltage returns to 70% or more before 1024 cycles, and the output voltage returns to the set value.
Ths SCP automatically resets when after 1024 cycles of the frequency after detecting the short-circuit, and switching is restarted. Resetting triggers the soft start operation because the internal soft start circuit is initialized when the short-circuit detection is activated. The short-circuit detection circuit is not active while soft start is starting. In case the short-circuit continues after resetting, the cycle of starting with a soft start, turning off the output after 1024 cycles, and returning after 1024 cycles is repeated.

■ Output overvoltage detection
When the output overvoltage detection circuit (OVP) detects that the output voltage is exceeding 120% of a set value, the Pch FET and Nch FET of the output are turned off and the power supply is intercepted. Switching is restarted if after the power supply interception the output decreases and the overvoltage situation is released. The overvoltage detection voltage and the release voltage have a hysteresis of about 100mV.

■ UVLO
The UVLO circuit is activated and shuts down the circuit when the input voltage (VIN) decreases to 2.6V or less. When the UVLO is activated, the control circuit of the error amplifier, the oscillator, the driver and, the output is turned off. Via the FB terminal, the output capacitor is discharged at a resistance of 1kohm. Afterwards, UVLO is released when the input voltage VIN rises to 2.69V or more, and the output is restored. The output voltage starts with soft start when UVLO is reset.

■ Thermal shutdown(TSD)
Thermal shutdown (TSD) is activated when the IC junction part temperature exceeds 175 ℃(Typ.). When the TSD is activated the control circuit of the error amplifier, the oscillator, the driver, and the output is turned off. There is hysteresis in the detection temperature of TSD, which is reset when the junction temperature decreases to 150℃(Typ.) or less. The output voltage starts with soft start when TSD is reset.

●Absolute maximum rating

Parameter	Symbol	Rating	Unit
VIN voltage	VIN	-0.3～7 *1	V
PVIN voltage	PVIN	-0.3～7 *1	V
EN voltage	EN	-0.3～7	V
SW voltage	SW	-1.0～PVIN *1	V
FB voltage	FB	-0.3～7	V
MODE voltage	MODE	-0.3～7	V
Power dissipation	Pd	3.75 *2	W
Operating temperature range	Topr	-40～+125	℃
Storage temperature range	Tstg	-55～+150	℃
Junction temperature	Tj	+150	℃

*1 Pd should not be exceeded.
*2 33.3mW/°C reduction when Ta≧25°C if mounted on 4 layers glass epoxy board of 70mm×70mm×1.6mm

●Recommended operating range (Ta=-40~+125°C)

Parameter	Symbol	Operating Range	Unit
VIN voltage	VVIN	2.69～5.5	V
PVIN voltage	VPVIN	2.69～5.5	V
EN voltage	VEN	0～5.5(*1)	V
MODE voltage	VMODE	0～5.5	V
Output current	ISW	0～1	A

*1 The circuit goes into test mode when the terminal EN is set at 6V or higher.

●Electrical characteristics (unless otherwise specified: Ta=-40~+125°C, VIN=PVIN=5V, EN=3.3V)

Parameter	Symbol	Guaranteed Limit			Unit	Conditions
		Min.	Typ.	Max.		
Standby circuit current	IST	-	0	1	μA	EN=0V, Ta=25℃
Circuit current	ICC	-	650	1300	μA	FB=1.3V, Ta=25℃
UVLO detection voltage	VUVLO1	2.30	2.45	2.60	V	Sweep down
UVLO release voltage	VUVLO2	2.40	2.55	2.69	V	Sweep up
EN threshold voltage	VEN	0.7	1.4	2.1	V	
EN inflow current	IEN	0.8	1.4	2	μA	EN=3.3V
Operating frequency	FOSC	1.8	2.25	2.7	MHz	
Output voltage	VFB	1.176	1.20	1.224	V	Io=0mA
FB pull-down resistance	RFB	0.4	1	2	MΩ	FB=1.2V
Soft start time	TSS	0.4	1	2	ms	
Pch FET ON resistance	PRON	-	85	-	mΩ	
Nch FET ON resistance	NRON	-	70	-	mΩ	
Overcurrent detection current	IOCP	-	2.5	-	A	
Output overvoltage detection voltage	VOVP	1.3	1.45	1.6	V	
Output short-circuit detection voltage	VSCP	0.7	0.85	1.0	V	
MODE threshold voltage	VMODE	0.9	1.6	2.3	V	
MODE inflow current	IMODE	3.5	7	14	μA	MODE=3.3V

●Typical Performance Curve

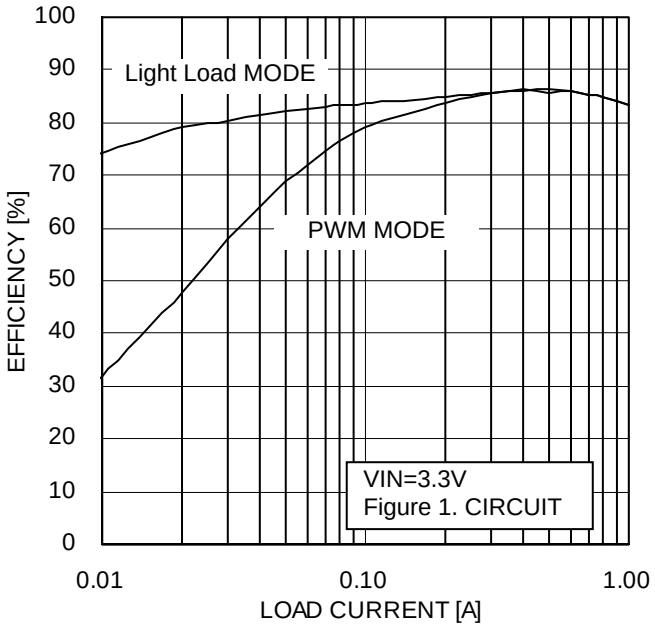


Figure 7. Efficiency (VIN=3.3V)

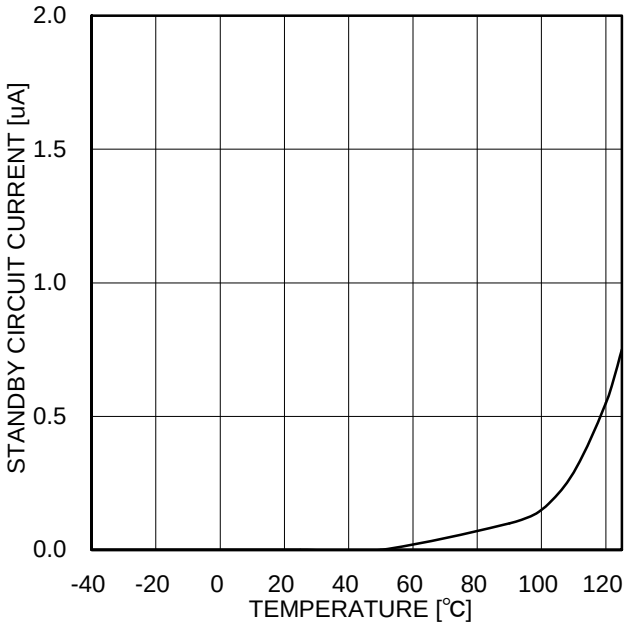


Figure 8. Standby circuit current

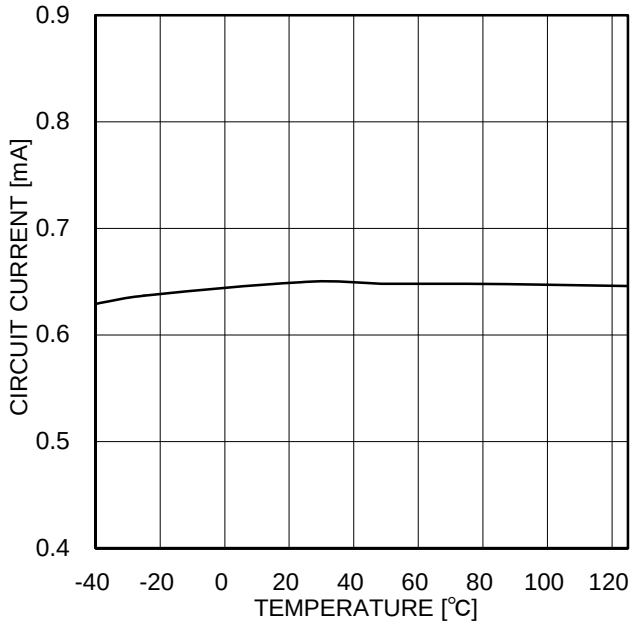


Figure 9. Circuit Current

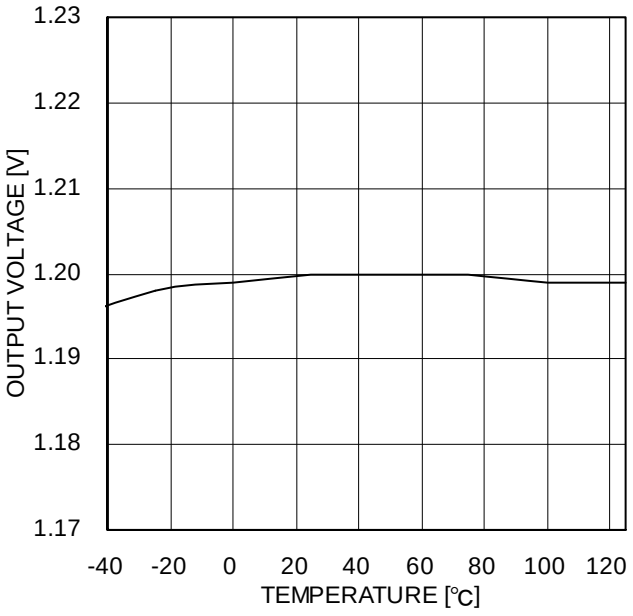


Figure 10. Output voltage vs. temperature

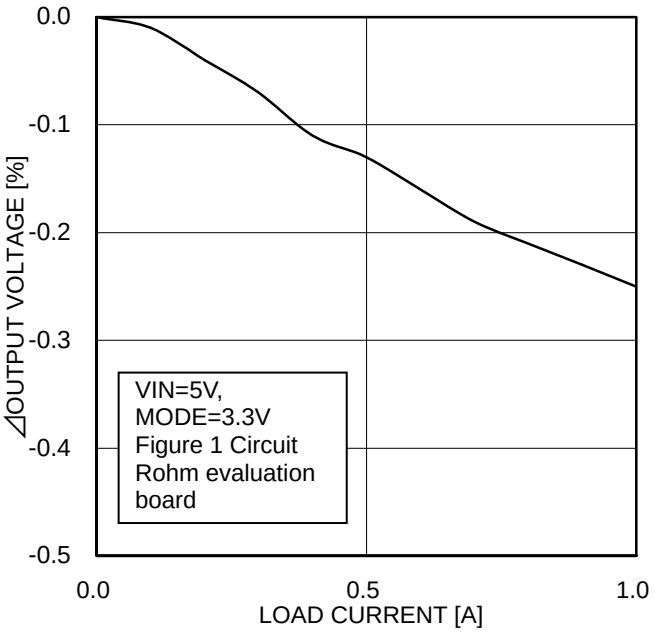


Figure 11. Load regulation

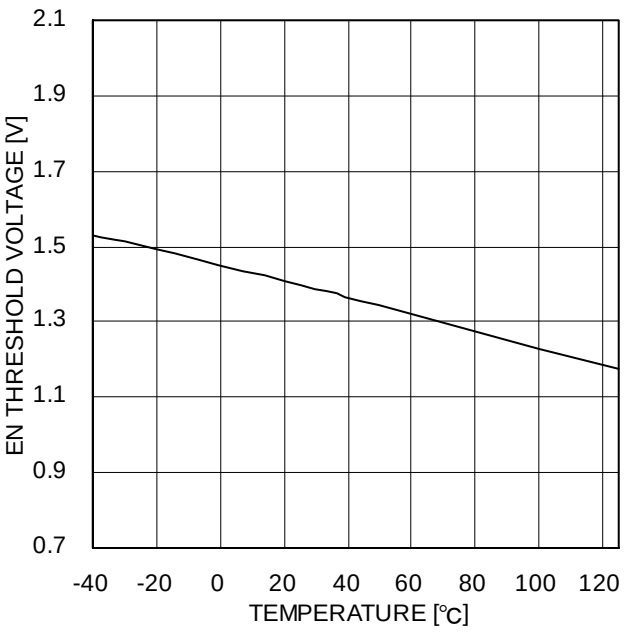


Figure 12. EN threshold voltage

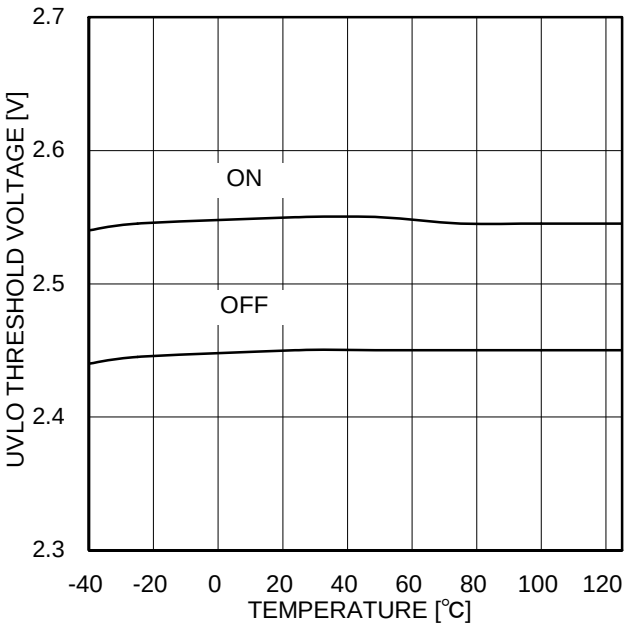


Figure 13. UVLO detect/release voltage

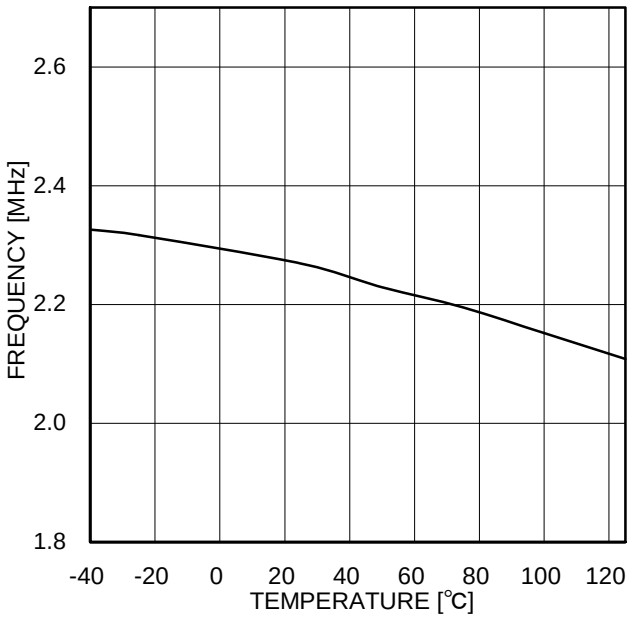


Figure 14. Frequency vs. temperature

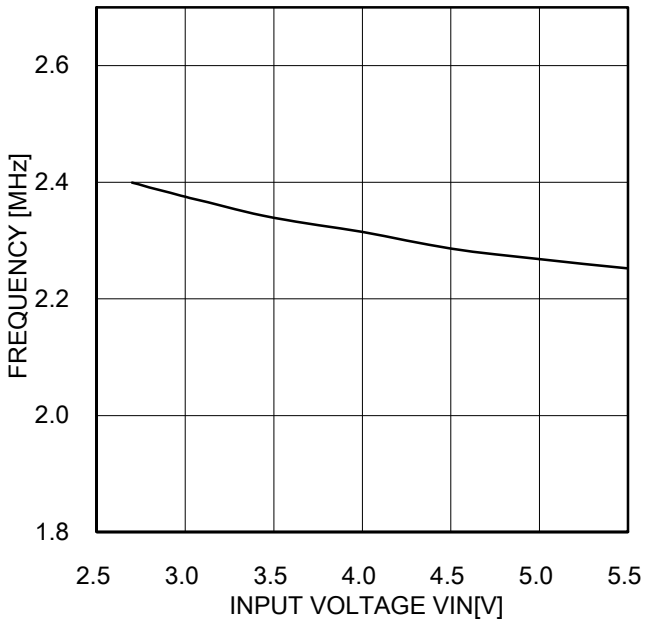


Figure 15. Frequency vs. input voltage

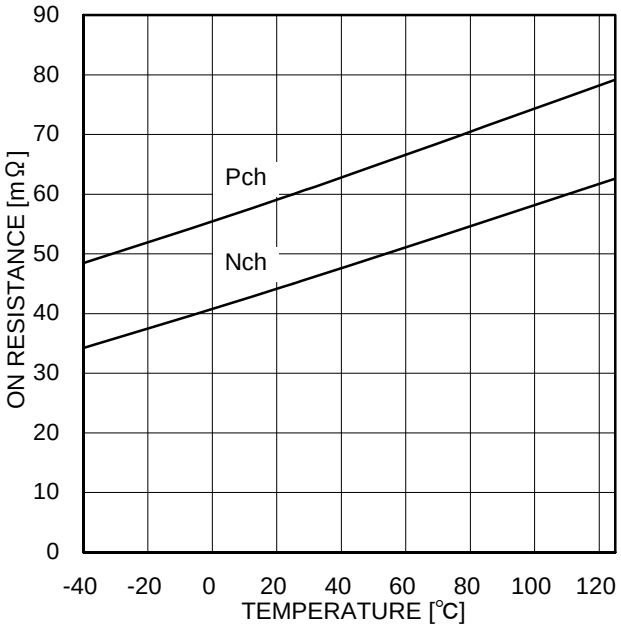


Figure 16. FET ON resistance

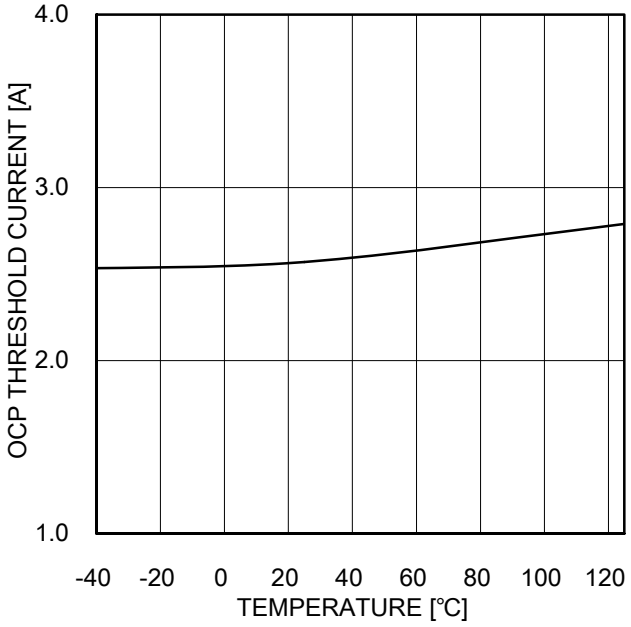


Figure 17. Over current detect vs. temperature

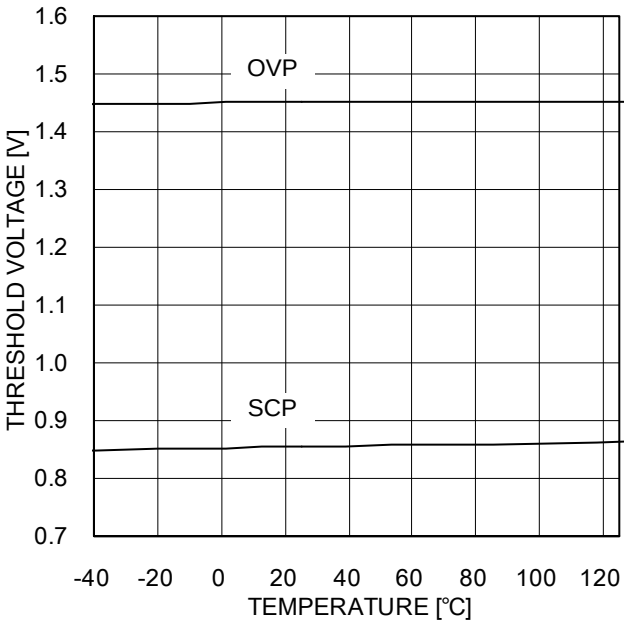


Figure 18. Output over/short detect voltage

The characteristics below are reference data which are measured with the typical application circuit as shown in Figure 1
Also, these characteristics are influenced by the external components and board layout.

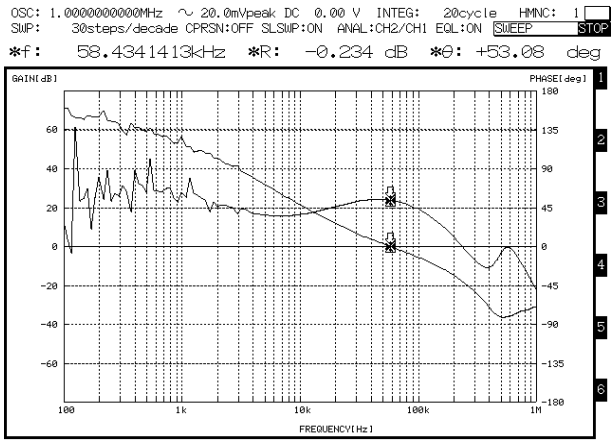


Figure 19. Loop response (VIN=5V, IOUT=1A)

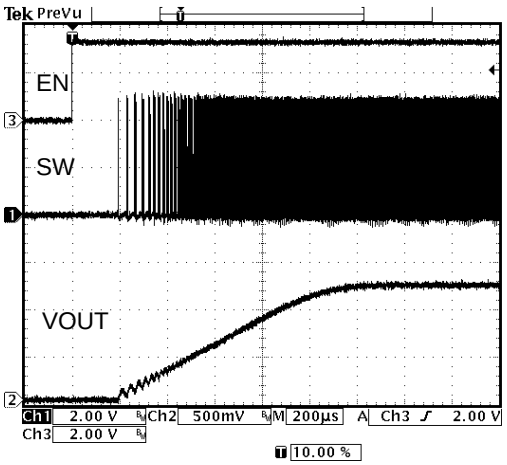


Figure 20. Start-up waveform (VIN=5V, MODE=3.3V)

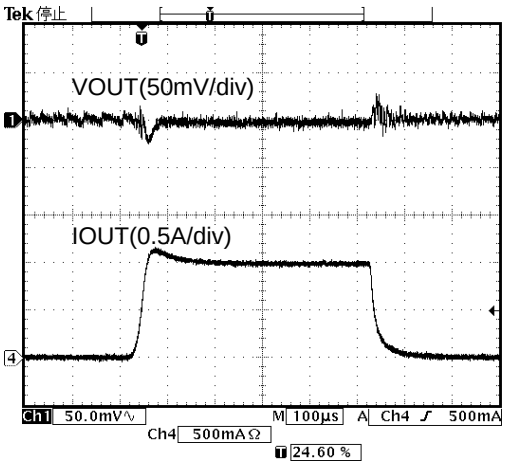


Figure 21. Load response (VIN=5V, MODE=0V)

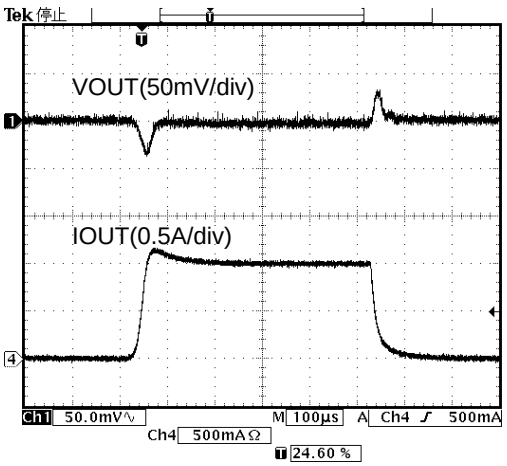


Figure 22. Load response (VIN=5V, MODE=3.3V)

●Timing chart

■ Start-up

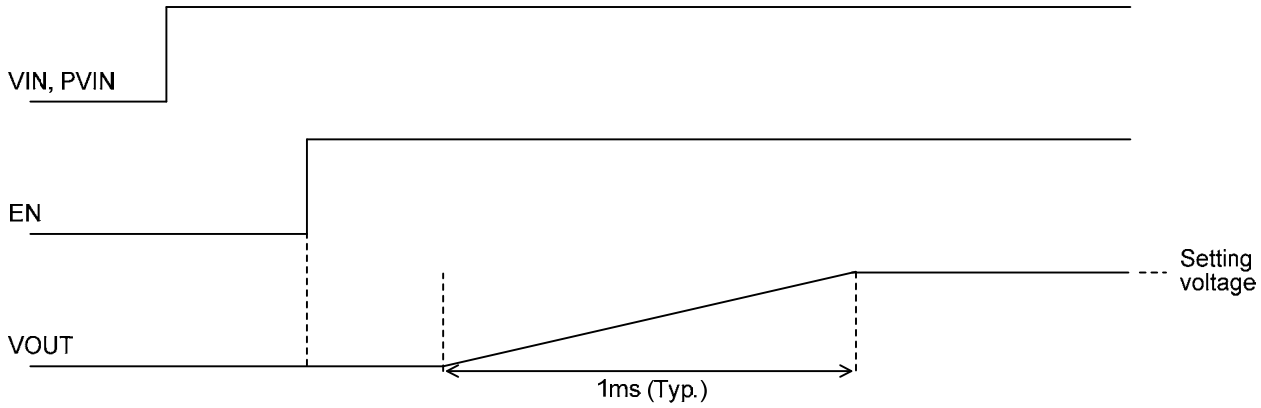


Figure 23. Start-up

■ OCP

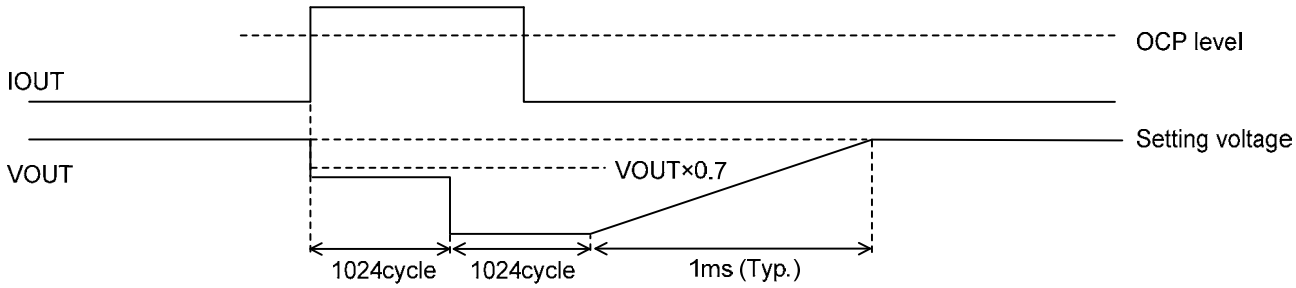


Figure 24. OCP

■ SCP

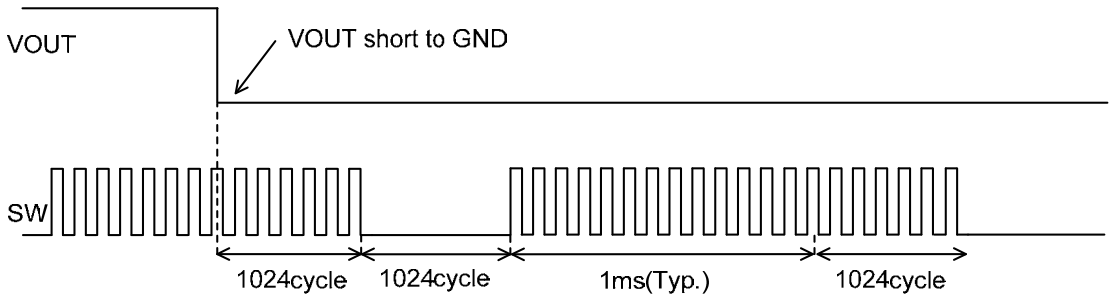
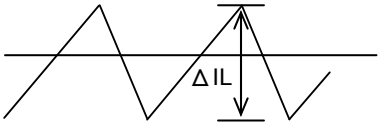


Figure 25. SCP

●Selection of external components

■ Selection of inductor
The inductor value greatly influences the output ripple current. The larger the coil is, the more the ripple current drops as shown in the equation below.



$$\Delta IL = \frac{(PVIN-VOUT) \times VOUT}{L \times PVIN \times f} \quad [A]$$

An inductor with a low value will cause the ripple current to increase and also cause an increase of the ripple element of the output voltage.
The optimal output ripple current setting is between 10% ~ 30% of the maximum output current.

$$\Delta IL = 0.2 \times IOUTmax. \quad [A]$$

$$L = \frac{(PVIN-VOUT) \times VOUT}{\Delta IL \times PVIN \times f} \quad [H]$$

(ΔIL: Output ripple current, f: switching frequency)

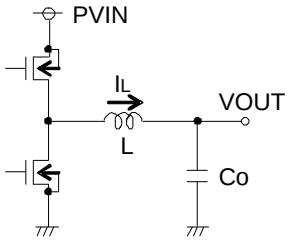


Figure 26. Ripple current

Supplying the coil with a current exceeding the coil's rated current will cause magnetic saturation of the coil and will decrease the efficiency of the coil. Please allow for a sufficient margin in selecting the inductor to ensure that the peak current does not exceed the inductor's rated current. Please select a coil with a small resistance element (DCR, ACR) to reduce the coil loss, and to improve efficiency.

■ Selection of input capacitor
The input capacitor serves to lower the impedance of the power supply connected to the input pin (VIN, PVIN). An increase of the impedance of this power supply can cause input voltage instability and may negatively impact oscillation and ripple rejection characteristics. Therefore, it is necessary to place an input capacitor in close proximity to the VIN, PVIN, GND and PGND pins.
We recommend selecting a ceramic capacitor with a value of 10uF or more that influenced by changes in temperature as little as possible and that has a sufficiently large permissible ripple current. The ripple current RMS can be calculated using the following equation.

$$IRMS = IOUT \times \sqrt{\frac{VOUT \ (VIN - VOUT)}{VIN}} \quad [A]$$

Note that depending on the capacitor, the capacitance may be greatly influenced by the applied voltage. Please select a capacitor with good DC bias characteristics and with a high voltage.

■ Selection of output capacitor
We recommend selecting a ceramic capacitor. The ripple element of the output voltage is determined by the ESR of the output capacitor. Please take the permissible voltage of the actual application into consideration when selecting the output capacitor. The ripple element of the output voltage can be calculated by using the equation below. Selecting a low-ESR capacitor can reduce the ripple element of the output voltage. Note that depending on the capacitor, the capacitance may be greatly influenced by the applied voltage. Please select a acapacitor with god DC bias characteristics and with a high voltage.

$$\Delta V_{PP} = \Delta I_L \times R_{ESR} + \frac{\Delta I_L}{Co} \times \frac{Vo}{VIN} \times \frac{1}{f} \quad [V] \qquad f: \text{Switching frequency}$$

The startup time needs to be within the soft start time. Therefore, please take the following equation into consideration when selecting the output capacitor
.

$$Co \leqq \frac{TSS \times (ILimit - IOUT)}{VOUT}$$

Tss: Soft start time (typ. 1ms)

ILimit: Overcurrent detection value (min. 1A)

Non-optimal capacitance values may cause startup problems. Especially in cases of extremely large capacitance values, the possibility exists that the inrush current at startup will activate the overcurrent protection, thus not starting the output. Therefore, verification and conformation with the actual application is recommended.

■ Selection of Schottky diode
Depending on the application the efficiency may be improved by placing a Schottky diode between the SW pin and PGND pin thereby creating a current path when the synchronous switching (Nch FET) is off. When selecting the Schottky diode ensure that the maximum reverse voltage is higher than the input voltage and that the rated current is higher than the maximum inductor current (the sum of the maximum output current and inductor ripple current).

●Notes on the substrate layout

The substrate layout greatly influences the stable operation of the IC. Depending on the substrate layout the IC might not show its original characteristics or might not function properly.
Please note the following points when creating the substrate layout.

- The input capacitors C1 and C2 should be placed as close as possible to the VIN, PVIN, GND and PGND pins.
- The output voltage feedback line should be separated from lines with a lot of noise such as the SW line.
- The GND signal should be separated from the input capacitor and the GND and PGND of the output capacitor and brought together at one point.
- The output capacitors C3 and C4 should be placed in close proximity to inductor L1.
- The inductor L1 should be placed as close as possible to the SW pin. The pattern area of the SW node should be as small as possible.
- The MODE pin should be pulled down via R1 by GND and pulled up via R2 by VIN.
  It is also possible to directly supple the MODE pin with voltage.
- The feedback frequency characteristics (phase margin) can be measured by inserting a resistor at the location of R3 and using FRA. However, this should be shorted during normal operation.

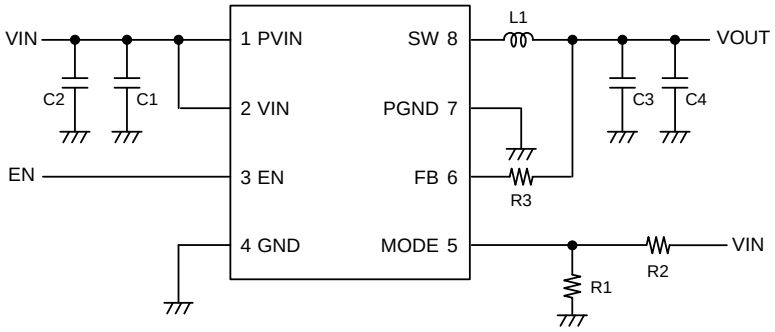
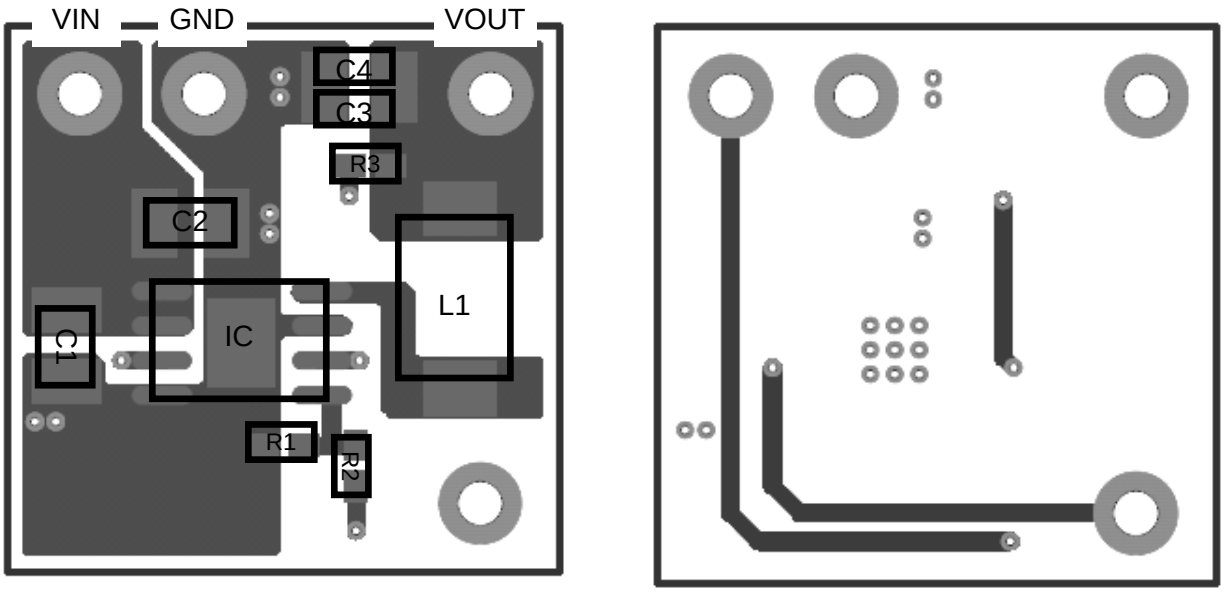


Figure 27. Reference circuit



<TOP VIEW> <BOTTOM VIEW>

Figure 28. Reference layout pattern

●Heat dissipation

The maximum allowable junction temperature Tj of BD90571EFJ-C is 150°C. In case Tj exceeds 150℃, the temperature protection circuit is activated and the circuit shuts down. Therefore, it is necessary to design the system requirements and the board layout so that the junction temperature does not exceed 150℃ in the power-supply voltage, the output load and the operating temperature range.

The maximum junction temperature can be calculated using the ambient temperature Ta, the thermal resistance θja of the package and heat dissipation P of the IC.

$$Tj = Ta + \theta ja \times P \ [°C]$$

The thermal resistance θja of the package changes depending on the number of layers and the copper foil area of the board.

The heat dissipation PTOTAL of the IC can be calculated by the equation below.

$P_{TOTAL} = P_{ICC} + P_{RON} + P_{SW}$ [W]
$P_{ICC} = VIN \times ICC$ ・・・ Heat dissipation in control circuit
$P_{RON} = R_{on} \times Io^2$ ・・・ Heat dissipation in output FET
$P_{SW} = Tr \times Io \times VIN \times F$ ・・・ Heat dissipation in switching

ICC: circuit current
Ron: ON resistance of the output FET
F: frequency
All values are specified in the electrical characteristics.
Tr is the rise time and fall time at switching. In the standard case is 5nsec and in the max case is 10nsec.
Also, these characteristics are influenced by the external components and board layout.

●Heat reduction characteristic

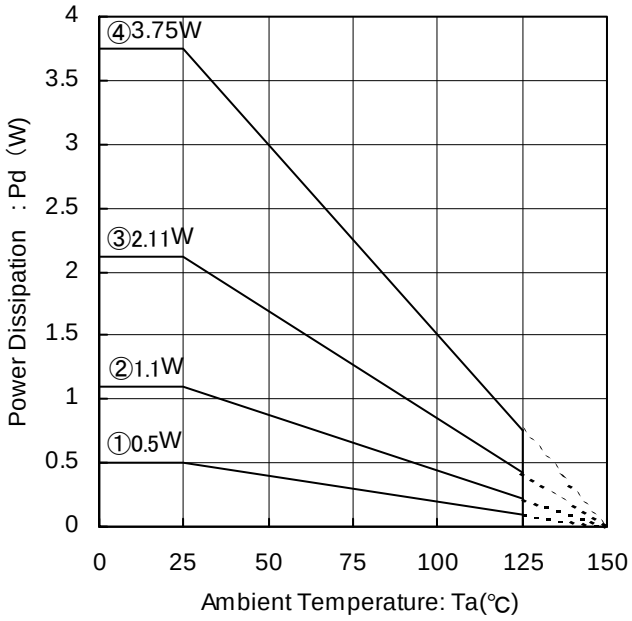


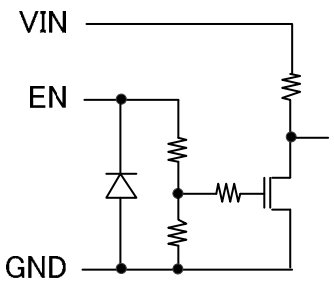
Figure 29. Heat reduction characteristic

IC mounted on ROHM standard board
・Board size：70mm×70mm×1.6mm
・The board and the back exposure heat radiation board part of package are connected with solder.

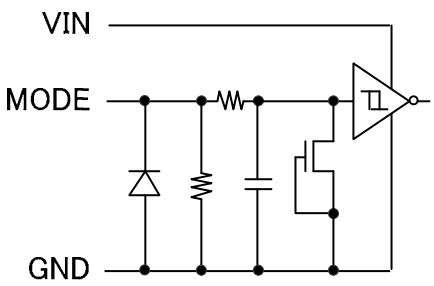
① IC unit, θja=249.5℃/W
② 2 layers board (Copper foil：15mm×15mm), θja =113.6℃/W
③ 2 layers board (Copper foil：70mm×70mm), θja =59.2℃/W
④ 4 layers board (Copper foil：70mm×70mm), θja =33.3℃/W

●I/O equivalence circuit

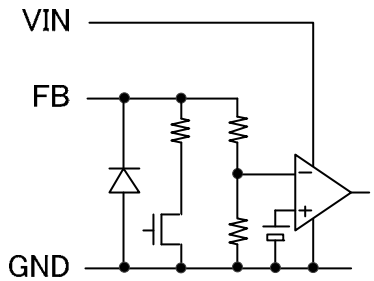
3PIN (EN)



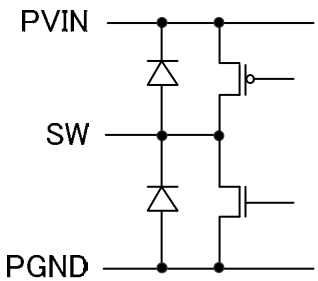
5PIN (MODE)



6PIN (FB)



8PIN (SW)



●Operational Notes

1. Absolute maximum ratings
   Exceeding the absolute maximum rating for supply voltage, operating temperature or other parameters may result in damages to or destruction of the chip. In this event it also becomes impossible to determine the cause of the damage (e.g. short circuit, open circuit, etc.). Therefore, if any special mode is being considered with values expected to exceed the absolute maximum ratings, implementing physical safety measures, such as adding fuses, should be considered.

2. Thermal protection circuit (TSD)
   If the junction temperature (Tj) exceeds 175℃(Typ.) the thermal protection circuit (TSD) is activated and the output is put in the OFF status. The releasing temperature has hysteresis of about 25°C(typ.). The thermal protection circuit only functions to block thermal overloads from reaching the IC. Its purpose is not to protect the circuit or to guarantee the operations of the IC. Therefore, the IC should not be continuously operated after this circuit has been activated, nor should the IC be used in applications where the activation of this circuit is a prerequisite.

3. Overcurrent protection circuit
   This IC incorporates an integrated overcurrent protection circuit that operates in accordance with the rated output capacity. This circuit serves to protect the IC from damage when the load becomes shorted. The protection circuit is effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous or transitive operation of the protection circuit.

4. High temperature, no load behavior
   In a situation where there is a high temperature and no load, it might be that the leak current of the output transistor causes output voltage to rise (up to maximum VIN). It case it is expected that in the application conditions the output load drops below 1mA, please place a 1kohm resistor at the output in order to prevent an no-load situation.

5. Power dissipation, ASO
   Should by any chance the power dissipation rating be exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip and lead to a decrease of the reliability. Therefore, allow for sufficient margins to ensure use within the power dissipation rating. Also, please ensure in the design that the absolute maximum rating of the output transistor and the ASO are not exceeded when operating the IC.

6. Operation in strong electromagnetic fields
   Use caution when operating in the presence of strong electromagnetic fields, as this may cause the IC to malfunction.

7. Connection to the power supply connector
   A reverse connection to the power supply connector may cause damages to the IC. In order to prevent against reverse connection damages please externally place a diode between the power supply and the power supply pin of the IC.

8. Inter-pin shorts and mounting errors
   Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply or GND pins (caused by poor soldering or foreign objects) may result in damage to the IC.

9. Short to power supply, short to ground, inter-pin shorts
   Please avoid shorts between the output pin and the power supply (VIN, PVIN), shorts between the output pin and ground (GND, PGND) and shorts between the output pins.

10. Testing on application boards
    When testing the IC on an application board, connecting a capacitor directly to a low-impedance pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from a jig or fixture during the evaluation process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

11. GND potential
    The potential of the GND pin must be the minimum potential in the system in all operating conditions. Ensure that no pins are at a voltage below the GND at any time, regardless of transient characteristics.

12. Wiring of VIN and GND
    For the wiring of VIN, PVIN, GND and PGND please create a layout with as wide as possible wires and a minimum distance in between the wires. In case of both small signal lines and high current lines, use single-point grounding to separate the small-signal and high current patterns and to ensure that voltage changes stemming from the wiring resistance and high current do not cause any voltage change in the small-signal. Also place a capacitor at the grounding point for stabilization.

13. Capacitor between PVIN and PGND
The capacitor between PVIN and PGND absorbs the steep changes in voltage and current caused by the PWM drive and thereby suppress fluctuations in the PVIN voltage. However, this effect is diminished due to wiring impedance the further the capacitor is removed from the IC.

14. Input pins
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. Relations between each potential may form as shown in the example below, where a resistor and transistor are connected to a pin:
- With the resistor, when GND＞ Pin A, and with the transistor (NPN), when GND＞Pin B:
  The P-N junction operates as a parasitic diode.
- With the transistor (NPN), when GND＞ Pin B:
  The P-N junction operates as a parasitic transistor by interacting with the N layers of elements in proximity to the parasitic diode described above.

Parasitic diodes inevitably occur in the structure of the IC. Their operation can result in mutual interference between circuits and can cause malfunctions and, in turn, physical damage to or destruction of the chip. Therefore do not employ any method in which parasitic diodes can operate such as applying a voltage to an input pin that is lower than the (P substrate) GND.

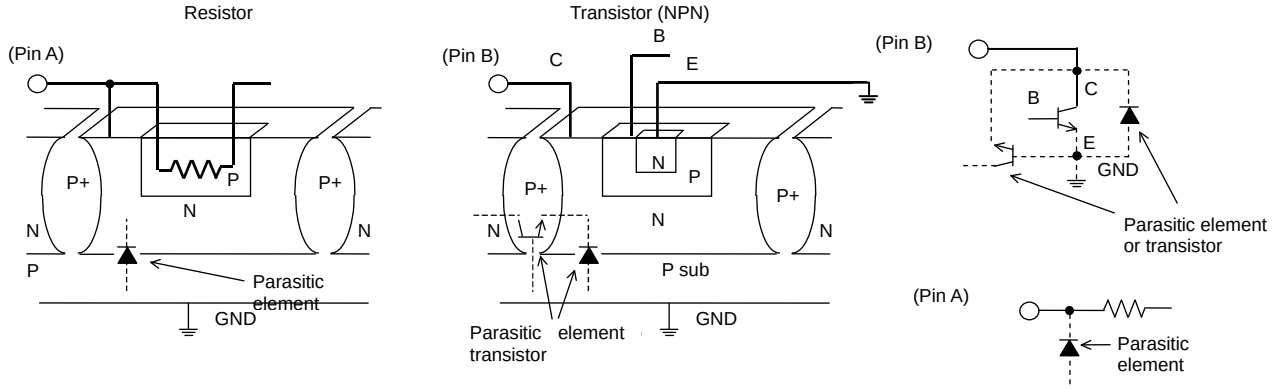


Figure 30. Example of IC structure

15. Application current and constants
The application circuit as shown in Figure 1. and the constants are examples to show the standard operation and application of this IC. In case of creating a design for mass production with different external components please contact ROHM for detailed information.

16. In some applications, the PVIN pin and SW pin potential might be reversed, possibly resulting in circuit internal damage or damage to the elements. For example, while the external capacitor is charged, the PVIN shorts to the GND. To prevent this we recommend reverse polarity diodes in series or placing a bypass diode between the SW pin and PVIN pin.

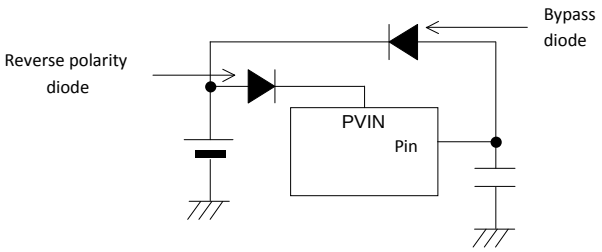


Figure 31. Measure for reverse

Note concerning this document
The Japanese version of this document is the official specification. This translation should be seen as a reference to aid reading the official specification. In case of any discrapencies between the two versions, the offical version always takes precedence.

●Ordering Information

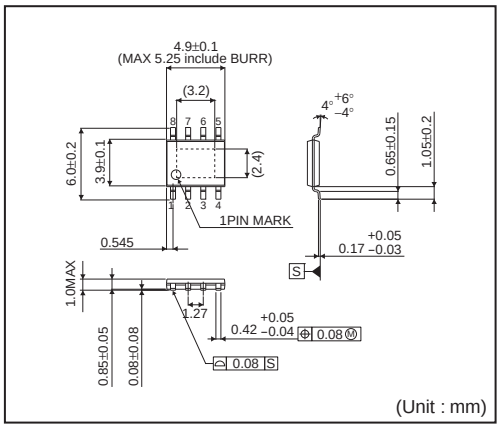
B	D	9	0	5	7	1	E	F	J	-	CE2

Package
EFJ: HTSOP-J8

Packaging and forming specification
CE2: Embossed tape and reel

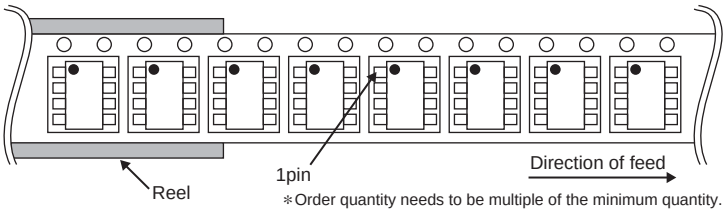
●Physical Dimension Tape and Reel Information

HTSOP-J8



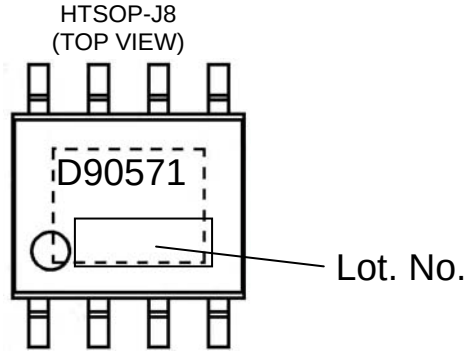
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●Marking Diagram



●Revision History

Rev.	Date	Notes
001	2012/07/31	New release

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CLASSⅢ	CLASSⅢ	CLASSⅡb	Ⅲ類
CLASSⅣ		CLASSⅢ	

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   ②直射日光・屋外暴露、塵埃中でのご使用
   ③潮風、Cl_2、H_2S、NH_3、SO_2、NO_2 等の腐食性ガスの多い場所でのご使用
   ④静電気や電磁波の強い環境でのご使用
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