



## Double channel high-side driver with analog current sense for automotive applications

Datasheet — production data

### Features

|                                   |            |                          |
|-----------------------------------|------------|--------------------------|
| Max transient supply voltage      | $V_{CC}$   | 41 V                     |
| Operating voltage range           | $V_{CC}$   | 4.5 to 28 V              |
| Max on-state resistance (per ch.) | $R_{ON}$   | 50 m $\Omega$            |
| Current limitation (typ)          | $I_{LIMH}$ | 27 A                     |
| Off-state supply current          | $I_S$      | 2 $\mu$ A <sup>(1)</sup> |

1. Typical value with all loads connected.

#### ■ General

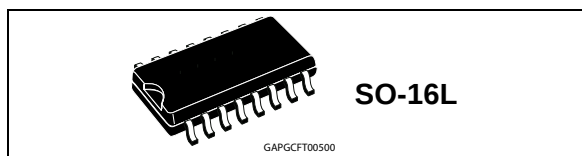
- Inrush current active management by power limitation
- Very low standby current
- 3.0 V CMOS compatible inputs
- Optimized electromagnetic emissions
- Very low electromagnetic susceptibility
- Compliant with European directive 2002/95/EC
- Very low current sense leakage
- AEC-Q100 qualified

#### ■ Diagnostic functions

- Proportional load current sense
- High current sense precision for wide currents range
- Current sense disable
- Off-state open-load detection
- Output short to  $V_{CC}$  detection
- Overload and short to ground (power limitation) indication
- Thermal shutdown indication

#### ■ Protections

- Undervoltage shutdown
- Overvoltage clamp
- Load current limitation
- Self limiting of fast thermal transients
- Protection against loss of ground and loss of  $V_{CC}$



- Overtemperature shutdown with auto restart (thermal shutdown)
- Reverse battery protected
- Electrostatic discharge protection

### Applications

- All types of resistive, inductive and capacitive loads
- Suitable as LED driver

### Description

The VND5E050ASO-E is a double channel high-side driver manufactured using ST proprietary VIPower® M0-5 technology and housed in SO-16L package. The device is designed to drive 12 V automotive grounded loads, and to provide protection and diagnostics. It also implements a 3 V and 5 V CMOS-compatible interface for the use with any microcontroller.

The device integrates advanced protective functions such as load current limitation, inrush and overload active management by power limitation, overtemperature shut-off with auto-restart and overvoltage active clamp. A dedicated analog current sense pin is associated with every output channel providing enhanced diagnostic functions including fast detection of overload and short-circuit to ground through power limitation indication, overtemperature indication, short-circuit to  $V_{CC}$  diagnosis and on-state and off-state open-load detection. The current sensing and diagnostic feedback of the whole device can be disabled by pulling the CS\_DIS pin high to share the external sense resistor with similar devices.

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# 1 Block diagram and pin description

Figure 1. Block diagram

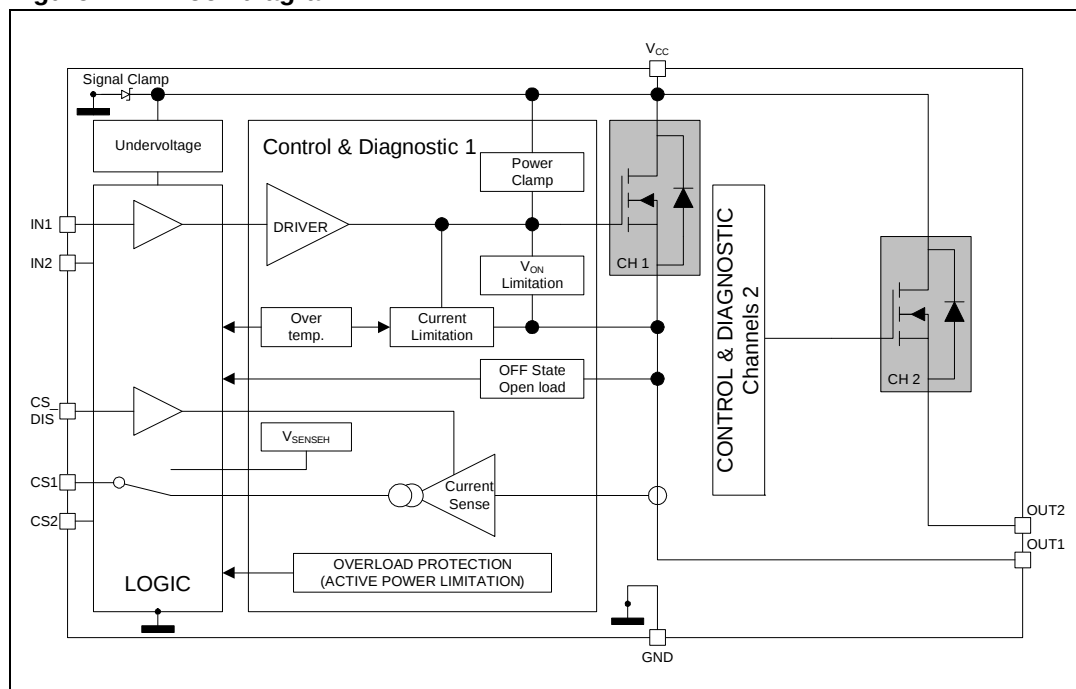


Table 1. Pin function

| Name                         | Function                                                                                     |
|------------------------------|----------------------------------------------------------------------------------------------|
| V <sub>CC</sub>              | Battery connection.                                                                          |
| OUTPUT <sub>1,2</sub>        | Power output.                                                                                |
| GND                          | Ground connection. Must be reverse battery protected by an external diode/resistor network.  |
| INPUT <sub>1,2</sub>         | Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state. |
| CURRENT SENSE <sub>1,2</sub> | Analog current sense pin, delivers a current proportional to the load current.               |
| CS_DIS                       | Active high CMOS compatible pin, to disable the current sense pin.                           |

Figure 2. Configuration diagram (top view)

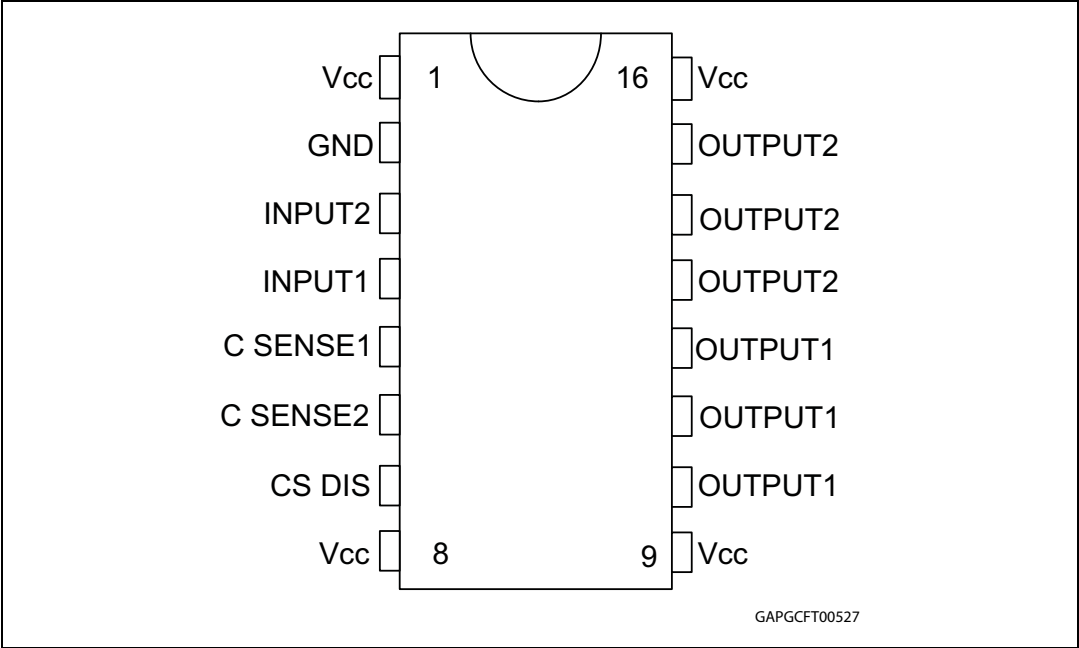
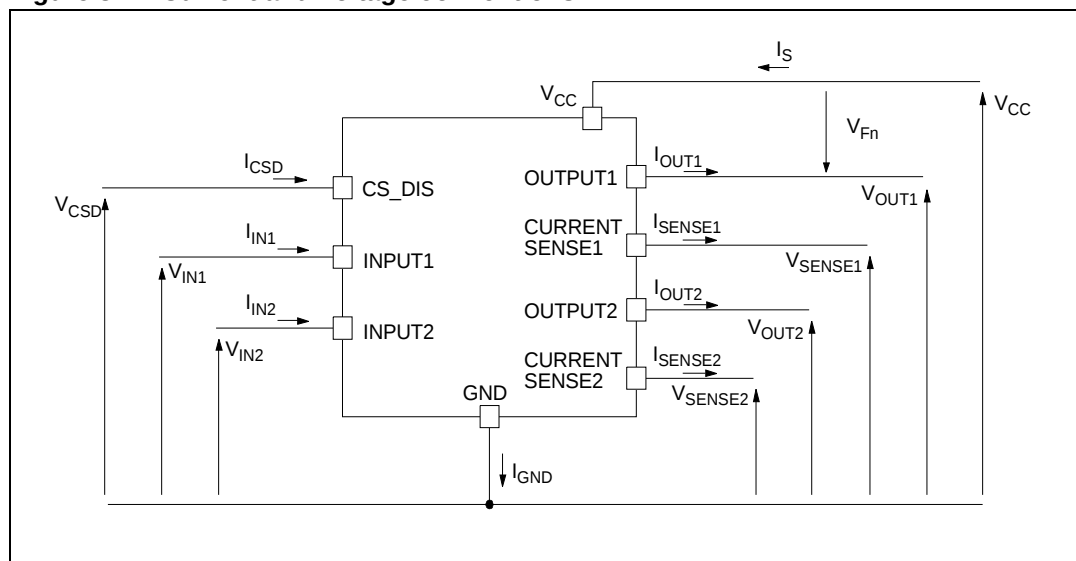


Table 2. Suggested connections for unused and not connected pins

| Connection / pin | Current sense         | N.C. | Output                 | Input                  | CS_DIS                 |
|------------------|-----------------------|------|------------------------|------------------------|------------------------|
| Floating         | Not allowed           | X    | X                      | X                      | X                      |
| To ground        | Through 1 KΩ resistor | X    | Through 22 KΩ resistor | Through 10 KΩ resistor | Through 10 KΩ resistor |

## 2 Electrical specifications

**Figure 3. Current and voltage conventions**



Note:  $V_{Fn} = V_{OUTn} - V_{CC}$  during reverse battery condition.

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 3: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

**Table 3. Absolute maximum ratings**

| Symbol        | Parameter                              | Value                      | Unit |
|---------------|----------------------------------------|----------------------------|------|
| $V_{CC}$      | DC supply voltage                      | 41                         | V    |
| $-V_{CC}$     | Reverse DC supply voltage              | 0.3                        | V    |
| $-I_{GND}$    | DC reverse ground pin current          | 200                        | mA   |
| $I_{OUT}$     | DC output current                      | Internally limited         | A    |
| $-I_{OUT}$    | Reverse DC output current              | 20                         | A    |
| $I_{IN}$      | DC input current                       | -1 to 10                   | mA   |
| $I_{CSD}$     | DC current sense disable input current | -1 to 10                   | mA   |
| $-I_{CSENSE}$ | DC reverse CS pin current              | 200                        | mA   |
| $V_{CSENSE}$  | Current sense maximum voltage          | $V_{CC} - 41$ to $+V_{CC}$ | V    |

**Table 3. Absolute maximum ratings (continued)**

| Symbol    | Parameter                                                                                                                                                                           | Value      | Unit             |
|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|------------------|
| $E_{MAX}$ | Maximum switching energy (single pulse)<br>( $L = 3\text{ mH}$ ; $R_L = 0\ \Omega$ ; $V_{bat} = 13.5\text{ V}$ ; $T_{jstart} = 150^\circ\text{C}$ ;<br>$I_{OUT} = I_{limL}(Typ.)$ ) | 104        | mJ               |
| $V_{ESD}$ | Electrostatic discharge<br>(human body model: $R = 1.5\text{ K}\Omega$ ; $C = 100\text{ pF}$ )                                                                                      |            |                  |
|           | – Input                                                                                                                                                                             | 4000       | V                |
|           | – Current sense                                                                                                                                                                     | 2000       | V                |
|           | – CS_DIS                                                                                                                                                                            | 4000       | V                |
|           | – Output                                                                                                                                                                            | 5000       | V                |
|           | – $V_{CC}$                                                                                                                                                                          | 5000       | V                |
| $V_{ESD}$ | Charge device model (CDM-AEC-Q100-011)                                                                                                                                              | 750        | V                |
| $T_j$     | Junction operating temperature                                                                                                                                                      | -40 to 150 | $^\circ\text{C}$ |
| $T_{stg}$ | Storage temperature                                                                                                                                                                 | -55 to 150 | $^\circ\text{C}$ |

## 2.2 Thermal data

**Table 4. Thermal data**

| Symbol        | Parameter                                                                 | Typ value                     | Unit               |
|---------------|---------------------------------------------------------------------------|-------------------------------|--------------------|
| $R_{thj-pcb}$ | Thermal resistance junction-pcb <sup>(1)</sup>                            | 18.5                          | $^\circ\text{C/W}$ |
| $R_{thj-amb}$ | Thermal resistance junction - ambient on two layers pcb                   | See <a href="#">Figure 36</a> | $^\circ\text{C/W}$ |
| $R_{thj-amb}$ | Thermal resistance junction - ambient on two layers<br>pcb <sup>(2)</sup> | 34.5                          | $^\circ\text{C/W}$ |

1. The measure is done in accordance with the JESD 51-8.

2. Four Layers PCB characteristics:

- Cu thickness: 70  $\mu\text{m}$  outer layers, 35  $\mu\text{m}$  inner layers
- Board finish thickness 1.6 mm +/- 10%
- Thermal vias separation 1.2 mm
- Thermal via diameter 0.3 mm +/- 0.08 mm
- Cu thickness on vias 0.025 mm
- Device soldered at about 2 cm from the PCB edge with two sqcm of exposed copper

## 2.3 Electrical characteristics

Values specified in this section are for  $8\text{ V} < V_{CC} < 28\text{ V}$ ;  $-40\text{ }^\circ\text{C} < T_j < 150\text{ }^\circ\text{C}$ , unless otherwise stated.

**Table 5. Power section**

| Symbol        | Parameter                                      | Test conditions                                                                                                | Min. | Typ.             | Max.             | Unit          |
|---------------|------------------------------------------------|----------------------------------------------------------------------------------------------------------------|------|------------------|------------------|---------------|
| $V_{CC}$      | Operating supply voltage                       |                                                                                                                | 4.5  | 13               | 28               | V             |
| $V_{USD}$     | Undervoltage shutdown                          |                                                                                                                |      | 3.5              | 4.5              | V             |
| $V_{USDhyst}$ | Undervoltage shutdown hysteresis               |                                                                                                                |      | 0.5              |                  | V             |
| $R_{ON}$      | On-state resistance <sup>(1)</sup>             | $I_{OUT} = 2\text{ A}; T_j = 25^\circ\text{C}$                                                                 |      | 50               |                  | m $\Omega$    |
|               |                                                | $I_{OUT} = 2\text{ A}; T_j = 150^\circ\text{C}$                                                                |      |                  | 100              |               |
|               |                                                | $I_{OUT} = 2\text{ A}; V_{CC} = 5\text{ V}; T_j = 25^\circ\text{C}$                                            |      |                  | 65               |               |
| $V_{clamp}$   | Clamp voltage                                  | $I_S = 20\text{ mA}$                                                                                           | 41   | 46               | 52               | V             |
| $I_S$         | Supply current                                 | Off-state; $V_{CC} = 13\text{ V}; T_j = 25^\circ\text{C}; V_{IN} = V_{OUT} = V_{SENSE} = V_{CSD} = 0\text{ V}$ |      | 2 <sup>(2)</sup> | 5 <sup>(2)</sup> | $\mu\text{A}$ |
|               |                                                | On-state; $V_{CC} = 13\text{ V}; V_{IN} = 5\text{ V}; I_{OUT} = 0\text{ A}$                                    |      | 3                | 6                | mA            |
| $I_{L(off1)}$ | Off-state output current <sup>(1)</sup>        | $V_{IN} = V_{OUT} = 0\text{ V}; V_{CC} = 13\text{ V}; T_j = 25^\circ\text{C}$                                  | 0    | 0.01             | 3                | $\mu\text{A}$ |
|               |                                                | $V_{IN} = V_{OUT} = 0\text{ V}; V_{CC} = 13\text{ V}; T_j = 125^\circ\text{C}$                                 | 0    |                  | 5                |               |
| $V_F$         | Output - $V_{CC}$ diode voltage <sup>(1)</sup> | $-I_{OUT} = 4\text{ A}; T_j = 150^\circ\text{C}$                                                               |      |                  | 0.7              | V             |

1. For each channel.

2. PowerMOS leakage included.

**Table 6. Switching ( $V_{CC} = 13\text{ V}; T_j = 25^\circ\text{C}$ )**

| Symbol                | Parameter                                 | Test conditions                                     | Min. | Typ.                          | Max. | Unit             |
|-----------------------|-------------------------------------------|-----------------------------------------------------|------|-------------------------------|------|------------------|
| $t_{d(on)}$           | Turn-on delay time                        | $R_L = 6.5\ \Omega$ (see <a href="#">Figure 6</a> ) | —    | 20                            | —    | $\mu\text{s}$    |
| $t_{d(off)}$          | Turn-off delay time                       | $R_L = 6.5\ \Omega$ (see <a href="#">Figure 6</a> ) | —    | 45                            | —    | $\mu\text{s}$    |
| $dV_{OUT}/dt_{(on)}$  | Turn-on voltage slope                     | $R_L = 6.5\ \Omega$                                 | —    | See <a href="#">Figure 26</a> | —    | V/ $\mu\text{s}$ |
| $dV_{OUT}/dt_{(off)}$ | Turn-off voltage slope                    | $R_L = 6.5\ \Omega$                                 | —    | See <a href="#">Figure 28</a> | —    | V/ $\mu\text{s}$ |
| $W_{ON}$              | Switching energy losses during $t_{won}$  | $R_L = 6.5\ \Omega$ (see <a href="#">Figure 6</a> ) | —    | 0.15                          | —    | mJ               |
| $W_{OFF}$             | Switching energy losses during $t_{woff}$ | $R_L = 6.5\ \Omega$ (see <a href="#">Figure 6</a> ) | —    | 0.3                           | —    | mJ               |

**Table 7. Logic inputs**

| Symbol   | Parameter               | Test conditions         | Min. | Typ. | Max. | Unit          |
|----------|-------------------------|-------------------------|------|------|------|---------------|
| $V_{IL}$ | Input low level voltage |                         |      |      | 0.9  | V             |
| $I_{IL}$ | Low level input current | $V_{IN} = 0.9\text{ V}$ | 1    |      |      | $\mu\text{A}$ |

**Table 7. Logic inputs (continued)**

| Symbol          | Parameter                 | Test conditions          | Min. | Typ. | Max. | Unit          |
|-----------------|---------------------------|--------------------------|------|------|------|---------------|
| $V_{IH}$        | Input high level voltage  |                          | 2.1  |      |      | V             |
| $I_{IH}$        | High level input current  | $V_{IN} = 2.1\text{ V}$  |      |      | 10   | $\mu\text{A}$ |
| $V_{I(hyst)}$   | Input hysteresis voltage  |                          | 0.25 |      |      | V             |
| $V_{ICL}$       | Input clamp voltage       | $I_{IN} = 1\text{ mA}$   | 5.5  |      | 7    | V             |
|                 |                           | $I_{IN} = -1\text{ mA}$  |      | -0.7 |      |               |
| $V_{CSDL}$      | CS_DIS low level voltage  |                          |      |      | 0.9  | V             |
| $I_{CSDL}$      | Low level CS_DIS current  | $V_{CSD} = 0.9\text{ V}$ | 1    |      |      | $\mu\text{A}$ |
| $V_{CSDH}$      | CS_DIS high level voltage |                          | 2.1  |      |      | V             |
| $I_{CSDH}$      | High level CS_DIS current | $V_{CSD} = 2.1\text{ V}$ |      |      | 10   | $\mu\text{A}$ |
| $V_{CSD(hyst)}$ | CS_DIS hysteresis voltage |                          | 0.25 |      |      | V             |
| $V_{CSCL}$      | CS_DIS clamp voltage      | $I_{CSD} = 1\text{ mA}$  | 5.5  |      | 7    | V             |
|                 |                           | $I_{CSD} = -1\text{ mA}$ |      | -0.7 |      |               |

**Table 8. Protections and diagnostics <sup>(1)</sup>**

| Symbol      | Parameter                                    | Test conditions                                                                                                        | Min.        | Typ.        | Max.        | Unit               |
|-------------|----------------------------------------------|------------------------------------------------------------------------------------------------------------------------|-------------|-------------|-------------|--------------------|
| $I_{limH}$  | DC short circuit current                     | $V_{CC} = 13\text{ V}$                                                                                                 | 19          | 27          | 38          | A                  |
|             |                                              | $5\text{ V} < V_{CC} < 28\text{ V}$                                                                                    |             |             | 38          | A                  |
| $I_{limL}$  | Short circuit current during thermal cycling | $V_{CC} = 13\text{ V};$<br>$T_R < T_j < T_{TSD}$                                                                       |             | 7           |             | A                  |
| $T_{TSD}$   | Shutdown temperature                         |                                                                                                                        | 150         | 175         | 200         | $^{\circ}\text{C}$ |
| $T_R$       | Reset temperature                            |                                                                                                                        | $T_{RS}+1$  | $T_{RS}+5$  |             | $^{\circ}\text{C}$ |
| $T_{RS}$    | Thermal reset of status                      |                                                                                                                        | 135         |             |             | $^{\circ}\text{C}$ |
| $T_{HYST}$  | Thermal hysteresis ( $T_{TSD} - T_R$ )       |                                                                                                                        |             | 7           |             | $^{\circ}\text{C}$ |
| $V_{DEMAG}$ | Turn-off output voltage clamp                | $I_{OUT} = 2\text{ A}; V_{IN} = 0;$<br>$L = 6\text{ mH}$                                                               | $V_{CC}-41$ | $V_{CC}-46$ | $V_{CC}-52$ | V                  |
| $V_{ON}$    | Output voltage drop limitation               | $I_{OUT} = 0.1\text{ A};$<br>$T_j = -40^{\circ}\text{C} \dots +150^{\circ}\text{C}$<br>(see <a href="#">Figure 8</a> ) |             | 25          |             | mV                 |

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

**Table 9. Current sense ( $8\text{ V} < V_{CC} < 18\text{ V}$ )**

| Symbol           | Parameter                                                     | Test conditions                                                                                                                                                                          | Min.         | Typ.         | Max.         | Unit          |
|------------------|---------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|--------------|--------------|---------------|
| $K_0$            | $I_{OUT}/I_{SENSE}$                                           | $I_{OUT} = 0.05\text{ A}$ ; $V_{SENSE} = 0.5\text{ V}$ ;<br>$V_{CSD} = 0\text{ V}$ ; $T_j = -40^\circ\text{C} \dots 150^\circ\text{C}$                                                   | 1440         | 2250         | 3630         |               |
| $K_1$            | $I_{OUT}/I_{SENSE}$                                           | $I_{OUT} = 1\text{ A}$ ; $V_{SENSE} = 4\text{ V}$ ;<br>$V_{CSD} = 0\text{ V}$ ;<br>$T_j = -40^\circ\text{C} \dots 150^\circ\text{C}$<br>$T_j = 25^\circ\text{C} \dots 150^\circ\text{C}$ | 1740<br>1750 | 2070<br>2070 | 2820<br>2562 |               |
| $dK_1/K_1^{(1)}$ | Current sense ratio drift                                     | $I_{OUT} = 1\text{ A}$ ; $V_{SENSE} = 4\text{ V}$ ;<br>$V_{CSD} = 0\text{ V}$ ;<br>$T_j = -40^\circ\text{C}$ to $150^\circ\text{C}$                                                      | -15          |              | 15           | %             |
| $K_2$            | $I_{OUT}/I_{SENSE}$                                           | $I_{OUT} = 2\text{ A}$ ; $V_{SENSE} = 4\text{ V}$ ;<br>$V_{CSD} = 0\text{ V}$ ;<br>$T_j = -40^\circ\text{C} \dots 150^\circ\text{C}$<br>$T_j = 25^\circ\text{C} \dots 150^\circ\text{C}$ | 1900<br>1899 | 2000<br>2000 | 2395<br>2282 |               |
| $dK_2/K_2^{(1)}$ | Current sense ratio drift                                     | $I_{OUT} = 2\text{ A}$ ; $V_{SENSE} = 4\text{ V}$ ;<br>$V_{CSD} = 0\text{ V}$ ;<br>$T_j = -40^\circ\text{C}$ to $150^\circ\text{C}$                                                      | -9           |              | 9            | %             |
| $K_3$            | $I_{OUT}/I_{SENSE}$                                           | $I_{OUT} = 4\text{ A}$ ;<br>$V_{SENSE} = 4\text{ V}$ ; $V_{CSD} = 0\text{ V}$ ;<br>$T_j = -40^\circ\text{C} \dots 150^\circ\text{C}$<br>$T_j = 25^\circ\text{C} \dots 150^\circ\text{C}$ | 1969<br>1950 | 1990<br>1990 | 2210<br>2153 |               |
| $dK_3/K_3^{(1)}$ | Current sense ratio drift                                     | $I_{OUT} = 4\text{ A}$ ; $V_{SENSE} = 4\text{ V}$ ;<br>$V_{CSD} = 0\text{ V}$ ;<br>$T_j = -40^\circ\text{C}$ to $150^\circ\text{C}$                                                      | -6           |              | 6            | %             |
| $I_{SENSE0}$     | Analog sense leakage current                                  | $I_{OUT} = 0\text{ A}$ ; $V_{SENSE} = 0\text{ V}$ ;<br>$V_{CSD} = 5\text{ V}$ ; $V_{IN} = 0\text{ V}$ ;<br>$T_j = -40^\circ\text{C} \dots 150^\circ\text{C}$                             | 0            |              | 1            | $\mu\text{A}$ |
|                  |                                                               | $I_{OUT} = 0\text{ A}$ ; $V_{SENSE} = 0\text{ V}$ ;<br>$V_{CSD} = 0\text{ V}$ ; $V_{IN} = 5\text{ V}$ ;<br>$T_j = -40^\circ\text{C} \dots 150^\circ\text{C}$                             | 0            |              | 2            |               |
|                  |                                                               | $I_{OUT} = 2\text{ A}$ ; $V_{SENSE} = 0\text{ V}$ ;<br>$V_{CSD} = 5\text{ V}$ ; $V_{IN} = 5\text{ V}$ ;<br>$T_j = -40^\circ\text{C} \dots 150^\circ\text{C}$                             | 0            |              | 1            |               |
| $I_{OL}$         | Open load on-state current detection threshold                | $V_{IN} = 5\text{ V}$ ; $8\text{ V} < V_{CC} < 18\text{ V}$ ;<br>$I_{SENSE} = 5\text{ }\mu\text{A}$                                                                                      | 4            |              | 20           | mA            |
| $V_{SENSE}$      | Max analog sense output voltage                               | $I_{OUT} = 4\text{ A}$ ; $V_{CSD} = 0\text{ V}$                                                                                                                                          | 5            |              |              | V             |
| $V_{SENSEH}$     | Analog sense output voltage in fault condition <sup>(2)</sup> | $V_{CC} = 13\text{ V}$ ; $R_{SENSE} = 3.9\text{ K}\Omega$                                                                                                                                |              | 8            |              | V             |
| $I_{SENSEH}$     | Analog sense output current in fault condition <sup>(2)</sup> | $V_{CC} = 13\text{ V}$ ; $V_{SENSE} = 5\text{ V}$                                                                                                                                        |              | 9            |              | mA            |

**Table 9. Current sense (8 V < V<sub>CC</sub> < 18 V) (continued)**

| Symbol                 | Parameter                                                                                  | Test conditions                                                                                                                                                                         | Min. | Typ. | Max. | Unit |
|------------------------|--------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| t <sub>DSENSE1H</sub>  | Delay response time from falling edge of CS_DIS pin                                        | V <sub>SENSE</sub> < 4 V; 0.5 A < I <sub>OUT</sub> < 4 A; I <sub>SENSE</sub> = 90% of I <sub>SENSEMAX</sub> (see <a href="#">Figure 4</a> )                                             |      | 40   | 100  | μs   |
| t <sub>DSENSE1L</sub>  | Delay response time from rising edge of CS_DIS pin                                         | V <sub>SENSE</sub> < 4 V; 0.5 A < I <sub>OUT</sub> < 4 A; I <sub>SENSE</sub> = 10% of I <sub>SENSEMAX</sub> (see <a href="#">Figure 4</a> )                                             |      | 5    | 20   | μs   |
| t <sub>DSENSE2H</sub>  | Delay response time from rising edge of INPUT pin                                          | V <sub>SENSE</sub> < 4 V; 0.5 A < I <sub>OUT</sub> < 4 A; I <sub>SENSE</sub> = 90% of I <sub>SENSEMAX</sub> (see <a href="#">Figure 4</a> )                                             |      | 80   | 250  | μs   |
| Δt <sub>DSENSE2H</sub> | Delay response time between rising edge of output current and rising edge of current sense | V <sub>SENSE</sub> < 4 V; I <sub>SENSE</sub> = 90% of I <sub>SENSEMAX</sub> , I <sub>OUT</sub> = 90% of I <sub>OUTMAX</sub> , I <sub>OUTMAX</sub> = 2 A (see <a href="#">Figure 7</a> ) |      |      | 40   | μs   |
| t <sub>DSENSE2L</sub>  | Delay response time from falling edge of INPUT pin                                         | V <sub>SENSE</sub> < 4 V; 0.5 A < I <sub>OUT</sub> < 4 A; I <sub>SENSE</sub> = 10% of I <sub>SENSEMAX</sub> (see <a href="#">Figure 4</a> )                                             |      | 80   | 250  | μs   |

1. Parameter guaranteed by design; it is not tested.
2. Fault condition includes: power limitation, overtemperature and open-load off-state detection.

**Table 10. Open load detection (8 V < V<sub>CC</sub> < 18 V)**

| Symbol                | Parameter                                                                             | Test conditions                                                                                                       | Min. | Typ.                         | Max. | Unit |
|-----------------------|---------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------|------|------------------------------|------|------|
| V <sub>OL</sub>       | Open load off-state voltage detection threshold                                       | V <sub>IN</sub> = 0 V                                                                                                 | 2    | See <a href="#">Figure 5</a> | 4    | V    |
| t <sub>DSTKON</sub>   | Output short circuit to V <sub>CC</sub> detection delay at turn-off                   | See <a href="#">Figure 5</a>                                                                                          | 180  |                              | 1200 | μs   |
| I <sub>L(off2)r</sub> | Off-state output current at V <sub>OUT</sub> = 4V                                     | V <sub>IN</sub> = 0V; V <sub>SENSE</sub> = 0 V; V <sub>OUT</sub> rising from 0 V to 4 V                               | -120 |                              | 0    | μA   |
| I <sub>L(off2)f</sub> | Off-state output current at V <sub>OUT</sub> = 2V                                     | V <sub>IN</sub> = 0V; V <sub>SENSE</sub> = V <sub>SENSEH</sub> ; V <sub>OUT</sub> falling from V <sub>CC</sub> to 2 V | -50  |                              | 90   | μA   |
| td_vol                | Delay response from output rising edge to V <sub>SENSE</sub> rising edge in open load | V <sub>OUT</sub> = 4 V; V <sub>IN</sub> = 0V; V <sub>SENSE</sub> = 90% of V <sub>SENSEH</sub>                         |      |                              | 20   | μs   |

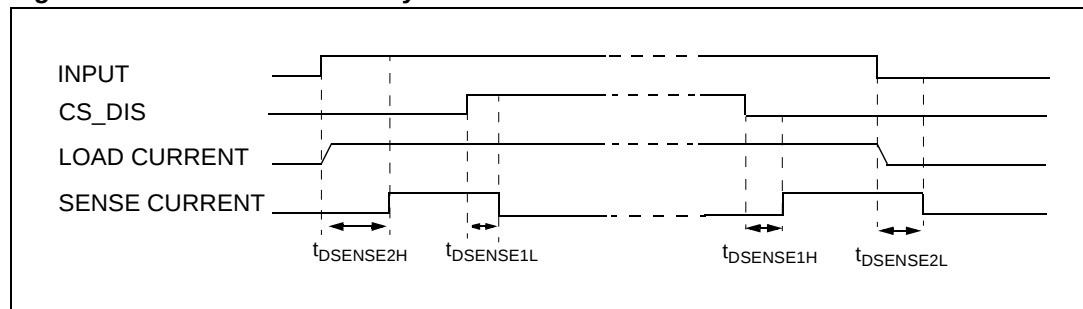
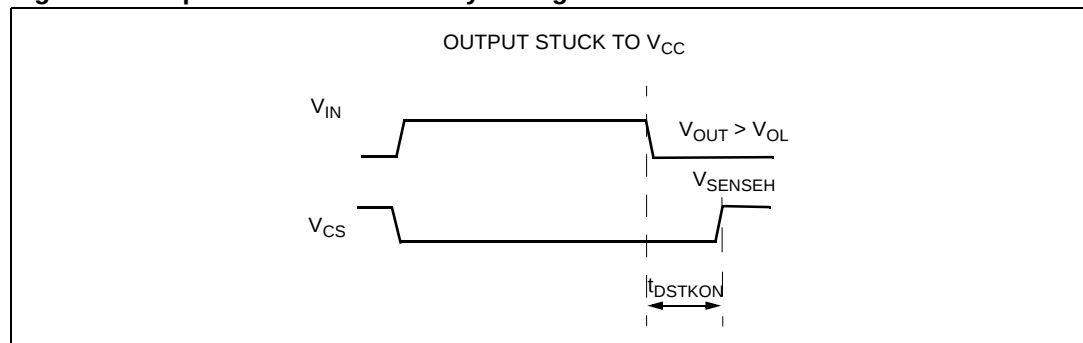
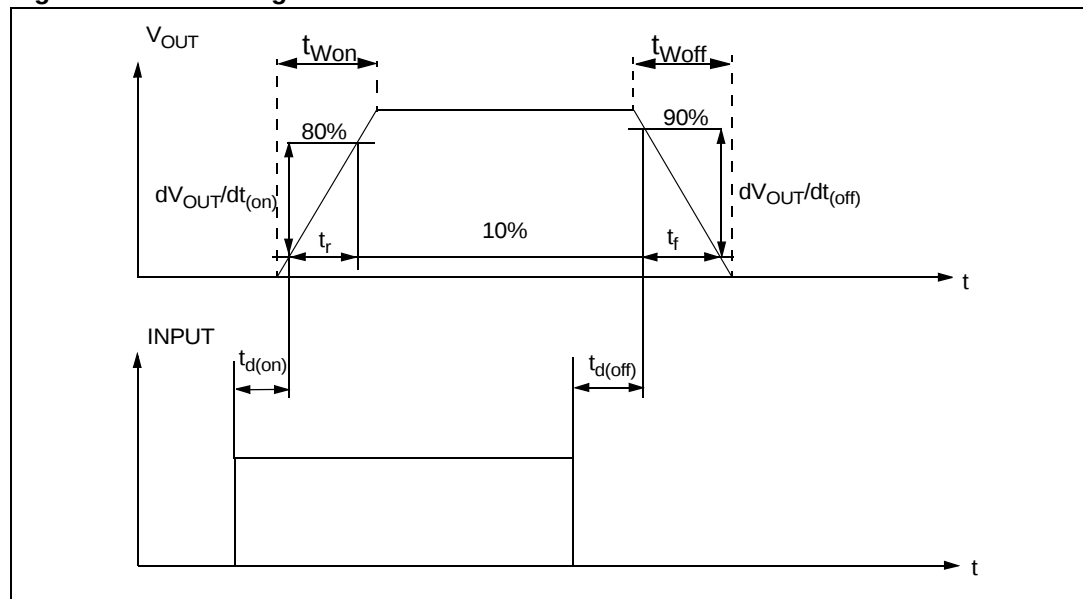
**Figure 4. Current sense delay characteristics****Figure 5. Open-load off-state delay timing****Figure 6. Switching characteristics**

Figure 7. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)

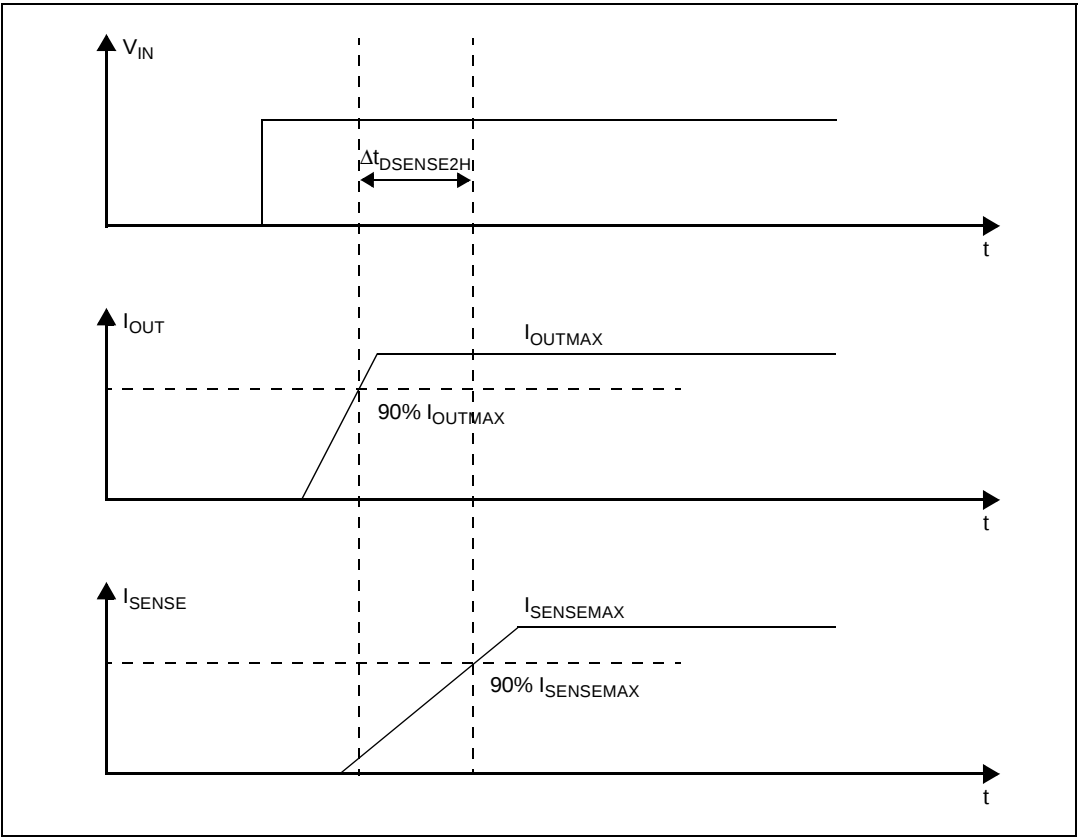


Figure 8. Output voltage drop limitation

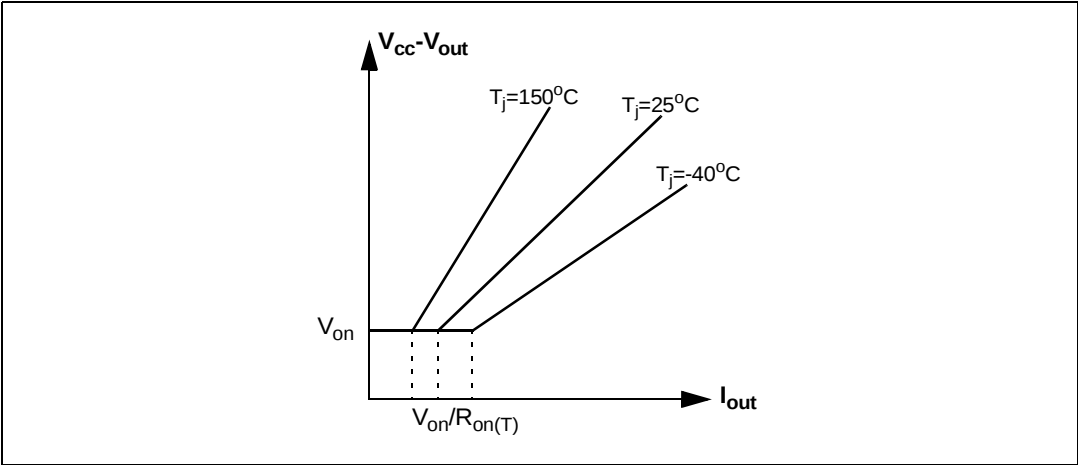


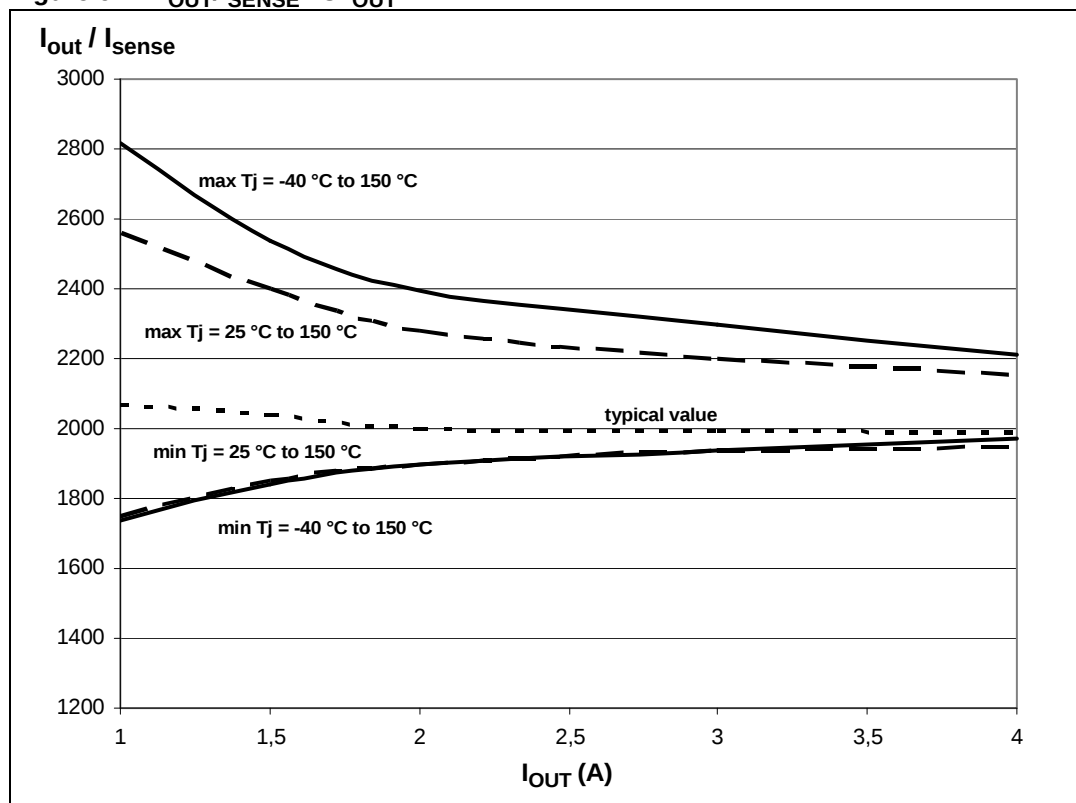
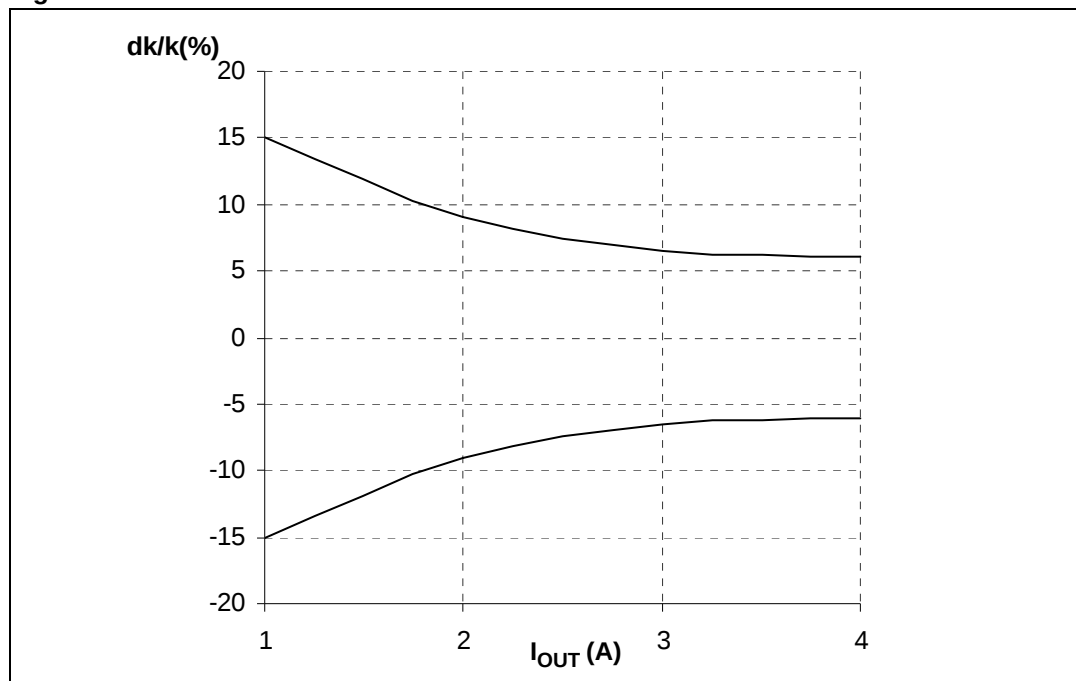
Figure 9.  $I_{OUT}/I_{SENSE}$  vs  $I_{OUT}$ 

Figure 10. Maximum current sense ratio drift vs load current



Note: Parameter guaranteed by design; it is not tested.

**Table 11. Truth table**

| Conditions                                                      | Input | Output                        | Sense ( $V_{CSD} = 0\text{ V}$ ) <sup>(1)</sup> |
|-----------------------------------------------------------------|-------|-------------------------------|-------------------------------------------------|
| Normal operation                                                | L     | L                             | 0                                               |
|                                                                 | H     | H                             | Nominal                                         |
| Overtemperature                                                 | L     | L                             | 0                                               |
|                                                                 | H     | L                             | $V_{SENSEH}$                                    |
| Undervoltage                                                    | L     | L                             | 0                                               |
|                                                                 | H     | L                             | 0                                               |
| Overload                                                        | H     | X<br>(no power limitation)    | Nominal                                         |
|                                                                 | H     | Cycling<br>(power limitation) | $V_{SENSEH}$                                    |
| Short circuit to GND<br>(power limitation)                      | L     | L                             | 0                                               |
|                                                                 | H     | L                             | $V_{SENSEH}$                                    |
| Open load off-state<br>(with external pull-up)                  | L     | H                             | $V_{SENSEH}$                                    |
| Short circuit to $V_{CC}$<br>(external pull-up<br>disconnected) | L     | H                             | $V_{SENSEH}$                                    |
|                                                                 | H     | H                             | $V_{SENSEH}$<br>< Nominal                       |
| Negative output voltage<br>clamp                                | L     | L                             | 0                                               |

1. If the  $V_{CSD}$  is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

**Table 12. Electrical transient requirements (part 1)**

| ISO 7637-2:<br>2004(E)<br>test pulse | Test levels <sup>(1)</sup> |       | Number of<br>pulses or<br>test times | Burst cycle/pulse<br>repetition time |       | Delays and<br>Impedance |
|--------------------------------------|----------------------------|-------|--------------------------------------|--------------------------------------|-------|-------------------------|
|                                      | III                        | IV    |                                      | Min.                                 | Max.  |                         |
| 1                                    | -75V                       | -100V | 5000 pulses                          | 0.5s                                 | 5s    | 2 ms, 10Ω               |
| 2a                                   | +37V                       | +50V  | 5000 pulses                          | 0.2s                                 | 5s    | 50μs, 2Ω                |
| 3a                                   | -100V                      | -150V | 1h                                   | 90ms                                 | 100ms | 0.1μs, 50Ω              |
| 3b                                   | +75V                       | +100V | 1h                                   | 90ms                                 | 100ms | 0.1μs, 50Ω              |
| 4                                    | -6V                        | -7V   | 1 pulse                              |                                      |       | 100ms, 0.01Ω            |
| 5b <sup>(2)</sup>                    | +65V                       | +87V  | 1 pulse                              |                                      |       | 400ms, 2Ω               |

1. The above test levels must be considered referred to  $V_{CC} = 13.5V$  except for pulse 5b.

2. Valid in case of external load dump clamp: 40V maximum referred to ground.

**Table 13. Electrical transient requirements (part 2)**

| ISO 7637-2:<br>2004E<br>test pulse | Test level results |    |
|------------------------------------|--------------------|----|
|                                    | III                | VI |
| 1                                  | C                  | C  |
| 2a                                 | C                  | C  |
| 3a                                 | C                  | C  |
| 3b                                 | C                  | C  |
| 4                                  | C                  | C  |
| 5b <sup>(1)</sup>                  | C                  | C  |

1. Valid in case of external load dump clamp: 40V maximum referred to ground.

**Table 14. Electrical transient requirements (part 3)**

| Class | Contents                                                                                                                                                               |
|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| C     | All functions of the device performed as designed after exposure to disturbance.                                                                                       |
| E     | One or more functions of the device did not perform as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device. |

## 2.4 Waveforms

Figure 11. Normal operation

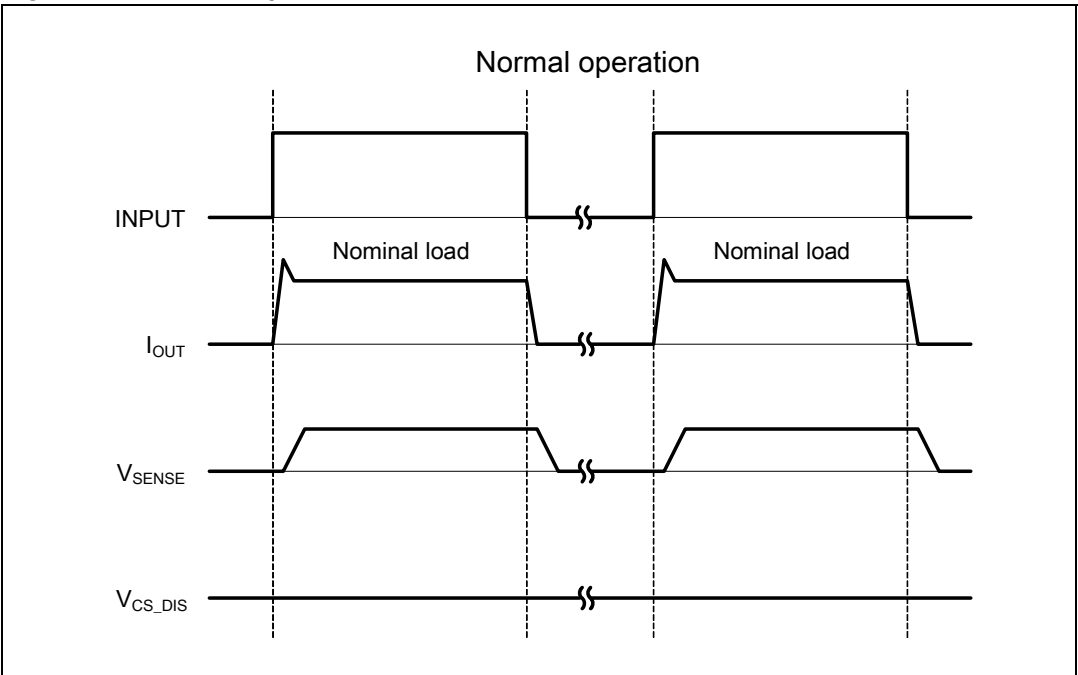


Figure 12. Overload or short to GND

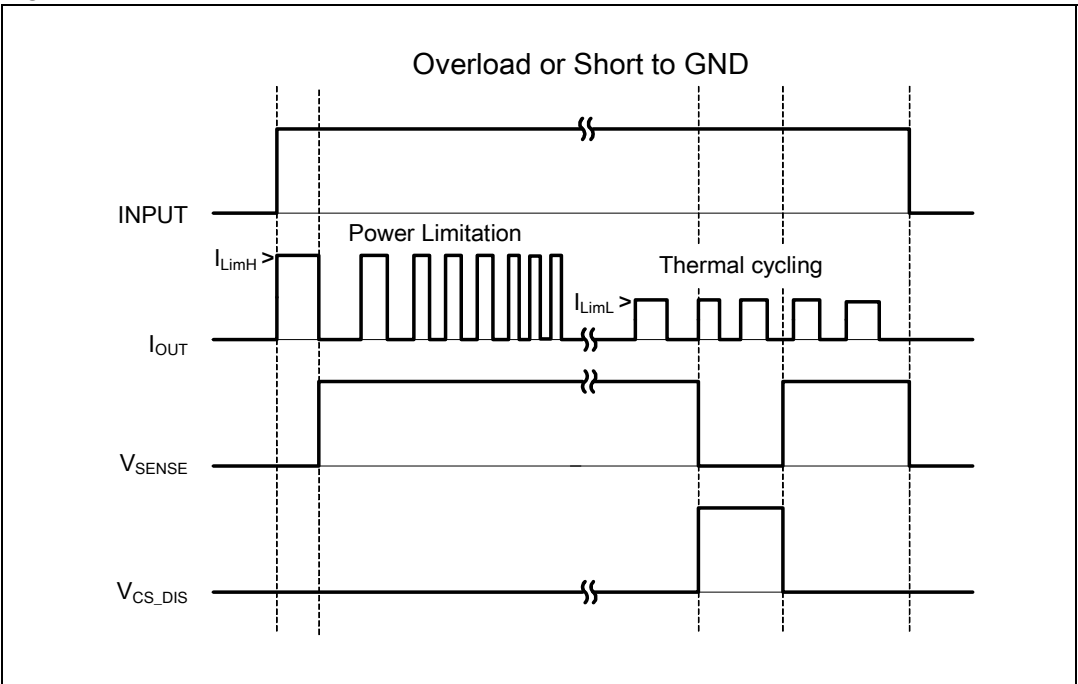


Figure 13. Intermittent overload

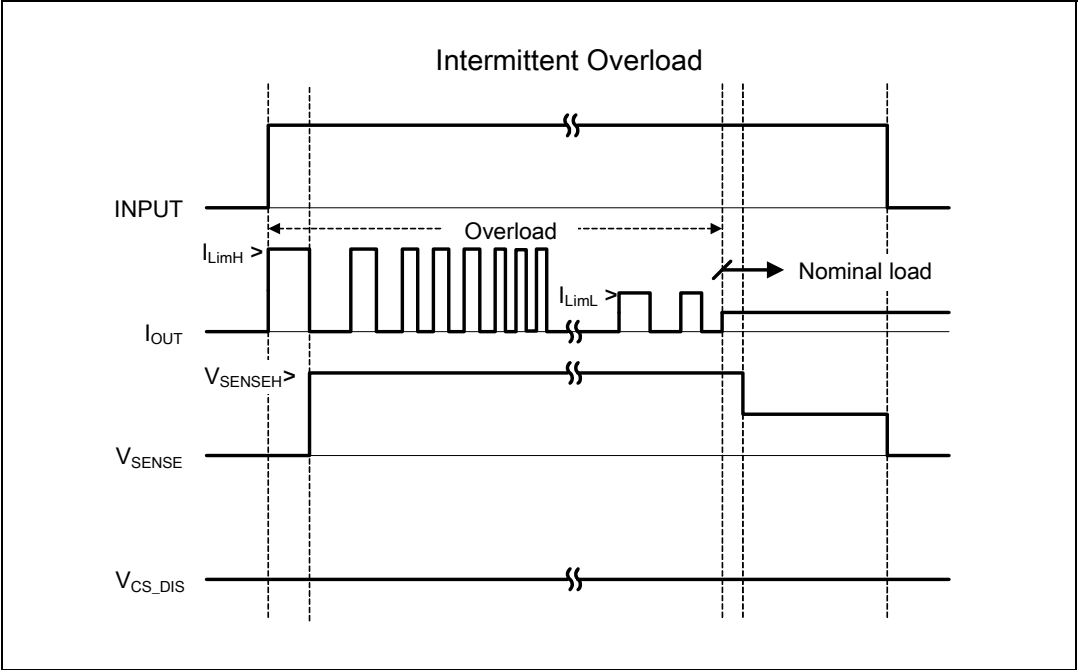


Figure 14. Off-state open-load with external circuitry

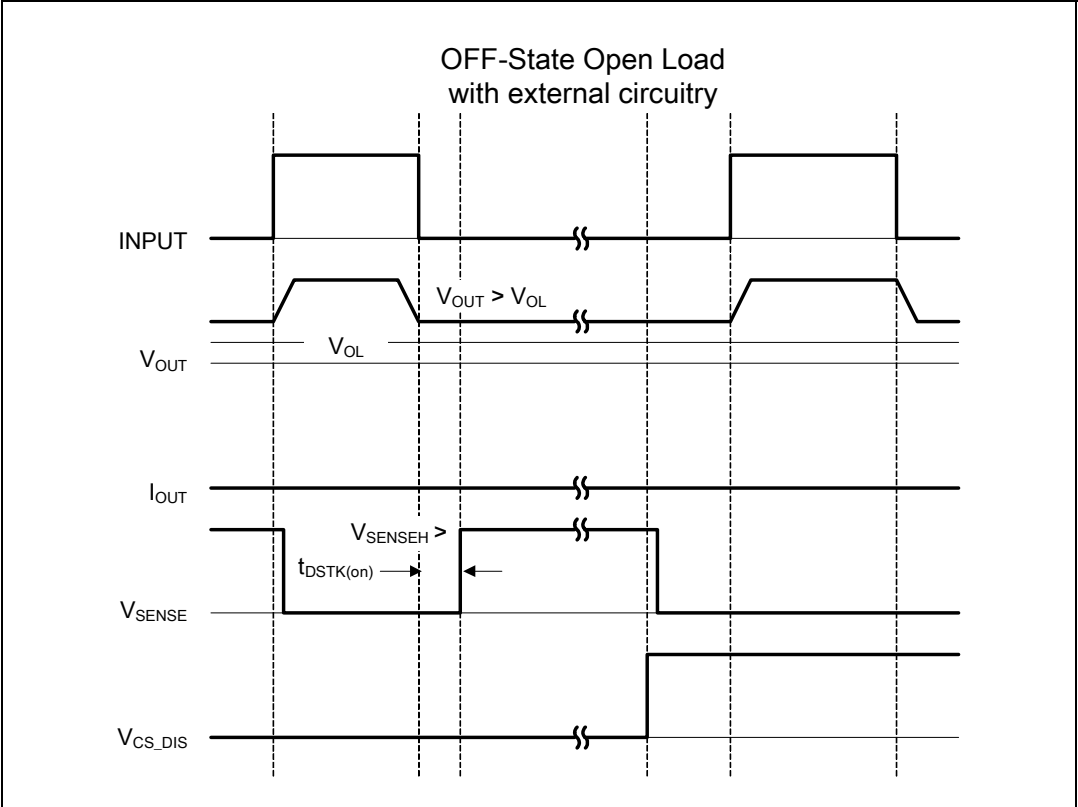


Figure 15. Short to  $V_{CC}$

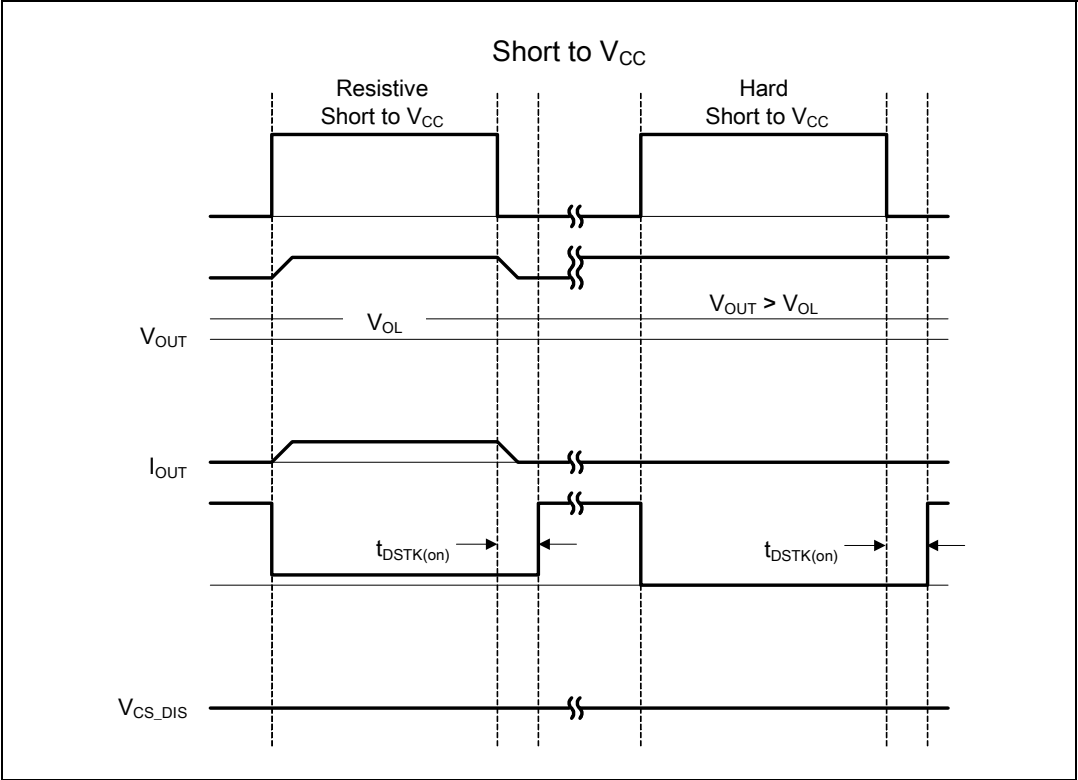
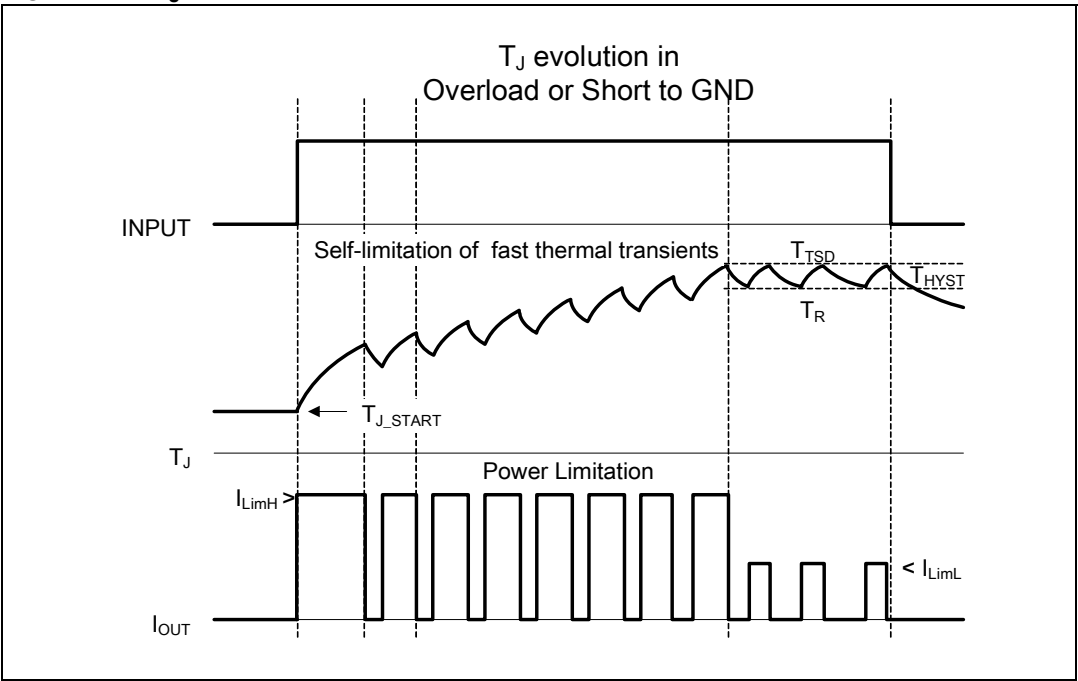


Figure 16.  $T_J$  evolution in overload or short to GND



2.5 Electrical characteristics curves

Figure 17. Off-state output current

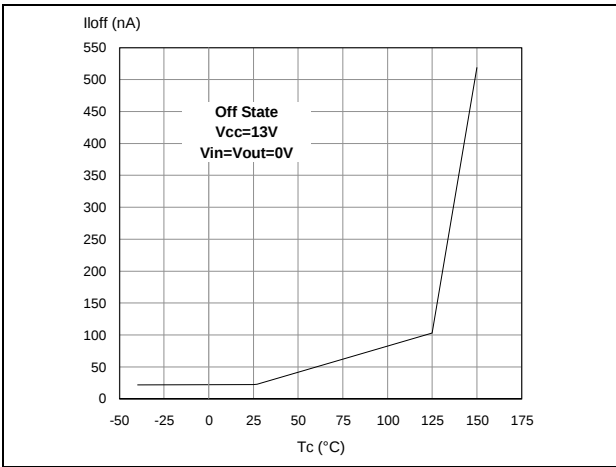


Figure 18. High level input current

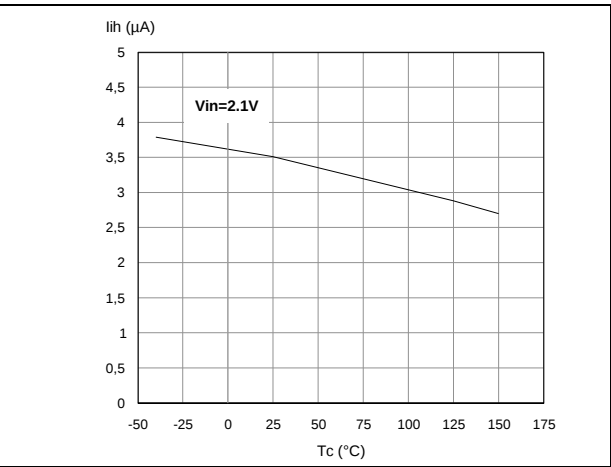


Figure 19. Input clamp voltage

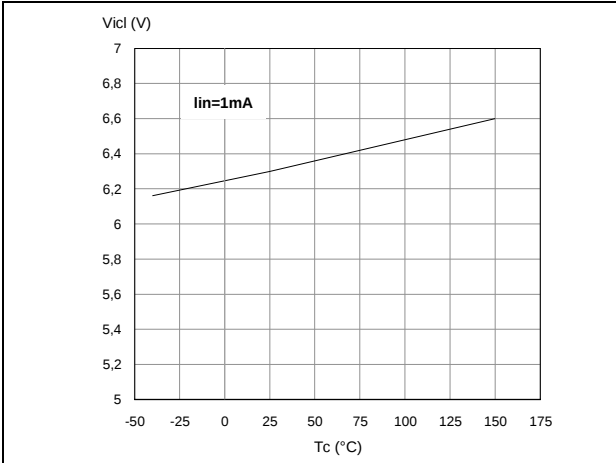


Figure 20. Input low level

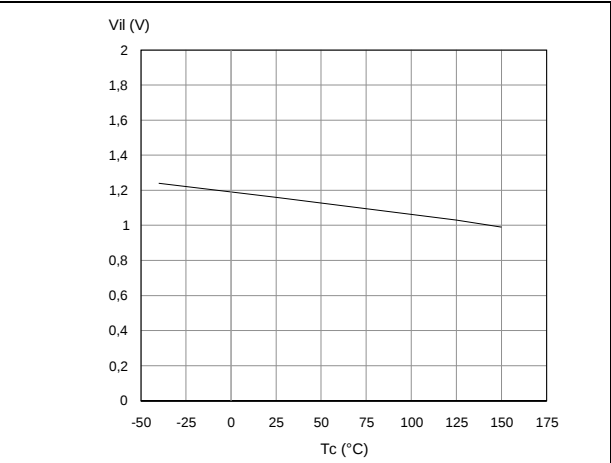


Figure 21. Input high level

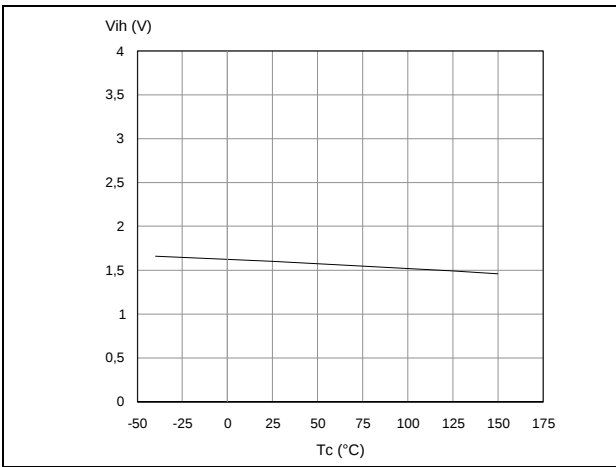


Figure 22. Input hysteresis voltage

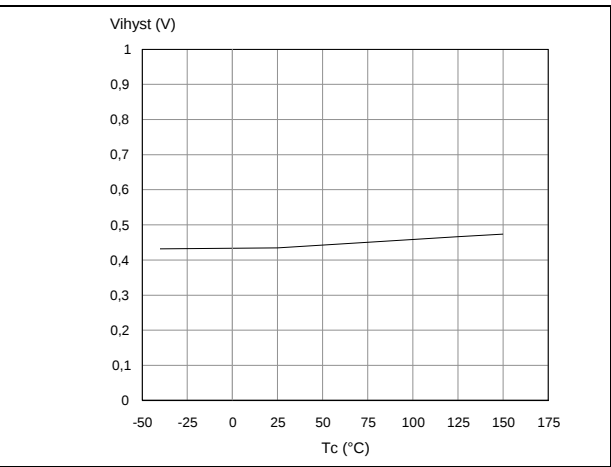


Figure 23. On-state resistance vs  $T_{case}$

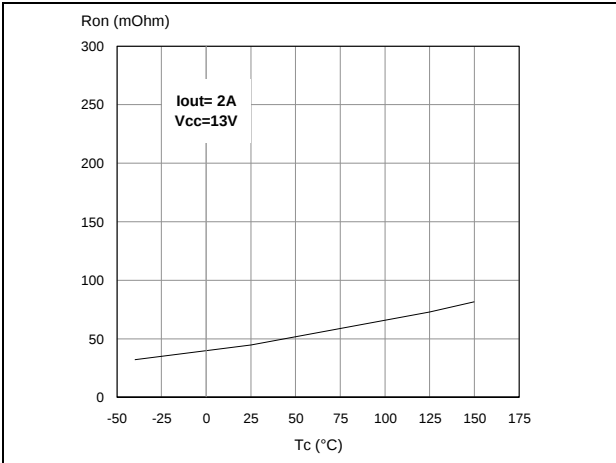


Figure 24. On-state resistance vs  $V_{CC}$

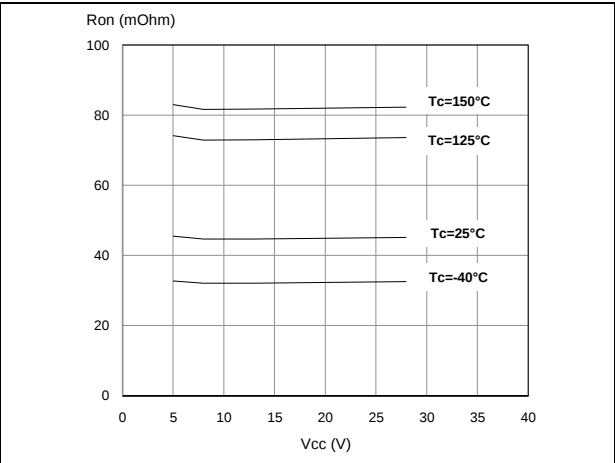


Figure 25. Undervoltage shutdown

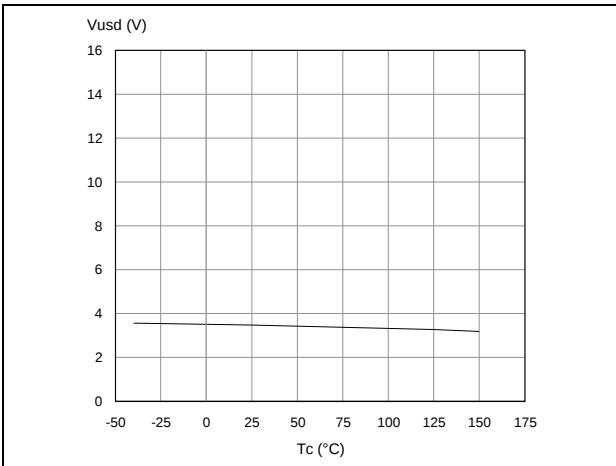


Figure 26. Turn-on voltage slope

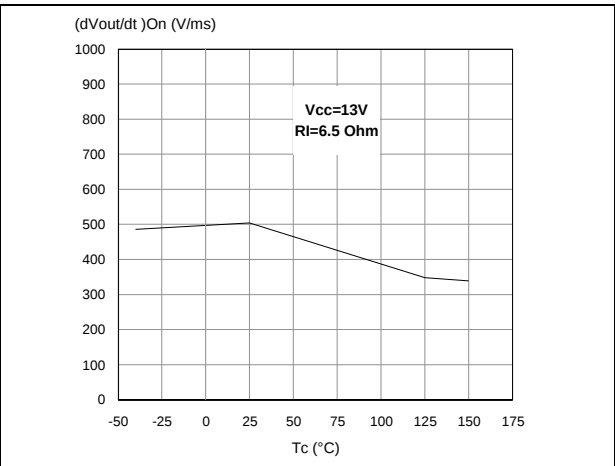


Figure 27.  $I_{LIMH}$  vs  $T_{case}$

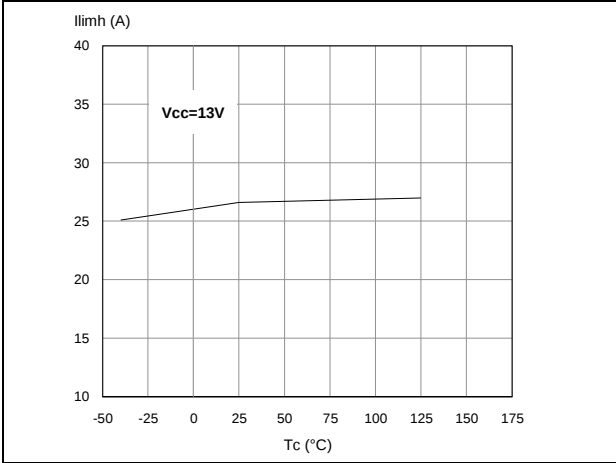


Figure 28. Turn-off voltage slope

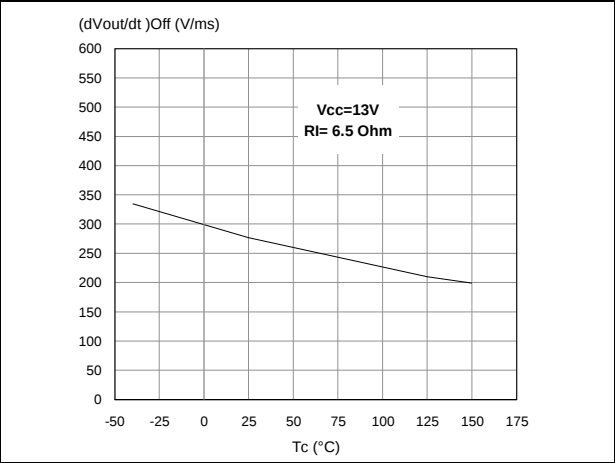


Figure 29. CS\_DIS high level voltage

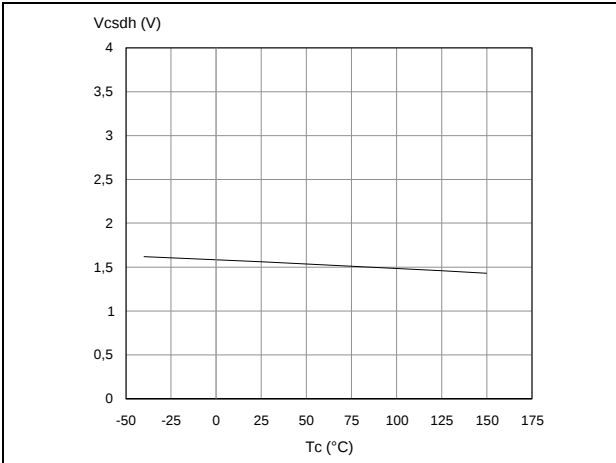


Figure 30. CS\_DIS clamp voltage

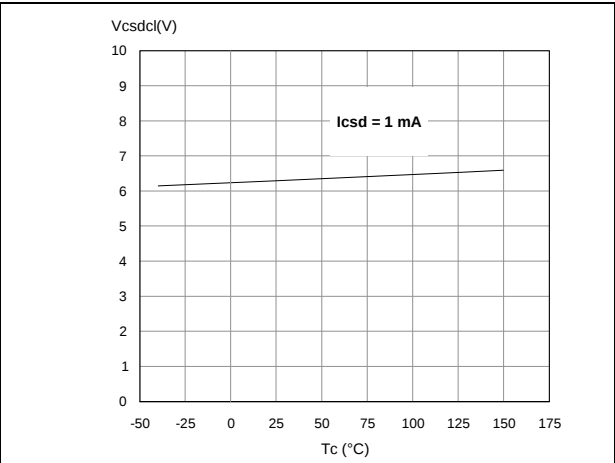
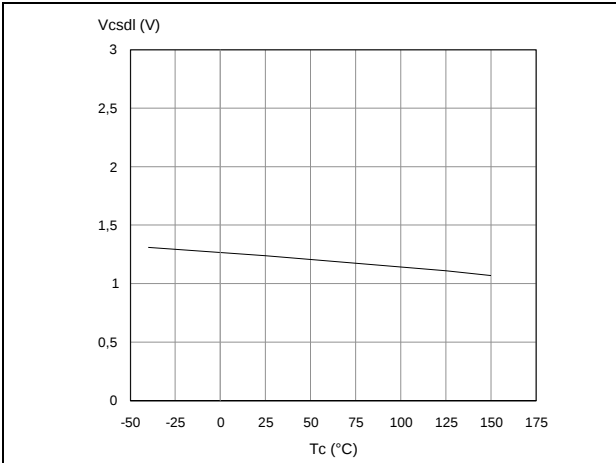


Figure 31. CS\_DIS low level voltage





If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize [Section 3.1.2: Solution 2: diode \(D<sub>GND</sub>\) in the ground line](#).

### 3.1.2 Solution 2: diode (D<sub>GND</sub>) in the ground line

A resistor (R<sub>GND</sub> = 1 kΩ) should be inserted in parallel to D<sub>GND</sub> if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift (≈600 mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD share the same diode/resistor network.

## 3.2 Load dump protection

D<sub>ld</sub> is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V<sub>CC</sub> maximum DC rating. The same applies if the device is subject to transients on the V<sub>CC</sub> line which are greater than the ones shown in the ISO 7637-2: 2004(E) table.

## 3.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the V<sub>CC</sub> line, the control pins are pulled negative. ST suggests to insert a resistor (R<sub>prot</sub>) in line to prevent the microcontroller I/O pins from latching-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os:

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For V<sub>CCpeak</sub> = - 100V and I<sub>latchup</sub> ≥ 20mA; V<sub>OHμC</sub> ≥ 4.5V

$$5k\Omega \leq R_{prot} \leq 180k\Omega$$

Recommended values: R<sub>prot</sub> = 10kΩ, C<sub>EXT</sub> = 10nF.

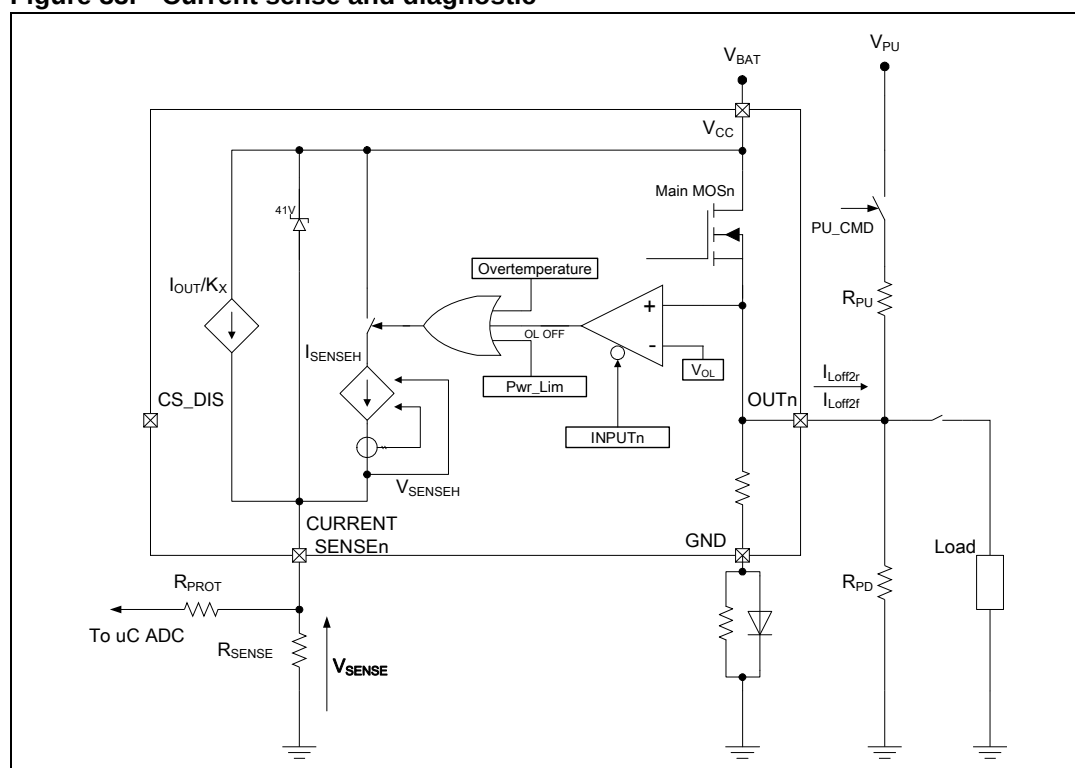
## 3.4 Current sense and diagnostic

The current sense pin performs a double function (see [Figure 33: Current sense and diagnostic](#)):

- **Current mirror of the load current in normal operation**, delivering a current proportional to the load current according to a known ratio K<sub>X</sub>.  
The current I<sub>SENSE</sub> can be easily converted to a voltage V<sub>SENSE</sub> by means of an external resistor R<sub>SENSE</sub>. Linearity between I<sub>OUT</sub> and V<sub>SENSE</sub> is ensured up to 5V minimum (see parameter V<sub>SENSE</sub> in [Table 9: Current sense \(8 V < V<sub>CC</sub> < 18 V\)](#)). The current sense accuracy depends on the output current (refer to current sense electrical

- **Diagnostic flag in fault conditions**, delivering a fixed voltage  $V_{SENSEH}$  up to a maximum current  $I_{SENSEH}$  in case of the following fault conditions (refer to [Table 11: Truth table](#)):
  - Power limitation activation
  - Overtemperature
  - Short to  $V_{CC}$  in off-state
  - Open-load in off-state with additional external components.

**Figure 33. Current sense and diagnostic**



### Short to $V_{CC}$

### Off-state open load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor ( $R_{PU}$ ) connecting the output to a positive supply voltage ( $V_{PU}$ ).

It is preferable that  $V_{PU}$  is switched off during the module standby mode to avoid an increase in overall standby current consumption in normal conditions, that is, when the load is connected.

An external pull-down resistor ( $R_{PD}$ ) connected between output and GND is mandatory to avoid misdetection in case of floating outputs in off-state (see [Figure 33: Current sense and diagnostic](#)).

$R_{PD}$  must be selected in order to ensure  $V_{OUT} < V_{OLmin}$  unless pulled up by the external circuitry:

$$V_{OUT}|_{Pull-up\_OFF} = R_{PD} \cdot I_{L(off)2f} < V_{OLmin} = 2V$$

$R_{PD} \leq 22\text{ K}\Omega$  is recommended.

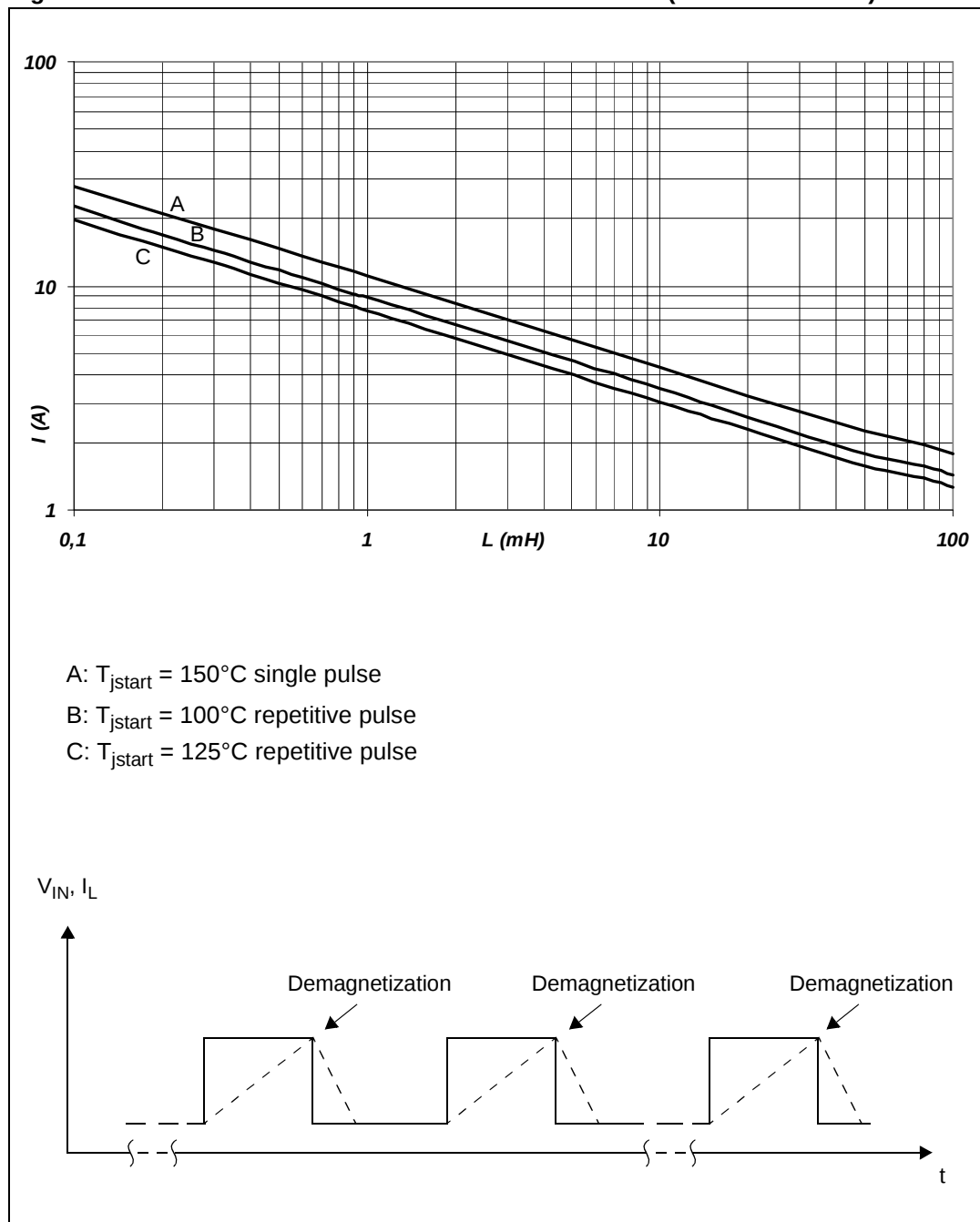
For proper open load detection in off-state, the external pull-up resistor must be selected according to the following formula:

$$V_{OUT}|_{Pull-up\_ON} = \frac{R_{PD} \cdot V_{PU} - R_{PU} \cdot R_{PD} \cdot I_{L(off)2r}}{R_{PU} + R_{PD}} > V_{OLmax} = 4V$$

For the values of  $V_{OLmin}$ ,  $V_{OLmax}$ ,  $I_{L(off)2r}$  and  $I_{L(off)2f}$  see [Table 10: Open load detection](#) ( $8\text{ V} < V_{CC} < 18\text{ V}$ ).

### 3.5 Maximum demagnetization energy ( $V_{CC} = 13.5V$ )

Figure 34. Maximum turn-off current versus inductance (for each channel)



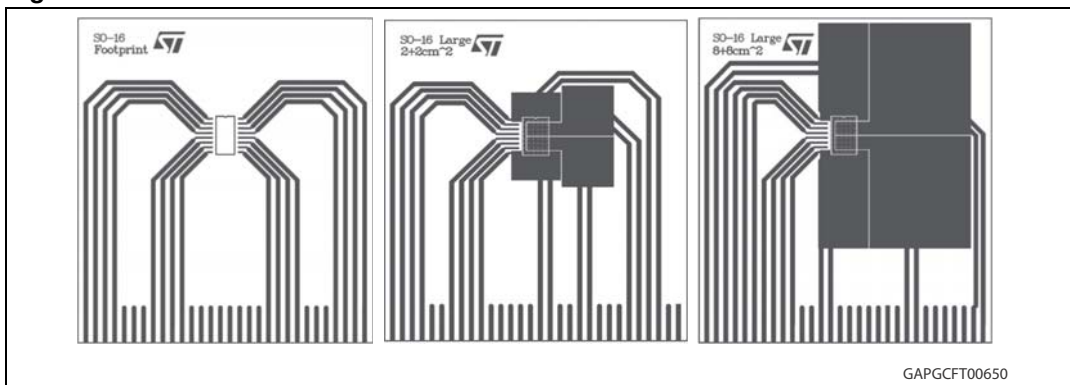
Note:

Values are generated with  $R_L = 0 \Omega$ . In case of repetitive pulses,  $T_{jstart}$  (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

## 4 Package and PCB thermal data

### 4.1 SO-16L thermal data

Figure 35. SO-16L PC board



Note:

Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: Double layer, Thermal Vias, FR4 area = 77 mm x 86 mm, PCB thickness = 1.6 mm, Cu thickness = 70  $\mu$ m (front and back side), Copper areas: from minimum pad lay-out to 8 cm<sup>2</sup>).

Figure 36.  $R_{thj-amb}$  vs PCB copper area in open box free air condition

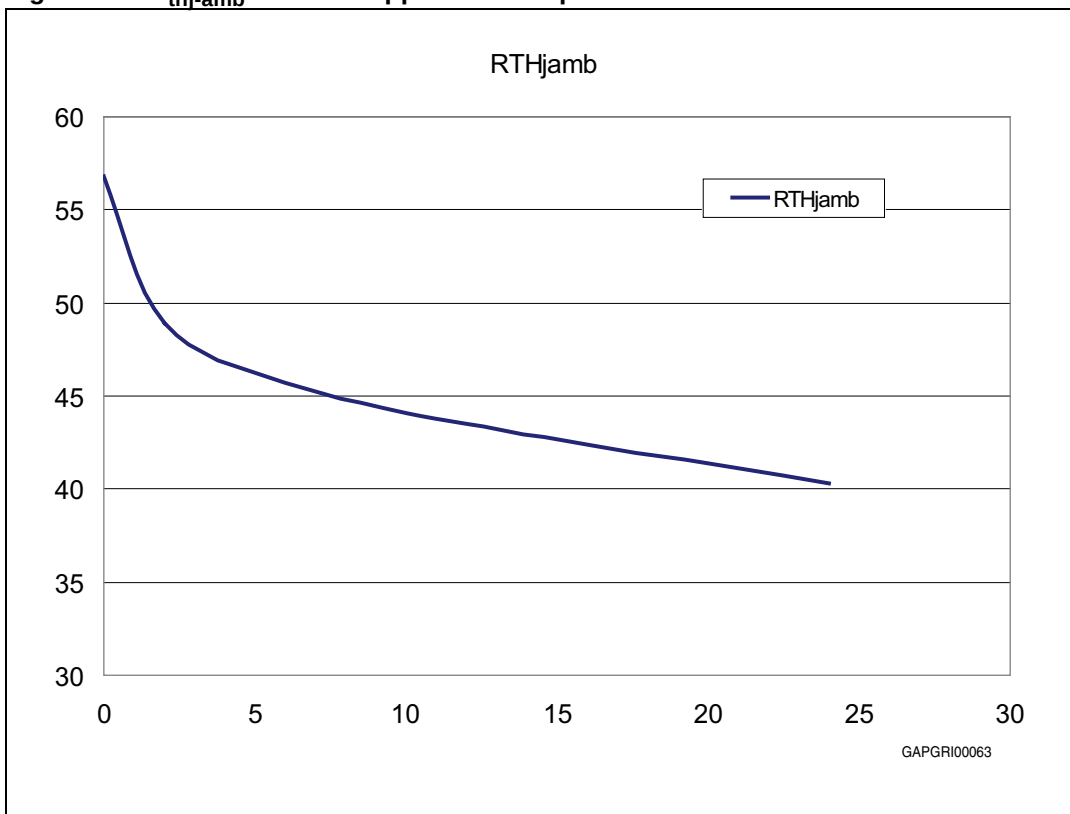
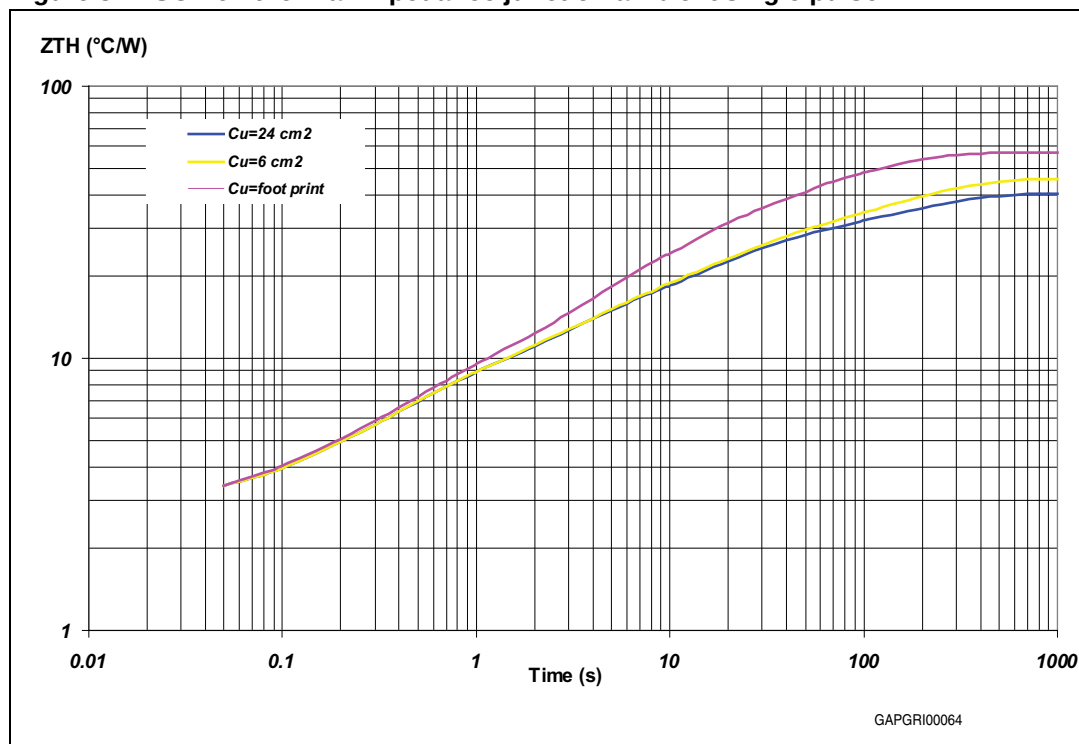


Figure 37. SO-16L thermal impedance junction ambient single pulse

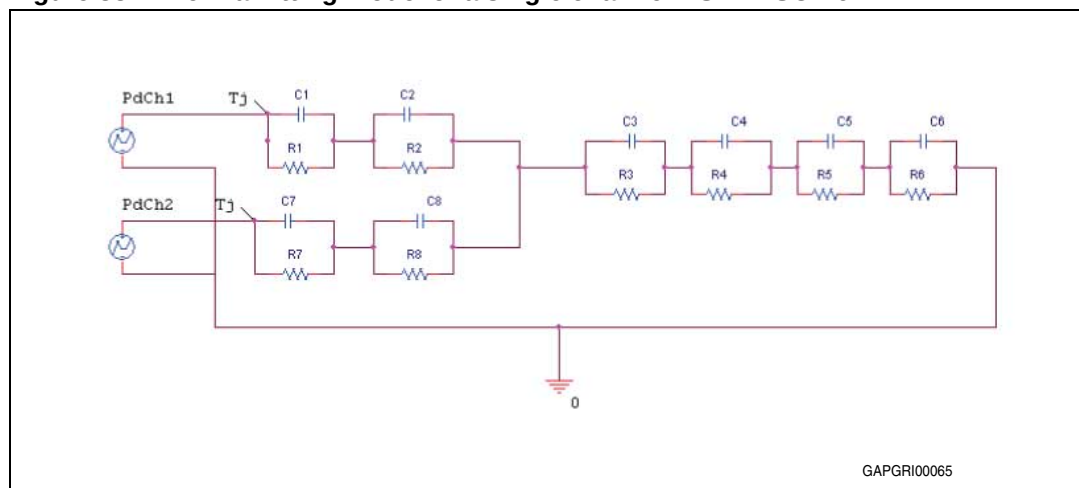


Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 38. Thermal fitting model of a single channel HSD in SO-16L (a)



- a. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 15. Thermal parameter

| Areal/island (cm <sup>2</sup> ) | Footprint | 2   | 8    |
|---------------------------------|-----------|-----|------|
| R1 (°C/W)                       | 0.7       |     |      |
| R2 (°C/W)                       | 2.1       |     |      |
| R3 (°C/W)                       | 4         |     |      |
| R4 (°C/W)                       | 8         | 6   | 6    |
| R5 (°C/W)                       | 14        | 13  | 13   |
| R6 (°C/W)                       | 28        | 20  | 14.5 |
| R7 (°C/W)                       | 0.7       |     |      |
| R8 (°C/W)                       | 2.1       |     |      |
| C1 (W.s/°C)                     | 0.001     |     |      |
| C2 (W.s/°C)                     | 0.005     |     |      |
| C3 (W.s/°C)                     | 0.1       |     |      |
| C4 (W.s/°C)                     | 0.5       |     |      |
| C5 (W.s/°C)                     | 1         | 1.5 | 1.5  |
| C6 (W.s/°C)                     | 3         | 9   | 12   |
| C7 (W.s/°C)                     | 0.001     |     |      |
| C8 (W.s/°C)                     | 0.005     |     |      |

## 5 Package information

### 5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).

ECOPACK® is an ST trademark.

### 5.2 Package mechanical data

Figure 39. SO-16L package dimensions

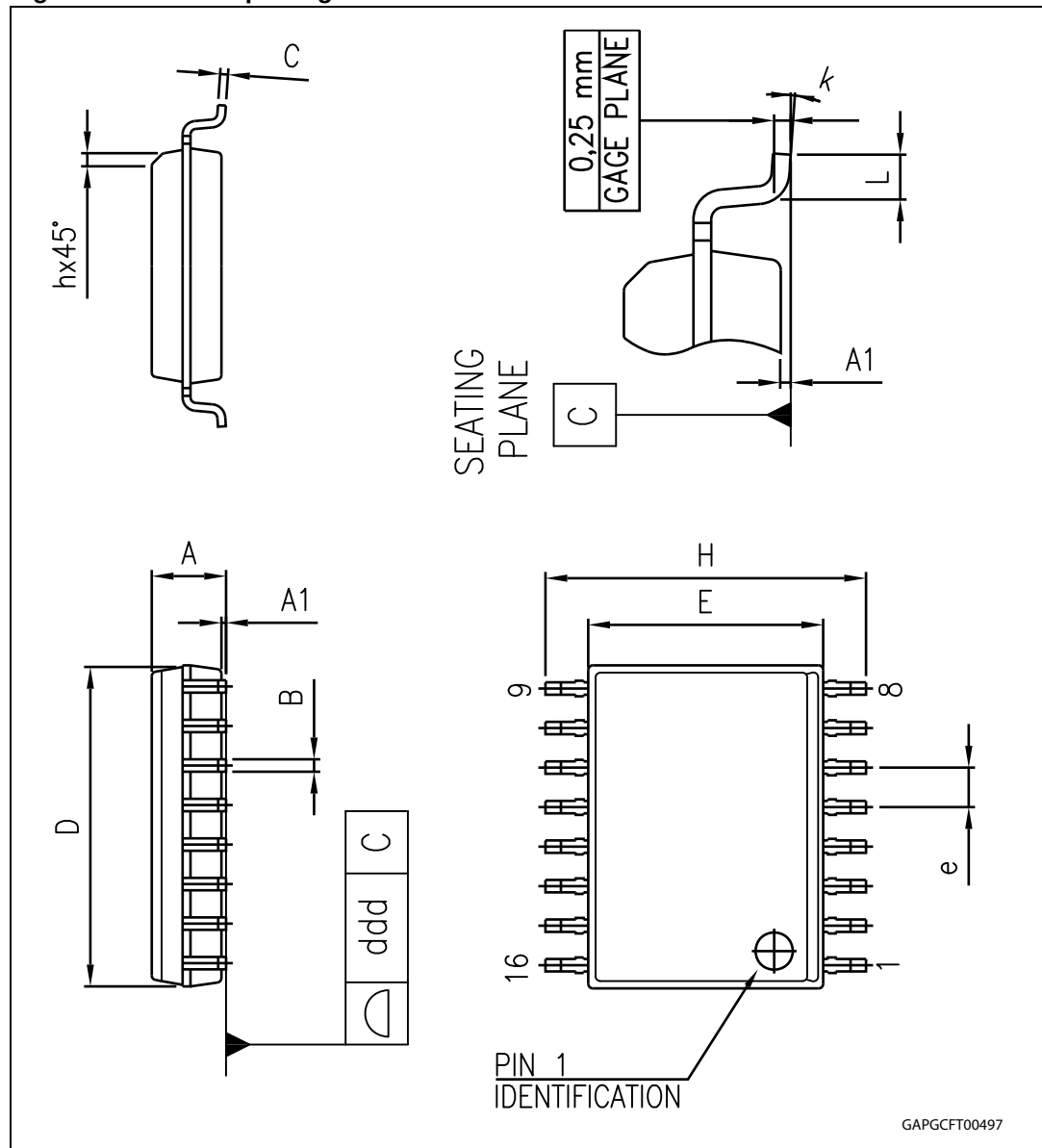


Table 16. SO-16L mechanical data

| Symbol | Millimeters |      |       |
|--------|-------------|------|-------|
|        | Min         | Typ  | Max   |
| A      | 2.35        |      | 2.65  |
| A1     | 0.10        |      | 0.30  |
| B      | 0.33        |      | 0.51  |
| C      | 0.23        |      | 0.32  |
| D      | 10.10       |      | 10.50 |
| E      | 7.40        |      | 7.60  |
| e      |             | 1.27 |       |
| H      | 10.00       |      | 10.65 |
| h      | 0.25        |      | 0.75  |
| L      | 0.40        |      | 1.27  |
| k      | 0°          |      | 8°    |
| ddd    |             |      | 0.10  |

# 5.3 Packing information

Figure 40. SO-16L tube shipment (no suffix)

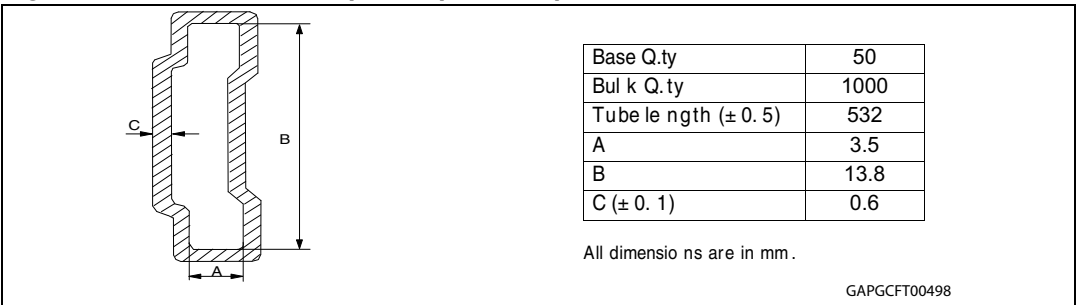
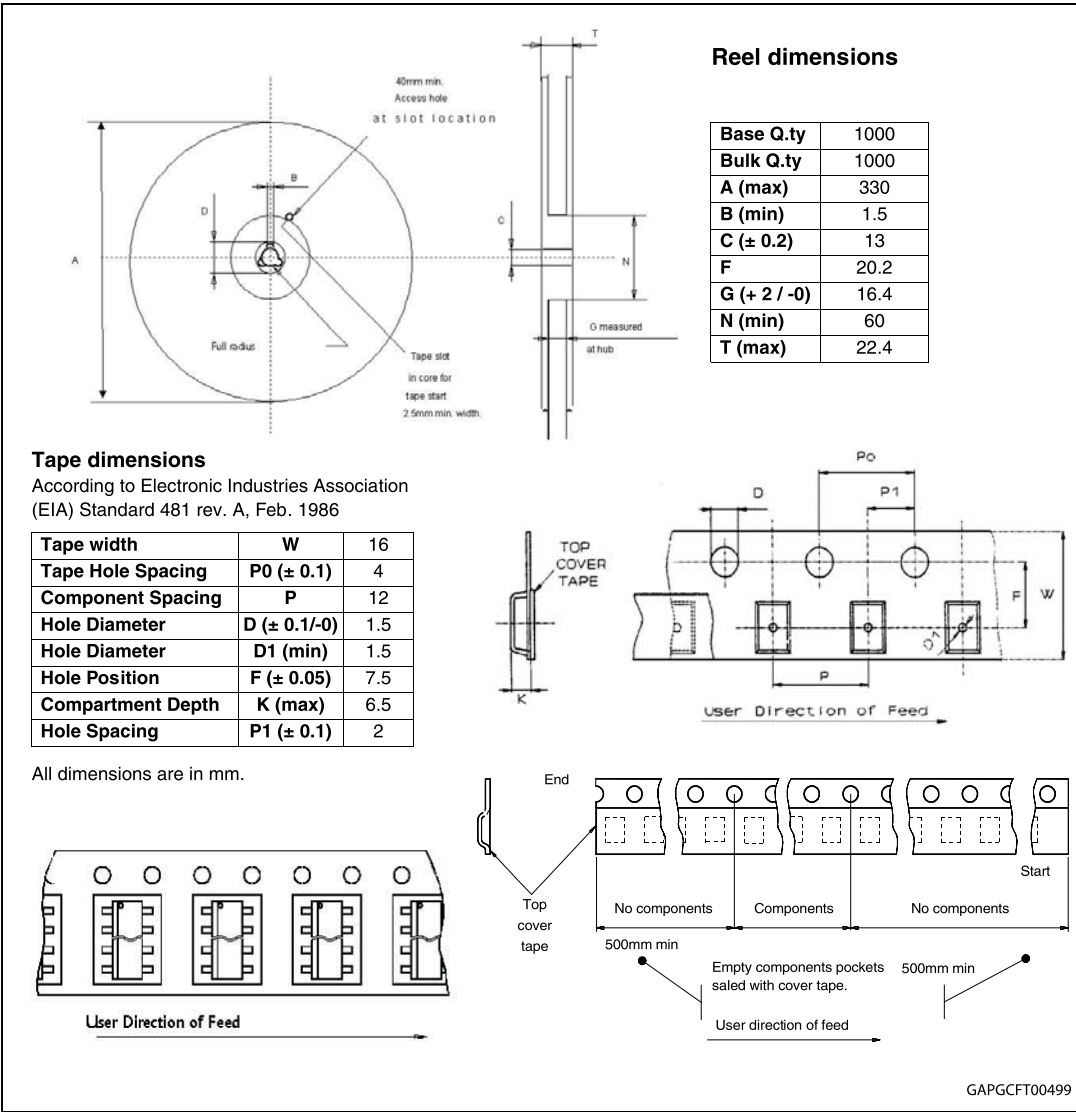


Figure 41. SO-16L tape and reel shipment (suffix “TR”)



## 6 Order codes

Table 17. Device summary

| Package | Order codes   |                 |
|---------|---------------|-----------------|
|         | Tube          | Tape and reel   |
| SO-16L  | VND5E050ASO-E | VND5E050ASOTR-E |

## 7 Revision history

**Table 18. Document revision history**

| Date         | Revision | Changes                                                                                            |
|--------------|----------|----------------------------------------------------------------------------------------------------|
| 10-Nov-2011  | 1        | Initial release.                                                                                   |
| 19-Dec-2011  | 2        | Updated <a href="#">Figure 2</a> .                                                                 |
| 15-Mar-2012  | 3        | Added <a href="#">Section 4: Package and PCB thermal data</a> and update <a href="#">Table 5</a> . |
| 26-June-2012 | 4        | Update <a href="#">Table 4: Thermal data</a> .                                                     |
| 25-Sep-2012  | 5        | Update <a href="#">Table 4: Thermal data</a> .                                                     |
| 18-Sep-2013  | 6        | Updated disclaimer.                                                                                |

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