

NLAS5213

1 Ω R_{ON} DPST and Dual SPST Switches

The NLAS5213A and NLAS5213B are DPST and Dual SPST devices, respectively. They each consist of 2 single throw switches and are both designed for audio applications within portable devices. The NLAS5213A is controlled with a single enable pin while the NLAS5213B has two independent enables.

Both the NLAS5213A and NLAS5213B operate over a wide V_{CC} range, 1.65 V to 4.5 V, and maintain a very low R_{ON} : 1.3 Ω Max @ $V_{CC} = 4.2$ V. Each is available in a choice of two packages: US8 and UDFN8.

Features

- PST and Dual SPST Pinouts
- R_{ON} : 1.3 Ω Max @ $V_{CC} = 4.2$ V
- V_{CC} Range: 1.65 V to 4.5 V
- 8 kV Human Body Model ESD on I/O to GND
- UDFN8 or US8 Packages Available
- These are Pb-Free Devices

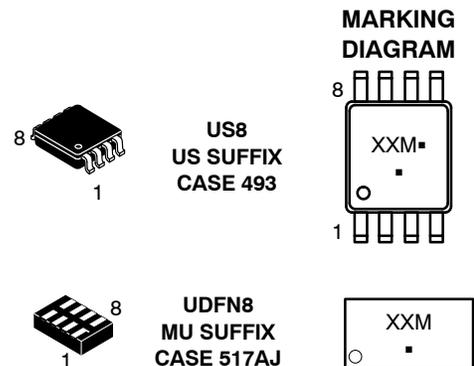
Typical Applications

- Mobile Phones
- Portable Devices



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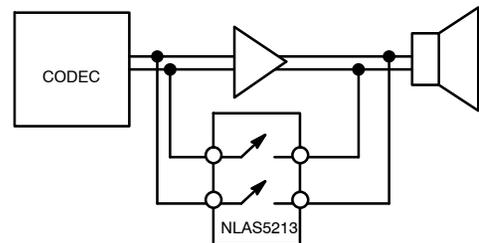
<http://onsemi.com>



XX = Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

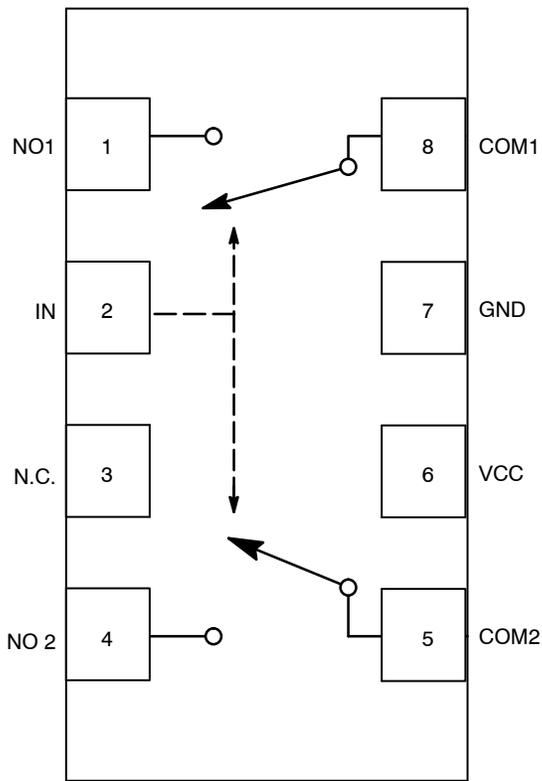
APPLICATION DIAGRAM



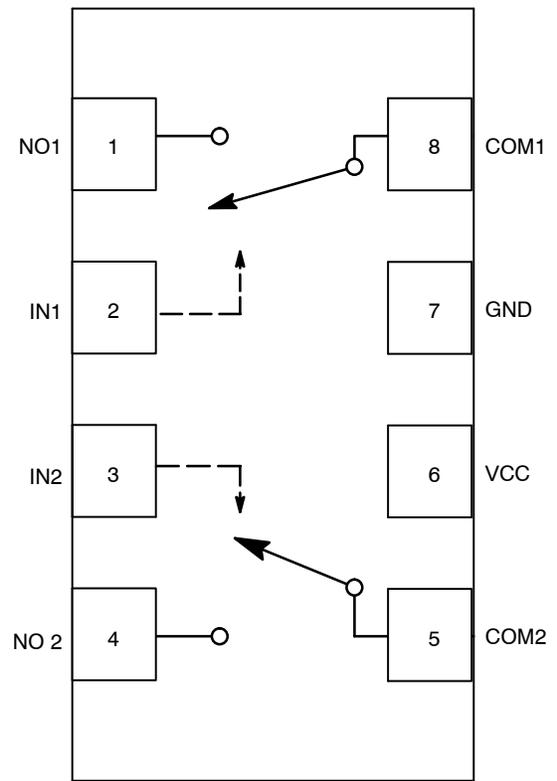
ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 9 of this data sheet.

NLAS5213

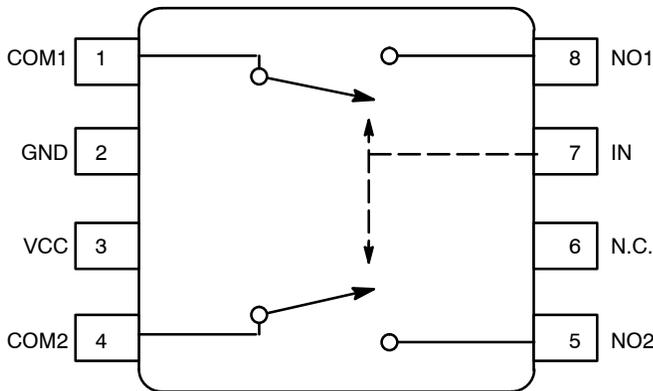


NLAS5213A

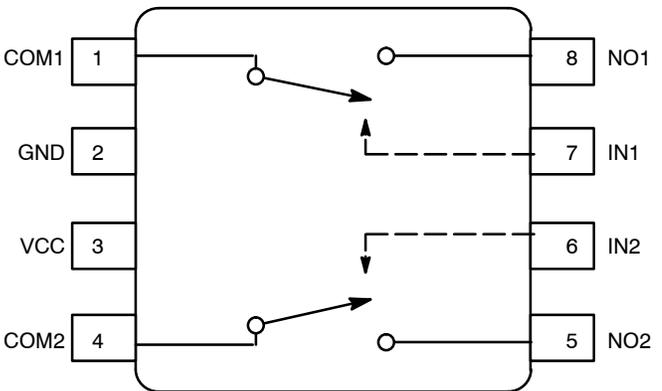


NLAS5213B

Figure 1. Functional Block Diagram Pinouts (UDFN8)



NLAS5213A



NLAS5213B

Figure 2. Functional Block Diagram Pinouts (US8)

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NLAS5213A

Pin #		Name	Direction	Description
UDFN8	US8			
1	8	NO1	I/O	Normally Open Signal Line of Switch 1
2	7	IN	Input	Control Input
3	6	N.C.	N/A	No Connect
4	5	NO2	I/O	Normally Open Signal Line of Switch 2
5	4	COM2	I/O	Common Signal Line of Switch 2
6	3	V _{CC}	Input	Analog Supply Voltage
7	2	GND	Input	Ground
8	1	COM1	I/O	Common Signal Line of Switch 1

NLAS5213B

Pin #		Name	Direction	Description
UDFN8	US8			
1	8	NO1	I/O	Normally Open Signal Line of Switch 1
2	7	IN1	Input	Control Input of Switch 1
3	6	IN2	Input	Control Input of Switch 2
4	5	NO2	I/O	Normally Open Signal Line of Switch 2
5	4	COM2	I/O	Common Signal Line of Switch 2
6	3	V _{CC}	Input	Analog Supply Voltage
7	2	GND	Input	Ground
8	1	COM1	I/O	Common Signal Line of Switch 1

NLAS5213A FUNCTION TABLE

IN	NO1, NO2
0	OFF
1	ON

NLAS5213B FUNCTION TABLE

IN	NO1, NO2
0	OFF
1	ON

NLAS5213

OPERATING CONDITIONS

MAXIMUM RATINGS

Symbol	Pins	Parameter	Value	Condition	Unit
V _{CC}	V _{CC}	Positive DC Supply Voltage	-0.5 to 5.5		V
V _{IS}	NOx, NCx, COMx	Analog Signal Voltage	-0.5 to V _{CC} + 0.5		V
V _{IN}	IN1, IN2	Control Input Voltage	-0.5 to 5.5		V
I _{CC}	V _{CC}	Positive DC Supply Current	50		mA
I _{IS_CON}	NOx, NCx, COMx	Analog Signal Continues Current	±300	Closed Switch	mA
I _{IS_PK}	NOx, NCx, COMx	Analog Signal Peak Current	±500	10% Duty Cycle	mA
I _{IN}	IN	Control Input Current	±20		mA
T _{STG}		Storage Temperature Range	-65 to 150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS*

Symbol	Pins	Parameter	Value	Condition	Unit
V _{CC}	V _{CC}	Positive DC Supply Voltage	1.65 to 4.5		V
V _{IS}	NOx, NCx, COMx	Analog Signal Voltage	0 to V _{CC}		V
V _{IN}	IN1, IN2	Control Input Voltage	0 to V _{CC}		V
T _A		Operating Temperature Range	-40 to 85		°C

Minimum and maximum values are guaranteed through test or design across the **Recommended Operating Conditions**, where applicable. Typical values are listed for guidance only and are based on the particular conditions listed for each section, where applicable. These conditions are valid for all values found in the characteristics tables unless otherwise specified in the test conditions.

ESD PROTECTION

Symbol	Parameter	Value	Unit
ESD	Human Body Model I/O to GND All Pins	8.0 4.0	kV

DC ELECTRICAL CHARACTERISTICS

CONTROL INPUT (Typical: T = 25°C, V_{CC} = 3.3 V)

Symbol	Pins	Parameter	Test Conditions	V _{CC} (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
V _{IH}	OE	Control Input HIGH Voltage		2.7 3.3 4.2	1.4 1.7 2.3	-	-	V
V _{IL}	OE	Control Input LOW Voltage		2.7 3.3 4.2	-	-	0.5 0.5 0.8	V
I _{IN}	OE	Control Input Leakage Current	0 ≤ V _{IS} ≤ V _{CC}	1.65 - 4.5	-	-	±1.0	μA

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SUPPLY CURRENT AND LEAKAGE (Typical: T = 25°C, V_{CC} = 3.3 V)

Symbol	Pins	Parameter	Test Conditions	V _{CC} (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
I _{CC}	V _{CC}	Quiescent Supply Current	V _{IS} = V _{CC} or GND; I _D = 0 A	1.65 – 4.5	–	–	1.0	μA
I _{CC(T)}	V _{CC}	Increase in I _{CC} per Control Voltage	V _{IN} = 2.6 V	3.6	–	–	10.0	μA
I _{OZ}		OFF State Leakage	0 ≤ V _{IS} ≤ V _{CC}	1.65 – 4.5	–	–	±1.0	μA
I _{OFF}	D+, D–	Power OFF Leakage Current	0 ≤ V _{IS} ≤ V _{CC}	0	–	–	±1.0	μA

ON RESISTANCE (Typical: T = 25°C, V_{CC} = 3.3 V)

Symbol	Pins	Parameter	Test Conditions	V _{CC} (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
R _{ON}		On-Resistance	I _{ON} = –100 mA V _{IS} = 0 to V _{CC}	2.7 3.3 4.2	–		2.0 1.4 1.3	Ω
R _{FLAT}		On-Resistance Flatness	I _{ON} = –100 mA V _{IS} = 0 to V _{CC}	2.7 3.3 4.2	–	0.32 0.35 0.37	–	Ω
ΔR _{ON}		On-Resistance Matching	I _{ON} = –100 mA V _{IS} = 0 to V _{CC}	2.7 3.3 4.2	–	0.16 0.16 0.15	–	Ω

AC ELECTRICAL CHARACTERISTICS

TIMING/FREQUENCY (Typical: T = 25°C, V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 5 pF, f = 1 MHz)

Symbol	Pins	Parameter	Test Conditions	V _{CC} (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
t _{ON}	Closed to Open	Turn-ON Time		1.65 – 4.5	–	20	–	ns
t _{OFF}	Open to Closed	Turn-OFF Time		1.65 – 4.5	–	15	–	ns
BW		–3 dB Bandwidth	C _L = 5 pF	1.65 – 4.5	–	496	–	MHz

ISOLATION (Typical: T = 25°C, V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 5 pF, f = 1 MHz)

Symbol	Pins	Parameter	Test Conditions	V _{CC} (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
O _{IRR}	Open	OFF-Isolation		1.65 – 4.5	–	–57	–	dB
X _{TALK}	HSD+, HSD–	Non-Adjacent Channel Crosstalk		1.65 – 4.5	–	–97	–	dB

CAPACITANCE (Typical: T = 25°C, V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 5 pF, f = 1 MHz)

Symbol	Pins	Parameter	Test Conditions	-40°C to +85°C			Unit
				Min	Typ	Max	
C _{IN}	OE	Control Pin Input Capacitance	V _{CC} = 0 V	–	8.5	–	pF
C _{ON}	HSD+, to D+	ON Capacitance	V _{IN} = 0 V	–	32	–	pF
C _{OFF}	HSD+, HSD–	OFF Capacitance	V _{IS} = 3.3 V; V _{IN} = 3.3 V	–	19	–	pF

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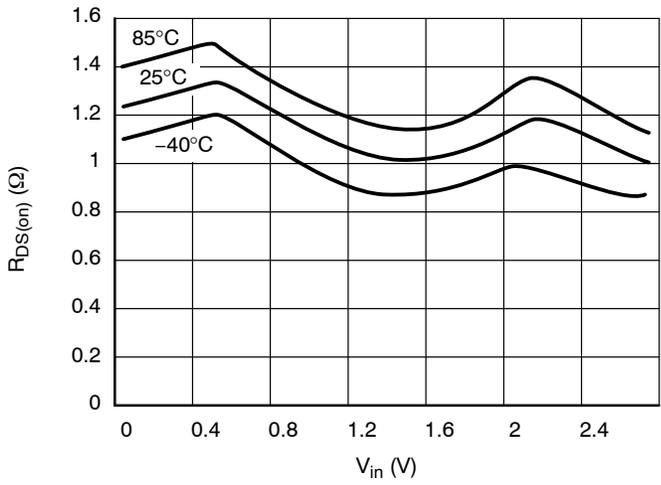


Figure 3. R_{ON} @ $V_{CC} = 2.7$ V

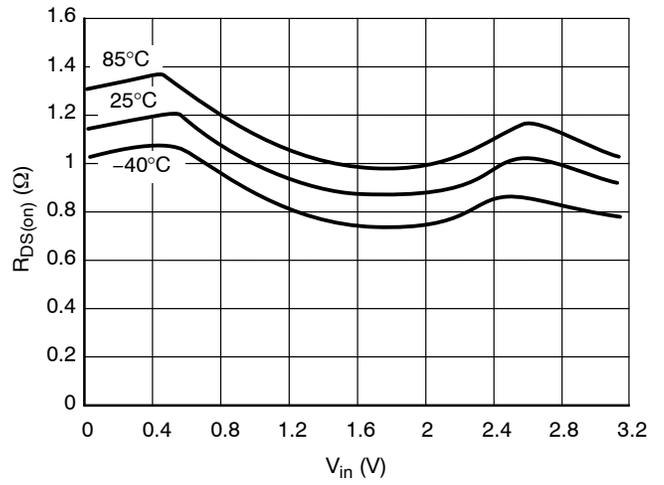


Figure 4. R_{ON} @ $V_{CC} = 3.3$ V

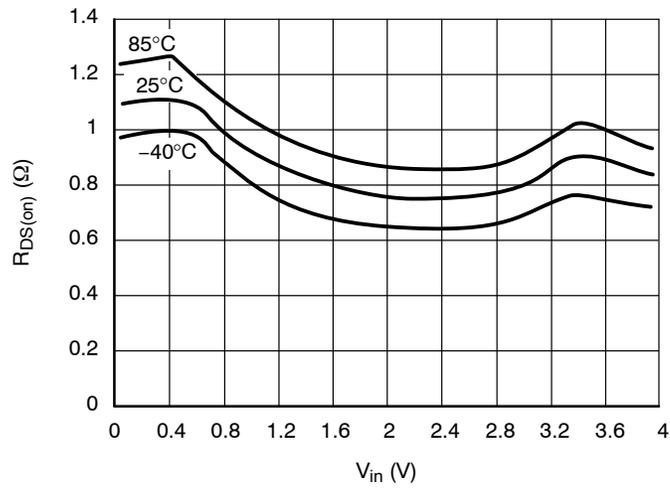


Figure 5. R_{ON} @ $V_{CC} = 4.2$ V

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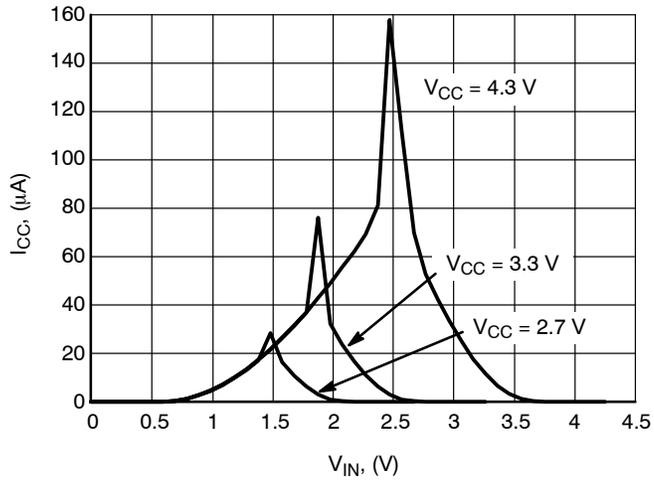


Figure 6. I_{CC} vs. V_{IN}

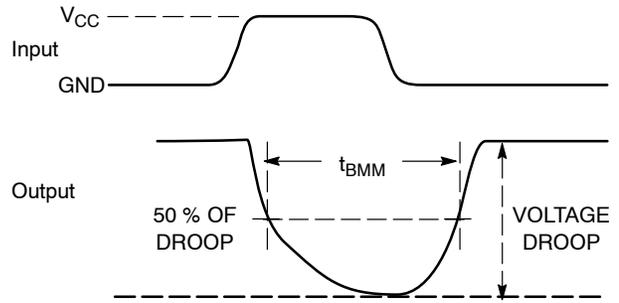
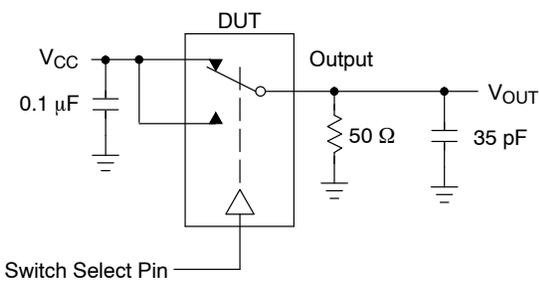


Figure 7. t_{BMM} (Time Break-Before-Make)

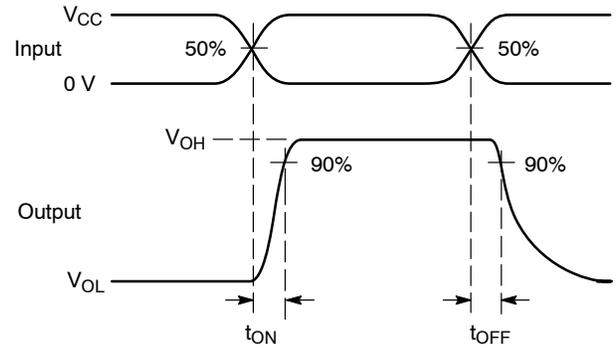
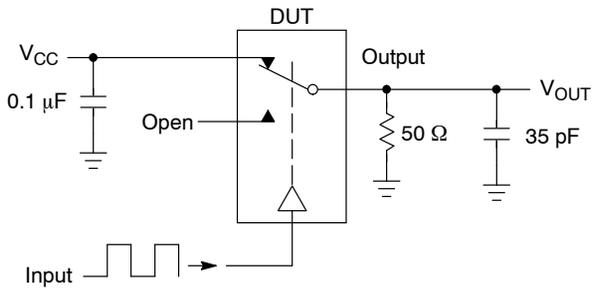


Figure 8. t_{ON}/t_{OFF}

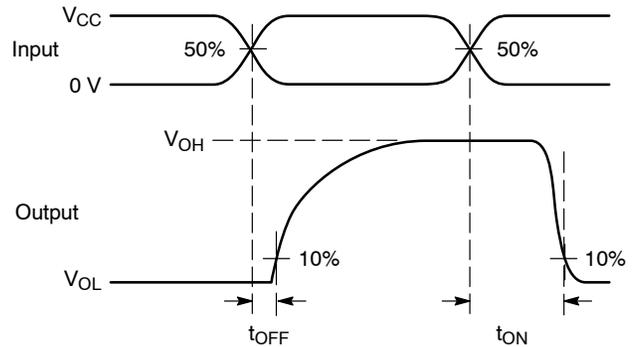
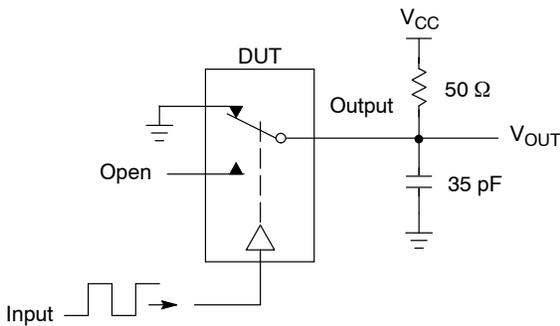
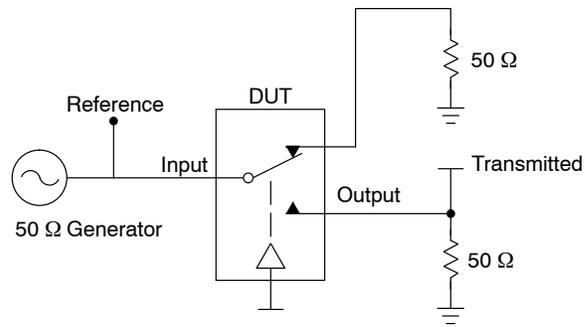


Figure 9. t_{ON}/t_{OFF}

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Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO} , Bandwidth and V_{ONL} are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

Figure 10. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ V_{ONL}

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DEVICE ORDERING INFORMATION

Device	Marking	Package Type	Shipping [†]
NLAS5213AUSG	VD	US8 (Pb-Free)	3,000 / Tape & Reel
NLAS5213AMUTAG	VD	UDFN8 (Pb-Free)	3,000 / Tape & Reel
NLAS5213BUSG	VE	US8 (Pb-Free)	3,000 / Tape & Reel
NLAS5213BMUTAG	VE	UDFN8 (Pb-Free)	3,000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

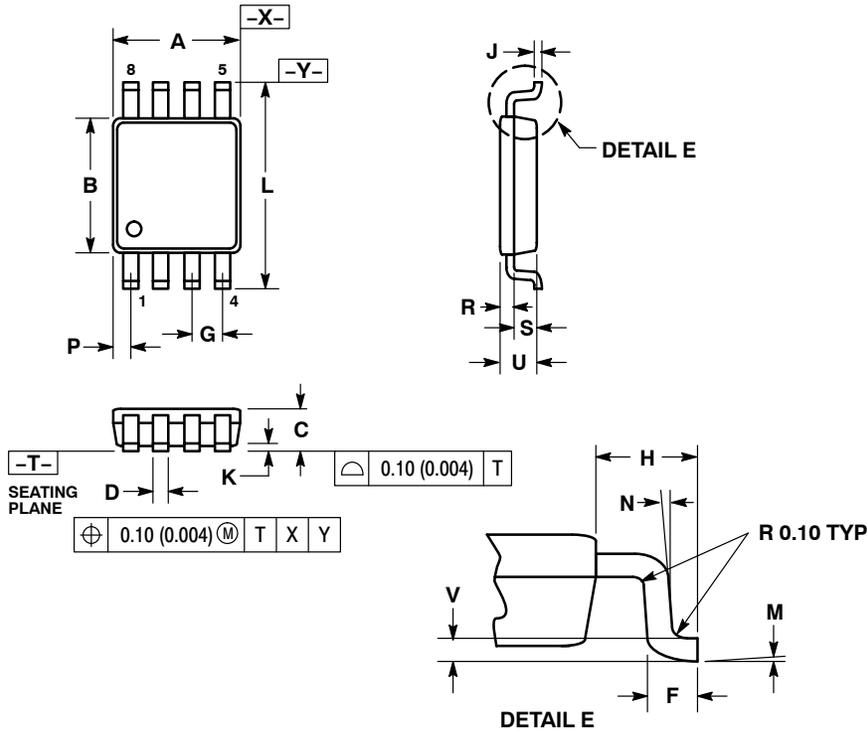
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PACKAGE DIMENSIONS

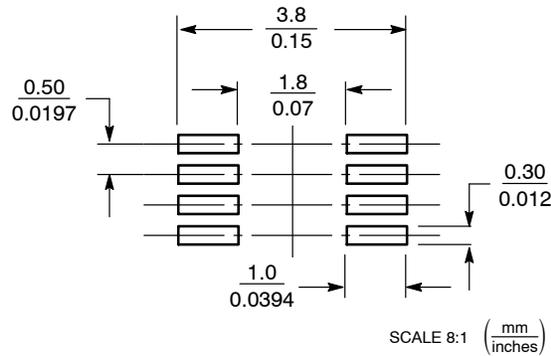
US8
CASE 493-02
ISSUE B

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH, PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.140 MM (0.0055") PER SIDE.
4. DIMENSION "B" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSION. INTER-LEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.140 (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076-0.0203 MM. (300-800 Å).
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508 (0.0020").



SOLDERING FOOTPRINT*

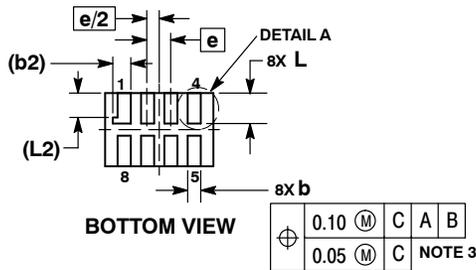
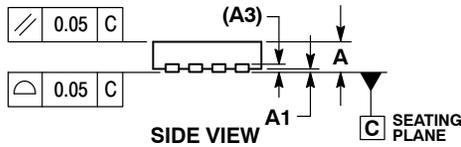
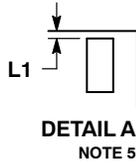
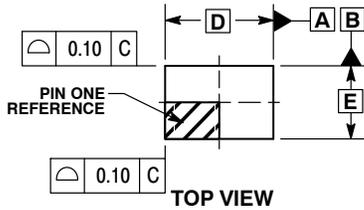


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

UDFN8 1.8x1.2, 0.4P
CASE 517AJ-01
ISSUE 0

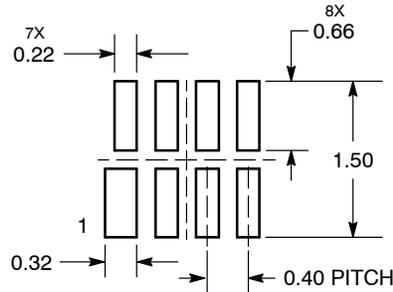


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH MAY NOT EXCEED 0.03 ONTO BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127	REF
b	0.15	0.25
b2	0.30	REF
D	1.80	BSC
E	1.20	BSC
e	0.40	BSC
L	0.45	0.55
L1	0.00	0.03
L2	0.40	REF

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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