TS5A3157
10-Ω SPDT ANALOG SWITCH

SCDS219A–NOVEMBER 2005–REVISED OCTOBER 2007

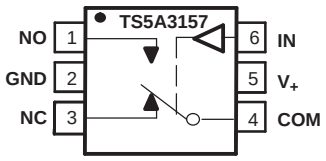
FEATURES

- **Low ON-State Resistance (10 Ω)**
- **Control Inputs Are 5-V Tolerant**
- **Low Charge Injection**
- **Excellent ON-State Resistance Matching**
- **Low Total Harmonic Distortion (THD)**
- **1.65-V to 5.5-V Single-Supply Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

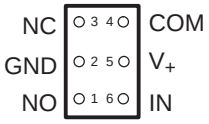
APPLICATIONS

- **Sample-and-Hold Circuits**
- **Battery-Powered Equipment**
- **Audio and Video Signal Routing**
- **Communication Circuits**

SOT-23 OR SC-70 PACKAGE
(TOP VIEW)



YZP PACKAGE
(BOTTOM VIEW)



DESCRIPTION/ORDERING INFORMATION

The TS5A3157 is a single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. This device can handle both digital and analog signals, and signals up to V_+ can be transmitted in either direction.

SUMMARY OF CHARACTERISTICS(1)

Configuration	Single Pole Double Throw (SPDT)
Number of channels	1
ON-state resistance (r_{on})	10 Ω
ON-state resistance match (Δr_{on})	0.15 Ω
ON-state resistance flatness ($r_{on(flat)}$)	4 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	5.7 ns/3.8 ns
Break-before-make time (t_{BBM})	0.5 ns
Charge injection (Q_C)	7 pC
Bandwidth (BW)	300 MHz
OFF isolation (O_{ISO})	–65 dB at 10 MHz
Crosstalk (X_{TALK})	–66 dB at 10 MHz
Total harmonic distortion (THD)	0.01%
Leakage current ($I_{NO(OFF)}/I_{NC(OFF)}$)	±0.1 µA
Power-supply current (I_+)	10 µA
Package options	6-pin DSBGA, DBV, or DCK

(1) V_+ = 5 V and T_A = 25°C

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Tape and reel	TS5A3157YZPR	_ _ _JC_
	SOT (SOT-23) – DBV	Tape and reel	TS5A3157DBVR	JC5_
	SOT (SC-70) – DCK	Tape and reel	TS5A3157DCKR	JC_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

Absolute Minimum and Maximum Ratings(1)(2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range(3)		–0.5	6.5	V
V_{NO} V_{NC} V_{COM}	Analog voltage range(3)(4)(5)		–0.5	V_+ + 0.5	V
I_K	Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0 or V_{NO}, V_{NC}, V_{COM} > V_+	–50	50	mA
I_{NO} I_{NC} I_{COM}	On-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to V_+	–50	50	mA
V_I	Digital input voltage range(3)(4)		–0.5	6.5	V
I_{IK}	Digital input clamp current	V_I < 0	–50		mA
I_+	Continuous current through V_+		–100	100	mA
I_{GND}	Continuous current through GND		–100	100	mA
θ_{JA}	Package thermal impedance(6)	DBV package		206	°C/W
		DCK package		252	
		YZP package		132	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

Electrical Characteristics for 5-V Supply(1)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{on}	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –30 mA,	Switch ON, See Figure 13	25°C	4.5 V		5.5	10	Ω
				Full				12	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 3.15 V, I_{COM} = –30 mA,	Switch ON, See Figure 13	25°C	4.5 V		0.15	0.2	Ω
				Full				0.3	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –30 mA,	Switch ON, See Figure 13	25°C	4.5 V		4	5	Ω
				Full				6	
NO, NC OFF leakage current	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_{NO} or V_{NC} = 1 V, V_{COM} = 4.5 V, or V_{NO} or V_{NC} = 4.5 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	5.5 V	–0.1	0.05	0.1	µA
				Full		–0.2	0.1	0.2	
NO, NC ON leakage current	$I_{NO(ON)}$, $I_{NC(ON)}$	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 4.5 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	5.5 V	–0.1	0.05	0.1	µA
				Full		–0.2	0.1	0.2	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NO} or V_{NC} = Open, or V_{COM} = 4.5 V, V_{NO} or V_{NC} = Open,	Switch ON, See Figure 15	25°C	5.5 V	–0.1	0.05	0.1	µA
				Full		–0.2	0.1	0.2	
Digital Control Input (IN)									
Input logic high	V_{IH}			Full		V_+ × 0.7		5.5	V
Input logic low	V_{IL}			Full		0		V_+ × 0.3	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	5.5 V	–0.1	0.05	0.1	µA
				Full		–1		1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 5-V Supply(1) (Continued)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = 3 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	5 V	1	6	8.5	ns
				Full	4.5 V to 5.5 V	1		9.5	
Turn-off time	t_{OFF}	V_{COM} = 3 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	5 V	1	3.5	6.5	ns
				Full	4.5 V to 5.5 V	1		7.5	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	5 V	1.8	2	3	ns
				Full	4.5 V to 5.5 V	1.8		3.5	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, See Figure 22	25°C	5 V		7		pC
NO, NC OFF capacitance	$C_{NO(OFF)}$, $C_{NC(OFF)}$	V_{NO} or V_{NC} = V_+ or GND, Switch OFF,	See Figure 16	25°C	5 V		5.5		pF
NO, NC ON capacitance	$C_{NO(ON)}$, $C_{NC(ON)}$	V_{NO} or V_{NC} = V_+ or GND, Switch ON,	See Figure 16	25°C	5 V		17.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	5 V		17.5		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	5 V		2.8		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 19	25°C	5 V		300		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 20	25°C	5 V		–65		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 21	25°C	5 V		–66		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 23	25°C	5 V		0.01		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	5.5 V		2.5	5	μA
				Full				10	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 3.3-V Supply(1)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{on}	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –24 mA,	Switch ON, See Figure 13	25°C	3 V		12	20	Ω
				Full				20	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 2.1 V, I_{COM} = –24 mA,	Switch ON, See Figure 13	25°C	3 V		0.2	0.4	Ω
				Full				0.3	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –24 mA,	Switch ON, See Figure 13	25°C	3 V		9	11	Ω
				Full				12	
NO, NC OFF leakage current	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_{NO} or V_{NC} = 1 V, V_{COM} = 3 V, or V_{NO} or V_{NC} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	3.6 V	–0.1	0.05	0.1	µA
				Full		–0.2	0.1	0.2	
NO, NC ON leakage current	$I_{NO(ON)}$, $I_{NC(ON)}$	V_{NO} or V_{NC} = 1 V, V_{COM} = Open, or V_{NO} or V_{NC} = 3 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	3.6 V	–0.1	0.05	0.1	µA
				Full		–0.2	0.1	0.2	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NO} or V_{NC} = Open, or V_{COM} = 3 V, V_{NO} or V_{NC} = Open,	Switch ON, See Figure 15	25°C	3.6 V	–0.1	0.05	0.1	µA
				Full		–0.2	0.1	0.2	
Digital Control Input (IN)									
Input logic high	V_{IH}			Full		V_+ × 0.7		5.5	V
Input logic low	V_{IL}			Full		0		V_+ × 0.3	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	3.6 V	–0.1	0.05	0.1	µA
				Full		–1		1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 3.3-V Supply[1] (Continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = 2 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	3.3 V	3.5	7	9.5	ns
				Full	3 V to 3.6 V	1.5		10.5	
Turn-off time	t_{OFF}	V_{COM} = 2 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	3.3 V	1	3.5	6.5	ns
				Full	3 V to 3.6 V	1		7.5	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	3.3 V	2.5	3	5	ns
				Full	3 V to 3.6 V	2		5	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, See Figure 22	25°C	3.3 V		3		pC
NO, NC OFF capacitance	$C_{NO(OFF)}$	V_{NO} or V_{NC} = V_+ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		5.5		pF
NO, NC ON capacitance	$C_{NO(ON)}$	V_{NO} or V_{NC} = V_+ or GND, Switch ON,	See Figure 16	25°C	3.3 V		17.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	3.3 V		17.5		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	3.3 V		2.8		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 19	25°C	3.3 V		300		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 20	25°C	3.3 V		–65		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 21	25°C	3.3 V		–66		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 23	25°C	3.3 V		0.015		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	3.6 V		2.5	5	μA
				Full				10	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 2.5-V Supply(1)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{on}	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –8 mA,	Switch ON, See Figure 13	25°C	2.3 V		35	45	Ω
				Full				50	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 1.6 V, I_{COM} = –8 mA,	Switch ON, See Figure 13	25°C	2.3 V		0.3	0.5	Ω
				Full				0.7	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –8 mA,	Switch ON, See Figure 13	25°C	2.3 V		30	40	Ω
				Full				40	
NO, NC OFF leakage current	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_{NO} or V_{NC} = 0.5 V, V_{COM} = 2.2 V, or V_{NO} or V_{NC} = 2.2 V, V_{COM} = 0.5 V,	Switch OFF, See Figure 14	25°C	2.7 V	–0.1	0.05	0.1	µA
				Full		–0.2	0.1	0.2	
NO, NC ON leakage current	$I_{NO(ON)}$, $I_{NC(ON)}$	V_{NO} or V_{NC} = 0.5 V, V_{COM} = Open, or V_{NO} or V_{NC} = 2.2 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	2.7 V	–0.1	0.05	0.1	µA
				Full		–0.2	0.1	0.2	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 0.5 V, V_{NO} or V_{NC} = Open, or V_{COM} = 2.2 V, V_{NO} or V_{NC} = Open,	Switch ON, See Figure 15	25°C	2.7 V	–0.1	0.05	0.1	µA
				Full		–0.2	0.1	0.2	
Digital Control Input (IN)									
Input logic high	V_{IH}			Full		V_+ × 0.7		5.5	V
Input logic low	V_{IL}			Full		0		V_+ × 0.3	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	2.7 V	–0.1	0.05	0.1	µA
				Full		–1		1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 2.5-V Supply[1] (Continued)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = 1.5 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	2.5 V	5	8	13.5	ns
				Full	2.3 V to 2.7 V	3.5		14	
Turn-off time	t_{OFF}	V_{COM} = 1.5 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	2.5 V	1	3.5	6.5	ns
				Full	2.3 V to 2.7 V	1		7.5	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	2.5 V	3.5	5	7	ns
				Full	2.3 V to 2.7 V	3		7.5	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, See Figure 22	25°C	2.5 V		2		pC
NO, NC OFF capacitance	$C_{NO(OFF)}$, $C_{NC(OFF)}$	V_{NO} or V_{NC} = V_+ or GND, Switch OFF,	See Figure 16	25°C	2.5 V		5.5		pF
NO, NC ON capacitance	$C_{NO(ON)}$, $C_{NC(ON)}$	V_{NO} or V_{NC} = V_+ or GND, Switch ON,	See Figure 16	25°C	2.5 V		17.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	2.5 V		17.5		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	2.5 V		2.8		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 19	25°C	2.5 V		300		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 20	25°C	2.5 V		–65		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 21	25°C	2.5 V		–66		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 23	25°C	2.5 V		0.025		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	2.7 V		2.5	5	μA
				Full				10	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 1.8-V Supply(1)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{on}	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –4 mA,	Switch ON, See Figure 13	25°C	1.65 V		140	160	Ω
				Full				160	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 1.16 V, I_{COM} = –4 mA,	Switch ON, See Figure 13	25°C	1.65 V		0.5	0.6	Ω
				Full				0.75	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –4 mA,	Switch ON, See Figure 13	25°C	1.65 V		125	130	Ω
				Full				140	
NO, NC OFF leakage current	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_{NO} or V_{NC} = 0.3 V, V_{COM} = 1.65 V, or V_{NO} or V_{NC} = 1.65 V, V_{COM} = 0.3 V,	Switch OFF, See Figure 14	25°C	1.95 V	–0.1	0.05	0.1	μA
				Full		–0.2	0.1	0.2	
NO, NC ON leakage current	$I_{NO(ON)}$, $I_{NC(ON)}$	V_{NO} or V_{NC} = 0.3 V, V_{COM} = Open, or V_{NO} or V_{NC} = 1.65 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	1.95 V	–0.1	0.05	0.1	μA
				Full		–0.2	0.1	0.2	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 0.3 V, V_{NO} or V_{NC} = Open, or V_{COM} = 1.65 V, V_{NO} or V_{NC} = Open,	Switch ON, See Figure 15	25°C	1.95 V	–0.1	0.05	0.1	μA
				Full		–0.2	0.1	0.2	
Digital Control Input (IN)									
Input logic high	V_{IH}			Full		V_+ × 0.65		5.5	V
Input logic low	V_{IL}			Full		0		V_+ × 0.35	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	1.95 V	–0.1	0.05	0.1	μA
				Full		–1		1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 1.8-V Supply[1](Continued)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = 1.3 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	1.8 V	5	15	23	ns
				Full	1.65 V to 1.95 V	7		24	
Turn-off time	t_{OFF}	V_{COM} = 1.3 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	1.8 V	1	3.5	6.5	ns
				Full	1.65 V to 1.95 V	1		7.5	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	1.8 V	5.5	7.5	9	ns
				Full	1.65 V to 1.95 V	5.2		12	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, See Figure 22	25°C	1.8 V		1		pC
NO, NC OFF capacitance	$C_{NO(OFF)}$, $C_{NC(OFF)}$	V_{NO} or V_{NC} = V_+ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		5.5		pF
NO, NC ON capacitance	$C_{NO(ON)}$, $C_{NC(ON)}$	V_{NO} or V_{NC} = V_+ or GND, Switch ON,	See Figure 16	25°C	1.8 V		17.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	1.8 V		17.5		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	1.8 V		2.8		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 19	25°C	1.8 V		300		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 20	25°C	1.8 V		–65		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 21	25°C	1.8 V		–66		dB
Total harmonic distortion	THD	R_L = 10 kΩ, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 23	25°C	1.8 V		0.015		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	1.95 V		2.5	5	μA
				Full				10	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

TYPICAL PERFORMANCE

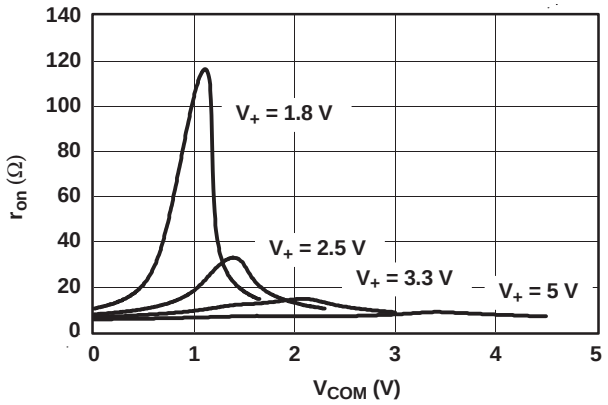


Figure 1. r_{on} vs V_{COM}

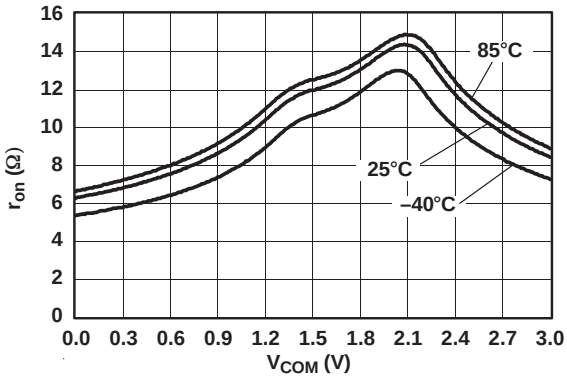


Figure 2. r_{on} vs V_{COM} (V_+ = 3 V)

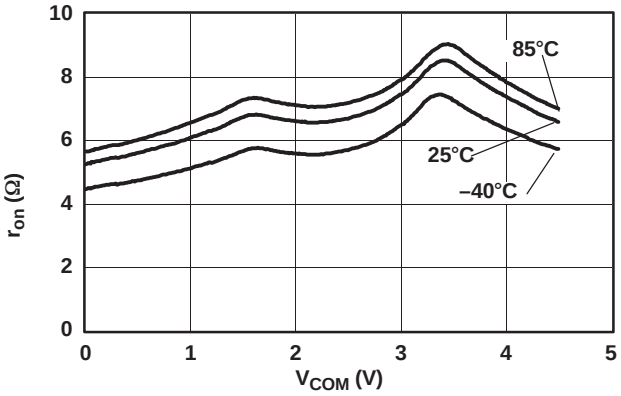


Figure 3. r_{on} vs V_{COM} (V_+ = 4.5 V)

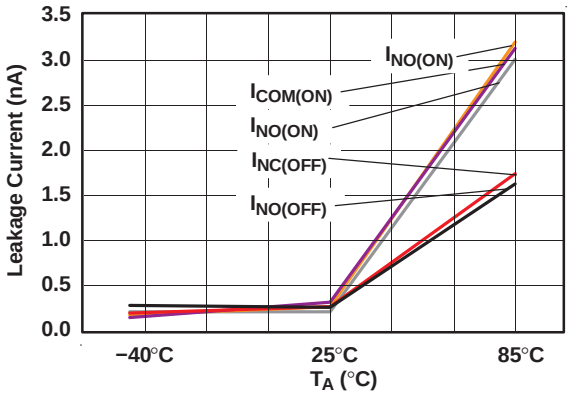


Figure 4. Leakage Current vs Temperature (V_+ = 5.5 V)

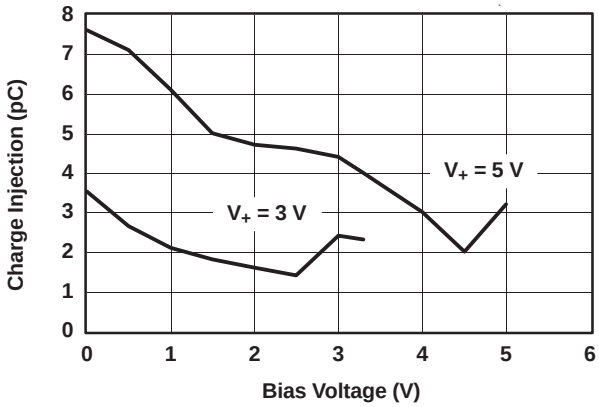


Figure 5. Charge Injection (Q_C) vs V_{COM}

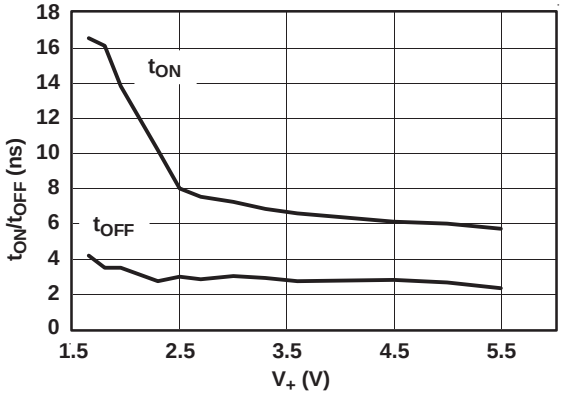


Figure 6. t_{ON} and t_{OFF} vs Supply Voltage

TYPICAL PERFORMANCE

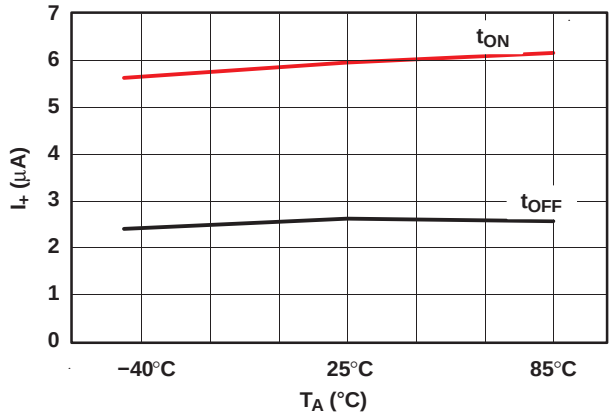


Figure 7. t_{ON} and t_{OFF} vs Temperature (V_+ = 5 V)

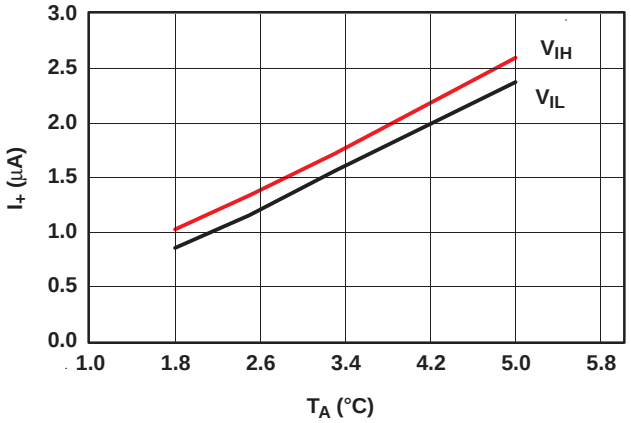


Figure 8. Logic-Level Threshold vs V_+

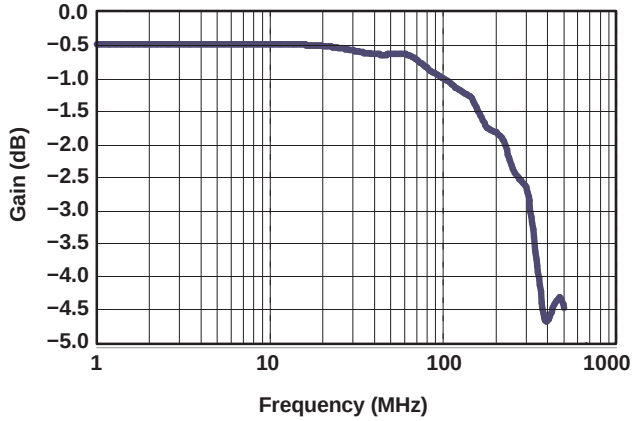


Figure 9. Bandwidth (Gain vs Frequency) (V_+ = 5 V)

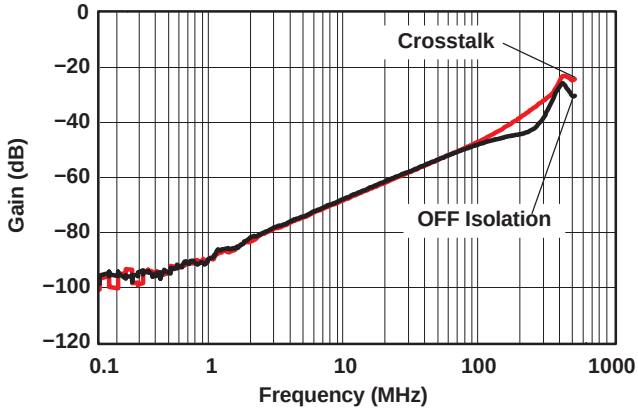


Figure 10. OFF Isolation (V_+ = 5 V)

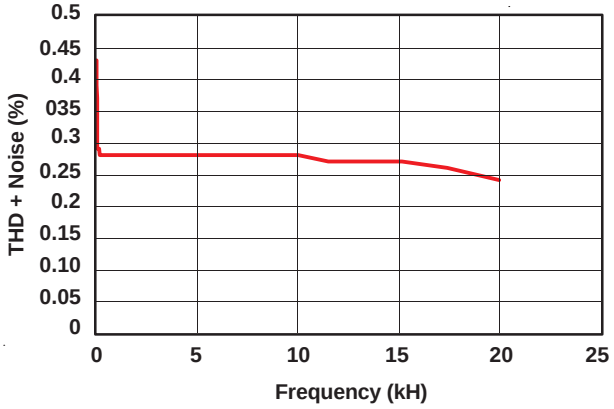


Figure 11. Total Harmonic Distortion vs Frequency

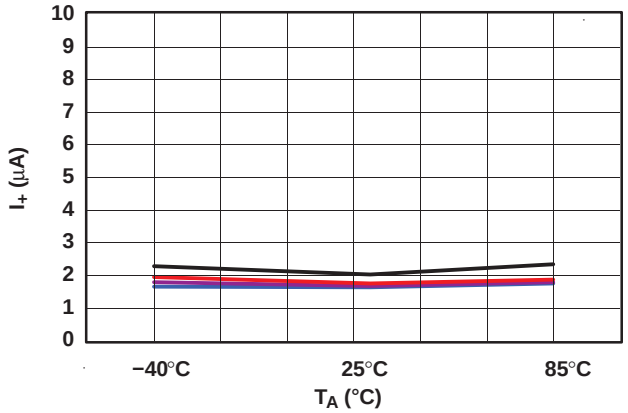


Figure 12. Power-Supply Current vs Temperature (V_+ = 5 V)

PIN DESCRIPTION

PIN NO.	NAME	DESCRIPTION
1	NO	Normally open
2	GND	Digital ground
3	NC	Normally closed
4	COM	Common
5	V_+	Power supply
6	IN	Digital control to connect the COM to NO or NC

PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NC or COM and NO ports when the channel is ON
Δr_{on}	Difference of r_{on} between channels in a specific device
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Maximum input voltage for logic low for the control input (IN)
V_I	Voltage at the control input (IN)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN)
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning OFF.
t_{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
C_I	Capacitance of control input (IN)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency where the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of fundamental harmonic.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND

PARAMETER MEASUREMENT INFORMATION

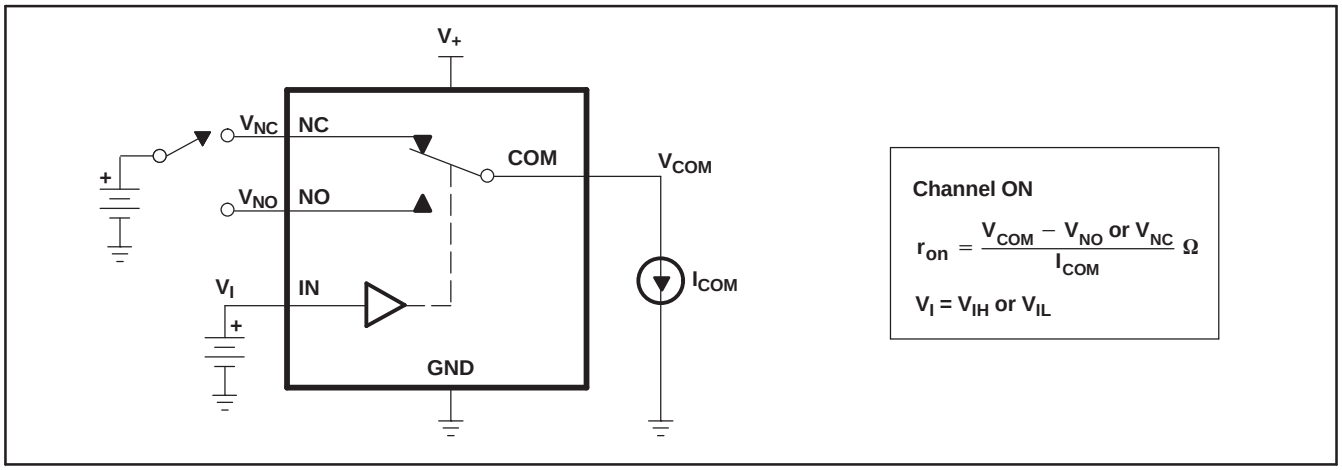


Figure 13. ON-State Resistance (r_{on})

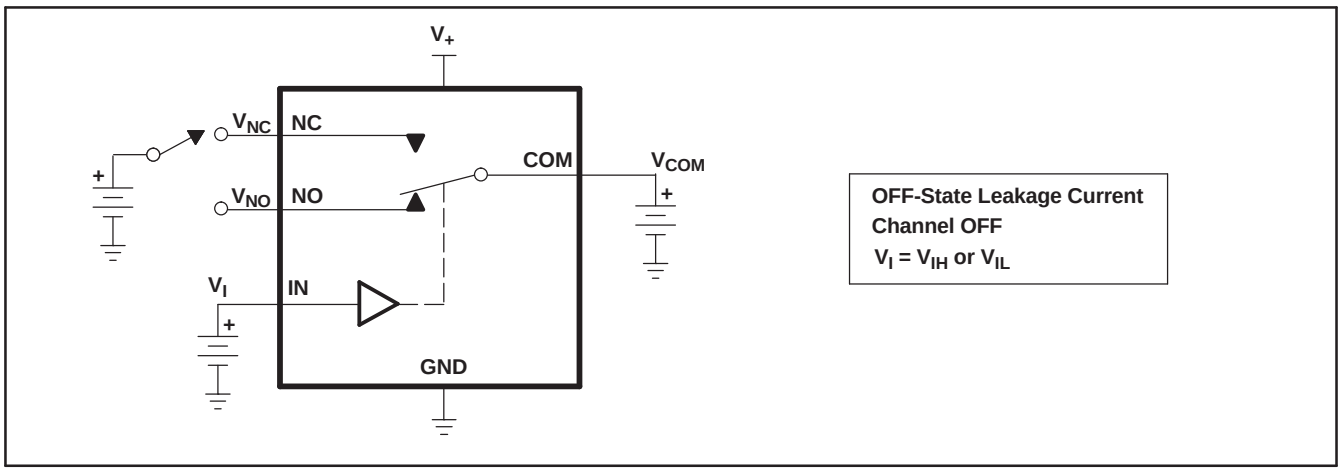


Figure 14. OFF-State Leakage Current ($I_{NC(OFF)}$, $I_{NO(OFF)}$)

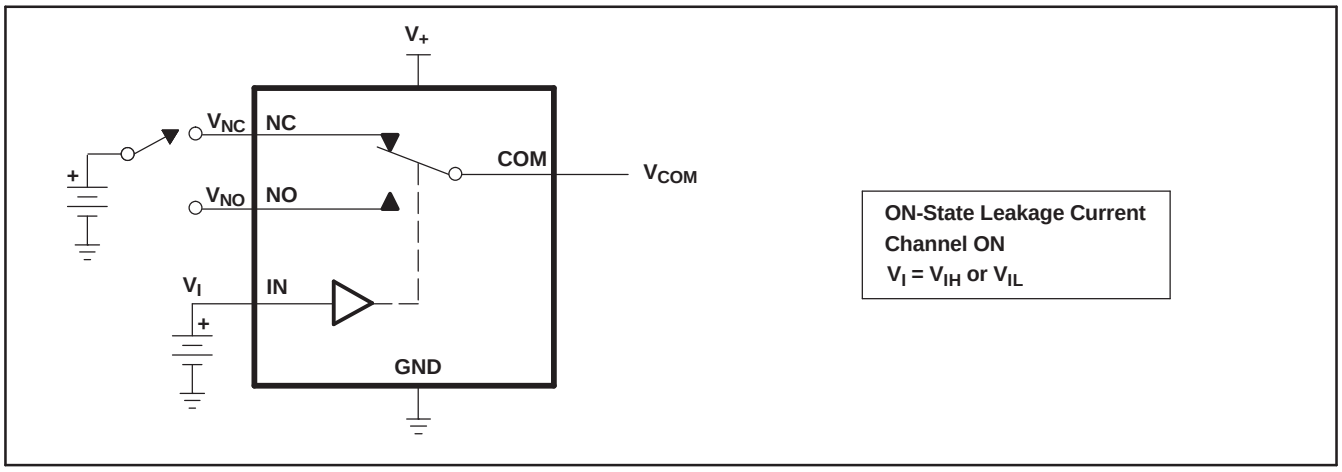


Figure 15. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

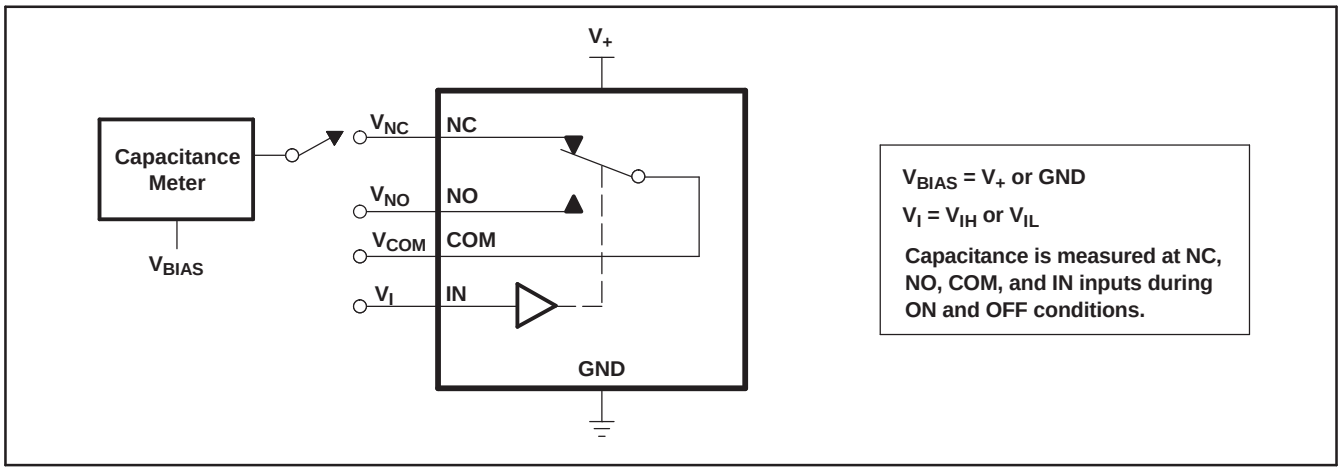
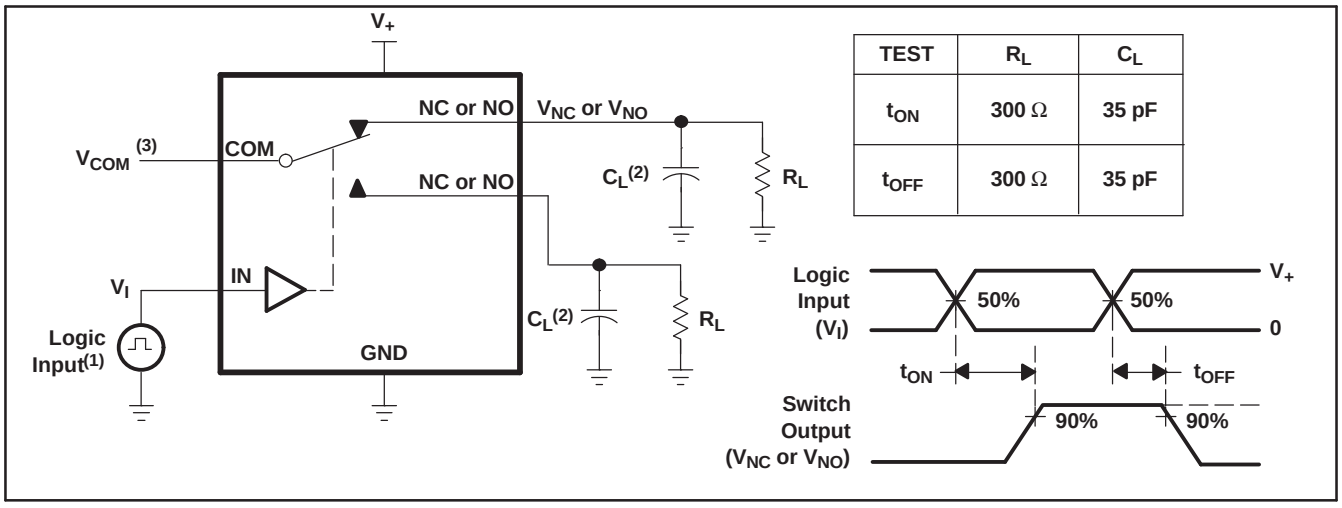
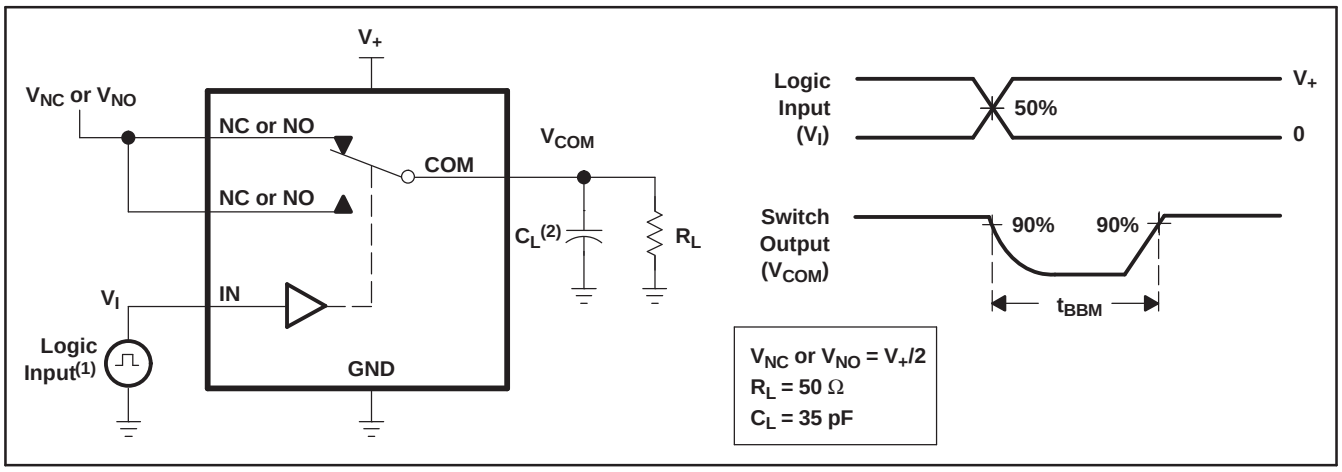


Figure 16. Capacitance (C_I, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.
(3) See Electrical Characteristic for V_{COM}.

Figure 17. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 18. Break-Before-Make Time (t_{BBM})

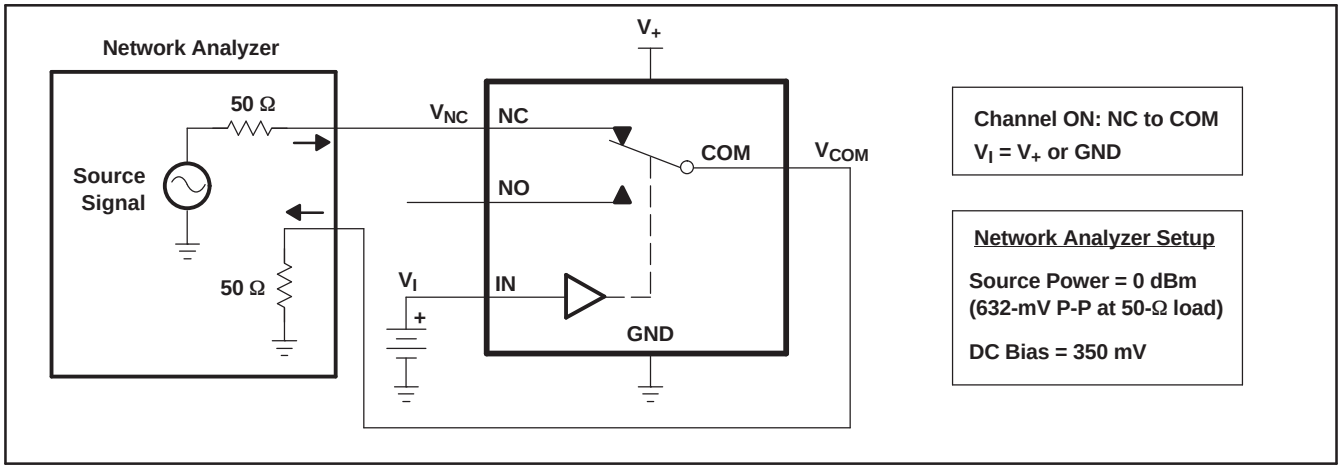


Figure 19. Bandwidth (BW)

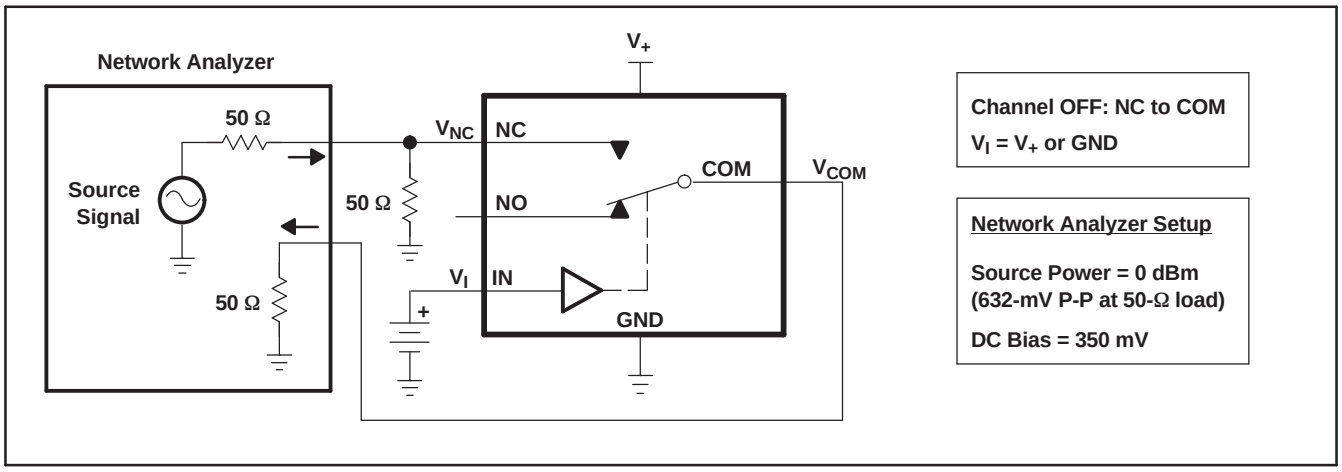


Figure 20. OFF Isolation (O_{ISO})

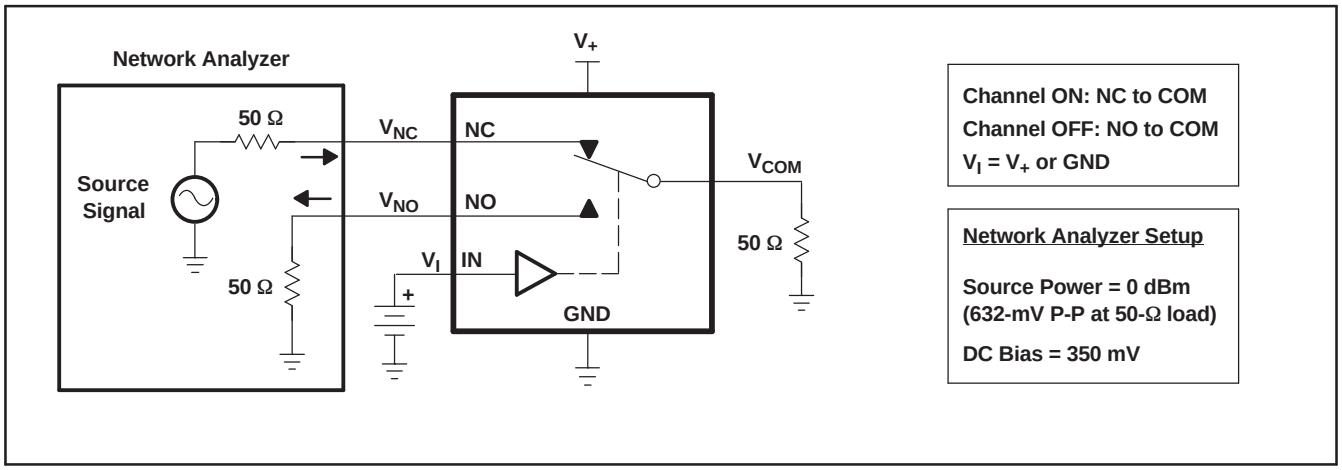
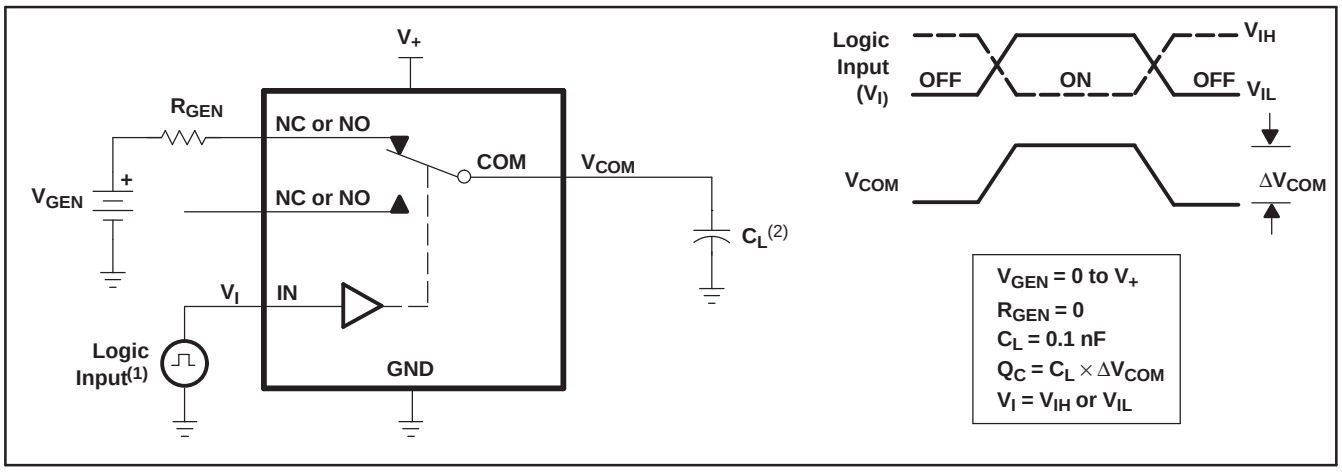
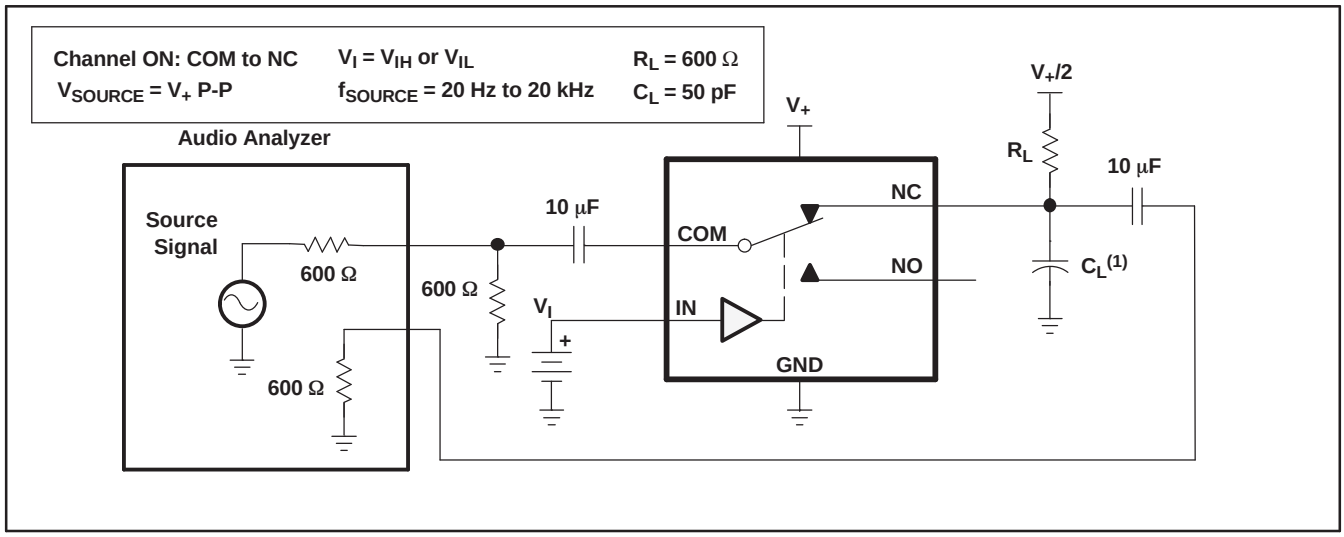


Figure 21. Crosstalk (X_{TALK})



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 22. Charge Injection (Q_C)



(1) C_L includes probe and jig capacitance.

Figure 23. Total Harmonic Distortion (THD)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TS5A3157DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JC5R	Samples
TS5A3157DBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JC5R	Samples
TS5A3157DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JC5R	Samples
TS5A3157DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JC5 ~ JCF ~ JCR)	Samples
TS5A3157DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JC5 ~ JCF ~ JCR)	Samples
TS5A3157DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JC5 ~ JCF ~ JCR)	Samples
TS5A3157YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(JC7 ~ JCN)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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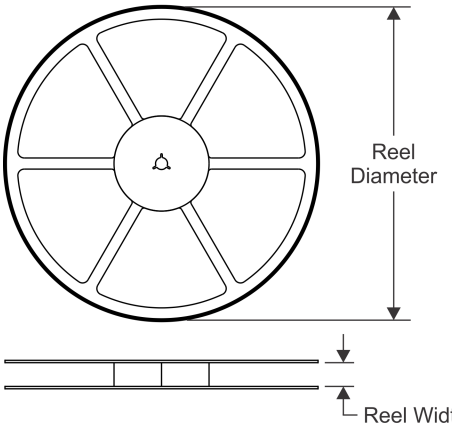
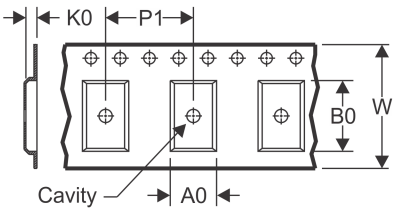
TAPE AND REEL INFORMATION

REEL DIMENSIONS

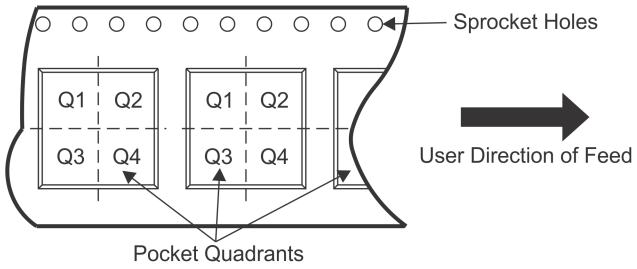


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

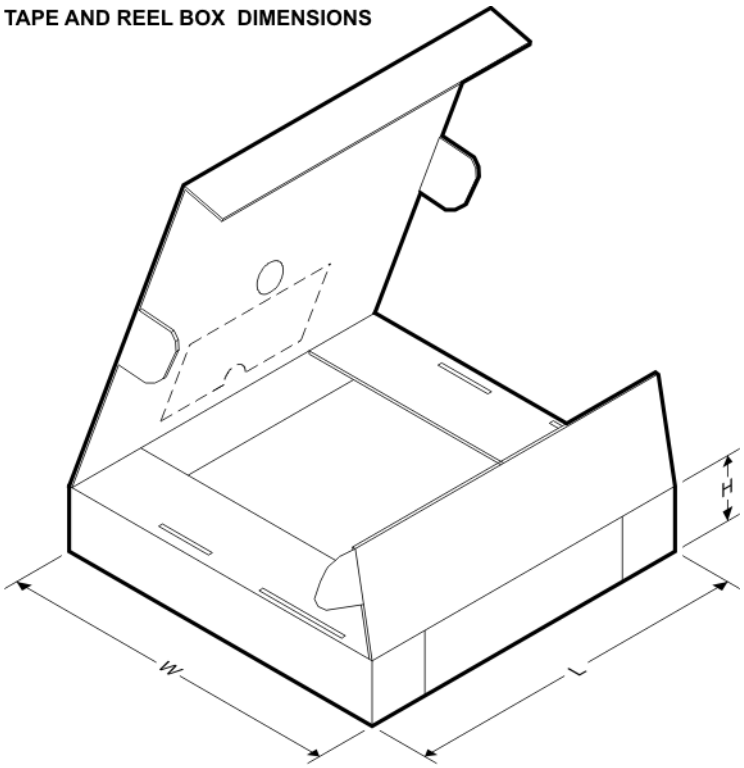
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3157DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS5A3157DCKR	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
TS5A3157DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TS5A3157YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

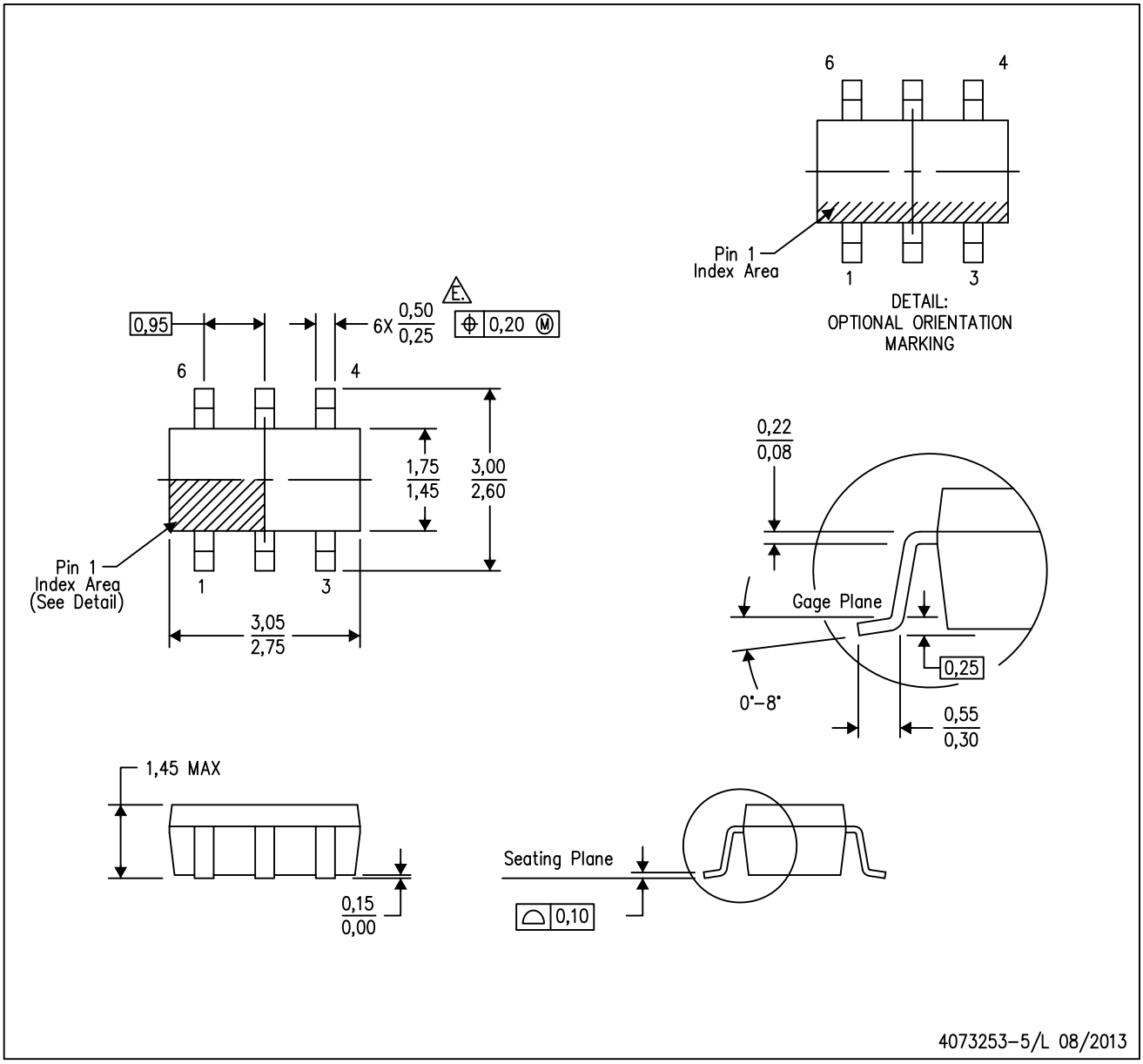
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

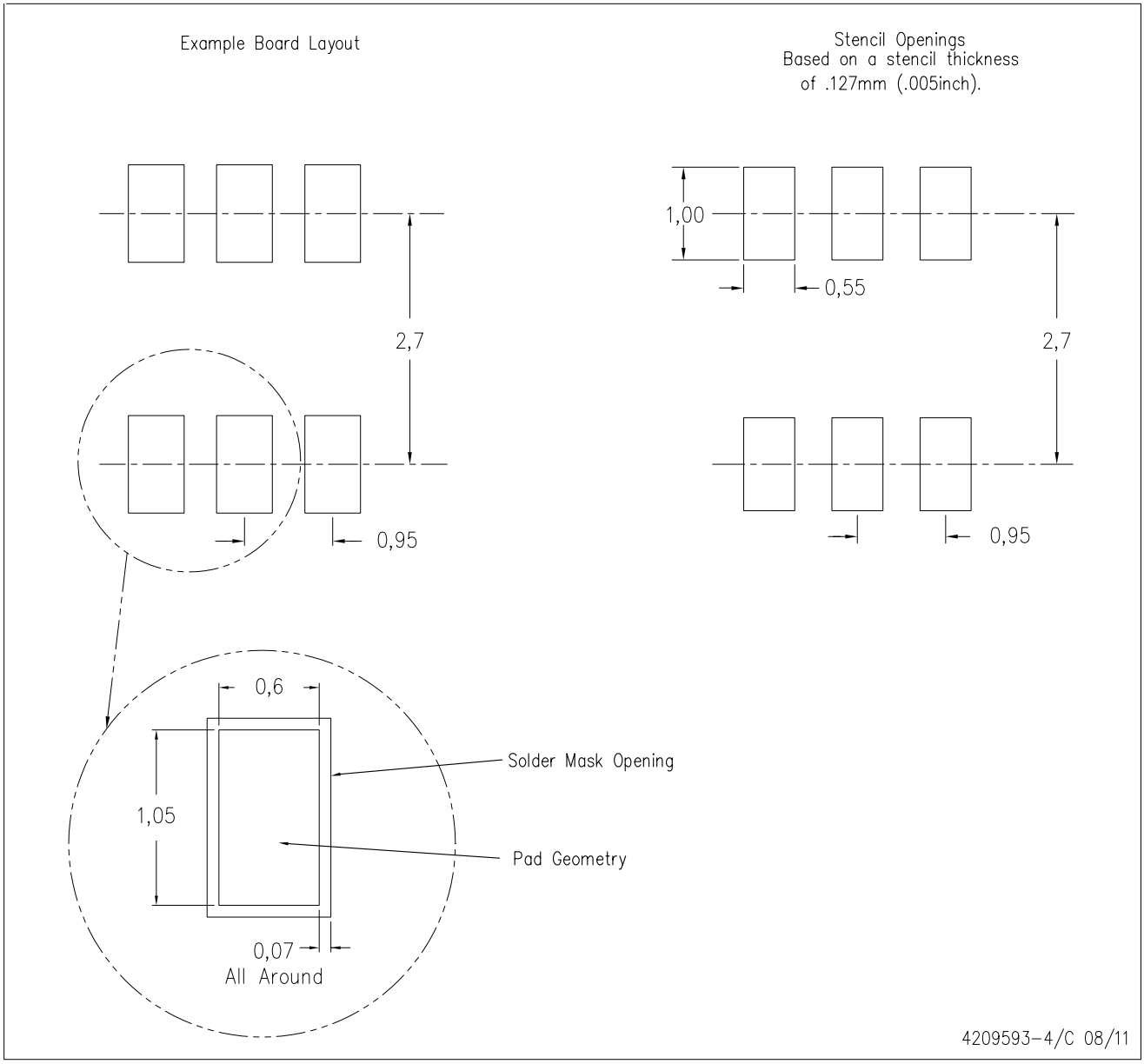
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3157DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
TS5A3157DCKR	SC70	DCK	6	3000	338.0	343.0	30.0
TS5A3157DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
TS5A3157YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



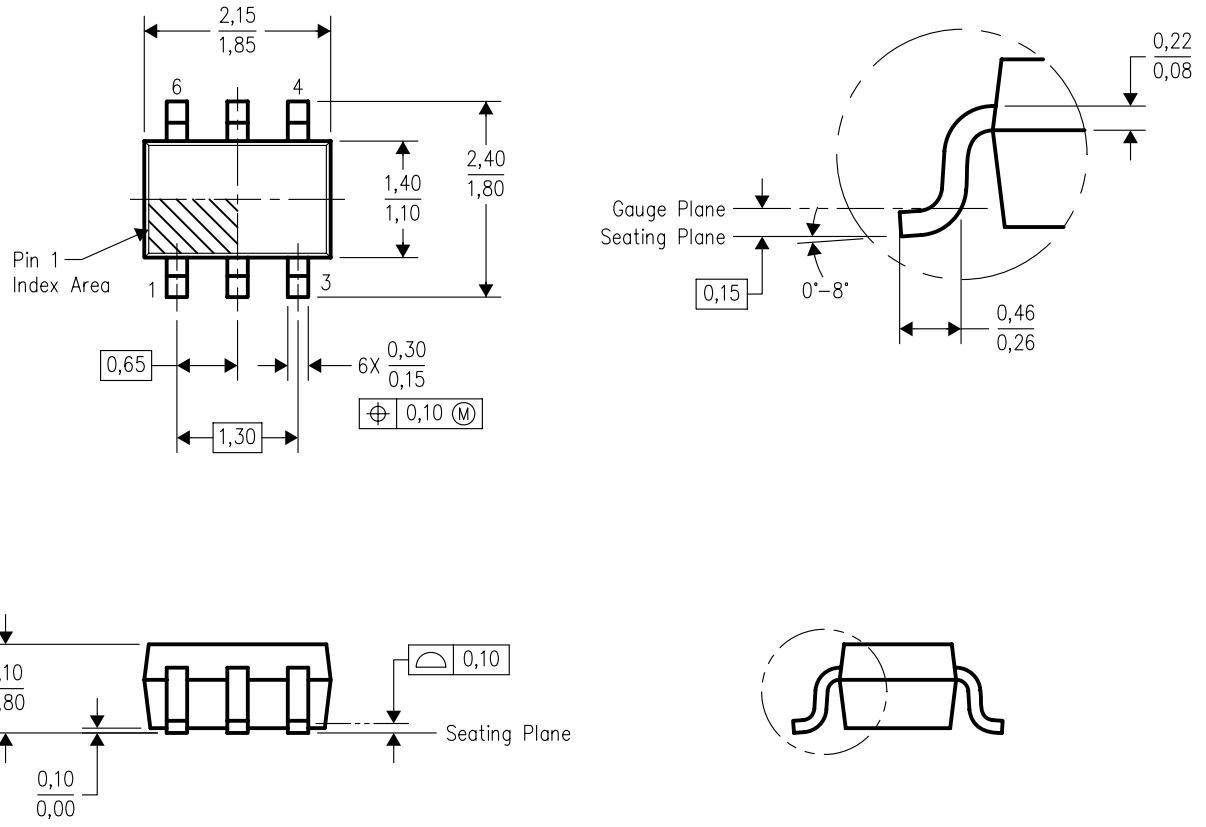
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

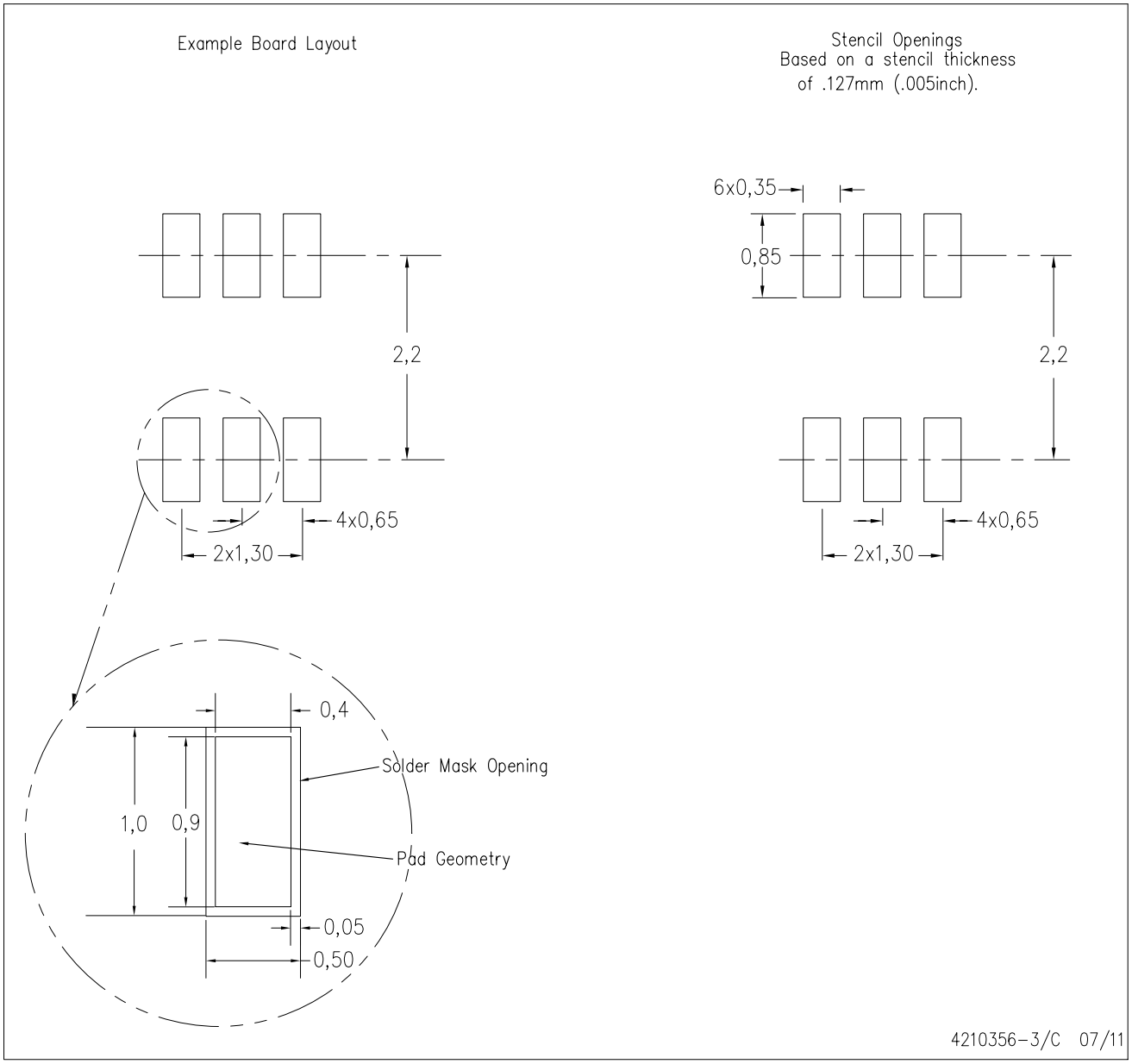
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

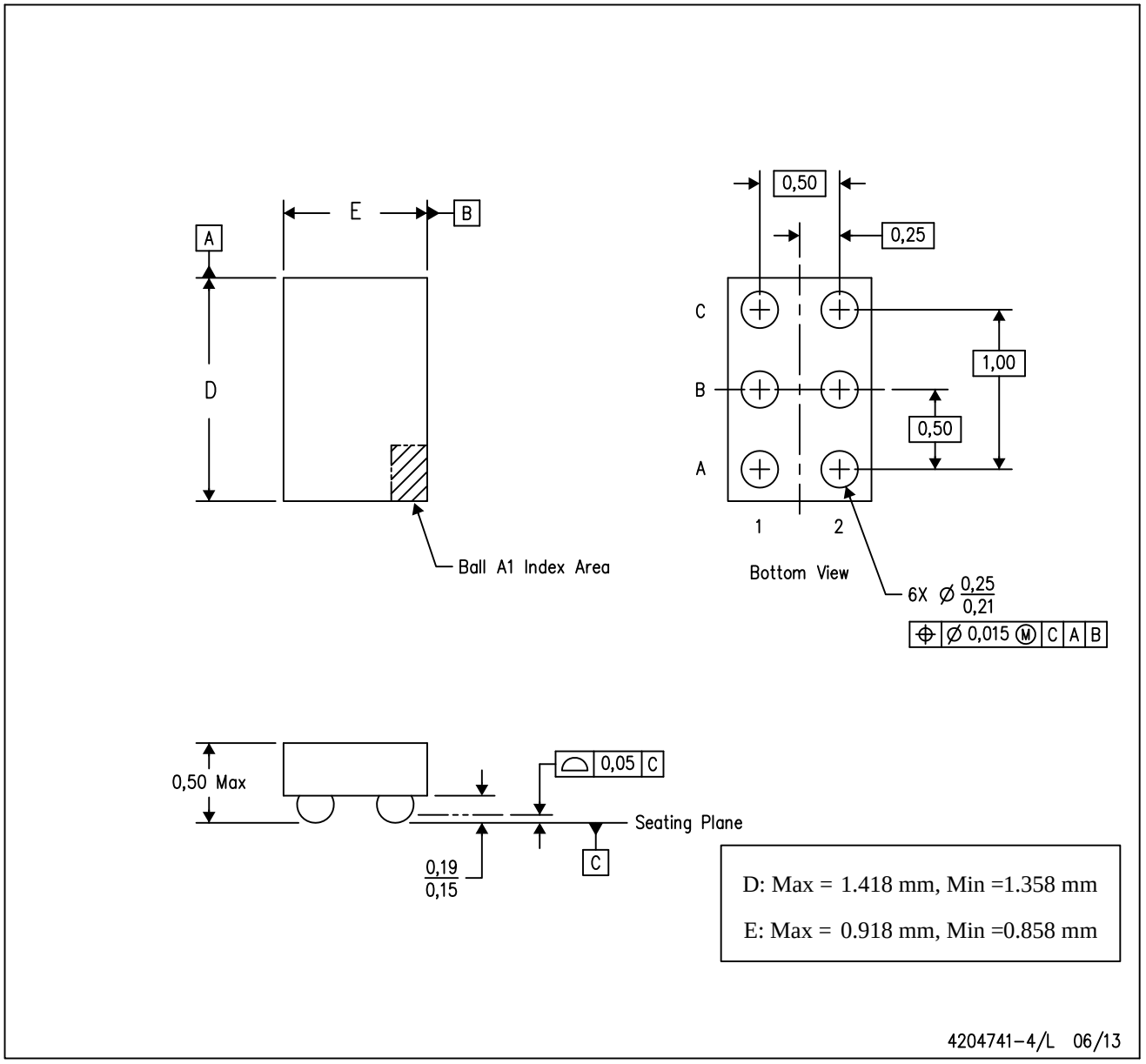
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

YZP (R–XBGA–N6) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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