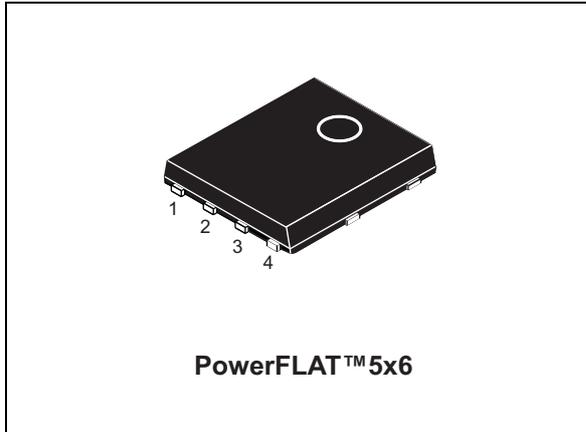


N-channel 100 V, 0.005 Ω typ., 107 A, STripFET™ H7 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data



Features

| Order code | V _{DS} | R _{DS(on)} max | I _D | P _{TOT} |
|-------------|-----------------|--|----------------|------------------|
| STL110N10F7 | 100 V | 0.006 Ω (V _{GS} = 10 V) | 107 A | 136 W |

- Among the lowest R_{DS(on)} on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes the STripFET™ H7 technology with a trench gate structure combined with extremely low on-resistance. The device also offers ultra-low capacitances for higher switching frequency operations.

Figure 1. Internal schematic diagram

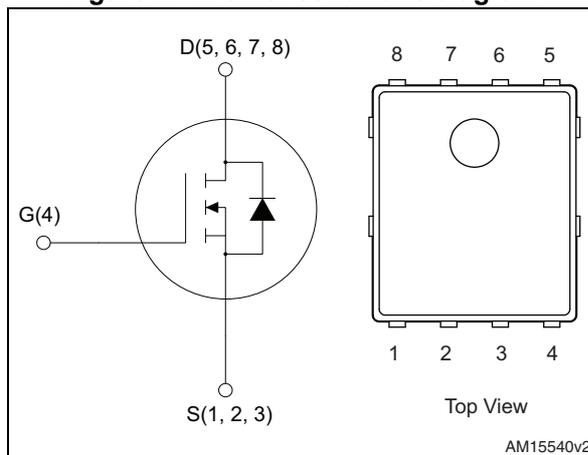


Table 1. Device summary

| Order code | Marking | Package | Packaging |
|-------------|----------|----------------|---------------|
| STL110N10F7 | 110N10F7 | PowerFLAT™ 5x6 | Tape and reel |

Contents

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1 Electrical ratings

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|--------------------|--|------------|------------------|
| V_{DS} | Drain-source voltage | 100 | V |
| V_{GS} | Gate-source voltage | ± 20 | V |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 107 | A |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 75 | A |
| $I_D^{(2)}$ | Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$ | 21 | A |
| $I_D^{(2)}$ | Drain current (continuous) at $T_{pcb}=100\text{ }^\circ\text{C}$ | 14 | A |
| $I_{DM}^{(2)(3)}$ | Drain current (pulsed) | 84 | A |
| $P_{TOT}^{(1)}$ | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ | 136 | W |
| $P_{TOT}^{(2)}$ | Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$ | 4.8 | W |
| $E_{AS}^{(4)}$ | Single pulse avalanche energy | 490 | mJ |
| T_J T_{stg} | Operating junction temperature Storage temperature | -55 to 175 | $^\circ\text{C}$ |

1. This value is rated according to R_{thj-c} .
2. This value is rated according to $R_{thj-pcb}$.
3. Pulse width limited by safe operating area.
4. Starting $T_J=25\text{ }^\circ\text{C}$, $I_d=18\text{ A}$, $V_{dd}=50\text{ V}$

Table 3. Thermal resistance

| Symbol | Parameter | Value | Unit |
|---------------------|----------------------------------|-------|--------------------|
| $R_{thj-case}$ | Thermal resistance junction-case | 1.1 | $^\circ\text{C/W}$ |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb | 31.3 | $^\circ\text{C/W}$ |

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10\text{ sec}$

2 Electrical characteristics

($T_{CASE}=25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-----------------------------------|--|------|-------|-------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}=0, I_D=250\text{ }\mu\text{A}$ | 100 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{GS}=0, V_{DS}=100\text{ V}$ | | | 1 | μA |
| | | $V_{GS}=0, V_{DS}=100\text{ V}, T_C=125\text{ °C}$ | | | 10 | μA |
| I_{GSS} | Gate body leakage current | $V_{DS}=0, V_{GS}=20\text{ V}$ | | | 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}=V_{GS}, I_D=250\text{ }\mu\text{A}$ | 2.5 | | 4.5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}=10\text{ V}, I_D=10\text{ A}$ | | 0.005 | 0.006 | Ω |

Table 5. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------|------------------------------|---|------|------|------|------|
| C_{iss} | Input capacitance | $V_{DS}=50\text{ V}, f=1\text{ MHz}, V_{GS}=0$ | - | 5117 | - | pF |
| C_{oss} | Output capacitance | | - | 992 | - | pF |
| C_{rss} | Reverse transfer capacitance | | - | 39 | - | pF |
| Q_g | Total gate charge | $V_{DD}=50\text{ V}, I_D=21\text{ A}$ $V_{GS}=10\text{ V}$ <i>Figure 14</i> | - | 72 | - | nC |
| Q_{gs} | Gate-source charge | | - | 30 | - | nC |
| Q_{gd} | Gate-drain charge | | - | 17 | - | nC |

Table 6. Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|--|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}=50\text{ V}, I_D=10\text{ A}, R_G=4.7\text{ }\Omega, V_{GS}=10\text{ V}$ <i>Figure 13</i> | - | 25 | - | ns |
| t_r | Rise time | | - | 36 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 52 | - | ns |
| t_f | Fall time | | - | 21 | - | ns |

Table 7. Source drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|---|------|------|------|------|
| I_{SD} | Source-drain current | | - | | 21 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 84 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $V_{GS}=0, I_{SD} = 21 \text{ A}$ | - | | 1.2 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 21 \text{ A},$ $di/dt = 100 \text{ A}/\mu\text{s},$ $V_{DD}=80 \text{ V}, T_j=150 \text{ }^\circ\text{C}$ | - | 77 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 150 | | nC |
| I_{RRM} | Reverse recovery current | | - | 4.3 | | A |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

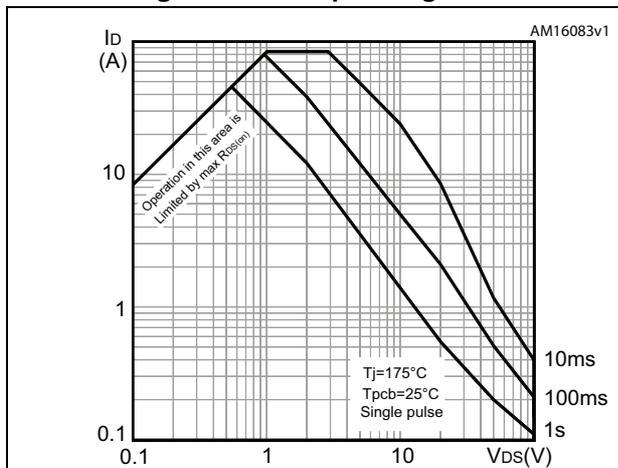


Figure 3. Thermal impedance

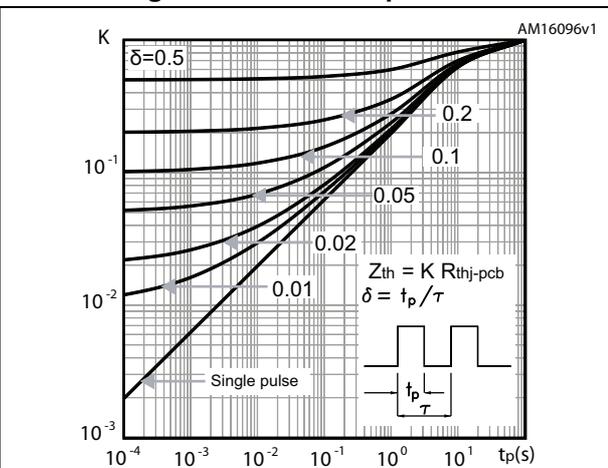


Figure 4. Output characteristics

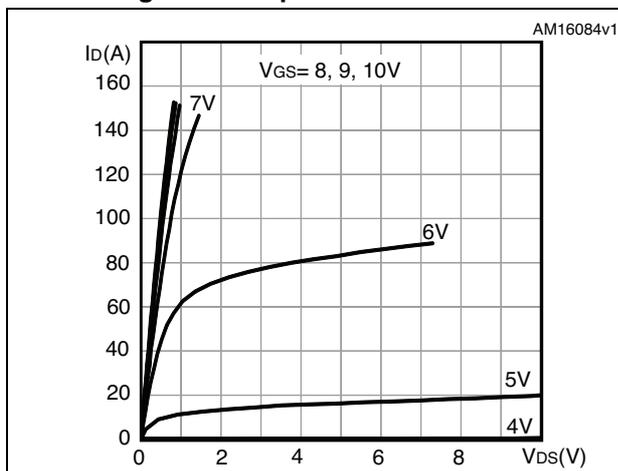


Figure 5. Transfer characteristics

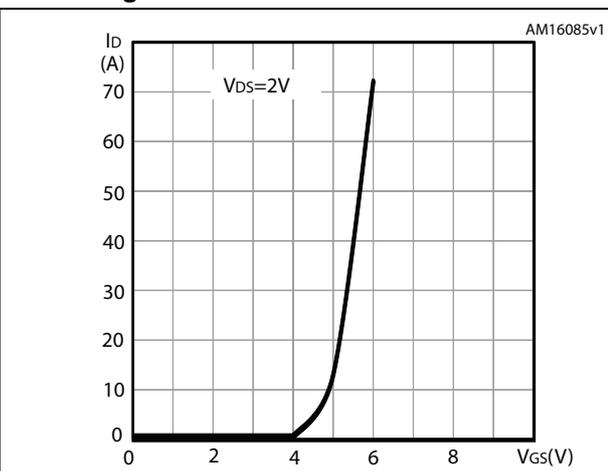


Figure 6. Gate charge vs gate-source voltage

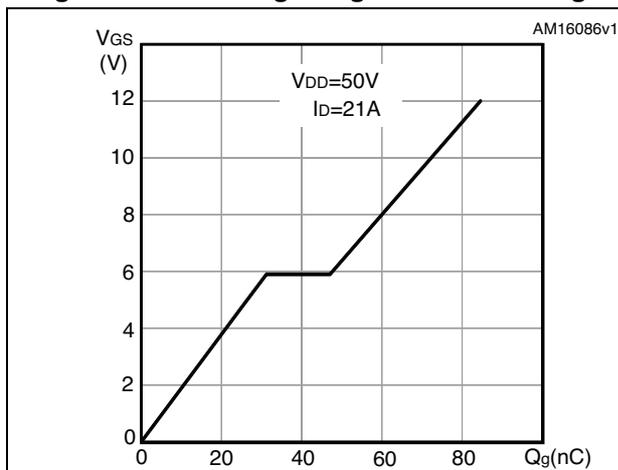


Figure 7. Static drain-source on-resistance

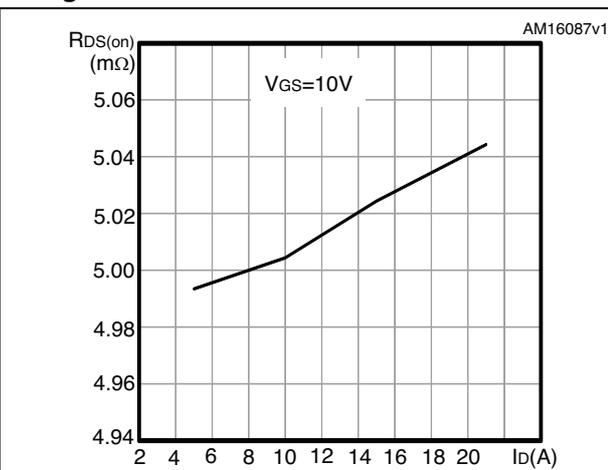


Figure 8. Capacitance variations

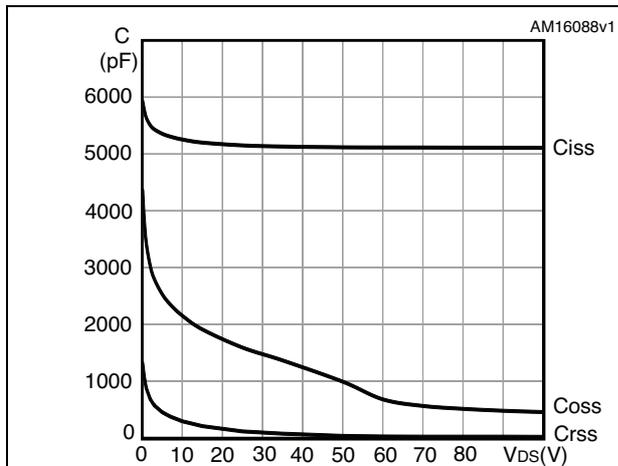


Figure 9. Normalized gate threshold voltage vs temperature

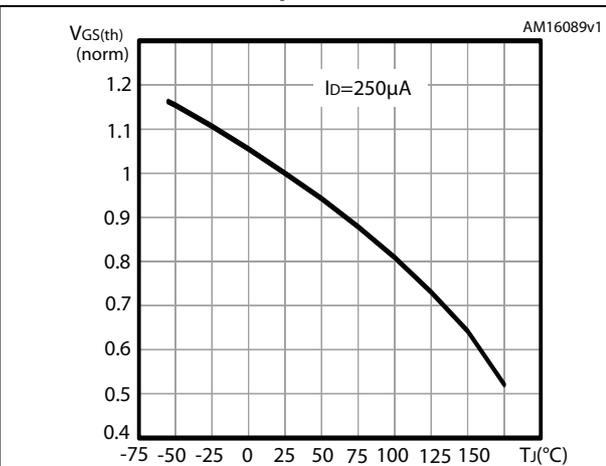


Figure 10. Normalized on-resistance vs temperature

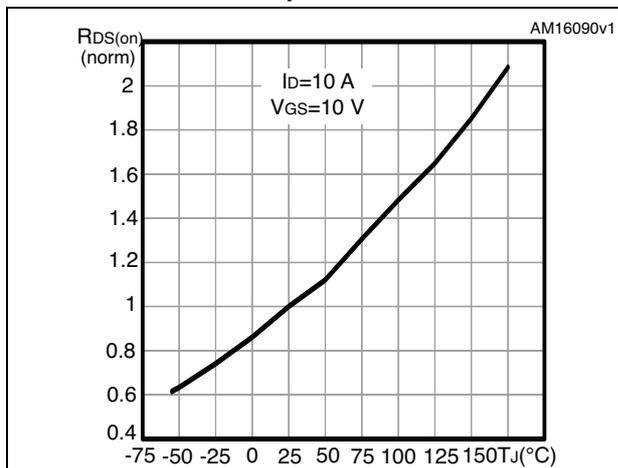


Figure 11. Source-drain diode forward characteristics

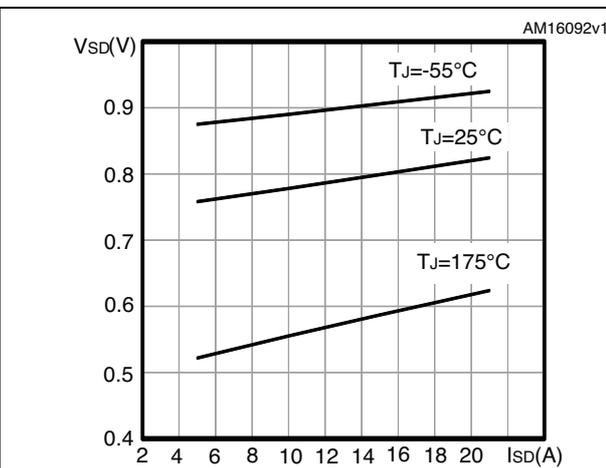
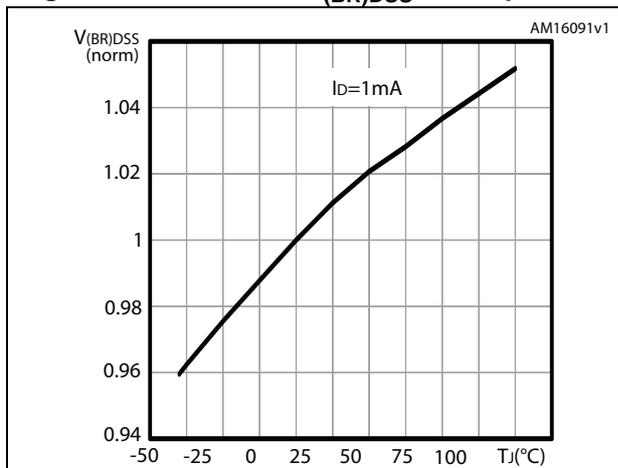


Figure 12. Normalized $V_{(BR)DSS}$ vs temperature



3 Test circuits

Figure 13. Switching times test circuit for resistive load

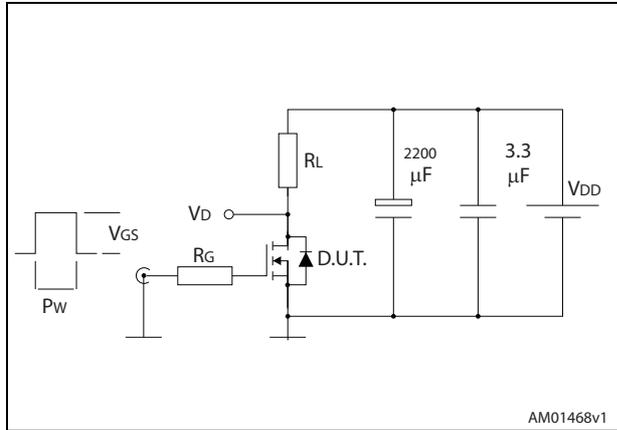


Figure 14. Gate charge test circuit

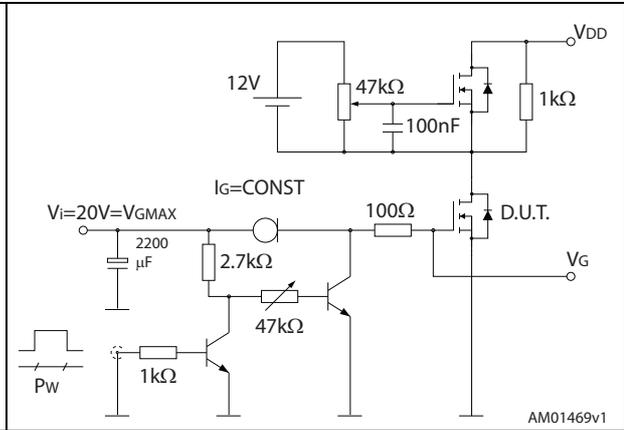


Figure 15. Test circuit for inductive load switching and diode recovery times

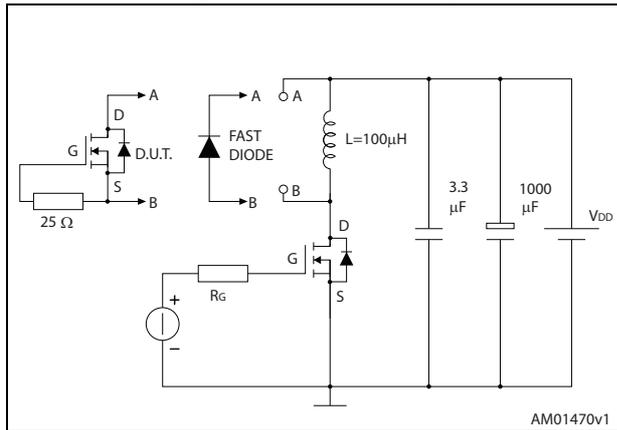


Figure 16. Unclamped inductive load test circuit

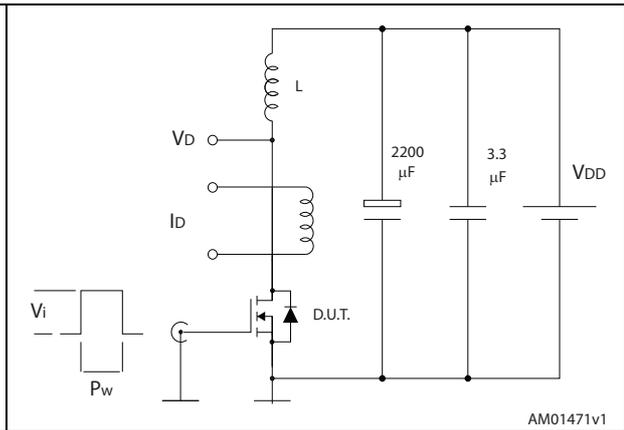


Figure 17. Unclamped inductive waveform

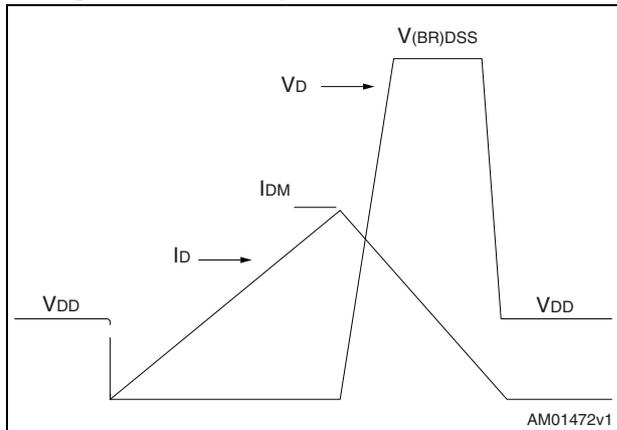
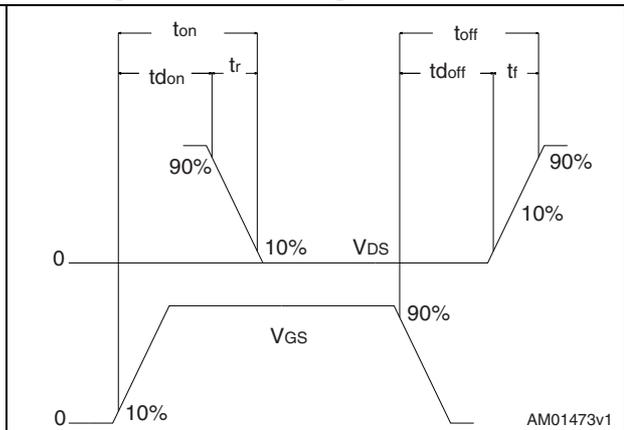


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 19. PowerFLAT™ 5x6 type S-C mechanical data

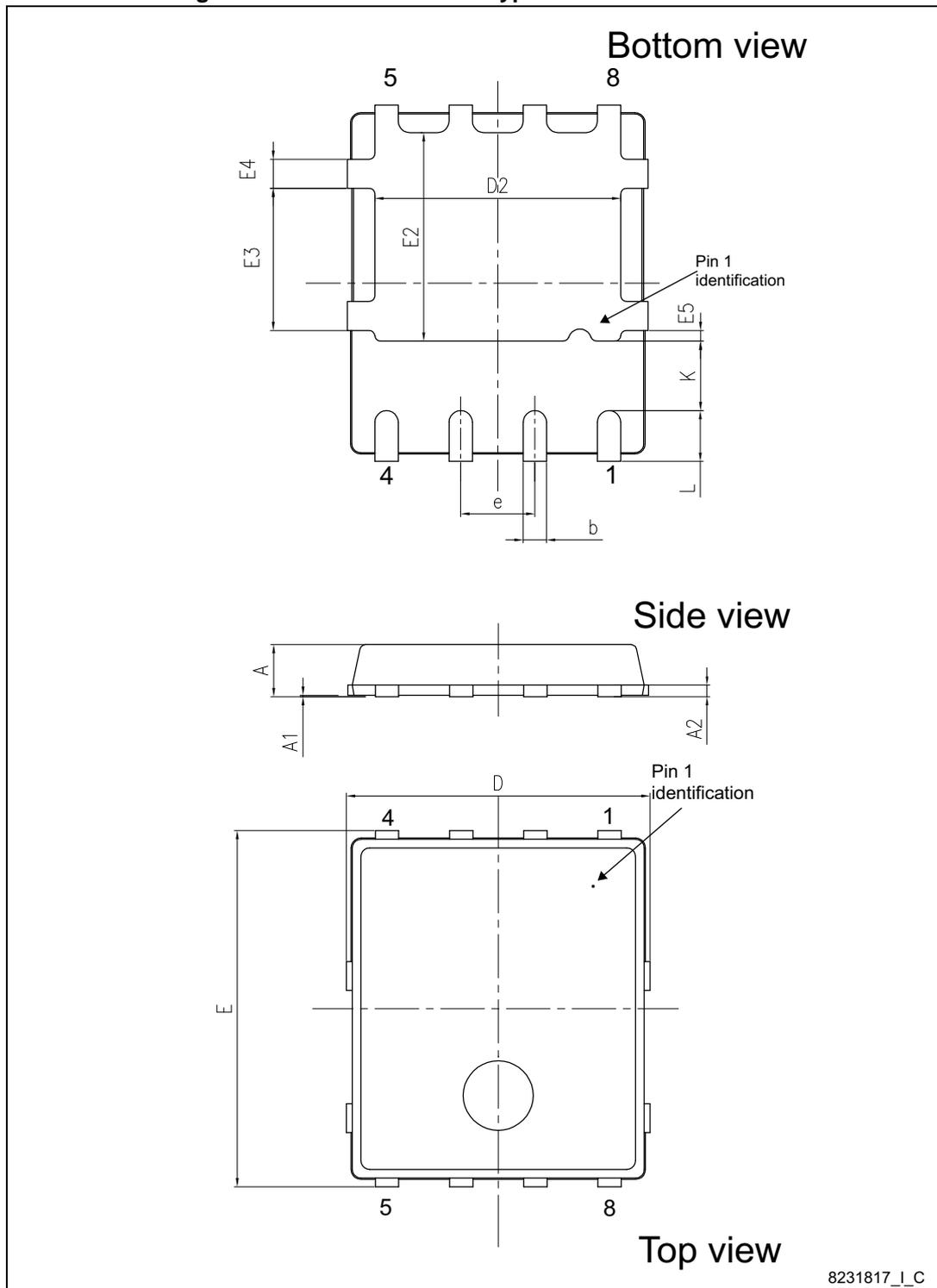
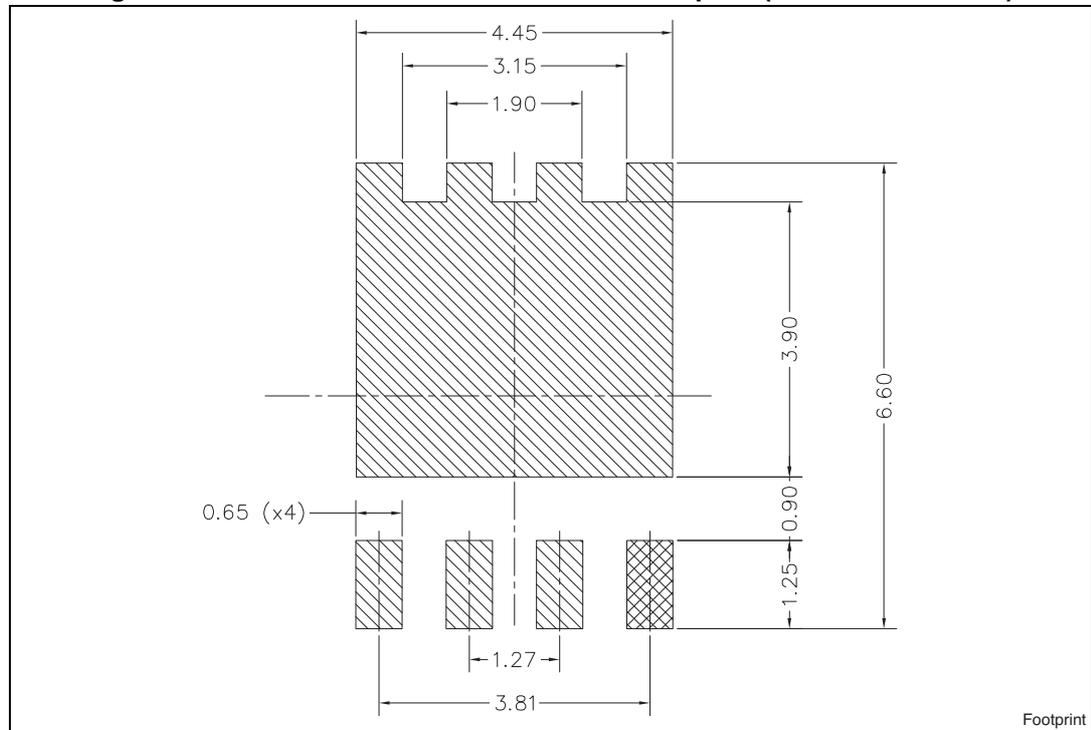


Table 8. PowerFLAT™ 5x6 type S-C mechanical data

| Dim. | mm | | |
|------|-------|------|-------|
| | Min. | Typ. | Max. |
| A | 0.80 | | 1.00 |
| A1 | 0.02 | | 0.05 |
| A2 | | 0.25 | |
| b | 0.30 | | 0.50 |
| D | | 5.20 | |
| D2 | 4.11 | | 4.31 |
| E | | 6.15 | |
| e | | 1.27 | |
| e1 | | 0.65 | |
| E2 | 3.50 | | 3.70 |
| E3 | 2.35 | | 2.55 |
| E4 | 0.40 | | 0.60 |
| E5 | 0.08 | | 0.28 |
| K | 1.05 | | 1.35 |
| L | 0.715 | | 1.015 |

Figure 20. PowerFLAT™ 5x6 recommended footprint (dimensions in mm)



5 Packaging mechanical data

Figure 21. PowerFLAT™ 5x6 tape(a)

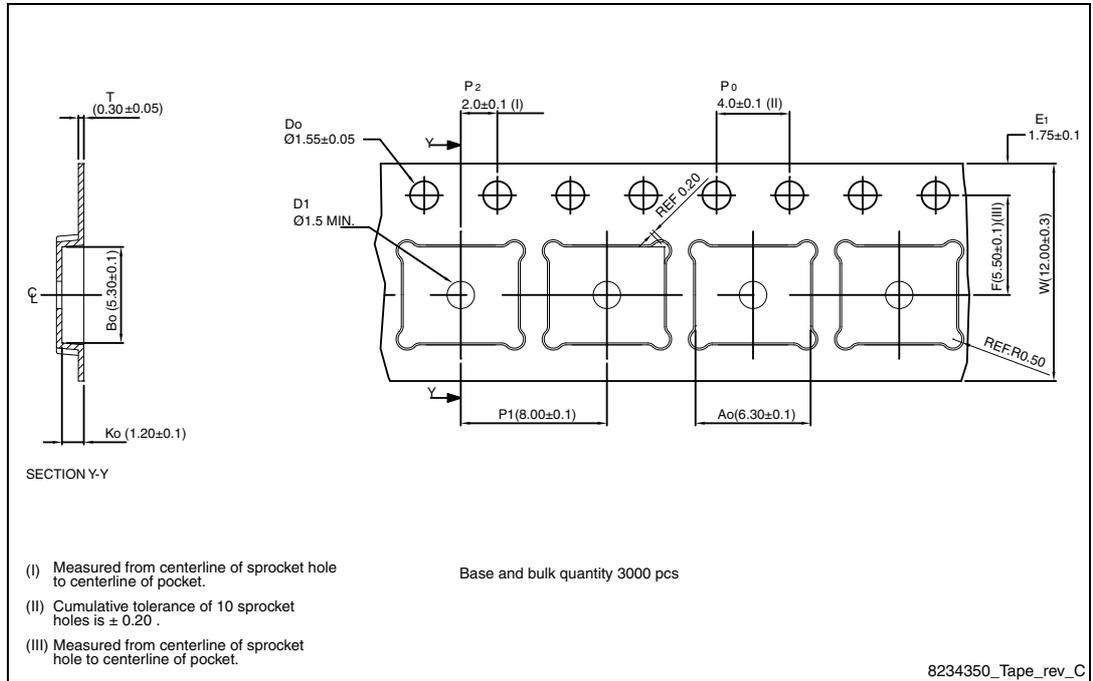
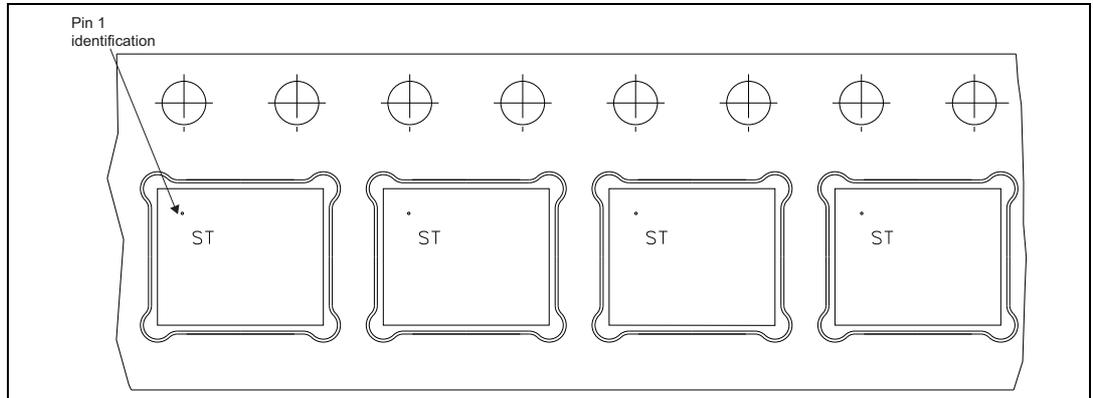


Figure 22. PowerFLAT™ 5x6 package orientation in carrier tape



a. All dimensions are in millimeters.

6 Revision history

Table 9. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 03-Dec-2012 | 1 | First release. |
| 12-Dec-2013 | 2 | <ul style="list-style-type: none"> – Modified: P_{TOT} value and <i>Figure 1</i> in cover page – Modified: I_D, I_{DM} and P_{TOT} values in <i>Table 2</i> – Added: E_{AS} value in <i>Table 2</i> – Modified: all values in <i>Table 3</i> – Modified: I_{DSS}, I_{GSS} and I_D for $R_{DS(on)}$ – Updated: the entire typical values in <i>Table 5, 6</i> and <i>7</i> – Updated: <i>Figure 13, 14, 15</i> and <i>16</i> – Minor text changes |
| 25-Mar-2014 | 3 | <ul style="list-style-type: none"> – Updated title and features on cover page. – Added P_{TOT} value at $T_C = 25\text{ °C}$ in <i>Table 2: Absolute maximum ratings</i>. – Updated <i>Section 4: Package mechanical data</i>. |
| 20-Aug-2014 | 4 | <ul style="list-style-type: none"> – Modified: title, features and description – Modified: <i>Figure 2</i> and <i>3</i> – Updated: <i>Section 4: Package mechanical data</i> – Minor text changes |

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