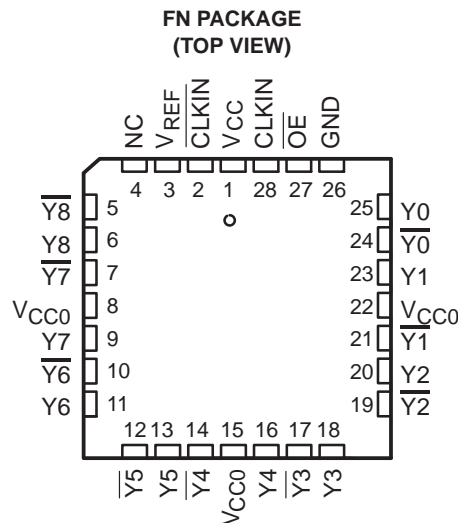


# CDC111

## 1-LINE TO 9-LINE DIFFERENTIAL LVPECL CLOCK DRIVER

SCAS321G – SEPTEMBER 1993 – REVISED AUGUST 1999

- **Low-Output Skew for Clock-Distribution Applications**
- **Differential Low-Voltage Pseudo-ECL (LVPECL)-Compatible Inputs and Outputs**
- **Distributes Differential Clock Inputs to Nine Differential Clock Outputs**
- **Output Reference Voltage,  $V_{REF}$ , Allows Distribution From a Single-Ended Clock Input**
- **Single-Ended LVPECL-Compatible Output Enable**
- **Packaged in Plastic Chip Carrier**



NC – No internal connection

### description

The differential LVPECL clock-driver circuit distributes one pair of differential LVPECL clock inputs (CLKIN,  $\overline{\text{CLKIN}}$ ) to nine pairs of differential clock (Y,  $\overline{\text{Y}}$ ) outputs with minimum skew for clock distribution. It is specifically designed for driving 50- $\Omega$  transmission lines.

When the output-enable ( $\overline{\text{OE}}$ ) is low, the nine differential outputs switch at the same frequency as the differential clock inputs. When  $\overline{\text{OE}}$  is high, the nine differential outputs are in static states (Y outputs are in the low state,  $\overline{\text{Y}}$  outputs are in the high state).

The  $V_{REF}$  output can be strapped to the  $\overline{\text{CLKIN}}$  input for a single-ended CLKIN input.

The CDC111 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUTS	
CLKIN	$\overline{\text{CLKIN}}$	$\overline{\text{OE}}$	Yn	$\overline{\text{Yn}}$
X	X	H	L	H
L	H	L	L	H
H	L	L	H	L
L	$V_{REF}$	L	L	H
H	$V_{REF}$	L	H	L
$V_{REF}$	L	L	H	L
$V_{REF}$	H	L	L	H



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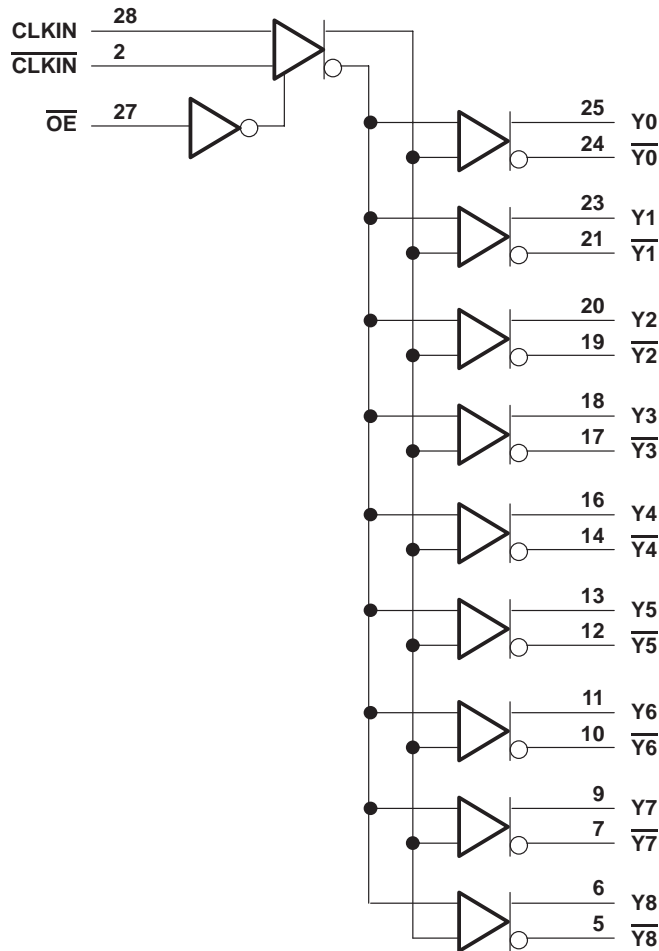
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# CDC111

## 1-LINE TO 9-LINE DIFFERENTIAL LVPECL CLOCK DRIVER

SCAS321G – SEPTEMBER 1993 – REVISED AUGUST 1999

### logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	–18 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	–50 mA
Continuous current through $V_{CC}$ or GND	$\pm 80$ mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2)	525 mW
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.



# CDC111

## 1-LINE TO 9-LINE DIFFERENTIAL LVPECL CLOCK DRIVER

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### recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		3	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC}-1.165$	$V_{CC}-0.88$	V
		$V_{CC} = 3.3\text{ V}$	2.135	2.420	V
$V_{IL}$	Low-level input voltage	$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC}-1.81$	$V_{CC}-1.475$	V
		$V_{CC} = 3.3\text{ V}$	1.49	1.825	V
$T_A$	Operating free-air temperature		0	70	°C
$f_{\text{clock}}$	Input frequency			500	MHz

NOTE 3:  $V_{CC} = V_{CCO}$

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$V_{REF}$	$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC}-1.38$	$V_{CC}-1.26$	V
	$V_{CC} = 3.3\text{ V}$	1.92	2.04	
$V_{OH}$	$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC}-1.025$	$V_{CC}-0.88$	V
	$V_{CC} = 3.3\text{ V}$	2.275	2.42	
$V_{OL}$	$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC}-1.81$	$V_{CC}-1.62$	V
	$V_{CC} = 3.3\text{ V}$	1.49	1.68	
$I_I$	$V_I = 2.4\text{ V},$ $V_{CC} = 3.6\text{ V}$		150	$\mu\text{A}$
$I_{CC}$	$I_O = 0,$ $V_{CC} = 3.6\text{ V}$		80	mA

### switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (see Figures 1 and 2)

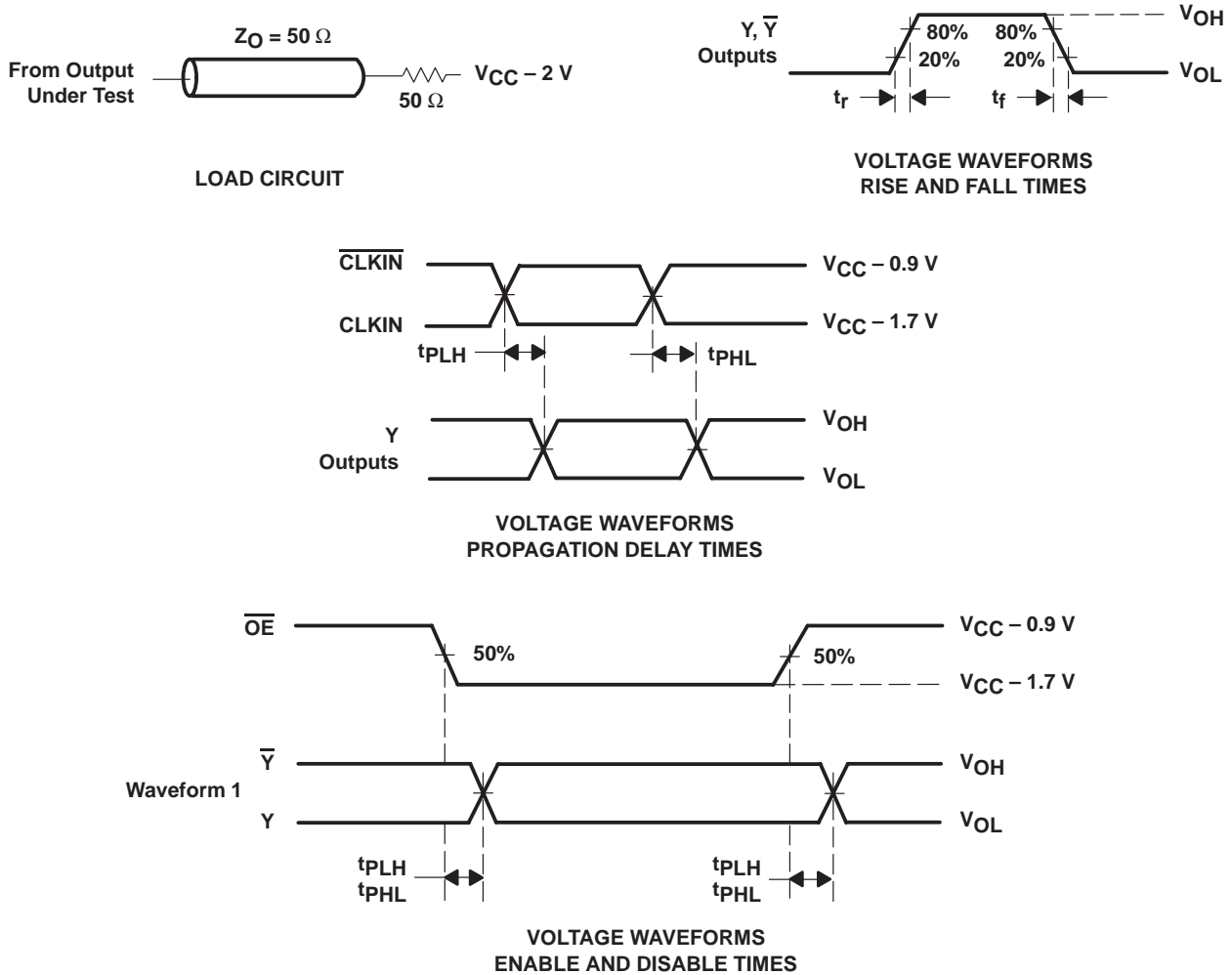
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{PLH}$	CLKIN, $\overline{\text{CLKIN}}$	Y, $\overline{\text{Y}}$	450	600	ps
$t_{PHL}$			450	600	
$t_{PHL}$	$\overline{\text{OE}}$	Y, $\overline{\text{Y}}$		900	ps
$t_{sk(o)}$		Y, $\overline{\text{Y}}$		50	ps
$t_{sk(pr)}$		Y, $\overline{\text{Y}}$		150	ps
$t_r$		Y, $\overline{\text{Y}}$	200	600	ps
$t_f$		Y, $\overline{\text{Y}}$	200	600	ps

# CDC111

## 1-LINE TO 9-LINE DIFFERENTIAL LVPECL CLOCK DRIVER

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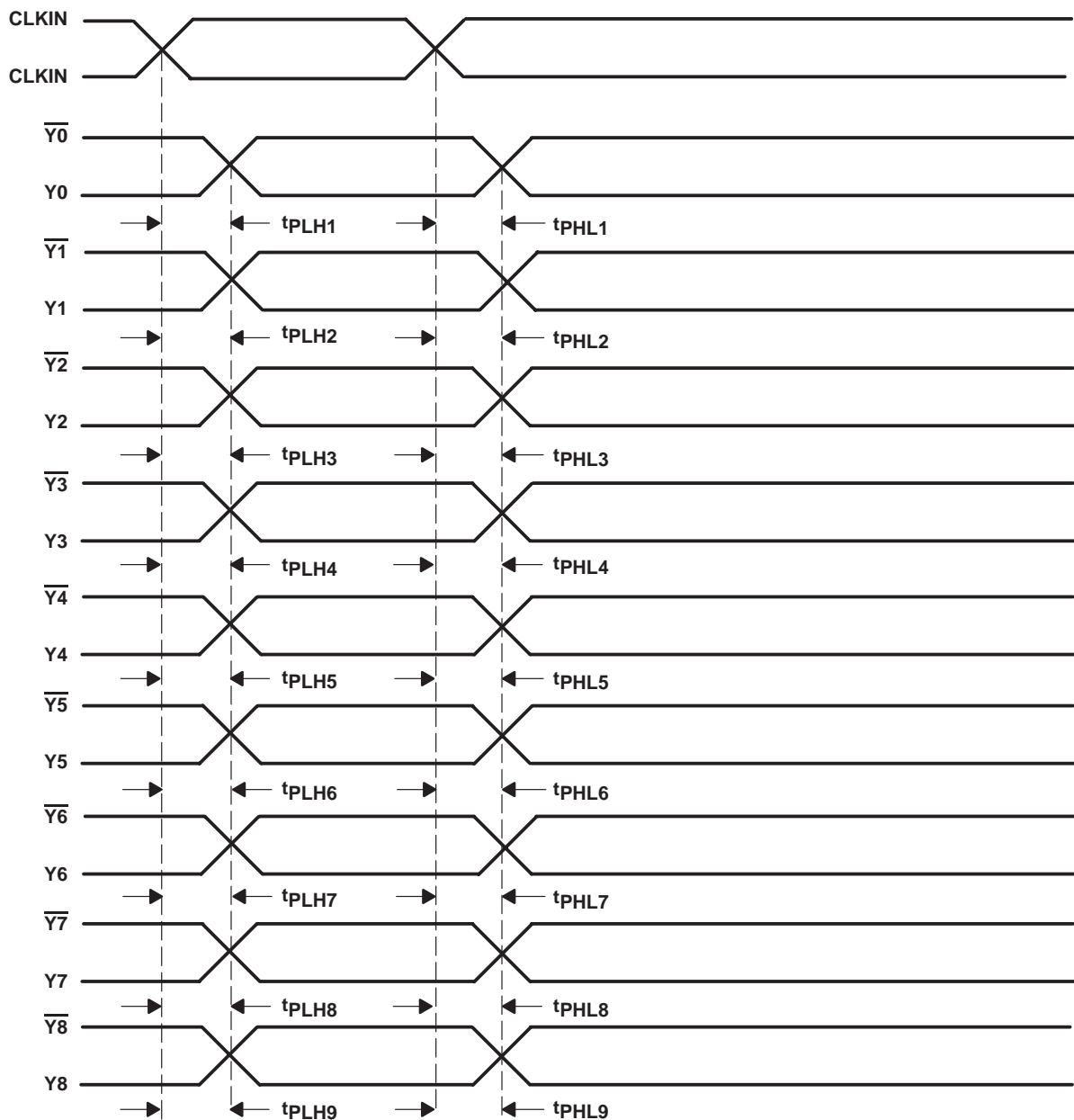
### PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 45 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 1 \text{ ns}$ ,  $t_f \leq 1 \text{ ns}$ .
  - B. Waveform 1 is for a  $\bar{Y}$  output with internal conditions such that the output is high except when disabled by the output control, and for a  $Y$  output with internal conditions such that the output is low except when disabled by the output control.
  - C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A. Output skew,  $t_{sk(o)}$ , is calculated as the greater of:
- The difference between the fastest and slowest  $t_{PLHn}$  ( $n = 1, 2, \dots, 9$ )
  - The difference between the fastest and slowest  $t_{PHLn}$  ( $n = 1, 2, \dots, 9$ )
- B. Process skew,  $t_{sk(pr)}$ , is calculated as the greater of:
- The difference between the fastest and slowest  $t_{PLHn}$  ( $n = 1, 2, \dots, 9$ )
  - The difference between the fastest and slowest  $t_{PHLn}$  ( $n = 1, 2, \dots, 9$ ) across multiple devices

**Figure 2. Waveforms for Calculation of  $t_{sk(o)}$ ,  $t_{sk(pr)}$**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CDC111FN	ACTIVE	PLCC	FN	28	37	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC111FNR	ACTIVE	PLCC	FN	28	750	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC111FNRG4	ACTIVE	PLCC	FN	28	750	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

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<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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CDC111FN	ACTIVE	PLCC	FN	28	37	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Request Free Samples</a>

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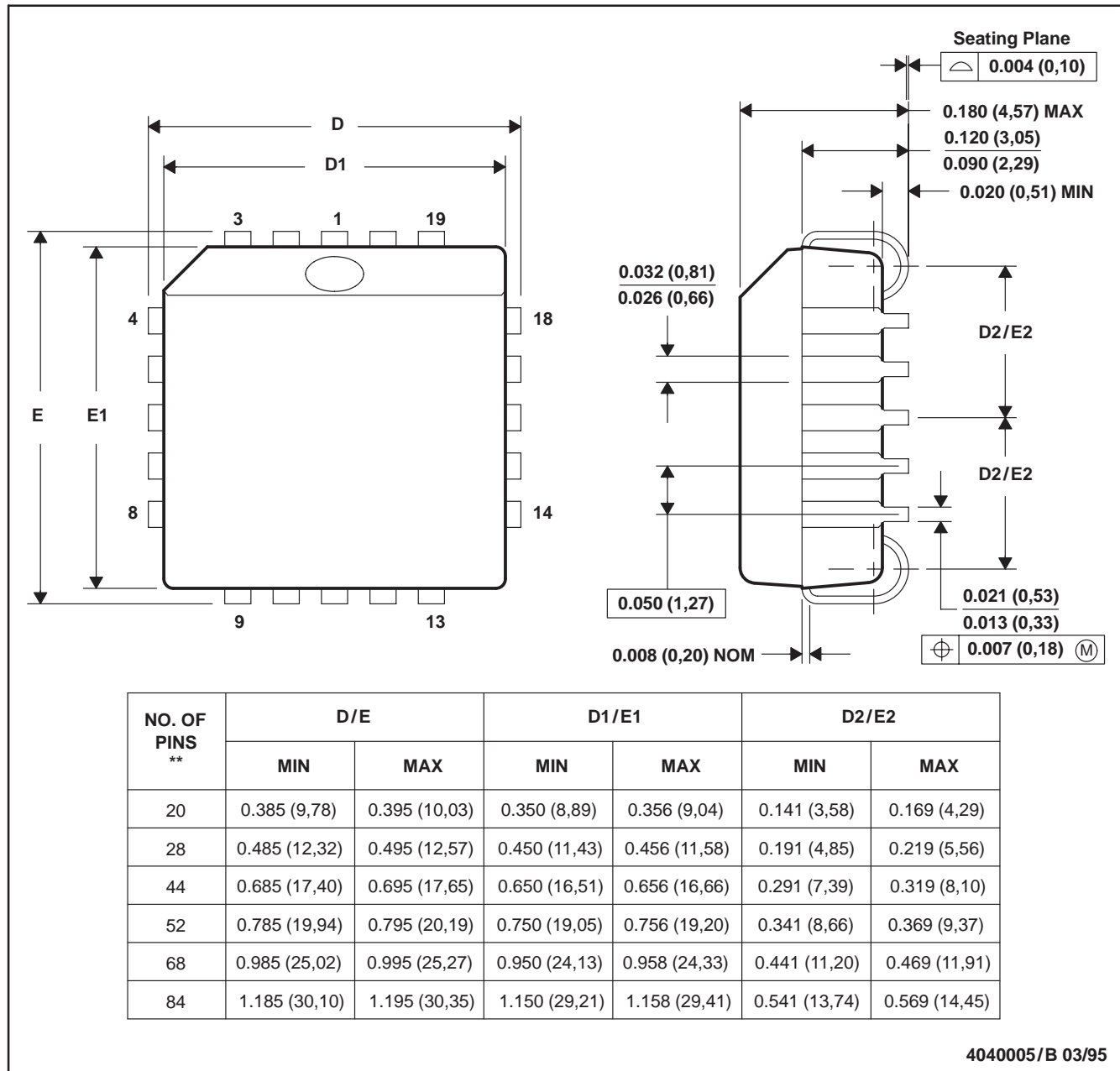
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FN (S-PQCC-J\*\*)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-018



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