LM6181 100 mA, 100 MHz Current Feedback Amplifier

1 Features(1)

- Slew Rate: 2000 V/μs
- Settling Time (0.1%): 50 ns
- Characterized for Supply Ranges: ± 5 V and ±15 V
- Low Differential Gain and Phase Error: 0.05%, 0.04°
- High Output Drive: ±10 V into 100 Ω
- Ensured Bandwidth and Slew Rate
- Improved Performance Over EL2020, OP160, AD844, LT1223 and HA5004

(1) Typical, unless otherwise noted

2 Applications

- Coax Cable Driver
- Video Amplifier
- Flash ADC Buffer
- High Frequency Filter
- Scanner and Imaging Systems

3 Description

The LM6181 current-feedback amplifier offers an unparalleled combination of bandwidth, slew-rate, and output current. The amplifier can directly drive up to 100 pF capacitive loads without oscillating and a 10-V signal into a 50-Ω or 75-Ω back-terminated coax cable system over the full industrial temperature range. This represents a radical enhancement in output drive capability for an 8-pin PDIP high-speed amplifier making it ideal for video applications.

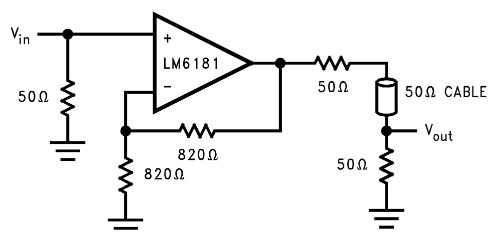
Built on TI's advanced high-speed VIP™ II (Vertically Integrated PNP) process, the LM6181 employs current-feedback providing bandwidth that does not vary dramatically with gain; 100 MHz at A_V = −1, 60 MHz at A_V = −10. With a slew rate of 2000V/μs, 2nd harmonic distortion of −50 dBc at 10 MHz and settling time of 50 ns (0.1%) the LM6181 dynamic performance makes it ideal for data acquisition, high speed ATE, and precision pulse amplifier applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM6181	PDIP (8)	9.81 mm × 6.35 mm
LM6181	CDIP (8)	10.16 mm × 6.502 mm
LM6181	SOIC (16)	9.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Cable Driver



Step Response

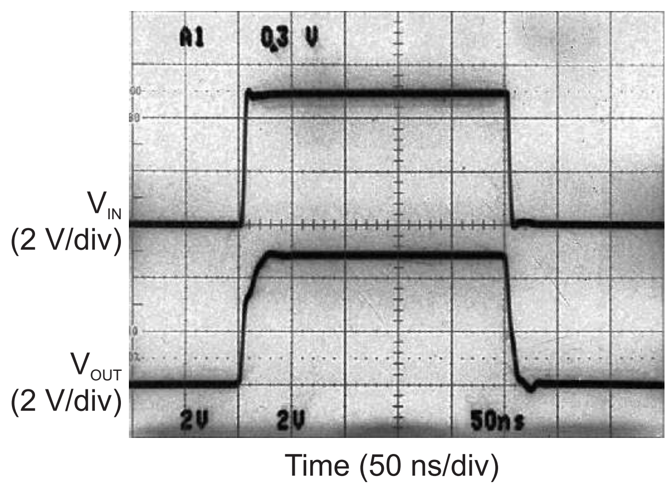


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

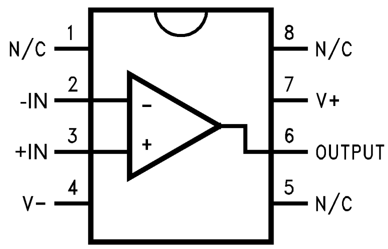
Changes from Revision B (May 2013) to Revision C	Page
• Changed data sheet structure and organization. Added, updated, or renamed the following sections: Device Information Table, Pin Configuration and Functions, Application and Implementation; Device and Documentation Support; Mechanical, Packaging, and Ordering Information. Updated selected plots for readability.	1
• Changed "Junction Temperature Range" to " Operating Temperature Range" and deleted T_J	4
• Deleted T_J = 25°C for Electrical Characteristics tables	5

Changes from Revision A (May 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	1

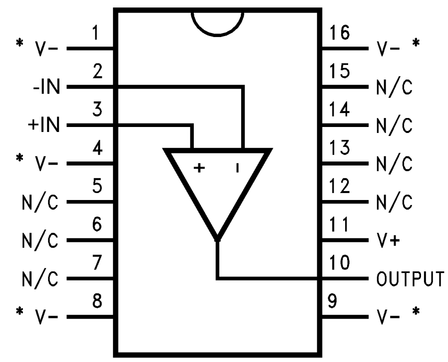
5 Pin Configuration and Functions

* indicates heat sinking pins(1)

**8–Pin CDIP, PDIP, or SOIC
Package NAB, P, or D
(Top View)**



**16-Pin SOIC
Package D
(Top View)**



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NUMBER			
	NAB, P, D (8)	D (16)		
-IN	2	2	I	Inverting Input
+IN	3	3	I	Non-inverting Input
N/C	1, 5, 8	5, 6, 7 12, 13, 14, 15	—	No Connection
OUTPUT	6	10	O	Output
V-	4	1, 4, 8, 9, 16	I	Negative Supply
V+	7	11	I	Positive Supply

(1) The typical junction-to-ambient thermal resistance of the molded PDIP package soldered directly into a PC board is 102°C/W. The junction-to-ambient thermal resistance of the SOIC package mounted flush to the PC board is 70°C/W when pins 1, 4, 8, 9 and 16 are soldered to a total 2 in^2 1 oz. copper trace. The 16-pin SOIC package must have pin 4 and at least one of pins 1, 8, 9, or 16 connected to V^- for proper operation. The typical junction-to-ambient thermal resistance of the SOIC package soldered directly into a PC board is 153°C/W.

6 Specifications

6.1 Absolute Maximum Ratings(1)(2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
Supply Voltage				±18	V
Differential Input Voltage				±6	V
Input Voltage				±Supply Voltage	V
Inverting Input Current				15	mA
Soldering Information	PDIP Package	Soldering (10 sec)		260	°C
	SOIC Package	Vapor Phase (60 seconds)		215	°C
		Infrared (15 seconds)		220	°C
Output Short Circuit				See(3)	
Maximum Junction Temperature				150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions the device is intended to be functional, but device parameter specifications may not be ensured under these conditions. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±130 mA over a long term basis may adversely affect reliability.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−65	+150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)		±3000	V

(1) JEDEC document JEP155 states that 3000-V HBM allows safe manufacturing with a standard ESD control process. Human body model 100 pF and 1.5 kΩ.

6.3 Recommended Operating Conditions(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply Voltage Range		7	32	V
Operating Temperature Range	LM6181AM	−55	+125	°C
	LM6181AI, LM6181I	−40	+85	°C

(1) For ensured Military Temperature Range parameters see RETS6181X.

6.4 Thermal Information

THERMAL METRIC(1)(2)		P (PDIP)	D (SOIC)	D (SOIC)	UNIT
		8 PINS	8 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102	153	70	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42	42	38	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The typical junction-to-ambient thermal resistance of the molded PDIP package soldered directly into a PC board is 102°C/W. The junction-to-ambient thermal resistance of the SOIC package mounted flush to the PC board is 70°C/W when pins 1, 4, 8, 9 and 16 are soldered to a total 2 in2 1 oz. copper trace. The 16-pin SOIC package must have pin 4 and at least one of pins 1, 8, 9, or 16 connected to V− for proper operation. The typical junction-to-ambient thermal resistance of the SOIC package soldered directly into a PC board is 153°C/W."

6.5 ±15V DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, R_F = 820 Ω, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	LM6181AM		LM6181AI		LM6181I		UNIT
			TYP(1)	LIMIT(2)	TYP(1)	LIMIT(2)	TYP(1)	LIMIT(2)	
V_{OS}	Input Offset Voltage		2.0	3.0 **4.0**	2.0	3.0 **3.5**	3.5	5.0 **5.5**	mV max
TC V_{OS}	Input Offset Voltage Drift		5.0		5.0		5.0		μV/°C
I_B	Inverting Input Bias Current		2.0	5.0 **12.0**	2.0	5.0 **12.0**	5.0	10 **17.0**	μA max
	Non-Inverting Input Bias Current		0.5	1.5 **3.0**	0.5	1.5 **3.0**	2.0	3.0 **5.0**	
TC I_B	Inverting Input Bias Current Drift		30		30		30		nA/°C
	Non-Inverting Input Bias Current Drift		10		10		10		
I_B PSR	Inverting Input Bias Current Power Supply Rejection	V_S = ±4.5V, ±16V	0.3	0.5 **3.0**	0.3	0.5 **3.0**	0.3	0.75 **4.5**	μA/V max
	Non-Inverting Input Bias Current Power Supply Rejection	V_S = ±4.5V, ±16V	0.05	0.5 **1.5**	0.05	0.5 **1.5**	0.05	0.5 **3.0**	
I_B CMR	Inverting Input Bias Current Common Mode Rejection	−10V ≤ V_{CM} ≤ +10V	0.3	0.5 **0.75**	0.3	0.5 **0.75**	0.3	0.75 **1.0**	
	Non-Inverting Input Bias Current Common Mode Rejection	−10V ≤ V_{CM} ≤ +10V	0.1	0.5 **0.5**	0.1	0.5 **0.5**	0.1	0.5 **0.5**	
CMRR	Common Mode Rejection Ratio	−10V ≤ V_{CM} ≤ +10V	60	50 **50**	60	50 **50**	60	50 **50**	dB min
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V, ±16V	80	70 **70**	80	70 **70**	80	70 **65**	dB min
R_O	Output Resistance	A_V = −1, f = 300 kHz	0.2		0.2		0.2		Ω
R_{IN}	Non-Inverting Input Resistance		10		10		10		MΩ min
V_O	Output Voltage Swing	R_L = 1 kΩ	12	11 **11**	12	11 **11**	12	11 **11**	V min
		R_L = 100Ω	11	10 **7.5**	11	10 **8.0**	11	10 **8.0**	
I_{SC}	Output Short Circuit Current		130	100 **75**	130	100 **85**	130	100 **85**	mA min
Z_T	Transimpedance	R_L = 1 kΩ	1.8	1.0 **0.5**	1.8	1.0 **0.5**	1.8	0.8 **0.4**	MΩ min
		R_L = 100Ω	1.4	0.8 **0.4**	1.4	0.8 **0.4**	1.4	0.7 **0.35**	
I_S	Supply Current	No Load, V_O = 0V	7.5	10 **10**	7.5	10 **10**	7.5	10 **10**	mA max
V_{CM}	Input Common Mode Voltage Range		$V^+ - 1.7$ $V^- + 1.7$		$V^+ - 1.7$ $V^- + 1.7$		$V^+ - 1.7$ $V^- + 1.7$		V

(1) Typical values represent the most likely parametric norm.
(2) All limits ensured at room temperature (standard type face) or at operating temperature extremes **(bold face type)**.

6.6 ±15V AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, R_F = 820 Ω, R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes.

	PARAMETER	TEST CONDITIONS	LM6181AM		LM6181AI		LM6181I		UNIT
			TYP(1)	LIMIT(2)	TYP(1)	LIMIT(2)	TYP(1)	LIMIT(2)	
BW	Closed Loop Bandwidth −3 dB	A_V = +2	100		100		100		MHz min
		A_V = +10	80		80		80		
		A_V = −1	100	80	100	80	100	80	
		A_V = −10	60		60		60		
PBW	Power Bandwidth	A_V = −1, V_O = 5 V_{PP}	60		60		60		
SR	Slew Rate	Overdriven	2000		2000		2000		V/μs min
		A_V = −1, V_O = ±10V, R_L = 150Ω(3)	1400	1000	1400	1000	1400	1000	
t_s	Settling Time (0.1%)	A_V = −1, V_O = ±5V R_L = 150Ω	50		50		50		ns
t_r, t_f	Rise and Fall Time	V_O = 1 V_{PP}	5		5		5		
t_p	Propagation Delay Time	V_O = 1 V_{PP}	6		6		6		
$i_{n(+)}$	Non-Inverting Input Noise Current Density	f = 1 kHz	3		3		3		pA/√Hz
$i_{n(-)}$	Inverting Input Noise Current Density	f = 1 kHz	16		16		16		pA/√Hz
e_n	Input Noise Voltage Density	f = 1 kHz	4		4		4		pA/√Hz
	Second Harmonic Distortion	2 V_{PP}, 10 MHz	−50		−50		−50		dBc
	Third Harmonic Distortion	2 V_{PP}, 10 MHz	−55		−55		−50		
	Differential Gain	R_L = 150Ω, A_V = +2, NTSC	0.05%		0.05%		0.05%		
	Differential Phase	R_L = 150Ω, A_V = +2, NTSC	0.04		0.04		0.04		Deg

(1) Typical values represent the most likely parametric norm.
(2) All limits ensured at room temperature (standard type face) or at operating temperature extremes **(bold face type)**.
(3) Measured from +25% to +75% of output waveform.

6.7 ±5V DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±5V, R_F = 820 Ω, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	LM6181AM		LM6181AI		LM6181I		UNIT
			TYP (1)	LIMIT (2)	TYP (1)	LIMIT (2)	TYP (1)	LIMIT (2)	
V_{OS}	Input Offset Voltage		1.0	2.0 **3.0**	1.0	2.0 **2.5**	1.0	3.0 **3.5**	mV max
TC V_{OS}	Input Offset Voltage Drift		2.5		2.5		2.5		μV/°C
I_B	Inverting Input Bias Current		5.0	10 **22**	5.0	10 **22**	5.0	17.5 **27.0**	μA max
	Non-Inverting Input Bias Current		0.25	1.5 **1.5**	0.25	1.5 **1.5**	0.25	3.0 **5.0**	μA max
TC I_B	Inverting Input Bias Current Drift		50		50		50		nA/°C
	Non-Inverting Input Bias Current Drift		3.0		3.0		3.0		nA/°C
I_B PSR	Inverting Input Bias Current Power Supply Rejection	V_S = ±4.0V, ±6.0V	0.3	0.5 **0.5**	0.3	0.5 **0.5**	0.3	1.0 **1.0**	μA/V max
	Non-Inverting Input Bias Current Power Supply Rejection	V_S = ±4.0V, ±6.0V	0.05	0.5 **0.5**	0.05	0.5 **0.5**	0.05	0.5 **0.5**	μA/V max
I_B CMR	Inverting Input Bias Current Common Mode Rejection	−2.5V ≤ V_{CM} ≤ +2.5V	0.3	0.5 **1.0**	0.3	0.5 **1.0**	0.3	1.0 **1.5**	μA/V max
	Non-Inverting Input Bias Current Common Mode Rejection	−2.5V ≤ V_{CM} ≤ +2.5V	0.12	0.5 **1.0**	0.12	0.5 **0.5**	0.12	0.5 **0.5**	μA/V max
CMRR	Common Mode Rejection Ratio	−2.5V ≤ V_{CM} ≤ +2.5V	57	50 **47**	57	50 **47**	57	50 **47**	dB min
PSRR	Power Supply Rejection Ratio	V_S = ±4.0V, ±6.0V	80	70 **70**	80	70 **70**	80	64 **64**	dB min
R_O	Output Resistance	A_V = −1, f = 300 kHz	0.25		0.25		0.25		Ω
R_{IN}	Non-Inverting Input Resistance		8		8		8		MΩ min
V_O	Output Voltage Swing	R_L = 1 kΩ	2.6	2.25 **2.2**	2.6	2.25 **2.25**	2.6	2.25 **2.25**	V min
		R_L = 100Ω	2.2	2.0 **2.0**	2.2	2.0 **2.0**	2.2	2.0 **2.0**	V min
I_{SC}	Output Short Circuit Current		100	75 **70**	100	75 **70**	100	75 **70**	mA min
Z_T	Transimpedance	R_L = 1 kΩ	1.4	0.75 **0.35**	1.4	0.75 **0.4**	1.0	0.6 **0.3**	MΩ min
		R_L = 100Ω	1.0	0.5 **0.25**	1.0	0.5 **0.25**	1.0	0.4 **0.2**	MΩ min
I_S	Supply Current	No Load, V_O = 0V	6.5	8.5 **8.5**	6.5	8.5 **8.5**	6.5	8.5 **8.5**	mA max
V_{CM}	Input Common Mode Voltage Range		V^+ − 1.7 V^- + 1.7		V^+ − 1.7 V^- + 1.7		V^+ − 1.7 V^- + 1.7		V

(1) Typical values represent the most likely parametric norm.
(2) All limits ensured at room temperature (standard type face) or at operating temperature extremes **(bold face type)**.

6.8 ±5V AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±5V, R_F = 820 Ω, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	LM6181AM		LM6181AI		LM6181I		UNIT
			TYP (1)	LIMIT (2)	TYP (1)	LIMIT (2)	TYP (1)	LIMIT (2)	
BW	Closed Loop Bandwidth −3 dB	A_V = +2	50		50		50		MHz min
		A_V = +10	40		40		40		
		A_V = −1	55	35	55	35	55	35	
		A_V = −10	35		35		35		
PBW	Power Bandwidth	A_V = −1, V_O = 4 V_{PP}	40		40		40		
SR	Slew Rate	A_V = −1, V_O = ±2V, R_L = 150Ω (3)	500	375	500	375	500	375	V/μs min
t_s	Settling Time (0.1%)	A_V = −1, V_O = ±2V R_L = 150Ω	50		50		50		ns
t_r, t_f	Rise and Fall Time	V_O = 1 V_{PP}	8.5		8.5		8.5		
t_p	Propagation Delay Time	V_O = 1 V_{PP}	8		8		8		
$i_{n(+)}$	Non-Inverting Input Noise Current Density	f = 1 kHz	3		3		3		pA/√Hz
$i_{n(−)}$	Inverting Input Noise Current Density	f = 1 kHz	16		16		16		pA/√Hz
e_n	Input Noise Voltage Density	f = 1 kHz	4		4		4		pA/√Hz
	Second Harmonic Distortion	2 V_{PP}, 10 MHz	−45		−45		−45		dBc
	Third Harmonic Distortion	2 V_{PP}, 10 MHz	−55		−55		−55		
	Differential Gain	R_L = 150 Ω, A_V = +2, NTSC	0.063%		0.063%		0.063%		
	Differential Phase	R_L = 150 Ω, A_V = +2, NTSC	0.16		0.16		0.16		Deg

(1) Typical values represent the most likely parametric norm.
(2) All limits ensured at room temperature (standard type face) or at operating temperature extremes **(bold face type)**.
(3) Measured from +25% to +75% of output waveform.

6.9 Typical Performance Characteristics

T_A = 25°C unless otherwise noted

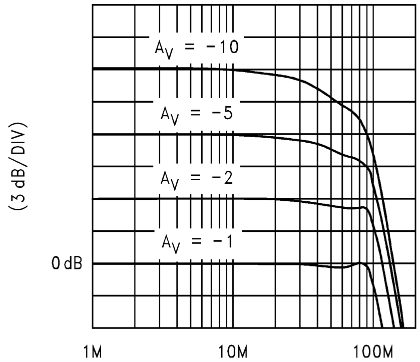


Figure 1. Closed-loop Frequency Response V_S = ±15V; R_f = 820 Ω; R_L = 1 kΩ

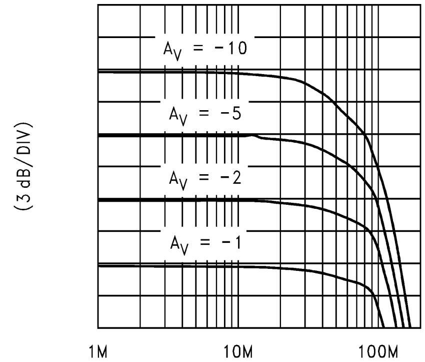


Figure 2. Closed-loop Frequency Response V_S = ±15V; R_f = 820 Ω; R_L = 150Ω

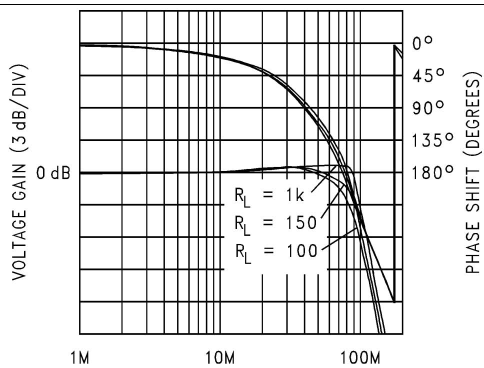


Figure 3. Unity Gain Frequency Response V_S = ±15V; A_V = +1; R_f = 820 Ω

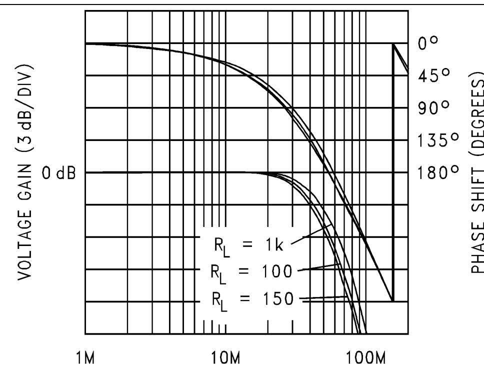


Figure 4. Unit Gain Frequency Response V_S = ±5V; A_V = +1; R_f = 820 Ω

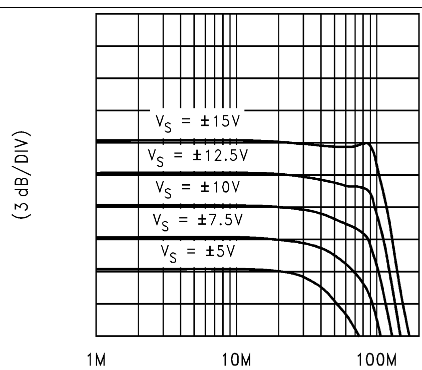


Figure 5. Frequency Response Vs Supply Voltage A_V = −1; R_f = 820 Ω; R_L = 1 kΩ

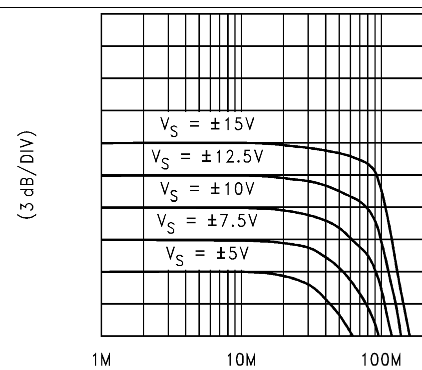


Figure 6. Frequency Response vs. Supply Voltage A_V = −1; R_f = 820 Ω; R_L = 150 Ω

Typical Performance Characteristics (continued)

T_A = 25°C unless otherwise noted

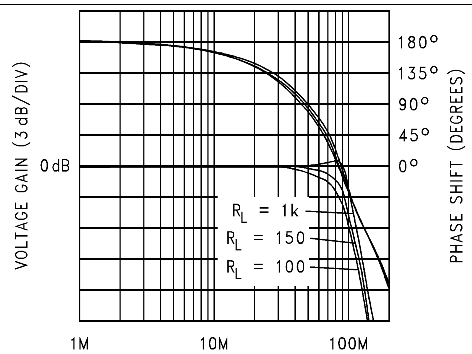


Figure 7. Inverting Gain Frequency Response V_S = ±15V; A_V = −1; R_f = 820 Ω

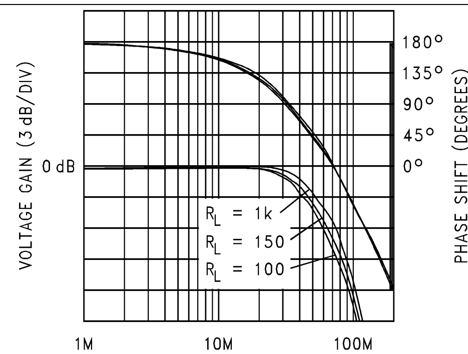


Figure 8. Inverting Gain Frequency Response V_S = ±5V; A_V = −1; R_f = 82 0Ω

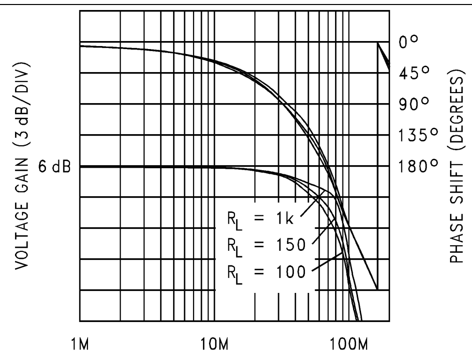


Figure 9. Non-inverting Gain Frequency Response V_S = ±15V; A_V = +2; R_f = 820 Ω

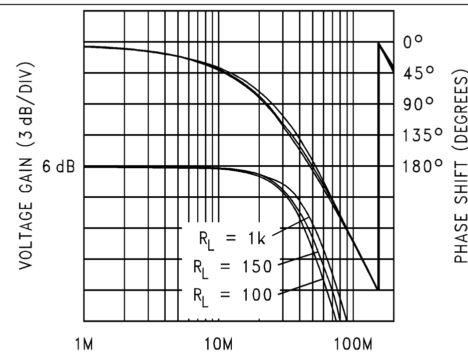


Figure 10. Non-inverting Gain Frequency Response V_S = ±5V; A_V = +2; R_f = 820 Ω

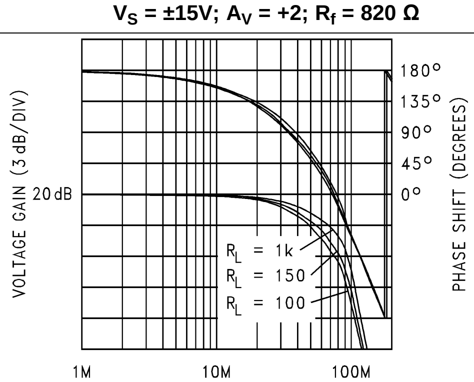


Figure 11. Inverting Gain Frequency Response V_S = ±15V; A_V = −10; R_f = 820 Ω

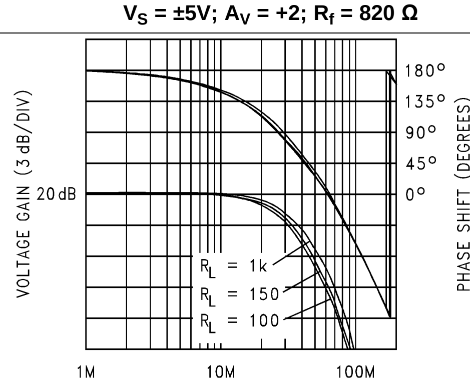


Figure 12. Inverting Gain Frequency Response V_S = ±5V; A_V = −10; R_f = 820 Ω

Typical Performance Characteristics (continued)

T_A = 25°C unless otherwise noted

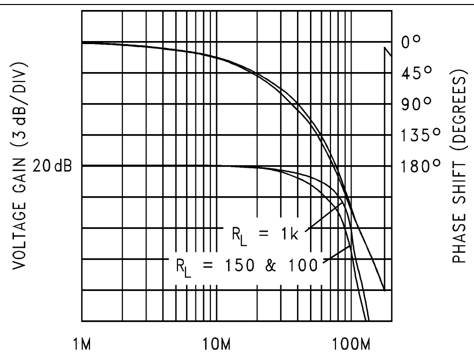


Figure 13. Non-inverting Gain Frequency Response
V_S = ±15V; A_V = +10; R_f = 820 Ω

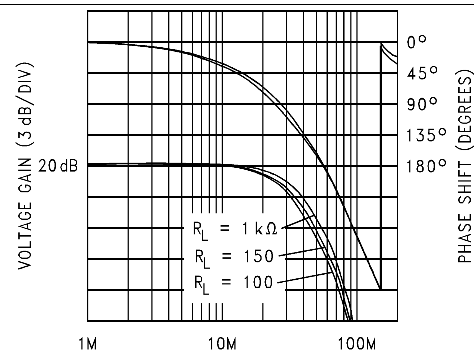


Figure 14. Non-inverting Gain Frequency Response
V_S = ±5V; A_V = +10; R_f = 820 Ω

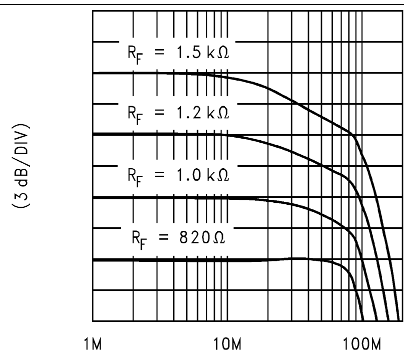


Figure 15. Non-inverting Gain Frequency Compensation
V_S = ±15V; A_V = +2; R_L = 150 Ω

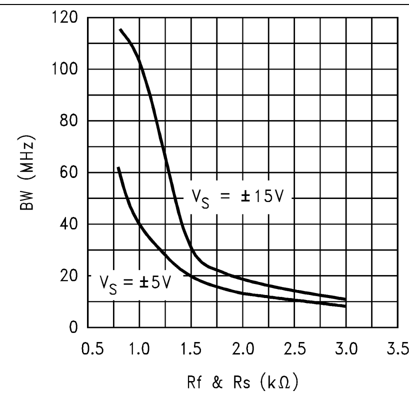


Figure 16. Bandwidth vs R_f & R_S A_V = −1, R_L = 1 kΩ

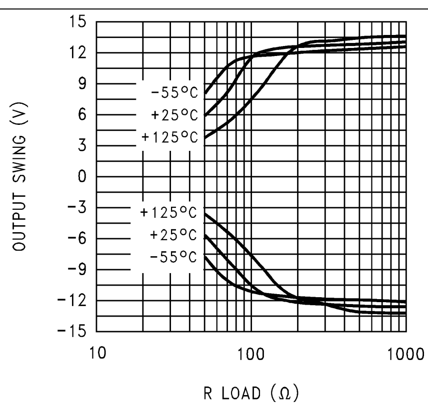


Figure 17. Output Swing vs R_{LOAD} Pulsed,
V_S = ±15V, I_{IN} = ±200 μA, V_{IN+} = 0V

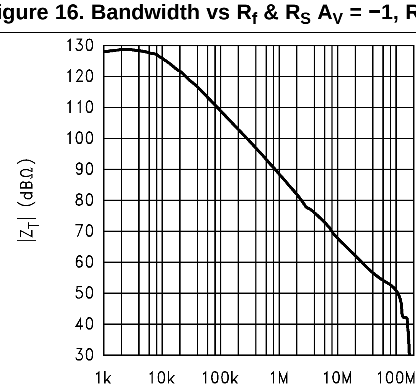


Figure 18. Transimpedance vs Frequency
V_S = ±15V R_L = 1 kΩ

Typical Performance Characteristics (continued)

T_A = 25°C unless otherwise noted

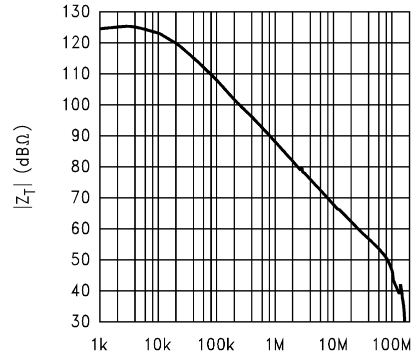


Figure 19. Transimpedance vs Frequency V_S = ±15V R_L = 100Ω

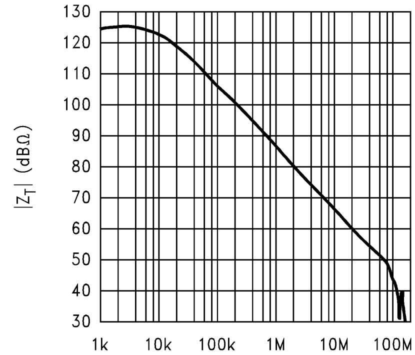


Figure 20. Transimpedance vs Frequency V_S = ±5V R_L = 1 kΩ

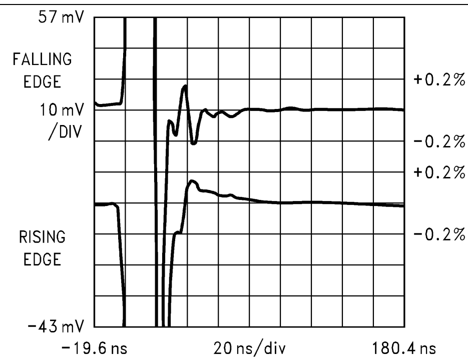


Figure 21. Settling Response V_S = ±15V; R_L = 150Ω; V_O = ±5V; A_V = −1

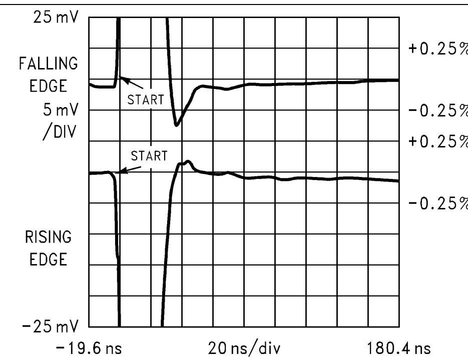


Figure 22. Settling Response V_S = ±5V; R_L = 150 Ω; V_O = ±2V; A_V = −1

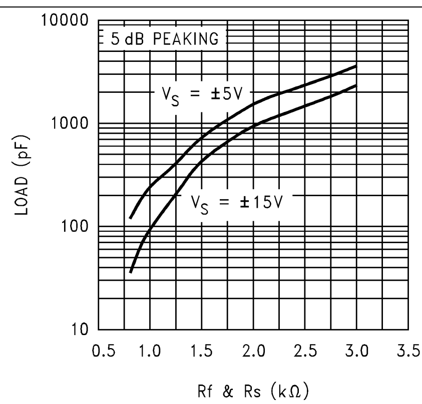


Figure 23. Suggested R_f and R_S for C_L A_V = − 1; R_L = 150Ω

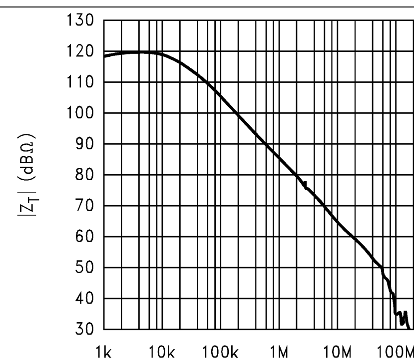


Figure 24. Transimpedance vs Frequency V_S = ±5V R_L = 100Ω

Typical Performance Characteristics (continued)

T_A = 25°C unless otherwise noted

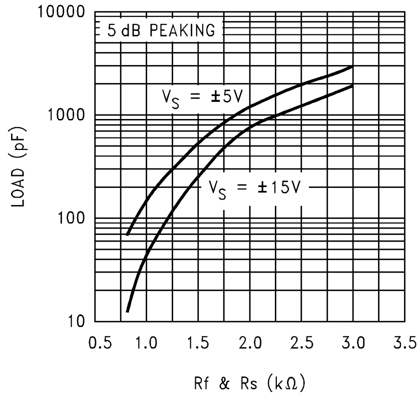


Figure 25. Suggested R_f and R_S for C_L A_V = −1

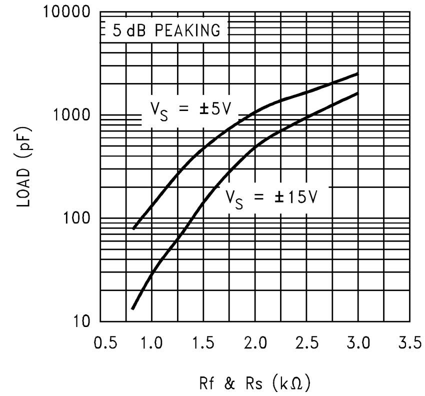


Figure 26. Suggested R_f and R_S for C_L A_V = +2; R_L = 150Ω

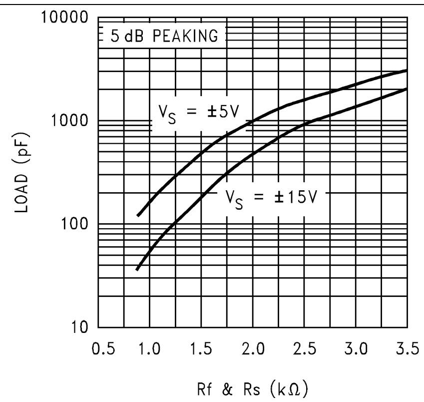


Figure 27. Suggested R_f and R_S for C_L A_V = +2

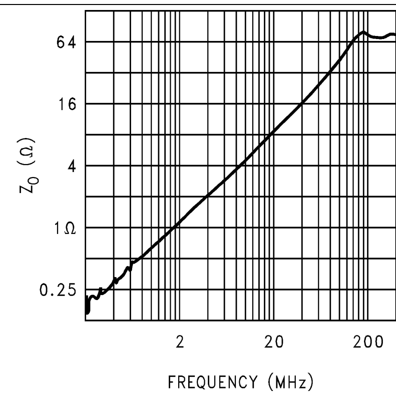


Figure 28. Output Impedance vs Freq
V_S = ±15V; A_V = −1 R_f = 820 Ω

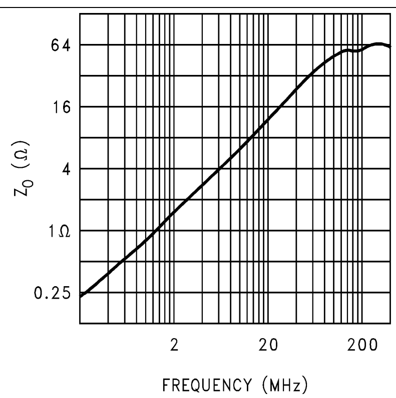


Figure 29. Output Impedance vs Freq
V_S = ±5V; A_V = −1 R_f = 820 Ω

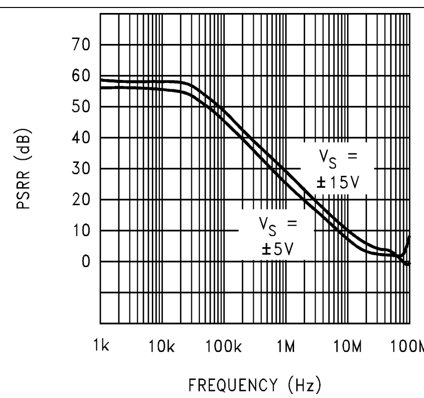


Figure 30. PSRR (V_S^+) vs Frequency

Typical Performance Characteristics (continued)

T_A = 25°C unless otherwise noted

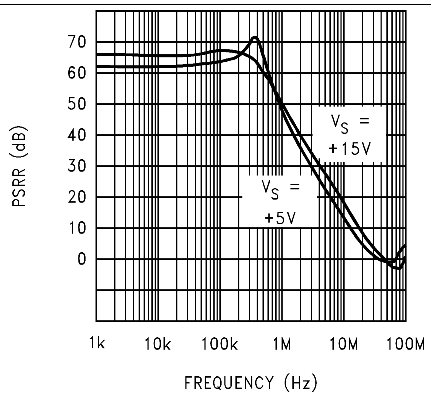


Figure 31. PSRR (V_S^-) vs Frequency

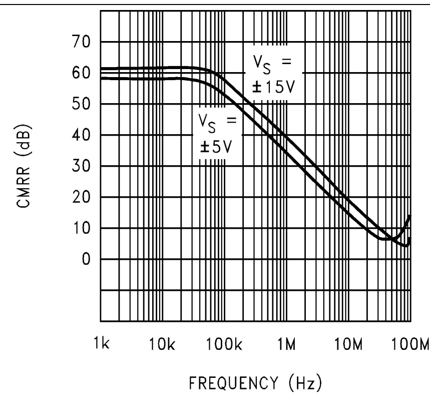


Figure 32. CMRR vs Frequency

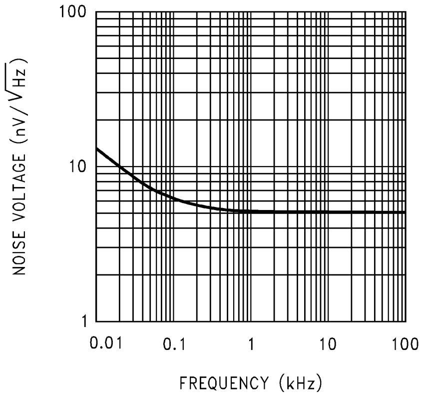


Figure 33. Input Voltage Noise vs Frequency

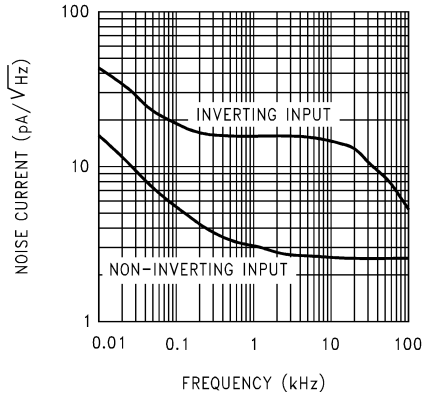


Figure 34. Input Current Noise vs Frequency

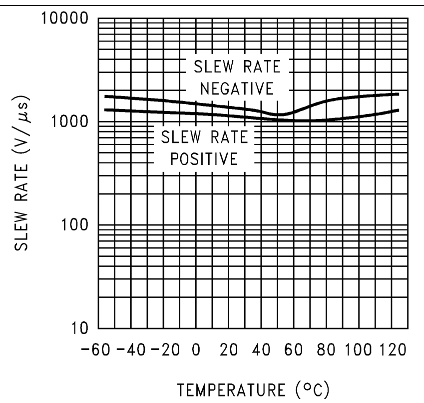


Figure 35. Slew Rate vs Temperature A_V = −1; R_L = 150 Ω, V_S = ±15V

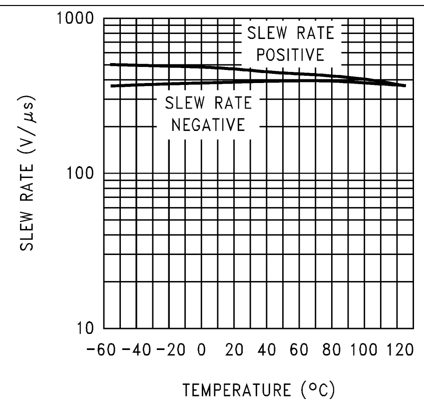


Figure 36. Slew Rate vs Temperature A_V = −1; R_L = 150 Ω, V_S = ±5V

Typical Performance Characteristics (continued)

T_A = 25°C unless otherwise noted

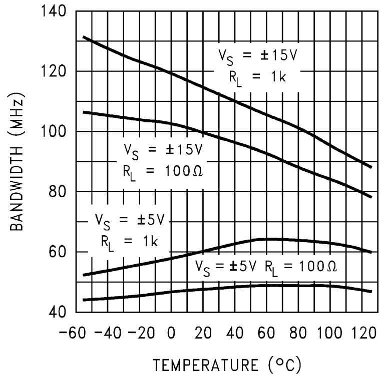


Figure 37. −3 dB Bandwidth vs Temperature A_V = −1

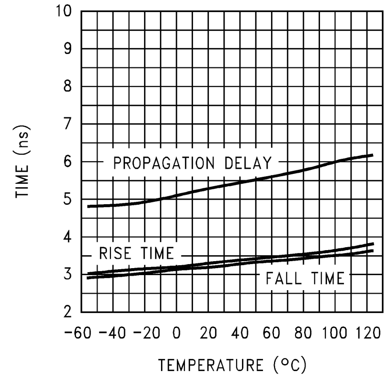


Figure 38. Small Signal Pulse response vs Temp, A_V = +1 V_S = ±15V; R_L = 1 kΩ

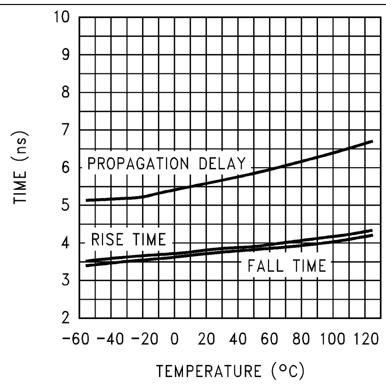


Figure 39. Small Signal Pulse Response vs Temp, A_V = +1 V_S = ±15V; R_L = 100Ω

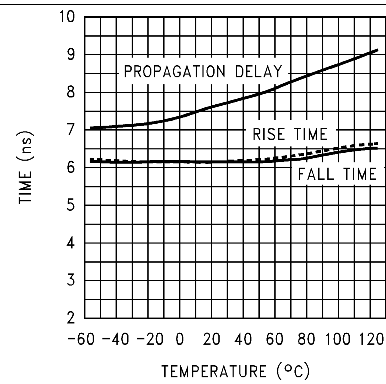


Figure 40. Small Signal Pulse Response vs Temp, A_V = +1 V_S = ±5V; R_L = 1 kΩ

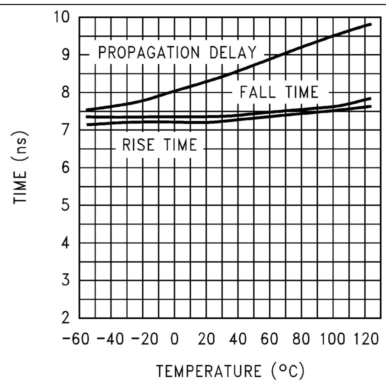


Figure 41. Small Signal Pulse Response vs Temp, A_V = +1 V_S = ±5V; R_L = 100Ω

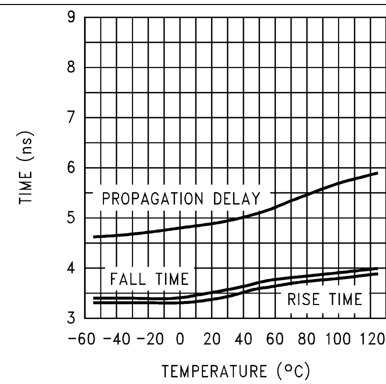


Figure 42. Small Signal Pulse Response vs Temp, A_V = −1 V_S = ±15V; R_L = 1 kΩ

Typical Performance Characteristics (continued)

T_A = 25°C unless otherwise noted

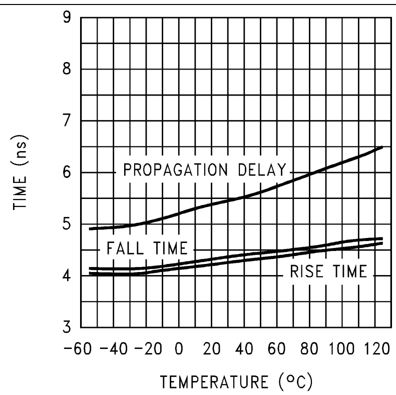


Figure 43. Small Signal Pulse Response vs Temp, A_V = −1 V_S = ±15V; R_L = 100Ω

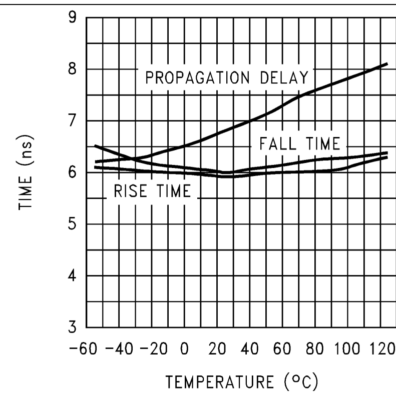


Figure 44. Small Signal Pulse Response vs Temp, A_V = −1 V_S = ±5V; R_L = 1 kΩ

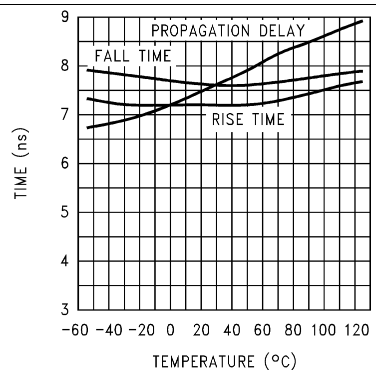


Figure 45. Small Signal Pulse Response vs Temp, A_V = −1 V_S = ±5V; R_L = 100 Ω

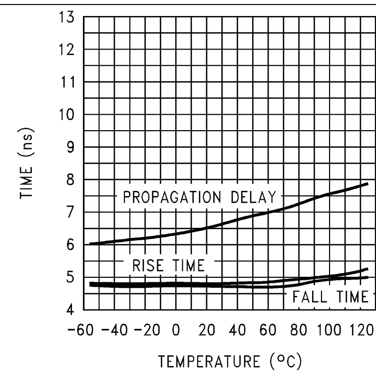


Figure 46. Small Signal Pulse Response vs Temp, A_V = +2 V_S = ±15V; R_L = 1 kΩ

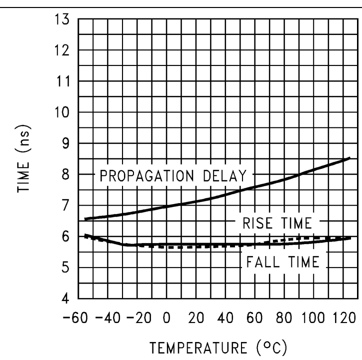


Figure 47. Small Signal Pulse Response vs Temp, A_V = +2 V_S = ±15V; R_L = 100 Ω

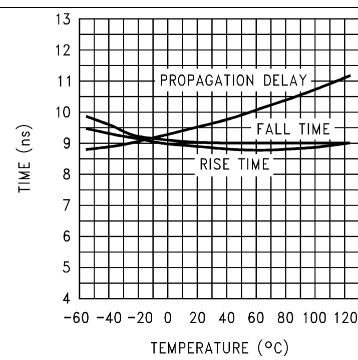


Figure 48. Small Signal Pulse Response vs Temp, A_V = +2 V_S = ±5V; R_L = 1 kΩ

Typical Performance Characteristics (continued)

T_A = 25°C unless otherwise noted

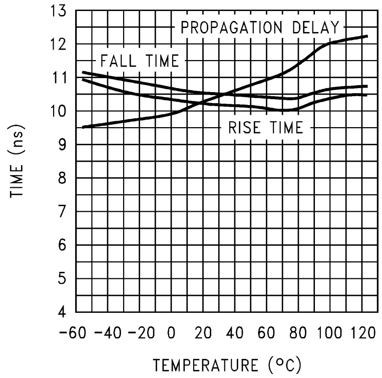


Figure 49. Small Signal Pulse Response vs Temp, A_V = +2 V_S = ±5V; R_L = 100 Ω

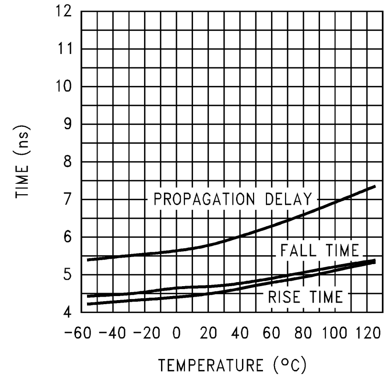


Figure 50. Small Signal Pulse Response vs Temp, A_V = −10 V_S = ±15V; R_L = 1 kΩ

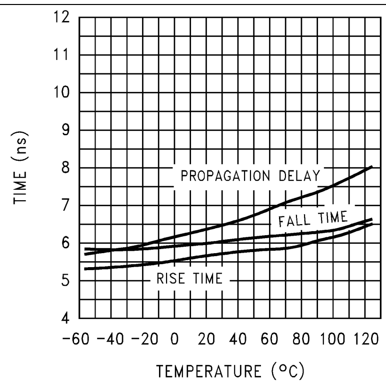


Figure 51. Small Signal Pulse Response vs Temp, A_V = −10 V_S = ±15V; R_L = 100Ω

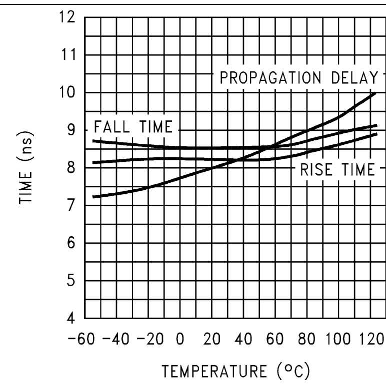


Figure 52. Small Signal Pulse Response vs Temp, A_V = −10 V_S = ±5V; R_L = 1 kΩ

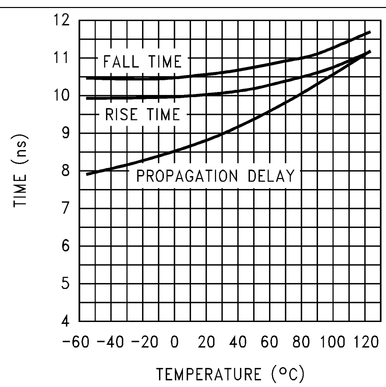


Figure 53. Small Signal Pulse Response vs Temp, A_V = −10 V_S = ±5V; R_L = 100Ω

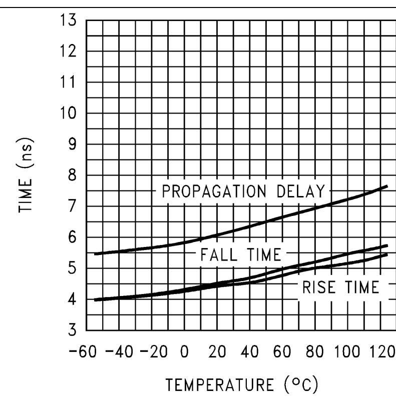


Figure 54. Small Signal Pulse Response Vs Temp, A_V = +10 V_S = ±15V; R_L = 1 kΩ

Typical Performance Characteristics (continued)

T_A = 25°C unless otherwise noted

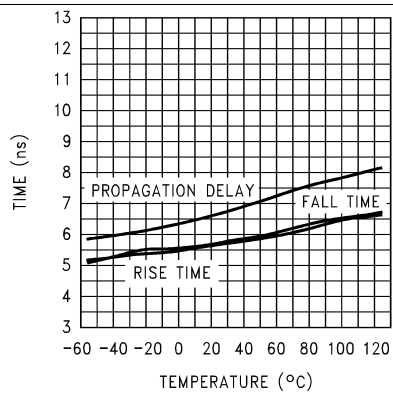


Figure 55. Small Signal Pulse Response vs Temp, A_V = +10 V_S = ±15V; R_L = 100Ω

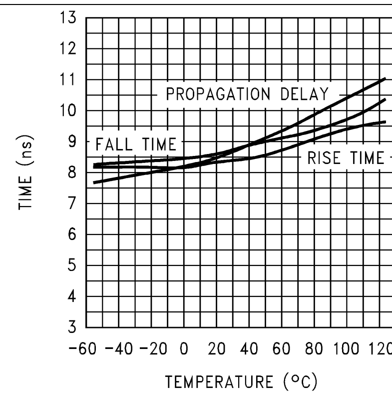


Figure 56. Small Signal Pulse Response vs Temp, A_V = +10 V_S = ±5V; R_L = 1 kΩ

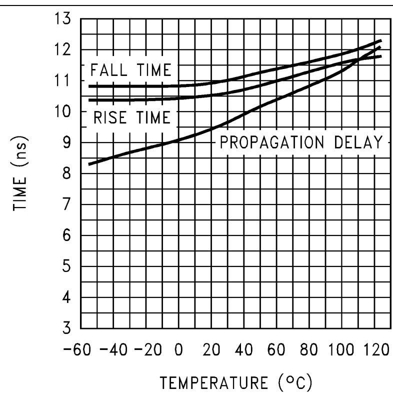


Figure 57. Small Signal Pulse Response vs Temp, A_V = +10 V_S = ±5V; R_L = 100Ω

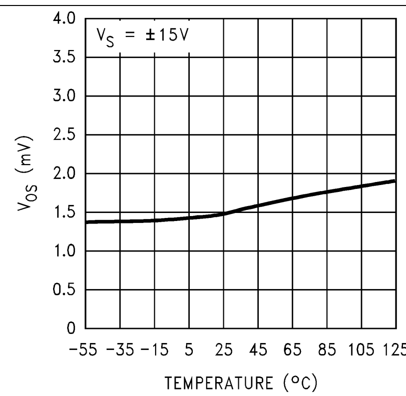


Figure 58. Offset Voltage vs temperature

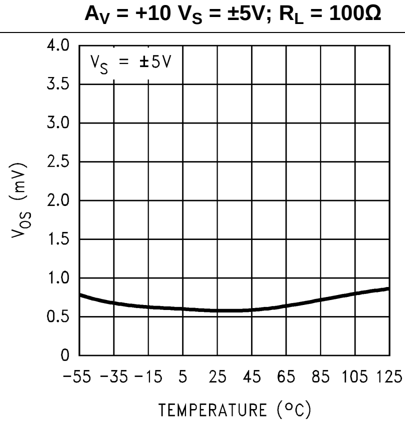


Figure 59. Offset Voltage vs Temperature

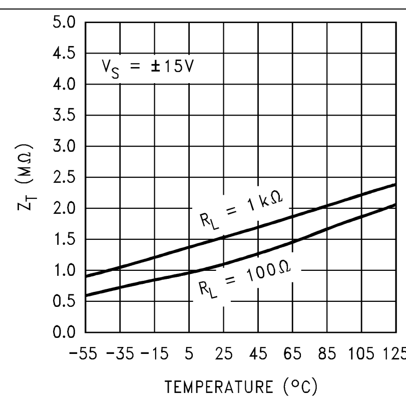


Figure 60. Transimpedance vs Temperature

Typical Performance Characteristics (continued)

T_A = 25°C unless otherwise noted

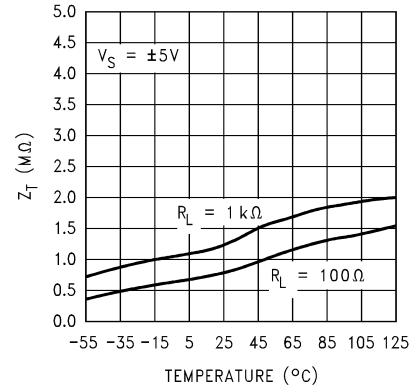


Figure 61. Transimpedance vs Temperature

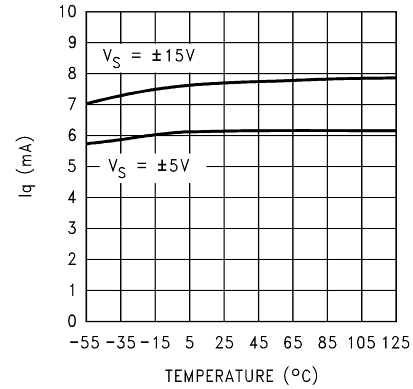


Figure 62. Quiescent Current vs Temperature

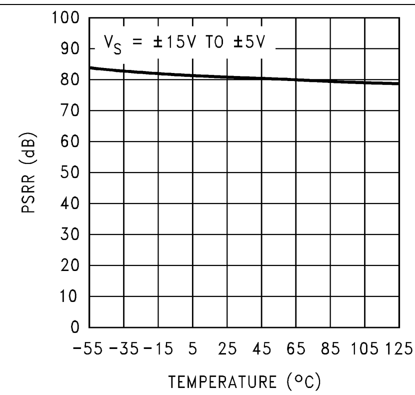


Figure 63. PSRR vs Temperature

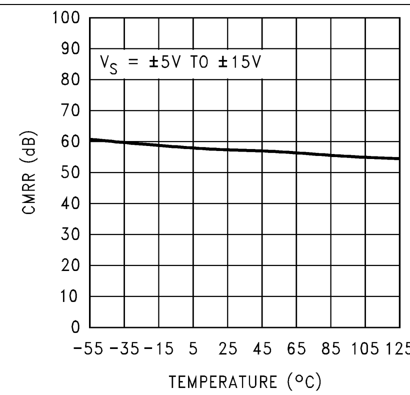


Figure 64. CMRR vs Temperature

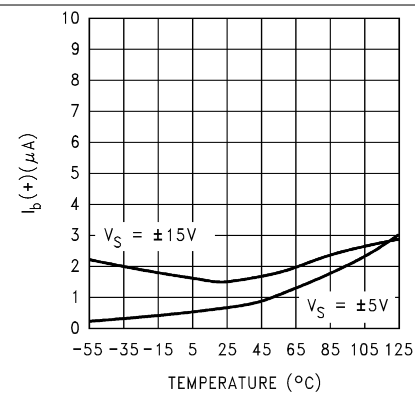


Figure 65. Non-inverting Bias Current vs Temperature

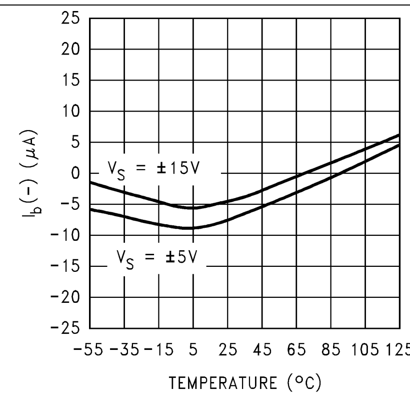


Figure 66. Inverting Bias Current vs Temperature

Typical Performance Characteristics (continued)

T_A = 25°C unless otherwise noted

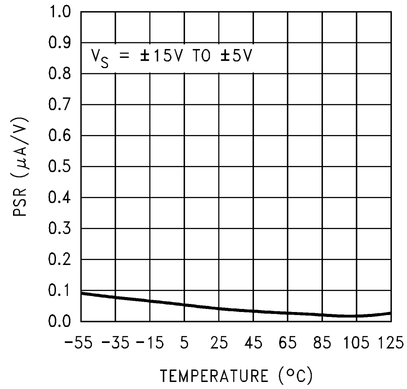


Figure 67. PSR $I_{B(+)}$ vs Temperature

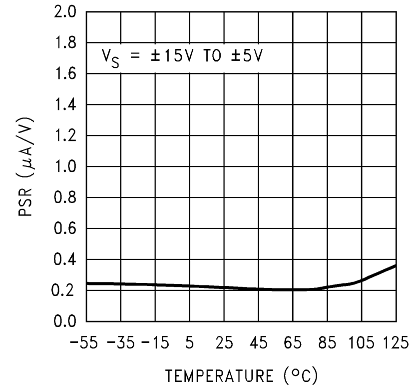


Figure 68. PSR $I_{B(-)}$ vs Temperature

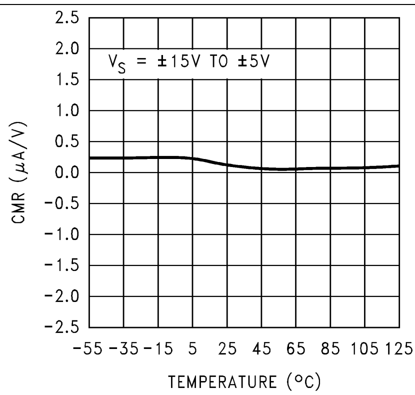


Figure 69. CMR $I_{B(+)}$ vs Temperature

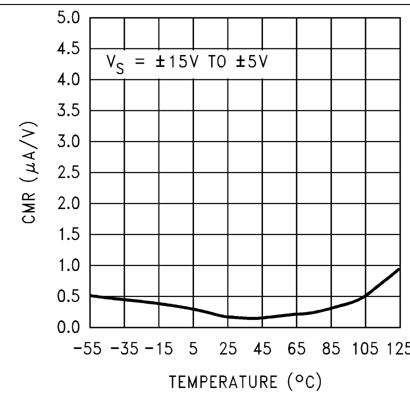


Figure 70. CMR $I_{B(-)}$ vs Temperature

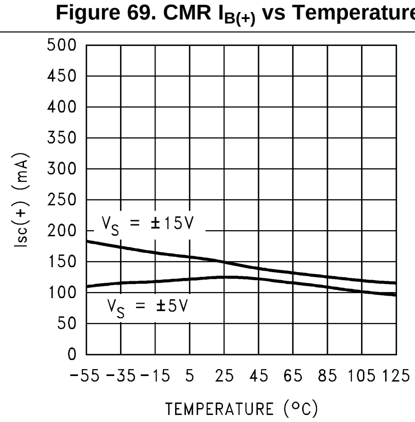


Figure 71. $I_{SC(+)}$ vs Temperature

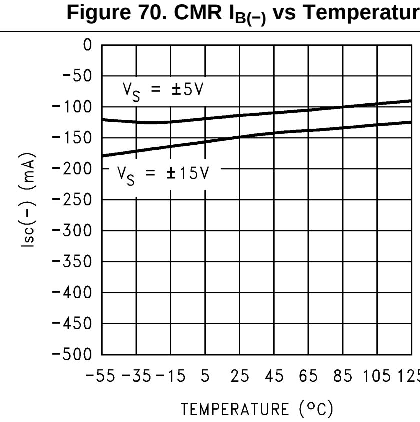


Figure 72. $I_{SC(-)}$ vs Temperature

Typical Performance Characteristics (continued)

T_A = 25°C unless otherwise noted

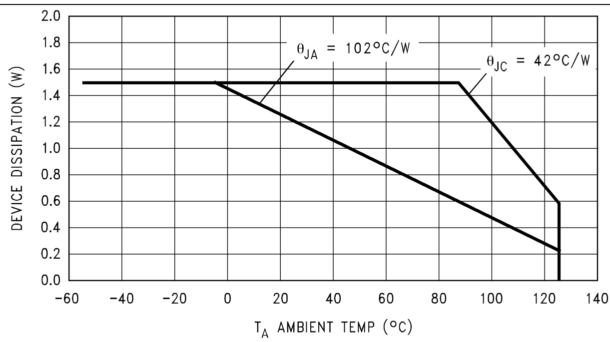
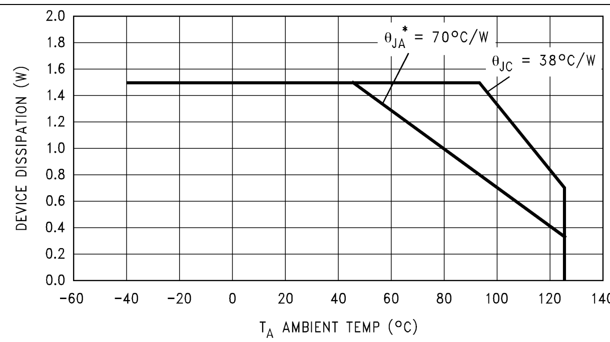


Figure 73. Absolute Maximum Power Derating: PDIP Package



*θ_{JA} = Thermal Resistance with 2 square inches of 1 ounce Copper tied to Pins 1, 8, 9 and 16.

Figure 74. Absolute Maximum Power Derating: SOIC-16 package

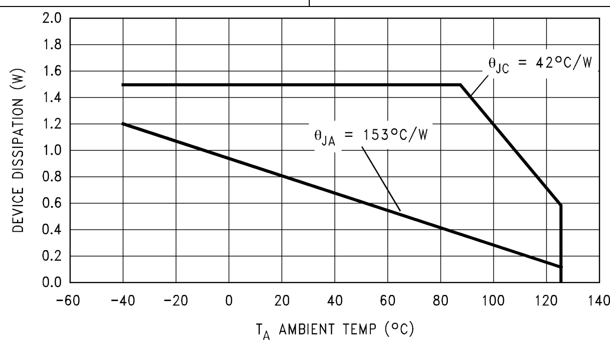


Figure 75. Absolute Maximum Power Derating: SOIC-8 package

7 Typical Applications

7.1 Current Feedback Topology

For a conventional voltage feedback amplifier the resulting small-signal bandwidth is inversely proportional to the desired gain to a first order approximation based on the gain-bandwidth concept. In contrast, the current feedback amplifier topology, such as the LM6181, transcends this limitation to offer a signal bandwidth that is relatively independent of the closed-loop gain. Figure 76 and Figure 77 illustrate that for closed loop gains of −1 and −5 the resulting pulse fidelity suggests quite similar bandwidths for both configurations.

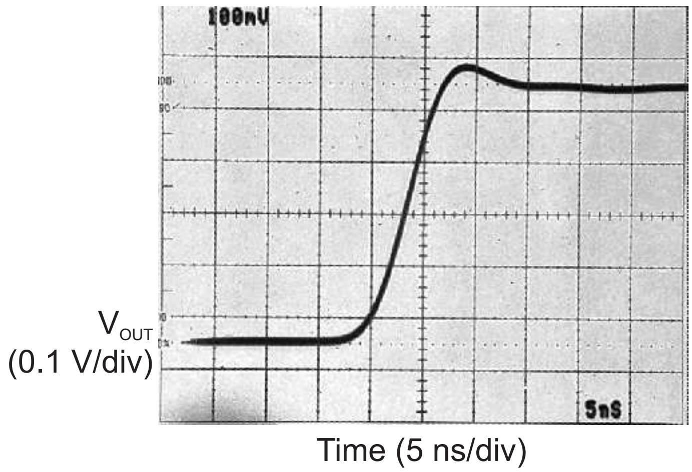
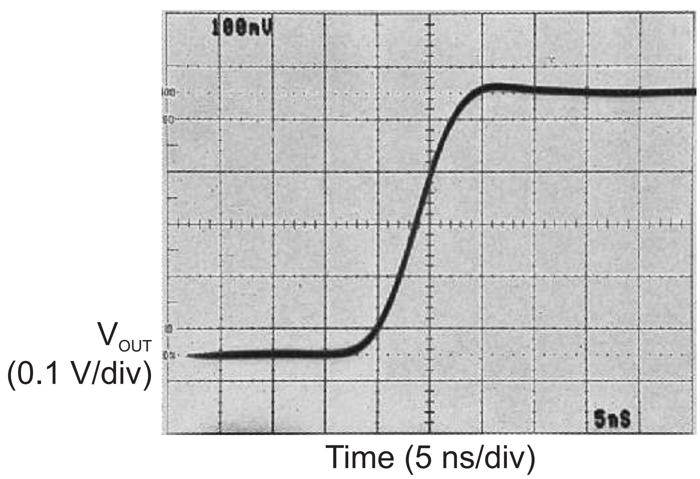


Figure 76. Step Response, Av = -1V/V



Variation of Closed Loop Gain
from −1 to −5 Yields Similar Responses

Figure 77. Step Response, Av = -5V/V

Current Feedback Topology (continued)

The closed-loop bandwidth of the LM6181 depends on the feedback resistance, R_f. Therefore, R_S and not R_f, must be varied to adjust for the desired closed-loop gain as in Figure 78.

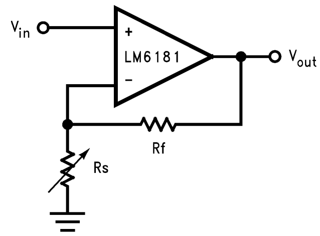


Figure 78. R_S Is Adjusted to Obtain the Desired Closed Loop Gain, A_{VCL}

7.2 Power Supply Bypassing and Layout Considerations

A fundamental requirement for high-speed amplifier design is adequate bypassing of the power supply. It is critical to maintain a wideband low-impedance to ground at the amplifiers supply pins to insure the fidelity of high speed amplifier transient signals. 10 µF tantalum and 0.1 µF ceramic bypass capacitors are recommended for each supply pin. The bypass capacitors should be placed as close to the amplifier pins as possible (0.5″ or less).

7.3 Feedback Resistor Selection: R_f

Selecting the feedback resistor, R_f, is a dominant factor in compensating the LM6181. For general applications the LM6181 will maintain specified performance with an 820Ω feedback resistor. Although this value will provide good results for most applications, it may be advantageous to adjust this value slightly. Consider, for instance, the effect on pulse responses with two different configurations where both the closed-loop gains are 2 and the feedback resistors are 820Ω and 1640Ω, respectively. Figure 79 and Figure 80 illustrate the effect of increasing R_f while maintaining the same closed-loop gain—the amplifier bandwidth decreases. Accordingly, larger feedback resistors can be used to slow down the LM6181 (see −3 dB bandwidth vs $R_f$typical curves) and reduce overshoot in the time domain response. Conversely, smaller feedback resistance values than 820Ω can be used to compensate for the reduction of bandwidth at high closed loop gains, due to 2nd order effects. For example Figure 81 illustrates reducing R_f to 500Ω to establish the desired small signal response in an amplifier configured for a closed loop gain of 25.

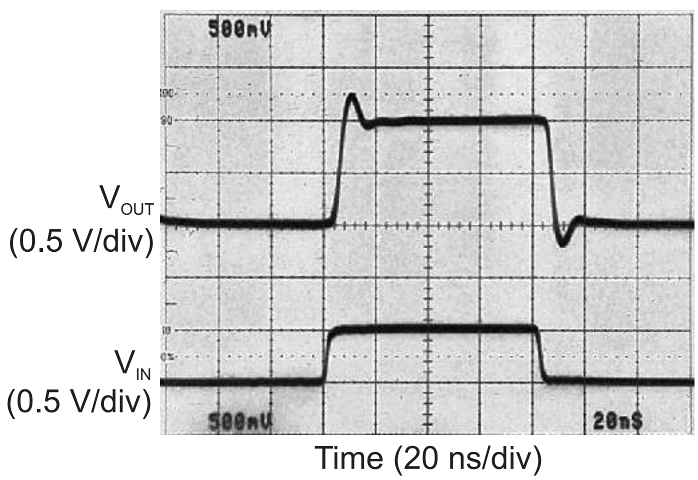
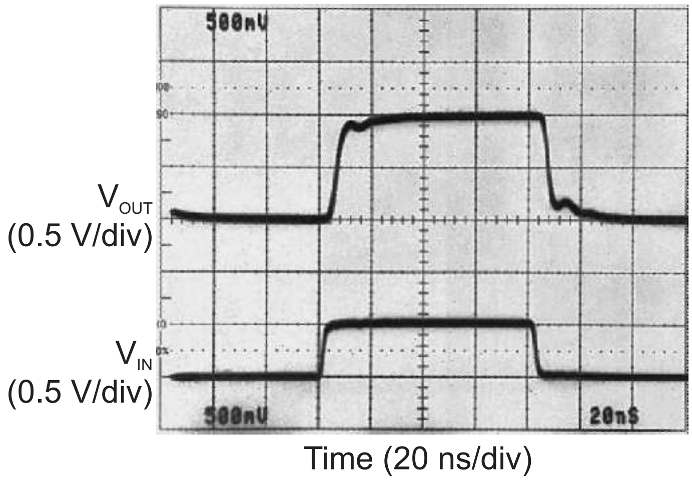


Figure 79. Step Response with Rf = 820 Ω

Feedback Resistor Selection: R_f (continued)



Increasing Compensation with Increasing R_f

Figure 80. Step Response with Rf = 1640 Ω

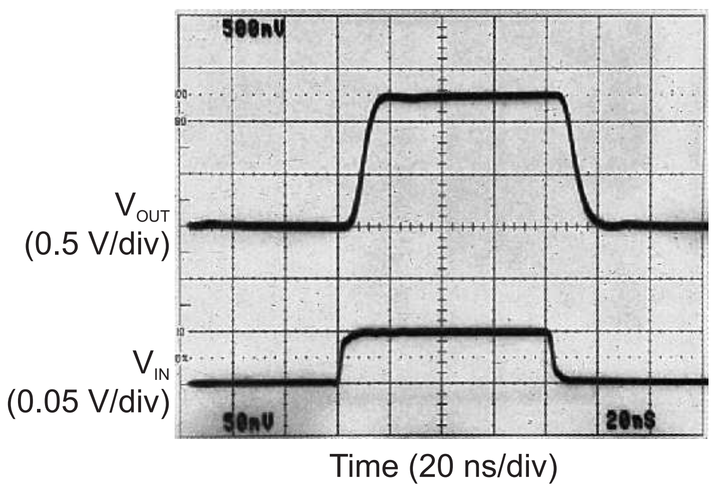


Figure 81. Reducing R_f for Large Closed Loop Gains, R_f = 500 Ω

7.4 Slew Rate Considerations

The slew rate characteristics of current feedback amplifiers are different than traditional voltage feedback amplifiers. In voltage feedback amplifiers slew rate limiting or non-linear amplifier behavior is dominated by the finite availability of the 1st stage tail current charging the compensation capacitor. The slew rate of current feedback amplifiers, in contrast, is not constant. Transient current at the inverting input determines slew rate for both inverting and non-inverting gains. The non-inverting configuration slew rate is also determined by input stage limitations. Accordingly, variations of slew rates occur for different circuit topologies.

7.5 Driving Capacitive Loads

The LM6181 can drive significantly larger capacitive loads than many current feedback amplifiers. Although the LM6181 can directly drive as much as 100 pF without oscillating, the resulting response will be a function of the feedback resistor value. Figure 83 illustrates the small-signal pulse response of the LM6181 while driving a 50 pF load. Ringing persists for approximately 70 ns. To achieve pulse responses with less ringing either the feedback resistor can be increased (see Figure 23, Figure 25, and Figure 26), or resistive isolation can be used (10 Ω–51 Ω typically works well). Either technique, however, results in lowering the system bandwidth.

Figure 85 illustrates the improvement obtained with using a 47Ω isolation resistor.

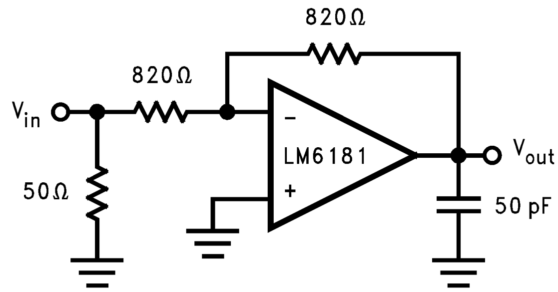


Figure 82. Cap Load Direct Drive

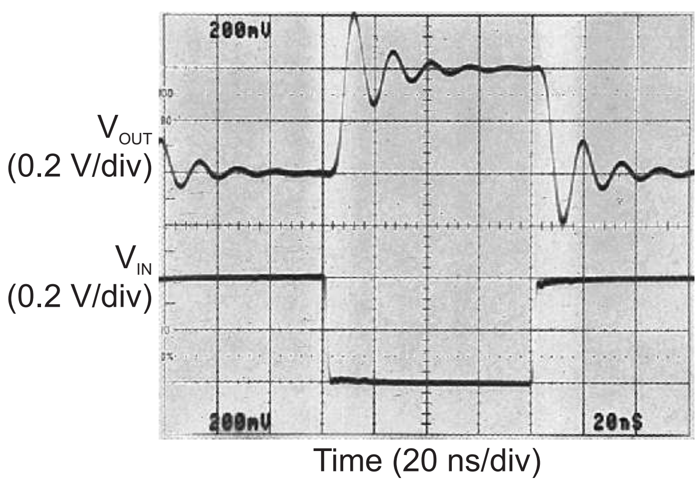


Figure 83. A_V = −1, LM6181 Can Directly Drive 50 pF of Load Capacitance with 70 ns of Ringing Resulting in Pulse Response

Driving Capacitive Loads (continued)

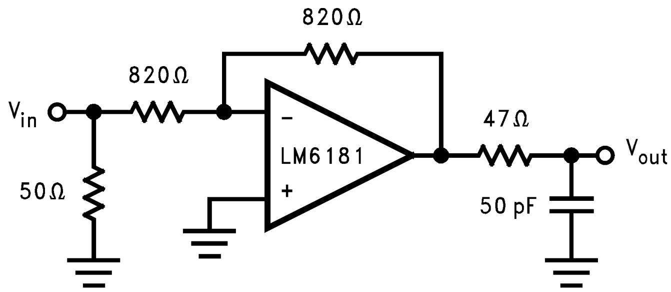
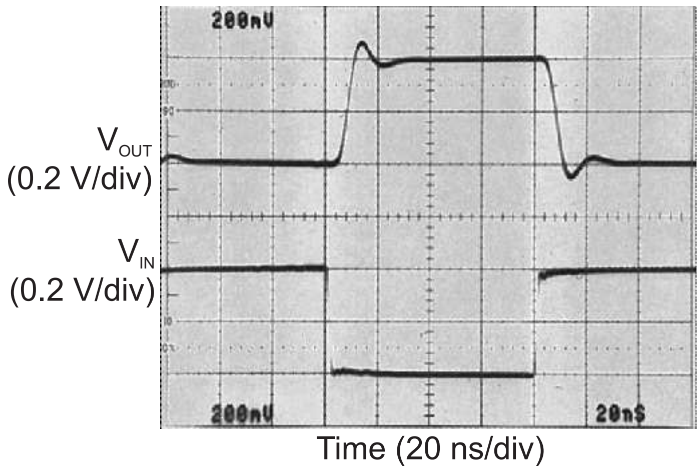


Figure 84. Cap Load Drive with Isolation Resistor



R_f and R_S Could Be Increased to Maintain $A_V = -1$
and Improve Pulse Response Characteristics.

Figure 85. Resistive Isolation of C_L Provides Higher Fidelity Pulse Response

7.6 Capacitive Feedback

For voltage feedback amplifiers it is quite common to place a small lead compensation capacitor in parallel with feedback resistance, R_f. This compensation serves to reduce the amplifier's peaking in the frequency domain which equivalently tames the transient response. To limit the bandwidth of current feedback amplifiers, do not use a capacitor across R_f. The dynamic impedance of capacitors in the feedback loop reduces the amplifier's stability. Instead, reduced peaking in the frequency response, and bandwidth limiting can be accomplished by adding an RC circuit, as illustrated in Figure 87.

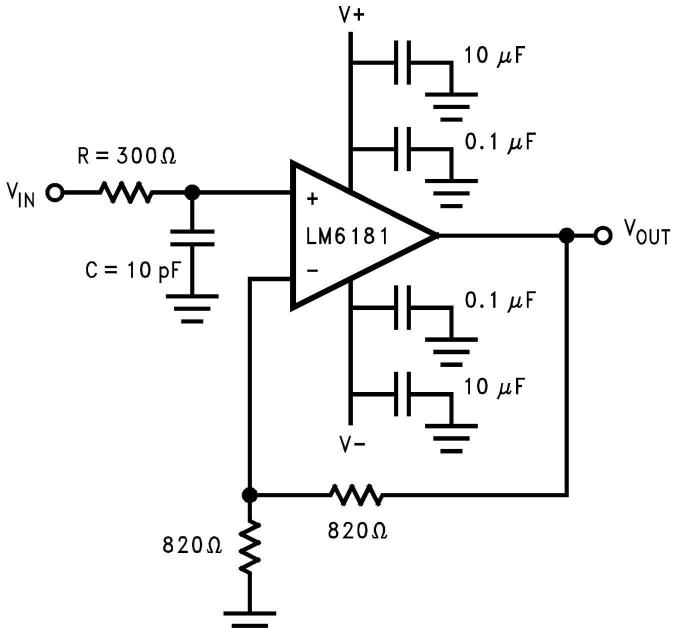


Figure 86. Using RC on Input to Affect Frequency Response

$$f - 3\text{ dB} = \frac{1}{2\pi RC} \tag{1}$$

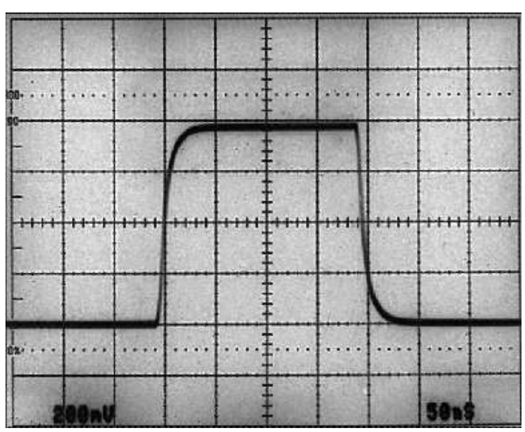


Figure 87. RC Limits Amplifier Bandwidth to 50 MHz, Eliminating Peaking in the Resulting Pulse Response

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Typical Application

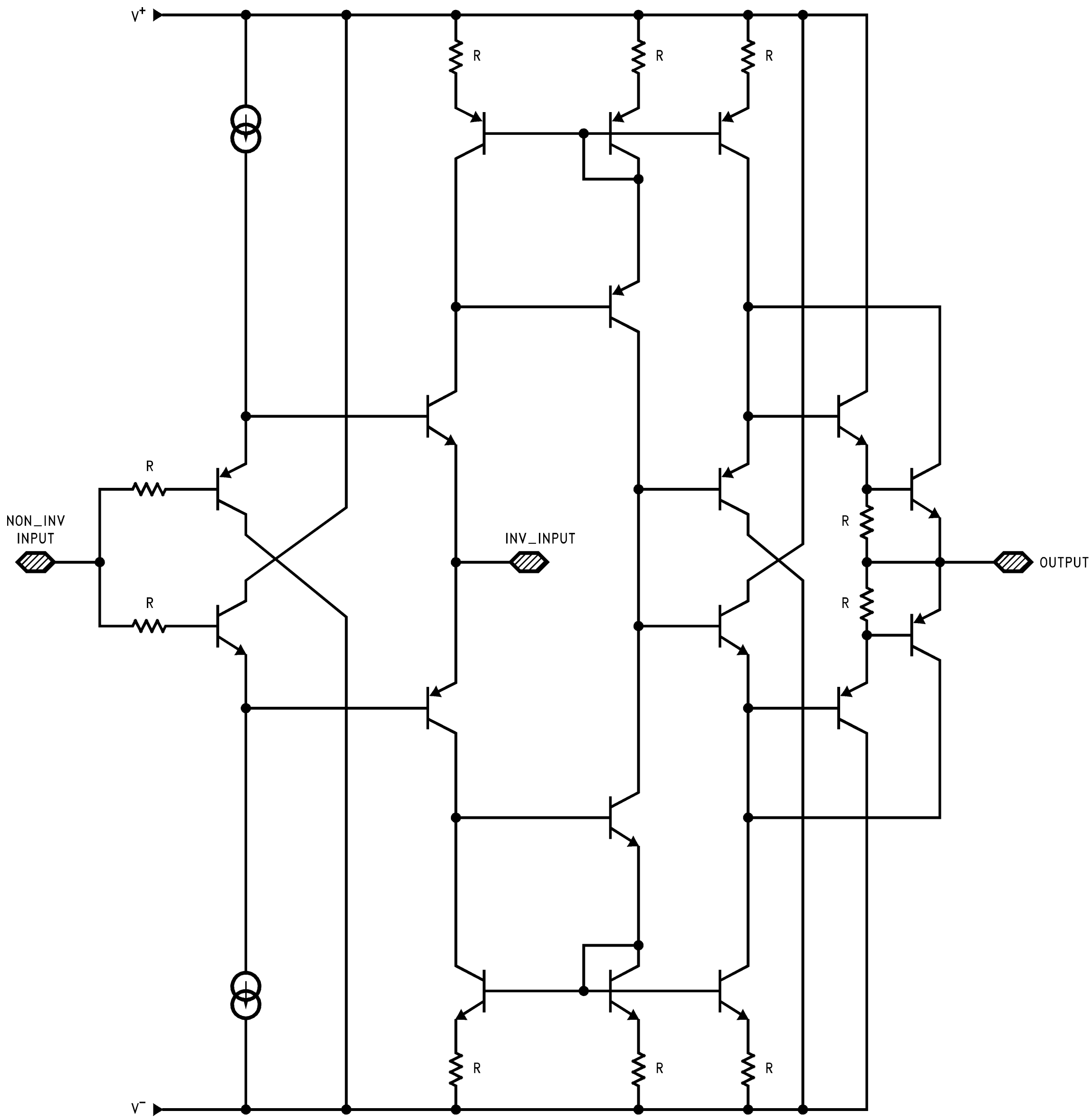


Figure 88. LM6181 Simplified Schematic

Typical Application (continued)

8.1.1 Typical Performance Characteristics

8.1.1.1 Overdrive Recovery

When the output or input voltage range of a high speed amplifier is exceeded, the amplifier must recover from an overdrive condition. The typical recovery times for open-loop, closed-loop, and input common-mode voltage range overdrive conditions are illustrated in Figure 90, Figure 92, and Figure 93, respectively.

The open-loop circuit of Figure 89 generates an overdrive response by allowing the ±0.5V input to exceed the linear input range of the amplifier. Typical positive and negative overdrive recovery times shown in Figure 90 are 5 ns and 25 ns, respectively.

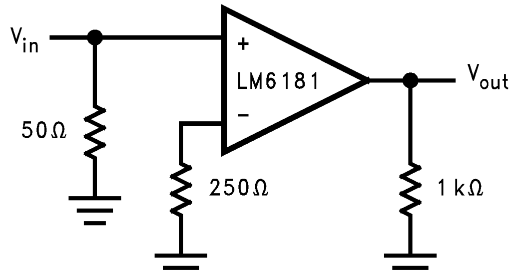


Figure 89. Open Loop Input Overdrive Test Circuit

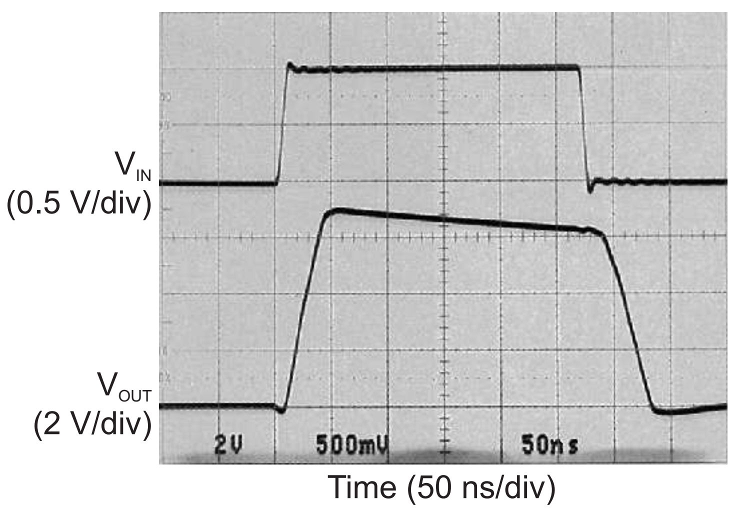


Figure 90. Open-Loop Overdrive Recovery Time of 5 ns, and 25 ns from Test Circuit in Figure 89

Typical Application (continued)

The large closed-loop gain configuration in Figure 91 forces the amplifier output into overdrive. Figure 92 displays the typical 30 ns recovery time to a linear output value.

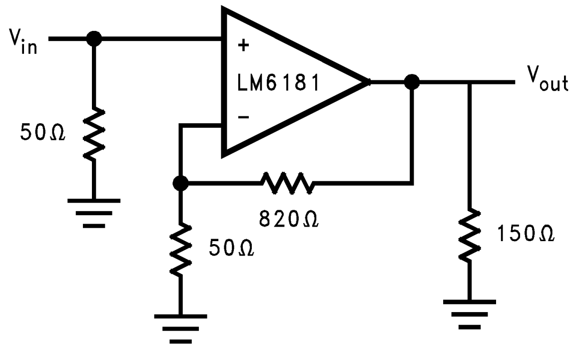


Figure 91. Overdrive Recovery Circuit under Large Closed Loop Gain Condition

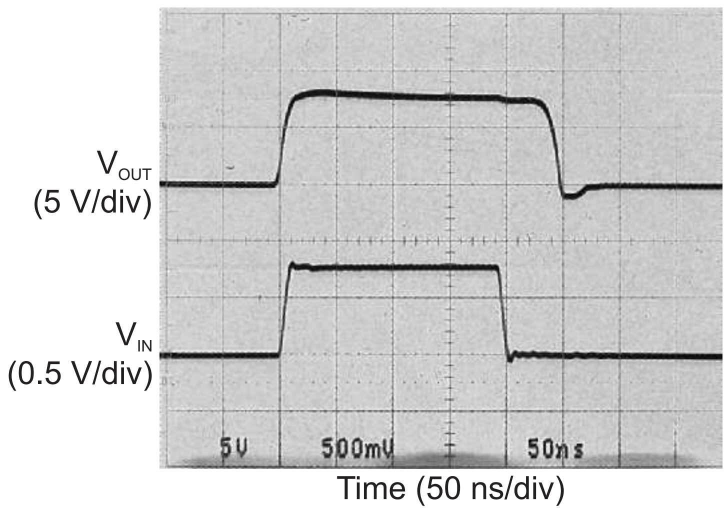


Figure 92. Closed-Loop Overdrive Recovery Time of 30 ns from Exceeding Output Voltage Range from Circuit in Figure 91

Typical Application (continued)

The common-mode input of the circuit in Figure 91 is exceeded by a 5V pulse resulting in a typical recovery time of 310 ns shown in Figure 93. The LM6181 supply voltage is ±5V.

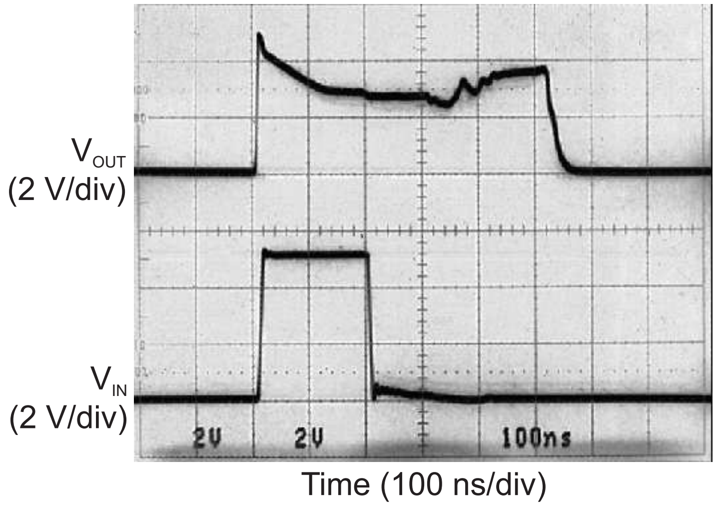


Figure 93. Exceptional Output Recovery from an Input that Exceeds the Common-Mode Range

9 Device and Documentation Support

9.1 Trademarks

VIP is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

9.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

9.3 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM6181IM-8	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	LM618 1IM8	
LM6181IM-8/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM618 1IM8	Samples
LM6181IMX-8/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM618 1IM8	Samples
LM6181IN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 85	LM6181IN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

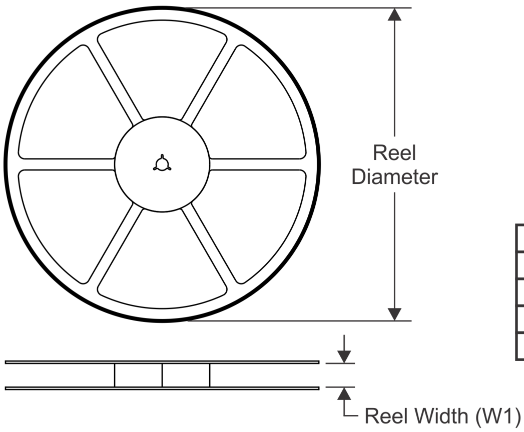
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

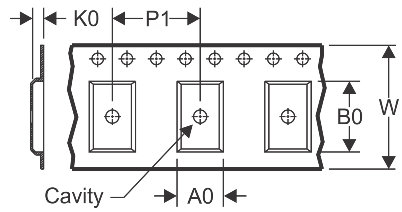
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

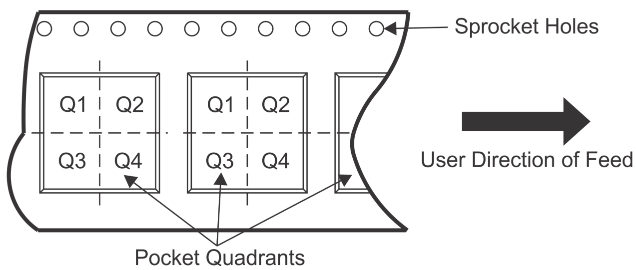


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

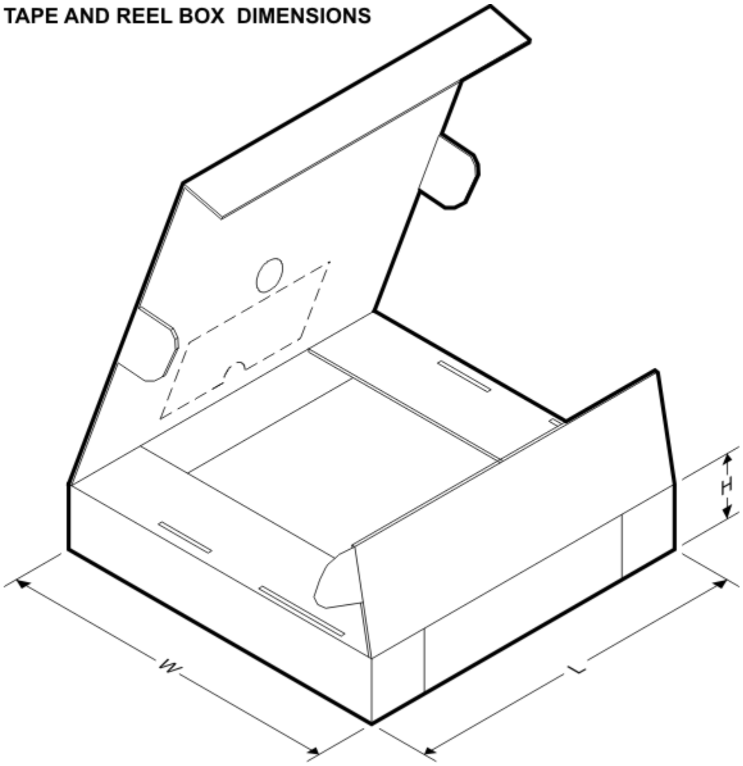
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM6181IMX-8/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

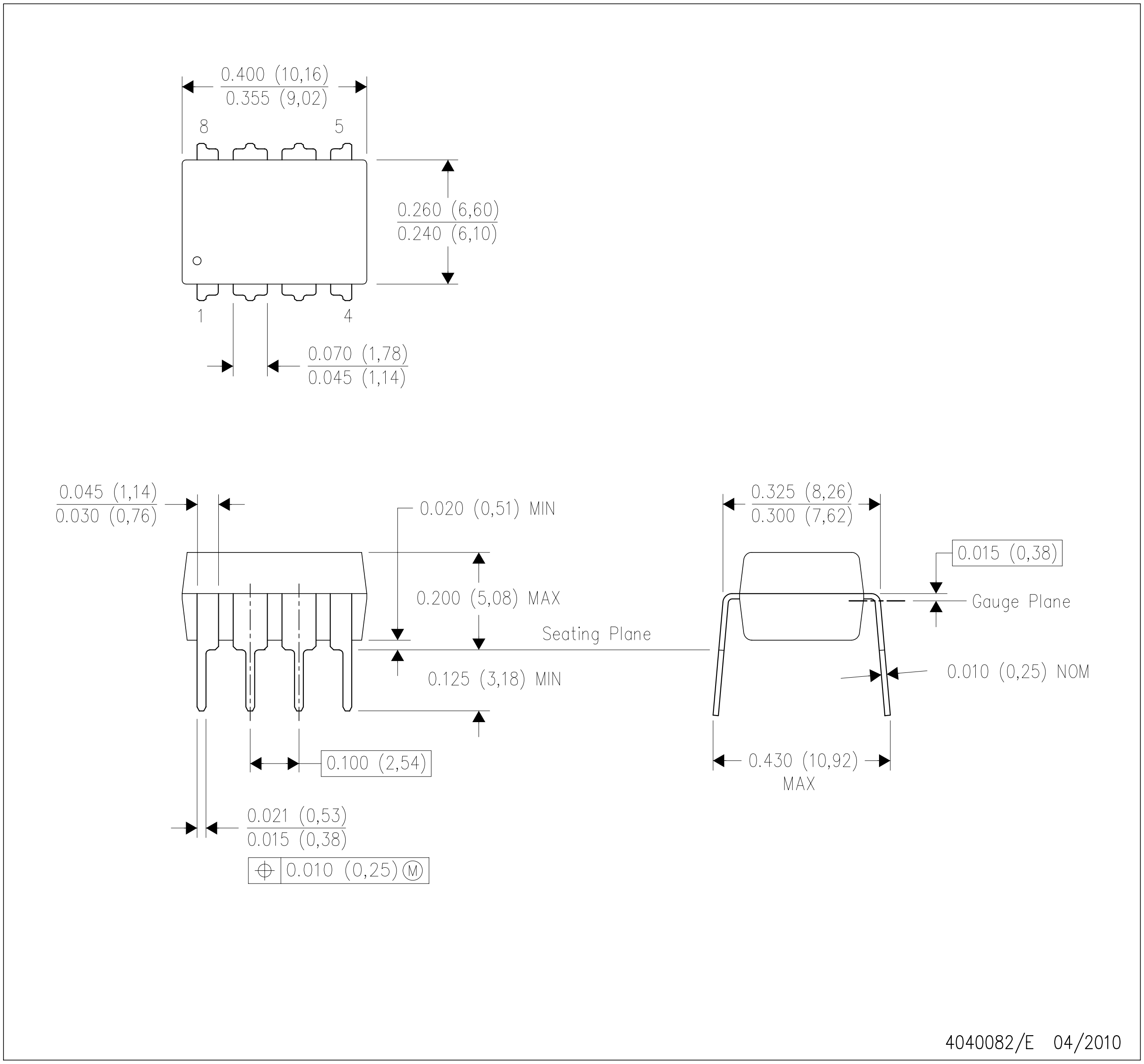
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

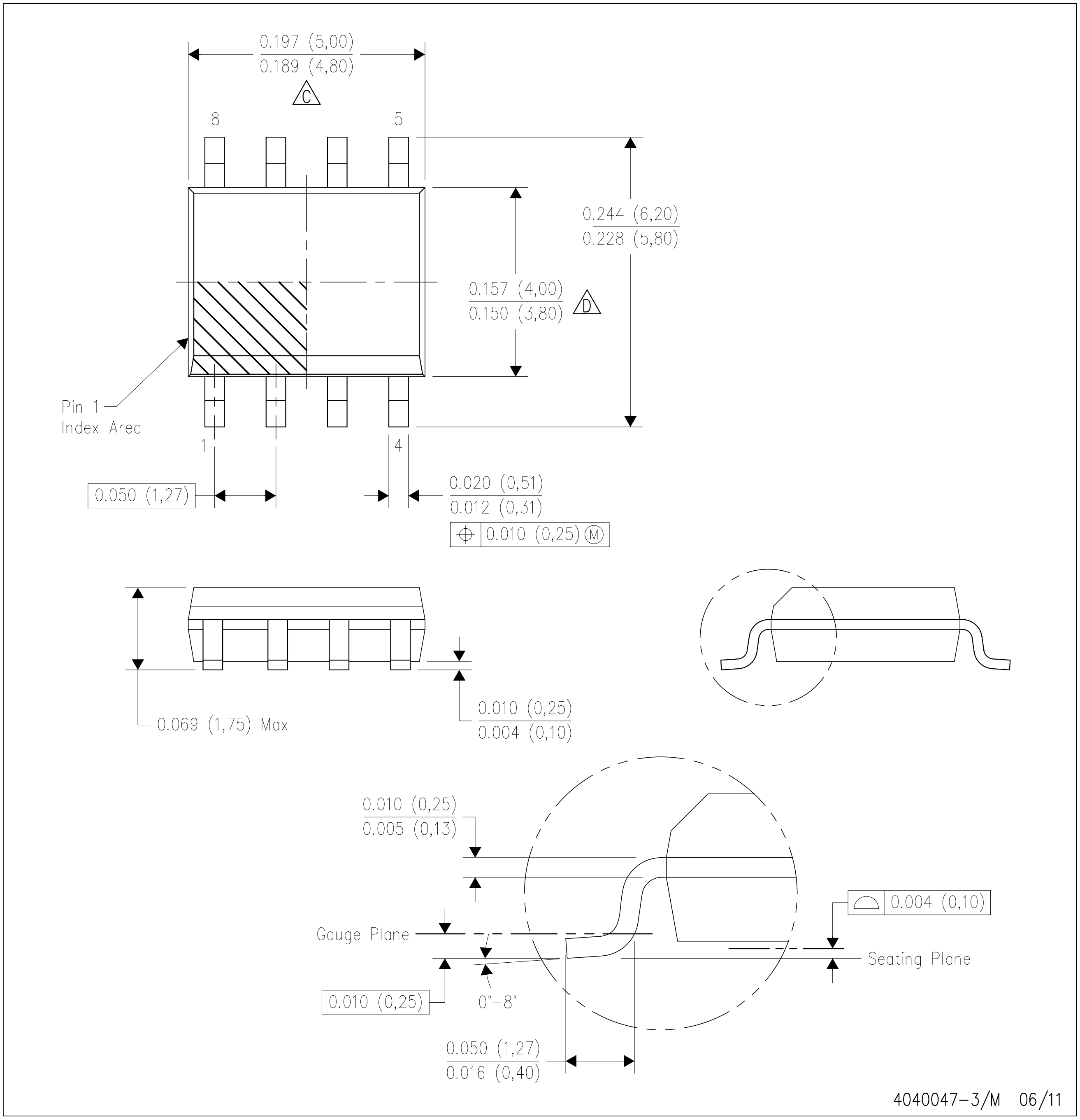
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM6181IMX-8/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

AMEYA360

Components Supply Platform

Authorized Distribution Brand :

Website :

Welcome to visit www.ameya360.com

Contact Us :

Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
Minhang District, Shanghai , China

Sales :

Direct +86 (21) 6401-6692

Email amall@ameya360.com

QQ 800077892

Skype ameyasales1 ameyasales2

Customer Service :

Email service@ameya360.com

Partnership :

Tel +86 (21) 64016692-8333

Email mkt@ameya360.com