24-Channel, 12-Bit PWM LED Driver with 7-Bit Dot Correction and 3-Group, 8-Bit Global Brightness Control

Check for Samples: TLC5951

FEATURES

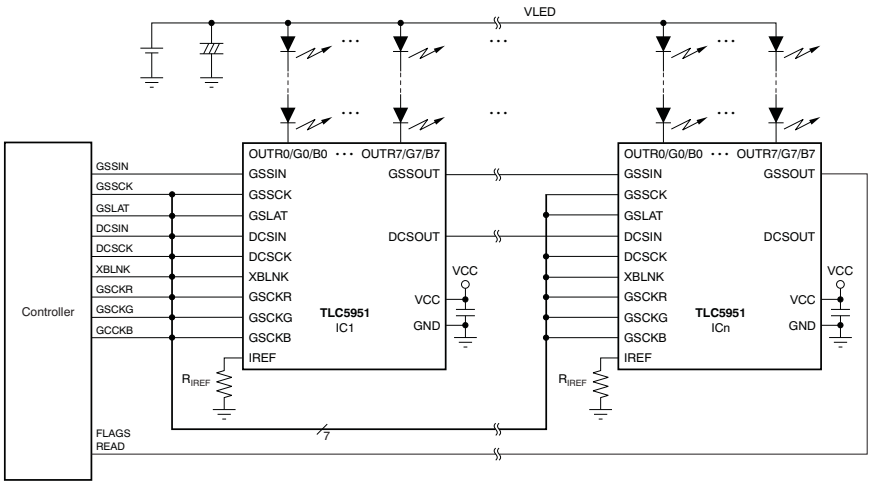
- 24-Channel Constant-Current Sink Output
- Current Capability: 40 mA
- Selectable Grayscale (GS) Control with PWM: 12-Bit (4096 Step), 10-Bit (1024 Step), 8-Bit (256 Step)
- Three Independent Grayscale Clocks for Three Color Groups
- Dot Correction (DC): 7-Bit (128 Step)
- Global Brightness Control (BC) for Each Color Group: 8-Bit (256 Step)
- Auto Display Repeat Function
- Independent Data Port for GS and BC/DC Data
- Communication Path Between Each Data Port
- LED Power-Supply Voltage up to 15 V
- V_{CC} = 3.0 V to 5.5 V
- Constant-Current Accuracy:
  - Channel-to-Channel = ±1.5%
  - Device-to-Device = ±3%
- CMOS Logic Level I/O
- Data Transfer Rate: 30 MHz
- 33-MHz Grayscale Control Clock
- Continuous Base LED Open Detection (LOD)
- Continuous Base LED Short Detection (LSD)
- Thermal Shutdown (TSD) with Auto Restart
- Grouped Delay to Prevent Inrush Current
- Operating Air Temperature: –40°C to +85°C
- Packages: HTSSOP-38, QFN-40

APPLICATIONS

- Full-Color LED Displays
- LED Signboards

DESCRIPTION

The TLC5951 is a 24-channel, constant-current sink driver. Each channel has an individually-adjustable, 4096-step, pulse width modulation (PWM) grayscale (GS) brightness control and 128 step constant-current dot correction (DC). The dot correction adjusts brightness deviation between channels and other LED drivers. The output channels are grouped into three groups of eight channels. Each channel group has a 256-step global brightness control (BC) function and an individual grayscale clock input.



Typical Application Circuit (Multiple Daisy-Chained TLC5951s)

DESCRIPTION (CONTINUED)

GS, DC, and BC data are accessible via a serial interface port. DC and BC can be programmed via a dedicated serial interface port.

The TLC5951 has three error detection circuits for LED open detection (LOD), LED short detection (LSD), and thermal error flag (TEF). LOD detects a broken or disconnected LED while LSD detects a shorted LED. TEF indicates an over-temperature condition.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Table 1. ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLC5951	HTSSOP-38 PowerPAD™	TLC5951DAPR	Tape and Reel, 2000
		TLC5951DAP	Tube, 40
TLC5951	6 mm × 6 mm QFN-40	TLC5951RHAR	Tape and Reel, 2500
		TLC5951RHAT	Tape and Reel, 250

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1) (2)

Over operating free-air temperature range, unless otherwise noted.

PARAMETER			TLC5951	UNIT
V_{CC}	Supply voltage	VCC	–0.3 to +6.0	V
I_{OUT}	Output current (dc)	OUTR0 to R7, OUTG0 to G7, OUTB0 to B7	50	mA
V_{IN}	Input voltage range	GSSIN, GSSCK, GSLAT, GSCKR, GSCKG, GSCKB, DCSIN, DCSCK, XBLNK, IREF	–0.3 to V_{CC} + 0.3	V
V_{OUT}	Output voltage range	GSSOUT, DCSOUT	–0.3 to V_{CC} + 0.3	V
		OUTR0 to 7, OUTG0 to 7, OUTB0 to 7	–0.3 to +16	V
$T_{J(max)}$	Operation junction temperature		+150	°C
T_{STG}	Storage temperature		–55 to +150	°C
	ESD rating	Human body model (HBM)	2000	V
		Charged device model (CDM)	500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS

PACKAGE	DERATING FACTOR ABOVE T_A = +25°C	T_A < +25°C POWER RATING	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
HTSSOP-38 with PowerPAD soldered(1)	38.8 mW/°C	4845 mW	3101 mW	2519 mW
HTSSOP-38 with PowerPAD not soldered(2)	19.9 mW/°C	2490 mW	1594 mW	1295 mW
QFN-40(3)	26.7 mW/°C	3342 mW	2139 mW	1738 mW

(1) With PowerPAD soldered onto copper area on printed circuit board (PCB); 2-oz. copper. For more information, see SLMA002 (available for download at www.ti.com).
(2) With PowerPAD not soldered onto copper area on PCB.
(3) The package thermal impedance is calculated in accordance with JESD51-5.

RECOMMENDED OPERATING CONDITIONS

At T_A = –40°C to +85°C, unless otherwise noted.

PARAMETER			TLC5951 MIN	TLC5951 NOM	TLC5951 MAX	UNIT
DC CHARACTERISTICS: V_{CC} = 3 V to 5.5 V						
V_{CC}	Supply voltage		3.0		5.5	V
V_O	Voltage applied to output	OUTR0-OUTR7, OUTG0-OUTG7, OUTB0-OUTB7			15	V
V_{IH}	High level input voltage		0.7 × V_{CC}		V_{CC}	V
V_{IL}	Low level input voltage		GND		0.3 × V_{CC}	V
I_{OH}	High level output current	GSSOUT, DCSOUT			–1	mA
I_{OL}	Low level output current	GSSOUT, DCSOUT			1	mA
I_{OLC}	Constant output sink current	OUTR0-OUTR7, OUTG0-OUTG7, OUTB0-OUTB7			40	mA
T_A	Operating free-air temperature		–40		+85	°C
T_J	Operating junction temperature		–40		+125	°C
AC CHARACTERISTICS, V_{CC} = 3V to 5.5V						
$f_{CLK\ (SCK)}$	Data shift clock frequency	GSSCK, DCSCK			30	MHz
$f_{CLK\ (GSCKR/G/B)}$	Grayscale clock frequency	GSCKR, GSCKG, GSCKB			33	MHz
T_{WH0}/T_{WL0}	Pulse duration	GSSCK, DCSCK, GSCKR, GSCKG, GSCKB	10			ns
T_{WH1}/T_{WL1}		GSLAT	30			ns
T_{WL2}		XBLNK	30			ns
T_{SU0}	Setup time	GSSIN – GSSCK↑, DCSIN – DCSCK↑	5			ns
T_{SU1}		XBLNK↑ – GSCKR↑, GSCKG↑, or GSCKB↑	10			ns
T_{SU2}		GSLAT↑ – GSSCK↑	150			ns
T_{SU3}		GSLAT↑ for GS data – GSCKR↑, GSCKG↑, or GSCKB↑ when display timing reset mode is disabled	40			ns
T_{SU4}		GSLAT↑ for GS data – GSCKR↑, GSCKG↑, or GSCKB↑ when display timing reset mode is enabled	100			ns
T_{H0}	Hold time	GSSIN – GSSCK↑, DCSIN – DCSCK↑	5			ns
T_{H1}		GSLAT↑ – GSSCK↑	35			ns
T_{H2}		GSLAT↓ – GSSCK↑	5			ns

ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +85°C, V_{CC} = 3 V to 5.5 V, and V_{LED} = 5 V, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = 3.3 V.

PARAMETER		TEST CONDITIONS	TLC5951			UNIT
			MIN	TYP	MAX	
V_{OH}	High level output voltage	At GSSOUT, DCSOUT, I_{OH} = –1 mA	V_{CC} – 0.4		V_{CC}	V
V_{OL}	Low level output voltage	At GSSOUT, DCSOUT, I_{OL} = 1 mA			0.4	V
I_I	Input current	At GSSCK, GSLAT, DCSIN, DCSCK, GSCKR/G/B with $V_I = V_{CC}$, At GSSIN, GSSCK, GSLAT, DCSIN, XBLNK, DCSCK, GSCKR/G/B with V_I = GND	–1		1	µA
I_{CC1}	Supply current	GSSIN, GSSCK, GSLAT, DCSIN, DCSCK = low, XBLNK = low, GSCKR/G/B = low, $V_{OUTRn/Gn/Bn}$ = 1 V, BCR/G/B = FFh, DCRn/Gn/Bn = 7Fh with DC high adjustment range, R_{IREF} = 24 kΩ ($I_{OUTRn/Gn/Bn}$ = 2 mA target)		1	3	mA
I_{CC2}		GSSIN, GSSCK, GSLAT, DCSIN, DCSCK = low, XBLNK = low, GSCKR/G/B = low, $V_{OUTRn/Gn/Bn}$ = 1 V, BCR/G/B = FFh, DCRn/Gn/Bn = 7Fh with DC high adjustment range, R_{IREF} = 2.4 kΩ ($I_{OUTRn/Gn/Bn}$ = 20 mA target)		6	10	mA
I_{CC3}		GSSIN, GSSCK, GSLAT, DCSIN, DCSCK = low, XBLNK = high, GSCKR/G/B = 33 MHz, $V_{OUTRn/Gn/Bn}$ = 1 V, GSRn/Gn/Bn = FFFh, BCR/G/B = FFh, DCRn/Gn/Bn = 7Fh with DC high adjustment range, R_{IREF} = 2.4 kΩ ($I_{OUTRn/Gn/Bn}$ = 20 mA target), auto repeat on		12	27	mA
I_{CC4}		GSSIN, GSSCK, GSLAT, DCSIN, DCSCK = low, XBLNK = high, GSCKR/G/B = 33 MHz, $V_{OUTRn/Gn/Bn}$ = 1 V, GSRn/Gn/Bn = FFFh, BCR/G/B = FFh, DCRn/Gn/Bn = 7Fh with DC high adjustment range, R_{IREF} = 1.2 kΩ ($I_{OUTRn/Gn/Bn}$ = 40 mA target), auto repeat on		21	55	mA
I_{OLC}	Constant output current	At OUTR0-OUTR7, OUTG0-OUTG7, OUTB0-OUTB7, All OUTRn/Gn/Bn = on, BCR/G/B = FFh, DCRn/Gn/Bn = 7Fh with DC high adjustment range, $V_{OUTRn/Gn/Bn}$ = 1 V, V_{OUTfix} = 1 V, R_{IREF} = 1.2 kΩ ($I_{OUTRn/Gn/Bn}$ = 40 mA target)	35	40	45	mA
I_{OLKG}	Leakage output current	At OUTR0-OUTR7, OUTG0-OUTG7 and OUTB0-OUTB7, XBLNK = low, $V_{OUTRn/Gn/Bn} = V_{OUTfix}$ = 15 V, R_{IREF} = 1.2 kΩ			0.1	µA
ΔI_{OLC}	Constant-current error(1) (channel-to-channel in same color group)	At OUTR0-OUTR7, OUTG0-OUTG7 and OUTB0-OUTB7, All OUTRn/Gn/Bn = on, BCR/G/B = FFh, DCRn/Gn/Bn = 7Fh with DC high adjustment range, $V_{OUTRn/Gn/Bn}$ = 1 V, V_{OUTfix} = 1 V, R_{IREF} = 1.2 kΩ ($I_{OUTRn/Gn/Bn}$ = 40 mA target)		±1.5	±4	%
ΔI_{OLC1}	Constant-current error(2) (color group to color group in same device)	At OUTR0-OUTR7, OUTG0-OUTG7 and OUTB0-OUTB7, All OUTRn/Gn/Bn = on, BCR/G/B = FFh, DCRn/Gn/Bn = 7Fh with DC high adjustment range, $V_{OUTRn/Gn/Bn}$ = 1 V, V_{OUTfix} = 1 V, R_{IREF} = 1.2 kΩ ($I_{OUTRn/Gn/Bn}$ = 40 mA target)		±1	±3	%

(1) The deviation of each output in the same color group from the average of the same color group (OUTR0-OUTR7, OUTG0-OUTG7, or OUTB0-OUTB7) constant current. The deviation is calculated by the formula (X = R, G, or B; n = 0-7):

$$\Delta\ (\%) = \left(\frac{I_{OUTXn}\ (N = 0\text{-}7)}{\frac{(I_{OUTX0} + I_{OUTX1} + \ldots + I_{OUTX6} + I_{OUTX7})}{8}} - 1 \right) \times 100$$

(2) The deviation of each color group in the same device from the average of all constant current. The deviation is calculated by the formula (X = R, G, or B):

$$\Delta\ (\%) = \left(\frac{\frac{(I_{OUTX0} + I_{OUTX1} + \ldots + I_{OUTX6} + I_{OUTX7})}{8}}{\frac{(I_{OUTR0}+\ldots+I_{OUTR7} + I_{OUTG0}+\ldots+I_{OUTG7} + I_{OUTB0}+\ldots+I_{OUTB7})}{24}} - 1 \right) \times 100$$

ELECTRICAL CHARACTERISTICS (continued)

At T_A = –40°C to +85°C, V_{CC} = 3 V to 5.5 V, and V_{LED} = 5 V, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = 3.3 V.

PARAMETER		TEST CONDITIONS	TLC5951			UNIT
			MIN	TYP	MAX	
ΔI_{OLC2}	Constant-current error(3) (device to device)	At OUTR0-OUTR7, OUTG0-OUTG7 and OUTB0-OUTB7, All OUTRn/Gn/Bn = on, BCR/G/B = FFh, DCRn/Gn/Bn = 7Fh with DC high adjustment range, $V_{OUTRn/Gn/Bn}$ = 1 V, V_{OUTfix} = 1 V, R_{IREF} = 1.2 kΩ ($I_{OUTRn/Gn/Bn}$ = 40 mA target)		±1	±6	%
ΔI_{OLC3}	Line regulation(4)	At OUTR0-OUTR7, OUTG0-OUTG7 and OUTB0-OUTB7, All OUTRn/Gn/Bn = on, BCR/G/B = FFh, DCRn/Gn/Bn = 7Fh with DC high adjustment range, $V_{OUTRn/Gn/Bn}$ = 1 V, V_{OUTfix} = 1 V, R_{IREF} = 1.2 kΩ ($I_{OUTRn/Gn/Bn}$ = 40 mA target)		±0.5	±2	%/V
ΔI_{OLC4}	Load regulation(5)	At OUTR0-OUTR7, OUTG0-OUTG7 and OUTB0-OUTB7, All OUTRn/Gn/Bn = on, BCR/G/B = FFh, DCRn/Gn/Bn = 7Fh with DC high adjustment range, $V_{OUTRn/Gn/Bn}$ = 1 V, V_{OUTfix} = 1 V, R_{IREF} = 1.2 kΩ ($I_{OUTRn/Gn/Bn}$ = 40 mA target)		±1	±3	%/V
ΔI_{OLC5}	Constant-current error(6)(7) (channel-to-channel in same device)	At OUTR0-R7, OUTG0-G7, and OUTB0-B7, All OUTRn/Gn/Bn = On, BCR/G/B = FFh, DCRn/Gn/Bn = 7Fh with DC high adjustment range, V_{OUTRn}/Gn/Bn = 0.5 V, T_A = +25°C, R_{IREF} = 9.6 kΩ (I_{OUTRn}/Gn/Bn = 5 mA target)			10	%
ΔI_{OLC6}	Constant-current error(7)(8)(9) (device-to-device)	At OUTR0-R7, OUTG0-G7, and OUTB0-B7, All OUTRn/Gn/Bn = On, BCR/G/B = FFh, DCRn/Gn/Bn = 7Fh with DC high adjustment range, V_{OUTRn}/Gn/Bn = 0.5V, T_A = +25°C, R_{IREF} = 9.6 kΩ (I_{OUTRn}/Gn/Bn = 5 mA target)			12	%

(3) The deviation of the all constant-current average from the ideal constant-current value. The deviation is calculated by the formula:

$$\Delta\ (\%) = \left(\frac{\frac{(I_{OUTR0}+\ldots+I_{OUTR7} + I_{OUTG0}+\ldots+I_{OUTG7} + I_{OUTB0}+\ldots+I_{OUTB7})}{24} - (\text{Ideal Output Current})}{\text{Ideal Output Current}} \right) \times 100$$

Ideal current is calculated by the following equation:

$$I_{OUT(IDEAL,\ mA)} = 40 \times \left(\frac{1.20}{R_{IREF}\ (\Omega)} \right)$$

(4) Line regulation is calculated by the following equation (X = R, G, or B; n = 0-7):

$$\Delta\ (\%/V) = \left(\frac{(I_{OUTXn} \text{ at } V_{CC} = 5.5\ V) - (I_{OUTXn} \text{ at } V_{CC} = 3.0\ V)}{(I_{OUTXn} \text{ at } V_{CC} = 3.0\ V)} \right) \times \frac{100}{5.5\ V - 3\ V}$$

(5) Load regulation is calculated by the following equation (X = R, G, or B; n = 0-7):

$$\Delta\ (\%/V) = \left(\frac{(I_{OUTXn} \text{ at } V_{OUTXn} = 3\ V) - (I_{OUTXn} \text{ at } V_{OUTXn} = 1\ V)}{(I_{OUTXn} \text{ at } V_{OUTXn} = 1\ V)} \right) \times \frac{100}{3\ V - 1\ V}$$

(6) The deviation of the maximum of all 24 channels from the minimum of all 24 channels of the same device. The deviation is calculated by the formula:

$$\Delta\ (\%) = \frac{\text{Max}\ (I_{OUT24}) - \text{Min}\ (I_{OUT24})}{\frac{(I_{OUT}R0 + \ldots + I_{OUT}R7 + I_{OUT}G0 + \ldots + I_{OUT}G7 + I_{OUT}B0 + \ldots + I_{OUT}B7)}{24}}$$

(7) Applicable only to QFN-40 package.

(8) The deviation of the maximum of all 24 channels of 30 devices from the minimum of all 24 channels of 30 devices. The deviation is calculated by the formula:

$$\Delta\ (\%) = \frac{\text{Max}\ [I_{OUT}D1\ (24\ Ch),\ I_{OUT}D2\ (24\ Ch) \ldots I_{OUT}D30\ (24\ Ch)] - \text{Min}\ [I_{OUT}D1\ (24\ Ch),\ I_{OUT}D2\ (24\ Ch) \ldots I_{OUT}D30\ (24\ Ch)]}{\text{Average}\ [I_{OUT}D1\ (24\ Ch),\ I_{OUT}D2\ (24\ Ch) \ldots I_{OUT}D30\ (24\ Ch)]}$$

(9) Not production tested, verified by characterization.

ELECTRICAL CHARACTERISTICS (continued)

At T_A = –40°C to +85°C, V_{CC} = 3 V to 5.5 V, and V_{LED} = 5 V, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = 3.3 V.

PARAMETER		TEST CONDITIONS	TLC5951			UNIT
			MIN	TYP	MAX	
T_{TEF}	Thermal error flag threshold(10)	Junction temperature	150	163	175	°C
T_{HYS}	Thermal error flag hysteresis(10)	Junction temperature	5	10	20	°C
V_{LOD}	LED open detection threshold	All OUTRn/Gn/Bn = on	0.20	0.25	0.30	V
V_{LSD}	LED short detection threshold	All OUTRn/Gn/Bn = on	2.4	2.5	2.6	V
V_{IREF}	Reference voltage output	R_{IREF} = 1.2 kΩ	1.17	1.20	1.23	V
R_{PDWN}	Pull-down resistor	At XBLNK, GSSIN	250	500	750	kΩ

(10) Not tested; specified by design.

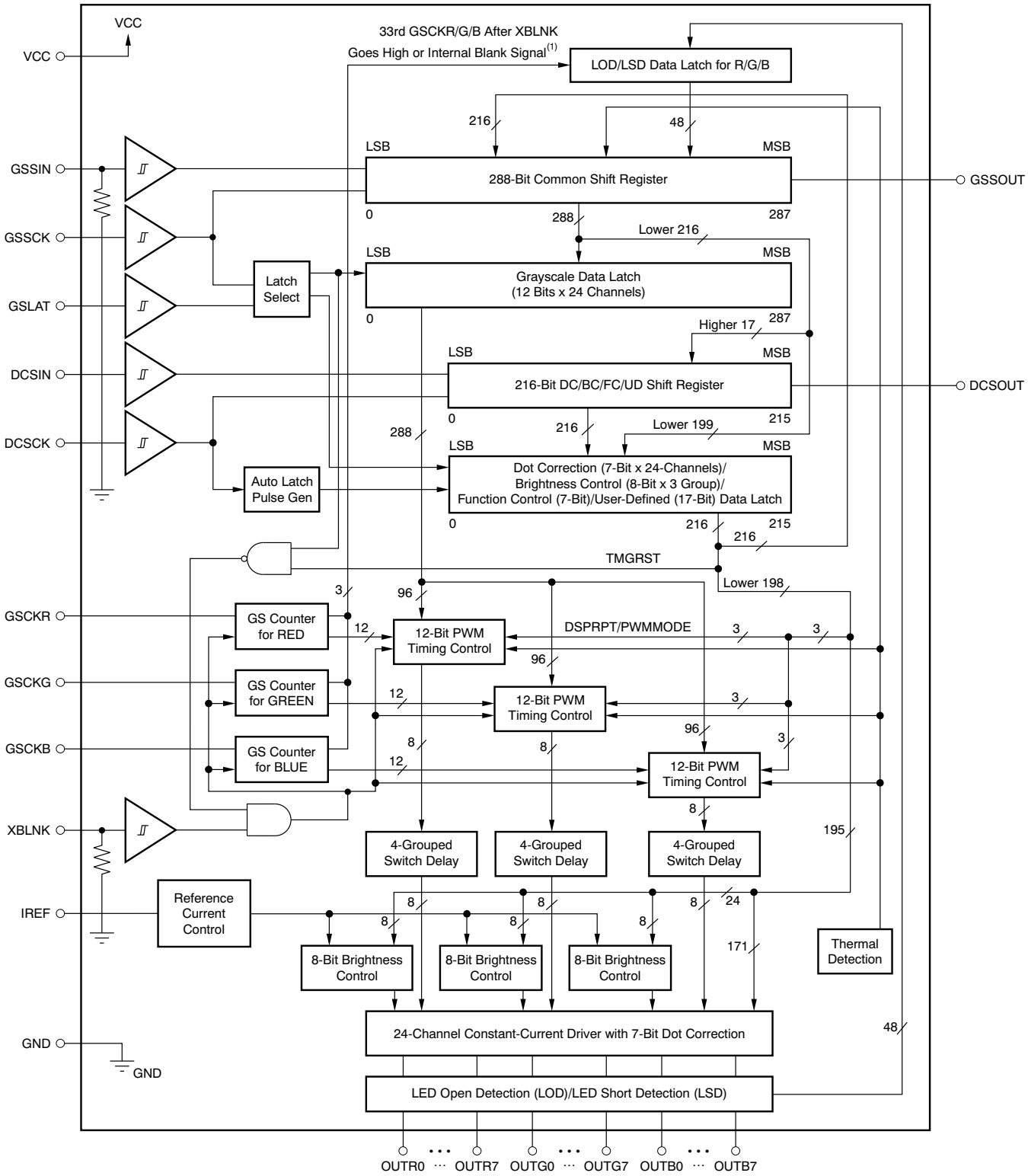
SWITCHING CHARACTERISTICS

At T_A = –40°C to +85°C, V_{CC} = 3 V to 5.5 V, C_L = 15 pF, R_L = 100 Ω, R_{IREF} = 1.2 kΩ, and V_{LED} = 5.0 V, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{R0}	Rise time	GSSOUT, DCSOUT		6	15	ns
t_{R1}		OUTR0-OUTR7, OUTG0-OUTG7, OUTB0-OUTB7, with BCR/G/B = FFh and DCRn/Gn/Bn = 7Fh with DC high adjustment range		10	30	ns
t_{F0}	Fall time	GSSOUT, DCSOUT		6	15	ns
t_{F1}		OUTR0-OUTR7, OUTG0-OUTG7, OUTB0-OUTB7, with BCR/G/B = FFh and DCRn/Gn/Bn = 7Fh with DC high adjustment range		10	30	ns
t_{D0}	Propagation delay	GSSCK↑ to GSSOUT, DCSCK↑ to DCSOUT		15	25	ns
t_{D1}		GSLAT↑ to GSSOUT		50	100	ns
t_{D2}		XBLNK↓ to OUTR0/G0/B0, OUTR4/G4/B4 off		20	40	ns
t_{D3}		GSCKR/G/B↑ to OUTR0/G0/B0, OUTR4/G4/B4 on, with BCR/G/B = FFh and DCRn/Gn/Bn = 7Fh with DC high adjustment range	5	18	40	ns
t_{D4}		GSCKR/G/B↑ to OUTR1/G1/B1, OUTR5/G5/B5 on, with BCR/G/B = FFh and DCRn/Gn/Bn = 7Fh with DC high adjustment range	20	42	73	ns
t_{D5}		GSCKR/G/B↑ to OUTR2/G2/B2, OUTR6/G6/B6 on, with BCR/G/B = FFh and DCRn/Gn/Bn = 7Fh with DC high adjustment range	35	66	106	ns
t_{D6}		GSCKR/G/B↑ to OUTR3/G3/B3, OUTR7/G7/B7 on, with BCR/G/B = FFh and DCRn/Gn/Bn = 7Fh with DC high adjustment range	50	90	140	ns
t_{D7}		Internal latch pulse generation delay from DCSCK	3	5	7	ms
t_{D8}		GSLAT↑ to $I_{OUTRn/Gn/Bn}$ changing by dot correction control (control data are 0Ch → 72h or 72h → 0Ch with DC high adjustment range), BCR/G/B = FFh		30	50	ns
t_{D9}		GSLAT↑ to $I_{OUTRn/Gn/Bn}$ changing by global brightness control (control data are 19h ≥ E6h or E6h ≥ 19h with DCRn/Gn/Bn = 7Fh with DC high adjustment range)		100	300	ns
t_{ON_ERR}	Output on-time error(1)	$t_{OUT\_ON} – T_{GSCKR/G/B}$, GS_{DATA} = 001h, GSCKR/G/B = 33 MHz, with BCR/G/B = FFh and DCRn/Gn/Bn = 7Fh with DC high adjustment range	–15		5	ns

(1) Output on-time error (t_{ON_ERR}) is calculated by the formula t_{ON_ERR} (ns) = $t_{OUT\_ON} – T_{GSCKR/G/B}$. t_{OUT_ON} indicates the actual on-time of the constant current driver. T_{GSCKR} is the period of GSCKR, T_{GSCKG} is the period of GSCKG, and T_{GSCKB} is the period of GSCKB.

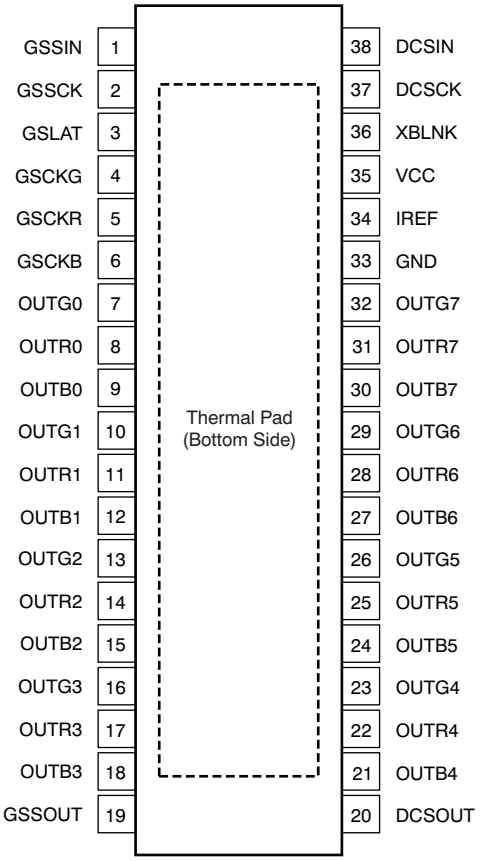
FUNCTIONAL BLOCK DIAGRAM



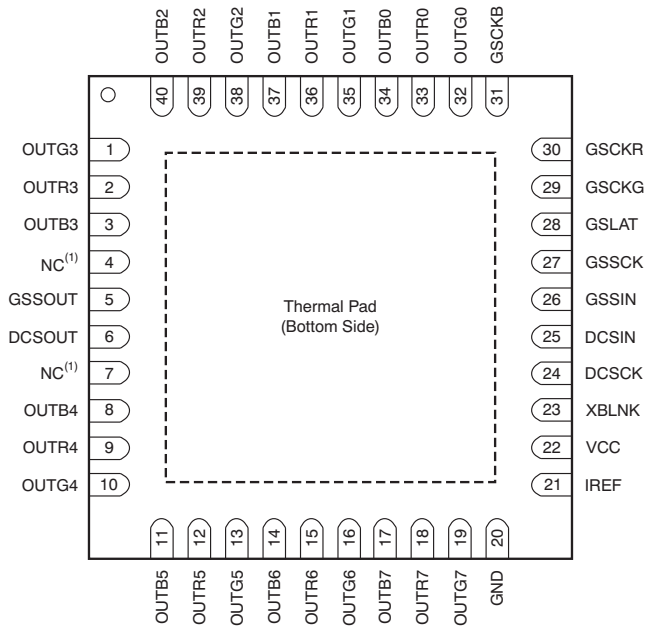
(1) The internal blank signal is generated when GSLAT is input for GS data with display timing reset enabling. Furthermore, the signal is generated at the 4096th GSCK when auto repeat mode is enabled. XBLNK can be connected to V_{CC} when the display timing reset or auto repeat is enabled.

PIN CONFIGURATIONS

DAP PACKAGE
HTSSOP-38 PowerPAD
(TOP VIEW)



RHA PACKAGE
6 mm × 6 mm QFN-40
(TOP VIEW)



(1) NC = no connection.

TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	NO. DAP	NO. RHA		
GSSIN	1	26	I	Serial data input for the 288-bit common shift register for grayscale (GS), dot correction (DC), global brightness control (BC), and function control (FC) data. GSSIN is connected to the LSB of the 288-bit common shift register. This pin is internally pulled to GND with a 500-kΩ resistor.
GSSCK	2	27	I	Serial data shift clock for the 288-bit common shift register for GS/DC/BC/FC data. Data present on GSSIN are shifted into the LSB of the shift register with the rising edge of GSSCK. Data in the shift register are shifted toward the MSB at each rising edge of GSSCK. The MSB data of the shift register appear on GSSOUT.
GSLAT	3	28	I	Data in the 288-bit common shift register are copied to the GS data latch or to the DC/BC/FC data latch at the rising edge of GSLAT. The level of GSLAT at the last GSSCK before the GSLAT rising edge determines which of the two latches the data are transferred into. When GSLAT is low at the last GSSCK rising edge, all 288 bits in the common shift register are copied to the GS data latch. When GSLAT is high at the last GSSCK rising edge, bits 0-198 are copied to the DC/BC/FC data latch and bits 199-215 are copied to the 216-bit DC/BC/FC/UD shift register. The GSLAT rising edge for a DC/BC/FC/UD data write must be input more than 7 ms after a data write through the DCSIN pin.
GSSOUT	19	5	O	Serial data output of the 288-bit common shift register. LED open detection (LOD), LED short detection (LSD), thermal error flag (TEF), and 199-bit data in the DC/BC/FC data latch can be read via GSSOUT. GSSOUT is connected to the MSB of the shift register. Data are clocked out at the rising edge of GSSCK.
DCSIN	38	25	I	Serial data input for the 216-bit DC/BC/FC/UD shift register. DCSIN is connected to the LSB of the shift register.
DCSCK	37	24	I	Serial data shift clock for the 216-bit DC/BC/FC/UD shift register. Data present on DCSIN are shifted into the LSB of the shift register with the DCSCK rising edge. Data in the shift register are shifted toward the MSB at each DCSCK rising edge. The MSB data of the register appear on DCSOUT. The 216-bit data in the shift register are automatically copied to DC/BC/FC/UD data latch 3 ms to 7 ms after the DCSCK rising edge is not input.
DCSOUT	20	6	O	Serial data output of the 216-bit shift register. DCSOUT is connected to the MSB of the shift register. Data are clocked out at the rising edge of DCSCK.
GSCKR	5	30	I	Reference clock for the GS pulse width modulation (PWM) control for the RED LED output group. When XBLNK is high, each GSCKR rising edge increments the RED LED GS counter for PWM control.
GSCKG	4	29	I	Reference clock for the GS PWM control for the GREEN LED output group. When XBLNK is high, each GSCKR rising edge increments the GREEN LED GS counter for PWM control.
GSCKB	6	31	I	Reference clock for the GS PWM control for the BLUE LED output group. When XBLNK is high, each GSCKR rising edge increments the BLUE LED GS counter for PWM control.
XBLNK	36	23	I	When XBLNK is low, all constant-current outputs (OUTR0-OUTR7, OUTG0-OUTG7, OUTB0-OUTB7) are forced off. The grayscale counters for each color group are reset to '0', and the grayscale PWM timing controller is initialized. When XBLNK is high, all constant current outputs are controlled by the grayscale PWM timing controller for each color LED. This pin is internally pulled to GND with a 500 kΩ resistor.
IREF	34	21	I/O	A resistor connected between IREF and GND sets the maximum current for all constant current outputs.
OUTR0-OUTR7	8, 11, 14, 17, 22, 25, 28, 31	2, 9, 12, 15, 18, 33, 36, 39	O	Constant-current outputs for the RED LED group. These outputs are controlled with the GSCKR clock signal. The RED LED group is divided into four subgroups: OUTR0/OUTR4, OUTR1/OUTR5, OUTR2/OUTR6, and OUTR3/OUTR7. Each paired output turns on/off with 24 ns (typ) time delay between other paired outputs. Multiple outputs can be tied together to increase the constant current capability. Different voltages can be applied to each output.

TERMINAL FUNCTIONS (continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO. DAP	NO. RHA		
OUTG0-OUTG7	7, 10, 13, 16, 23, 26, 29, 32	1, 10, 13, 16, 19, 32, 35, 38	O	Constant-current outputs for the GREEN LED group. These outputs are controlled with the GSCKG clock signal. The GREEN LED group is divided into four subgroups: OUTG0/OUTG4, OUTG1/OUTG5, OUTG2/OUTG6, and OUTG3/OUTG7. Each paired output turns on/off with 24 ns (typ) time delay between other paired outputs. Multiple outputs can be tied together to increase the constant current capability. Different voltages can be applied to each output.
OUTB0-OUTB7	9, 12, 15, 18, 21, 24, 27, 30	3, 8, 11, 14, 17, 34, 37, 40	O	Constant current outputs for the BLUE LED group. These outputs are controlled with the GSCKB clock signal. The BLUE LED group is divided into four subgroups: OUTB0/OUTB4, OUTB1/OUTB5, OUTB2/OUTB6, and OUTB3/OUTB7. Each paired output turns on/off with 24 ns (typ) time delay between other paired outputs. Multiple outputs can be tied together to increase the constant current capability. Different voltages can be applied to each output.
VCC	35	22	—	Power supply
GND	33	20	—	Power ground
NC	—	4, 7	—	No internal connection

PARAMETER MEASUREMENT INFORMATION

PIN EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

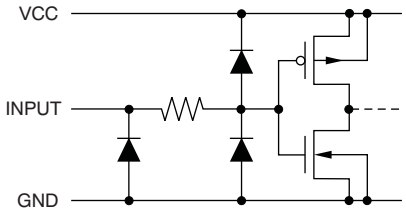


Figure 1. GSSCK, GSLAT, DCSIN, DCSCK, GSCKR, GSCKG, GSCKB

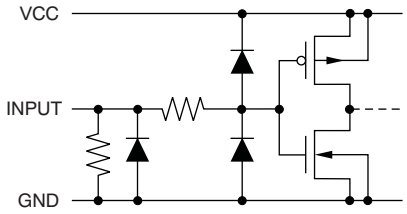


Figure 2. GSSIN, XBLNK

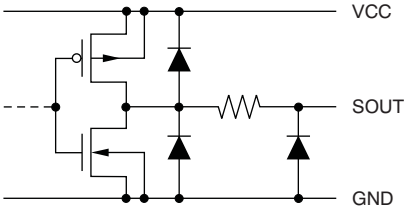


Figure 3. GSSOUT, DCSOUT

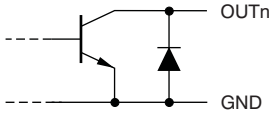


Figure 4. OUTR0/G0/B0 Through OUTR7/G7/B7

TEST CIRCUITS

(1) C_L includes measurement probe and jig capacitance.

(2) X = R, G, or B; n = 0-7.

(1) C_L includes measurement probe and jig capacitance.

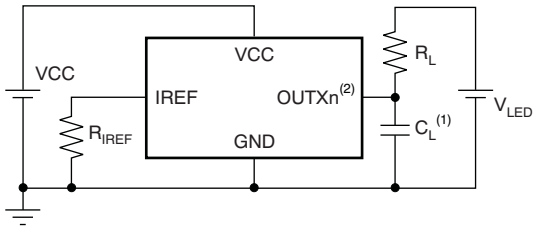


Figure 5. Rise Time and Fall Time Test Circuit for OUTRn/Gn/Bn

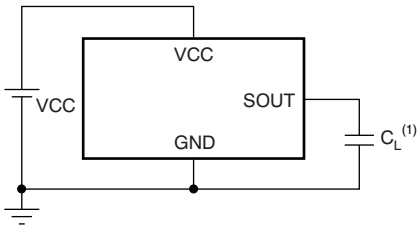
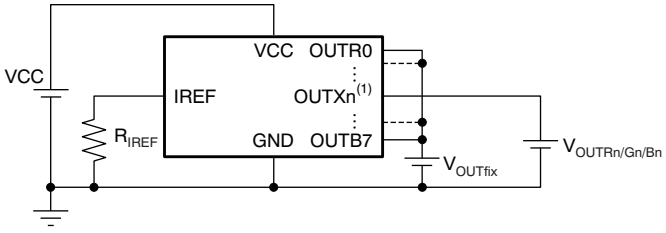


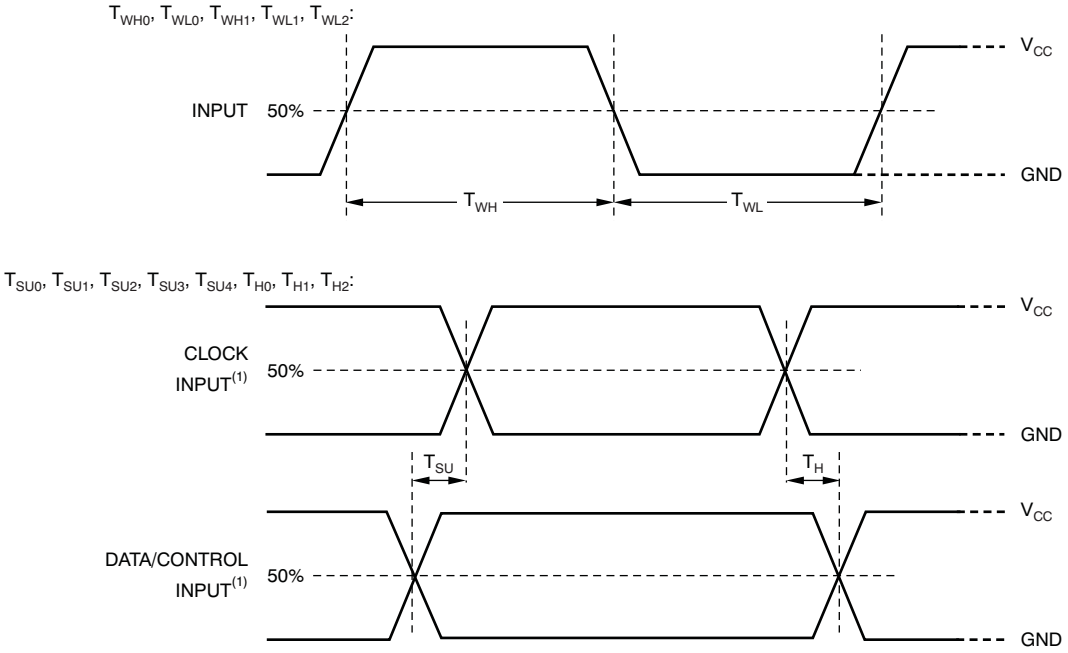
Figure 6. Rise Time and Fall Time Test Circuit for GSSOUT and DCSOUT



(1) X = R, G, or B; n = 0-7.

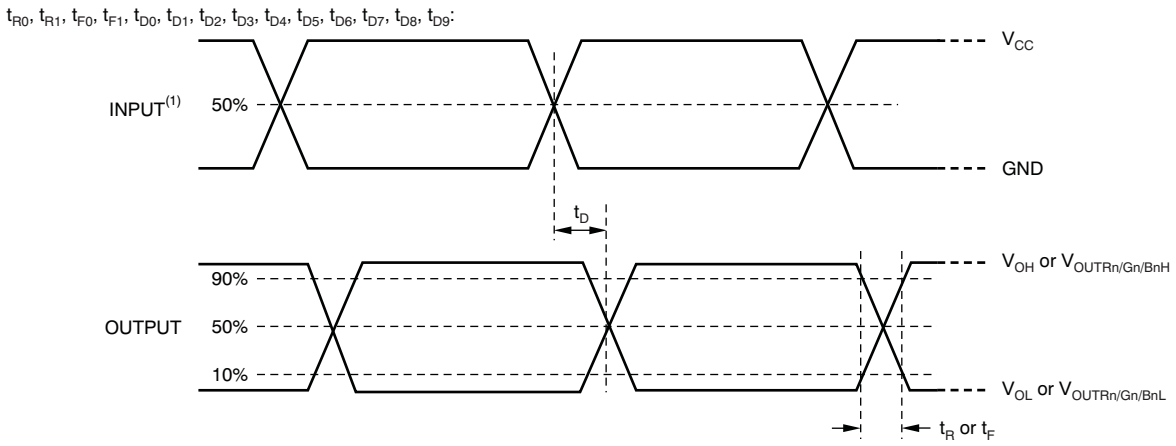
Figure 7. Constant-Current Test Circuit for OUTRn/Gn/Bn

TIMING DIAGRAMS



(2) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 8. Input Timing



(3) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 9. Output Timing

TIMING DIAGRAMS (continued)

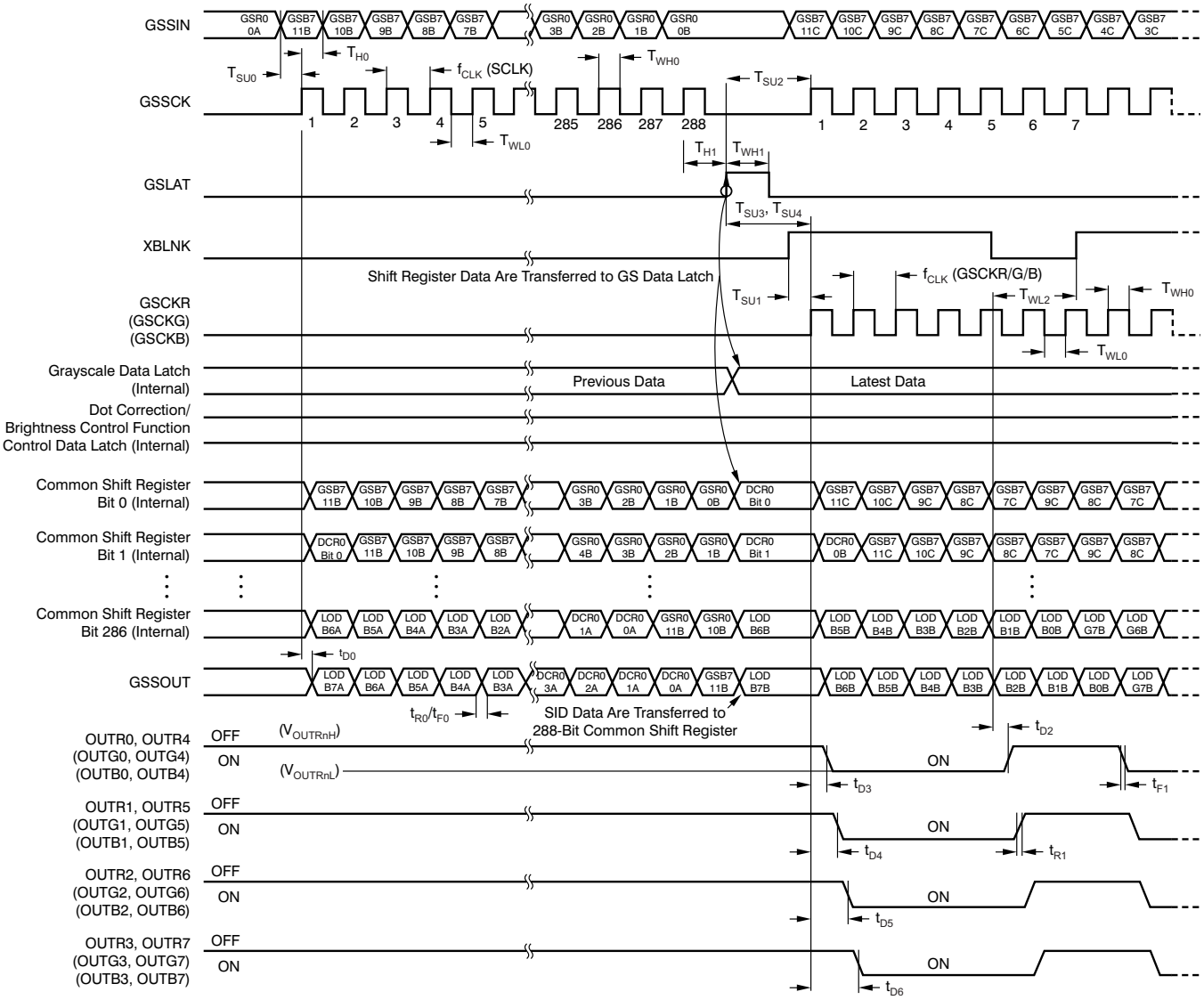


Figure 10. Grayscale Data Write Timing

TIMING DIAGRAMS (continued)

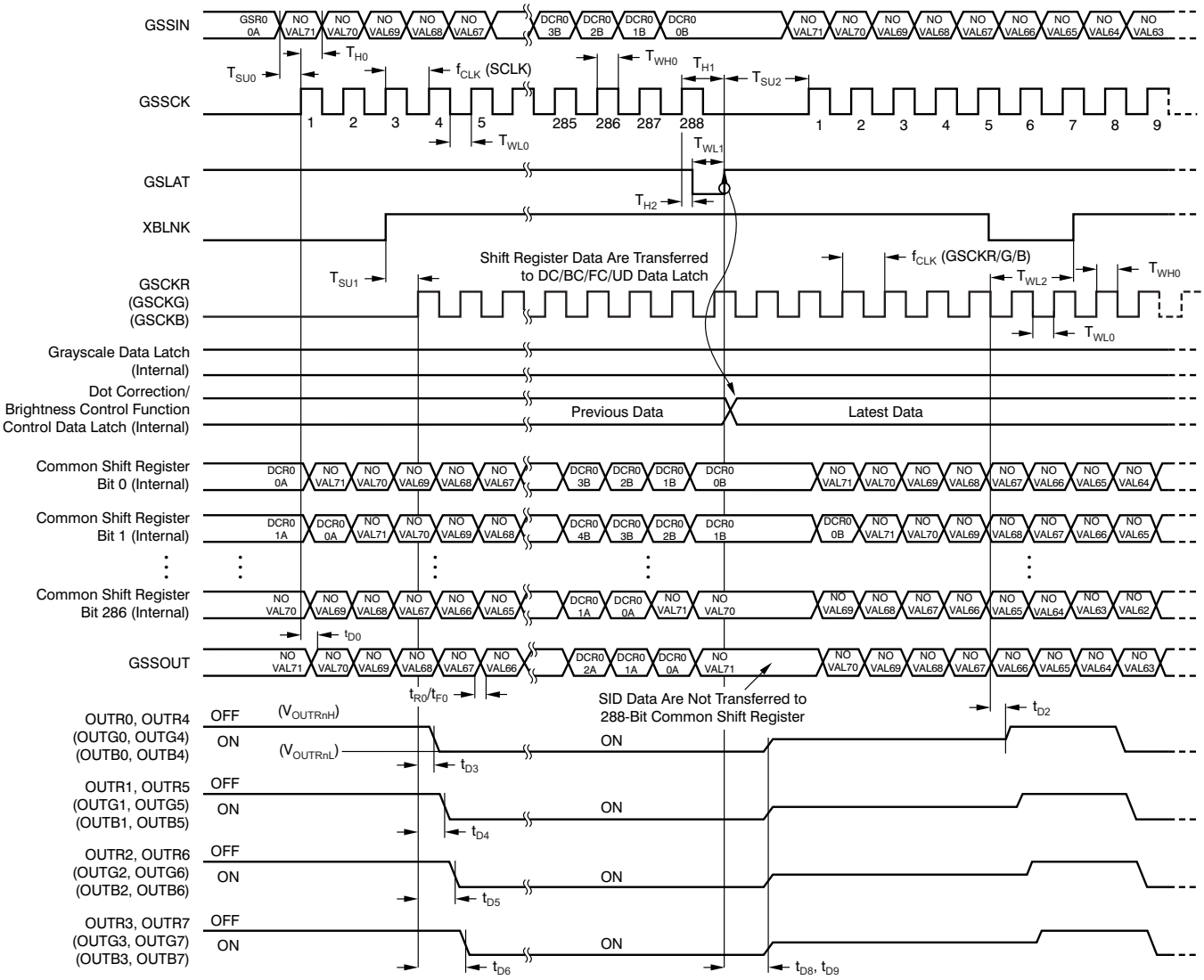


Figure 11. Dot Correction/Global Brightness Control/Function Control/User-Defined Data Write Timing from GS Data Path

TIMING DIAGRAMS (continued)

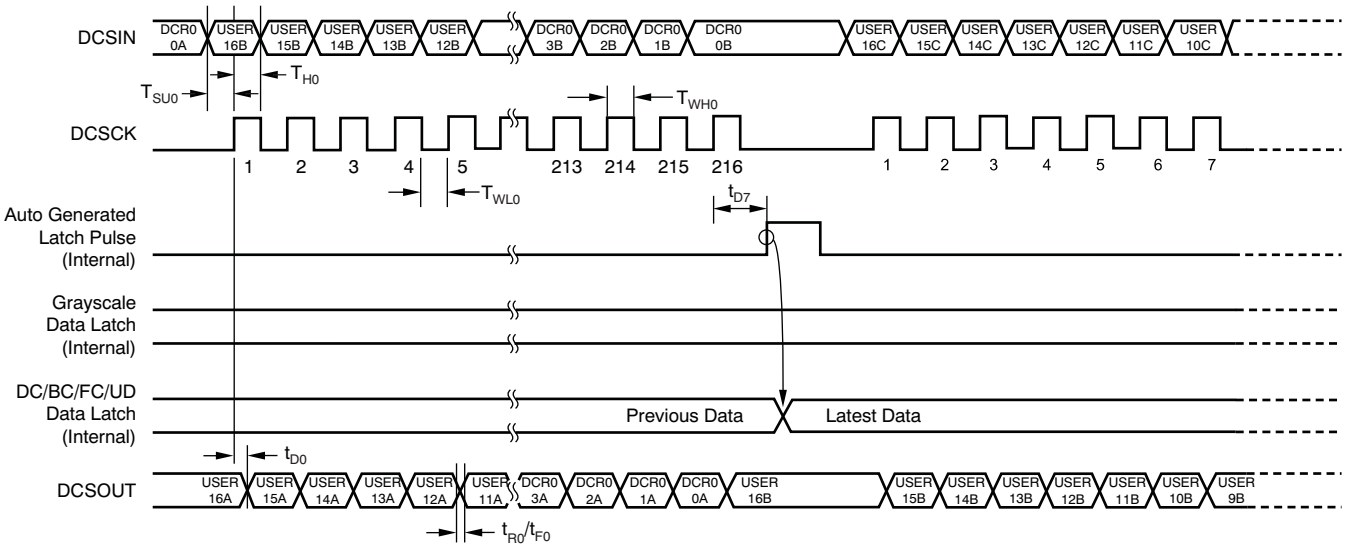


Figure 12. Dot Correction/Global Brightness Control/Function Control Data Write Timing from DC Data Path

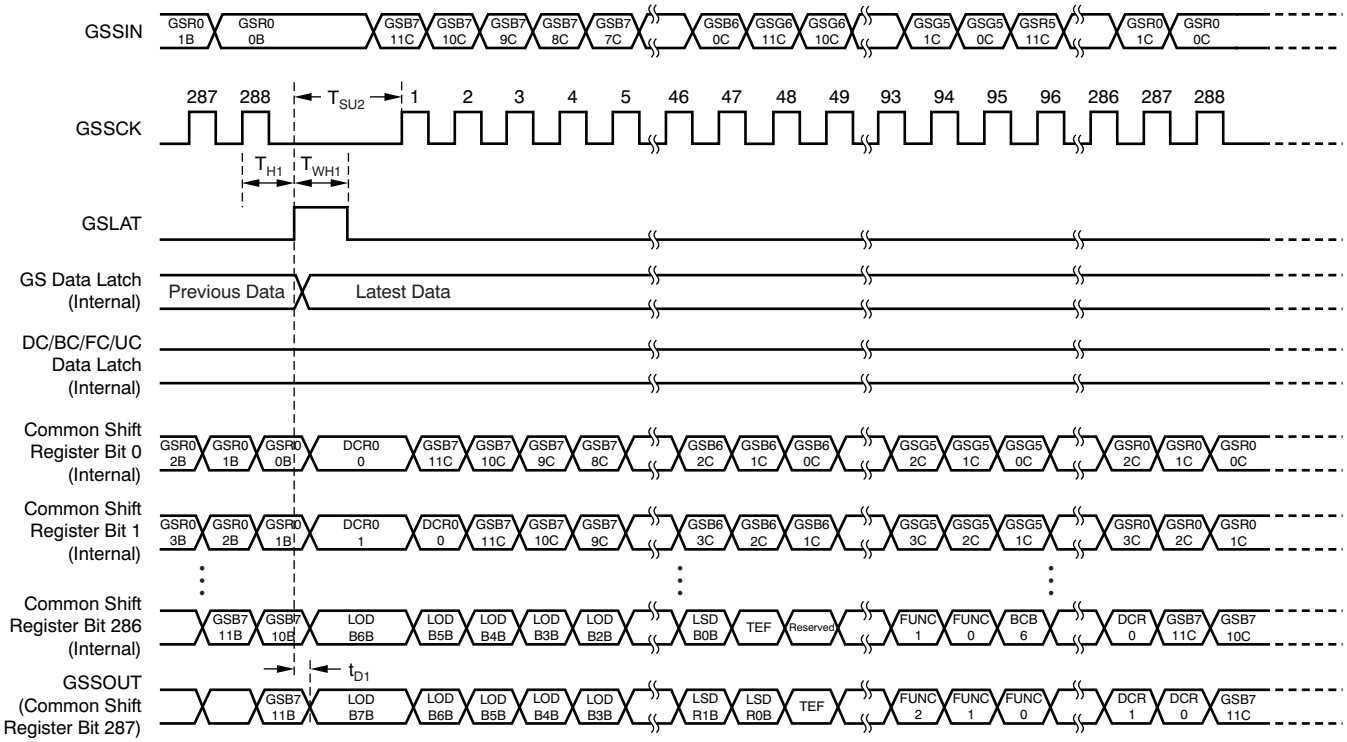


Figure 13. Status Information Data Read Timing

TYPICAL CHARACTERISTICS

At T_A = +25°C and V_{CC} = 3.3 V, unless otherwise noted.

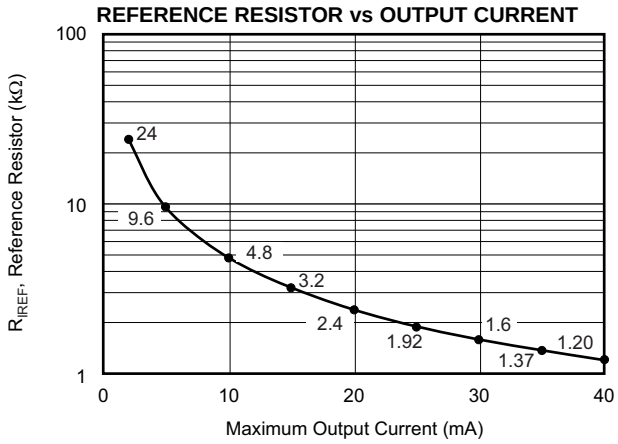


Figure 14.

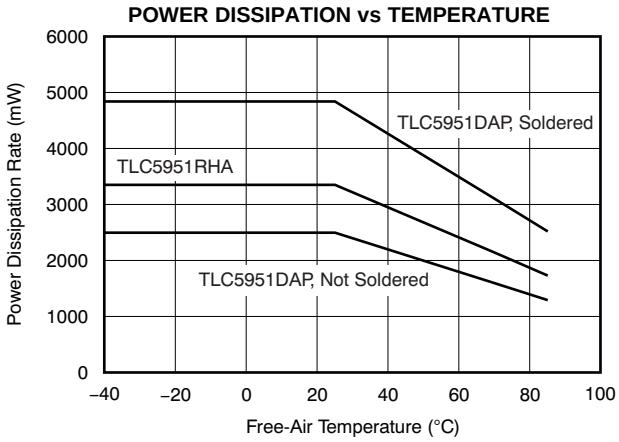


Figure 15.

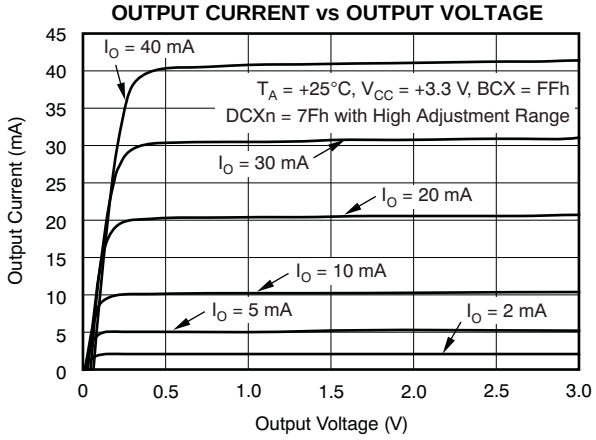


Figure 16.

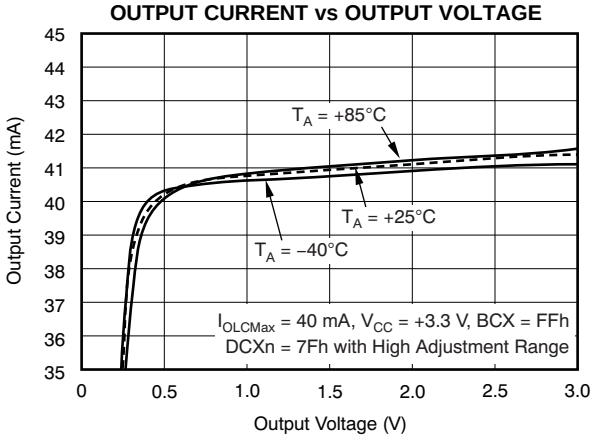


Figure 17.

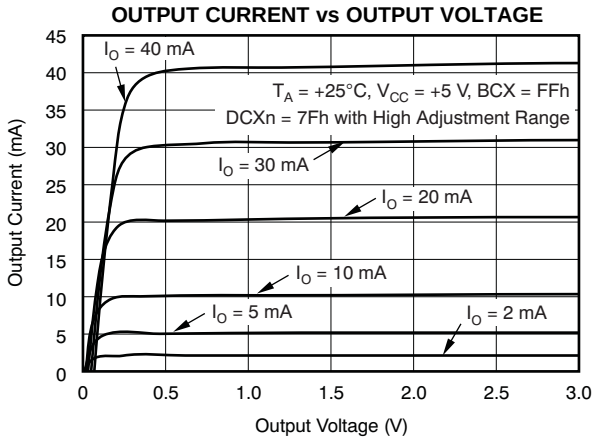


Figure 18.

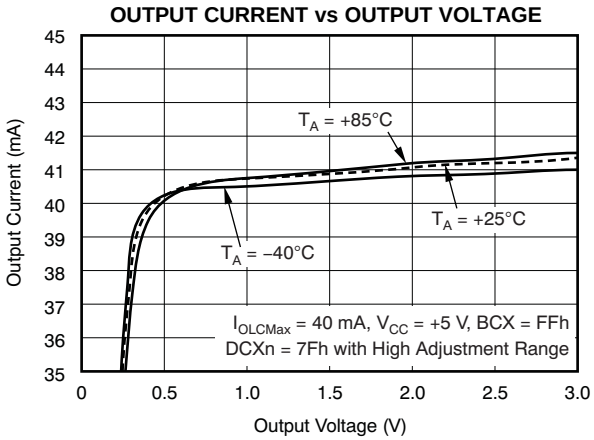


Figure 19.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V_{CC} = 3.3 V, unless otherwise noted.

CONSTANT-CURRENT ERROR vs AMBIENT TEMPERATURE (Channel-to-Channel, RED Color)

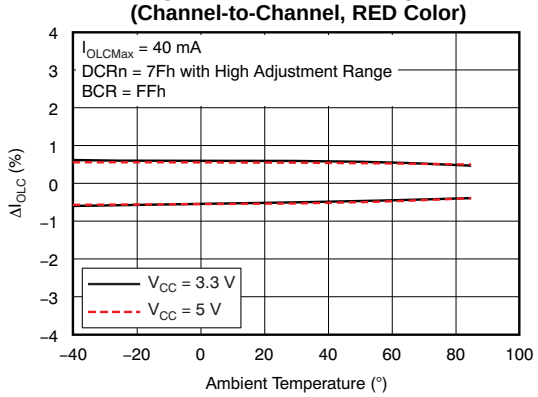


Figure 20.

CONSTANT-CURRENT ERROR vs AMBIENT TEMPERATURE (Channel-to-Channel, GREEN Color)

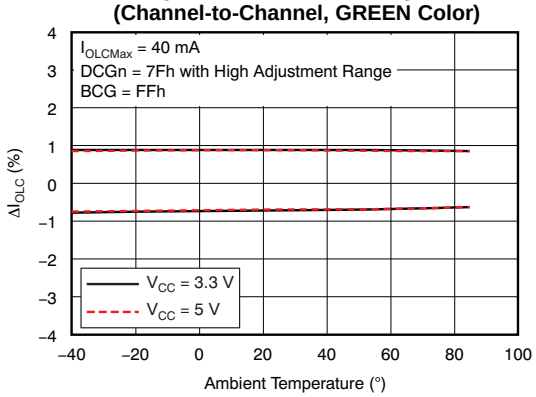


Figure 21.

CONSTANT-CURRENT ERROR vs AMBIENT TEMPERATURE (Channel-to-Channel, BLUE Color)

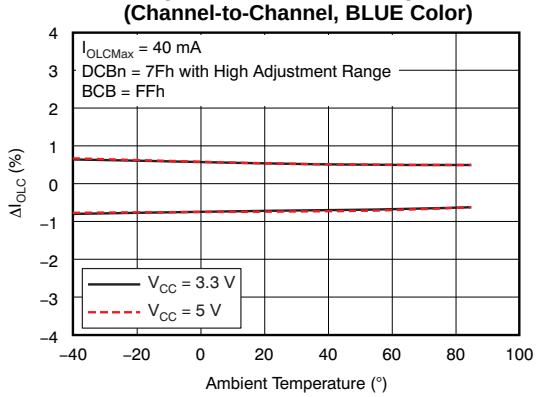


Figure 22.

CONSTANT-CURRENT ERROR vs OUTPUT (Channel-to-Channel, RED Color)

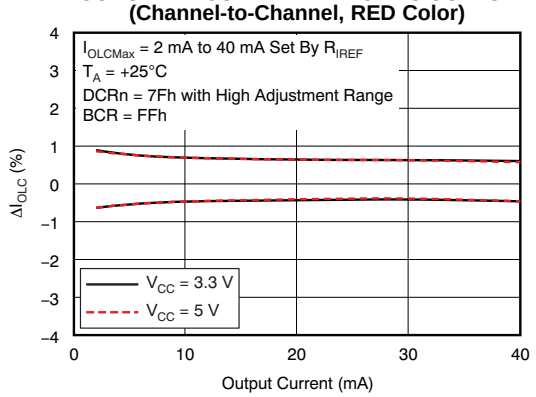


Figure 23.

CONSTANT-CURRENT ERROR vs OUTPUT (Channel-to-Channel, GREEN Color)

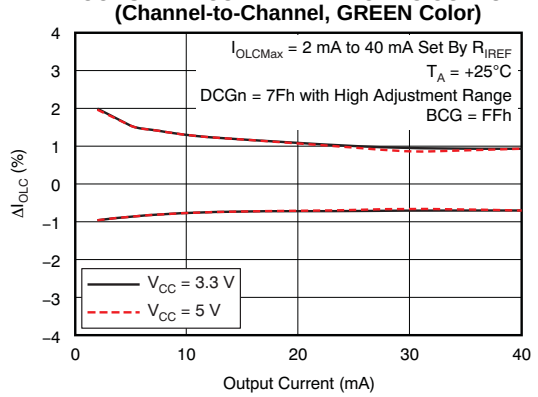


Figure 24.

CONSTANT-CURRENT ERROR vs OUTPUT (Channel-to-Channel, BLUE Color)

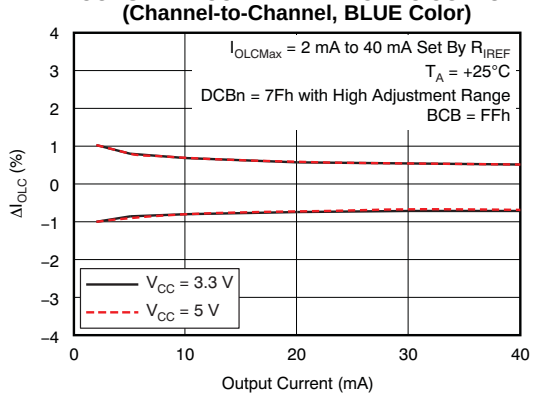


Figure 25.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V_{CC} = 3.3 V, unless otherwise noted.

CONSTANT-CURRENT ERROR vs OUTPUT (Channel-to-Channel, RED Color)

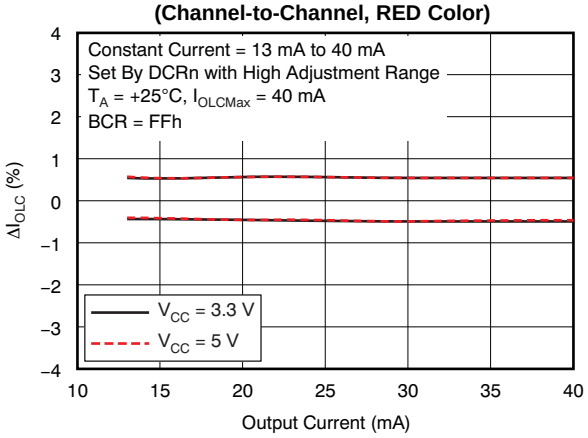


Figure 26.

CONSTANT-CURRENT ERROR vs OUTPUT (Channel-to-Channel, GREEN Color)

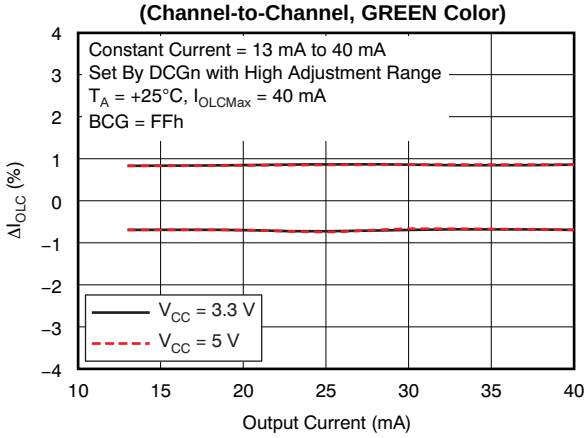


Figure 27.

CONSTANT-CURRENT ERROR vs OUTPUT (Channel-to-Channel, BLUE Color)

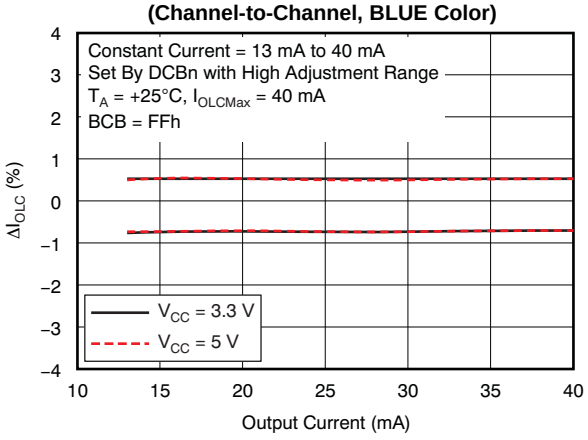


Figure 28.

CONSTANT-CURRENT ERROR vs OUTPUT (Channel-to-Channel, RED Color)

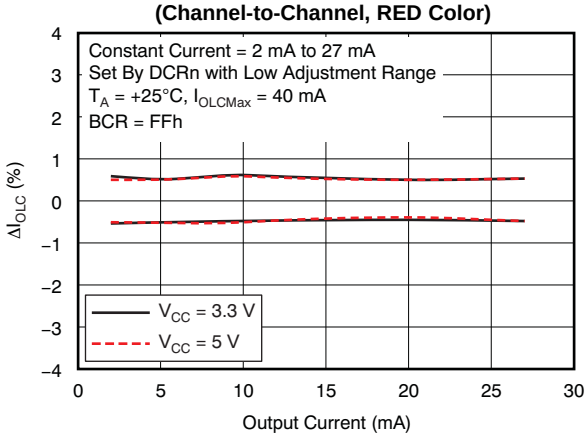


Figure 29.

CONSTANT-CURRENT ERROR vs OUTPUT (Channel-to-Channel, GREEN Color)

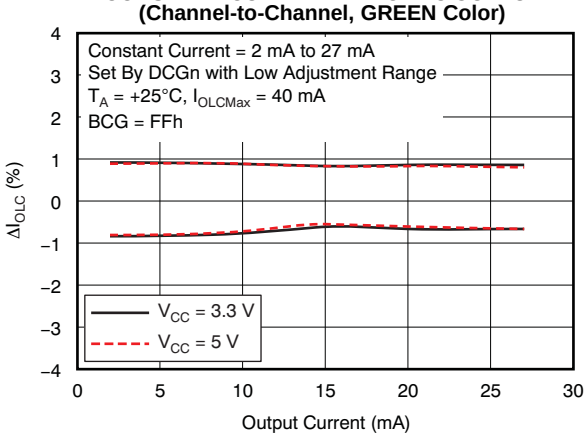


Figure 30.

CONSTANT-CURRENT ERROR vs OUTPUT (Channel-to-Channel, BLUE Color)

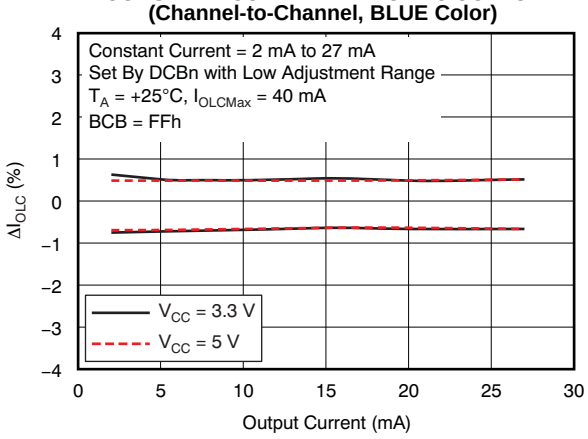


Figure 31.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V_{CC} = 3.3 V, unless otherwise noted.

CONSTANT-CURRENT ERROR vs OUTPUT (Channel-to-Channel, RED Color)

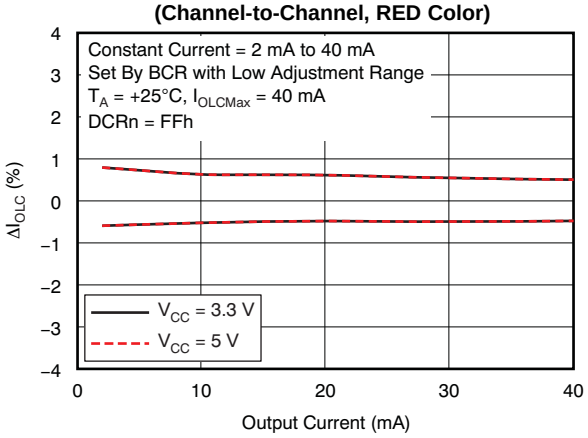


Figure 32.

CONSTANT-CURRENT ERROR vs OUTPUT (Channel-to-Channel, GREEN Color)

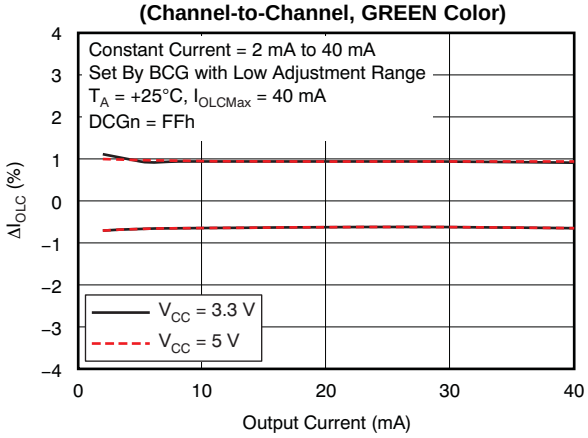


Figure 33.

CONSTANT-CURRENT ERROR vs OUTPUT (Channel-to-Channel, BLUE Color)

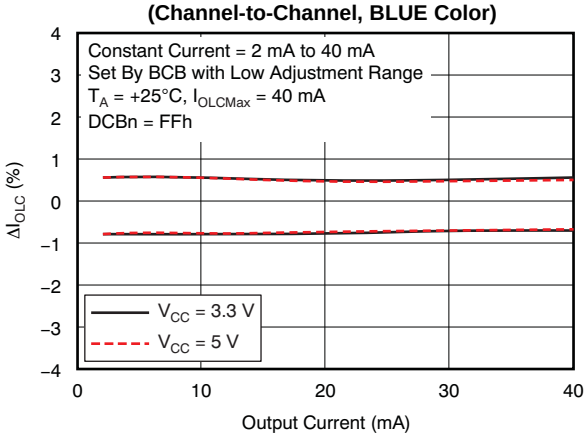


Figure 34.

DOT CORRECTION LINEARITY (I_{OLCMax} with Upper Range)

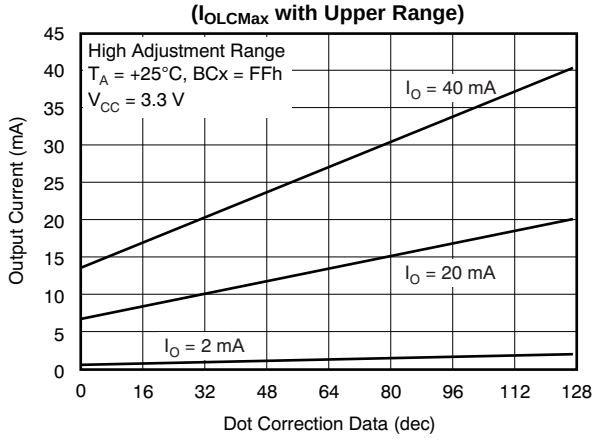


Figure 35.

DOT CORRECTION LINEARITY (I_{OLCMax} with Lower Range)

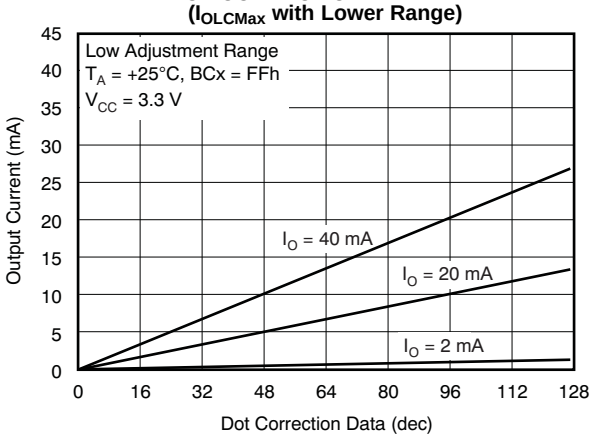


Figure 36.

DOT CORRECTION LINEARITY (I_{OLCMax} with Upper and Lower Range)

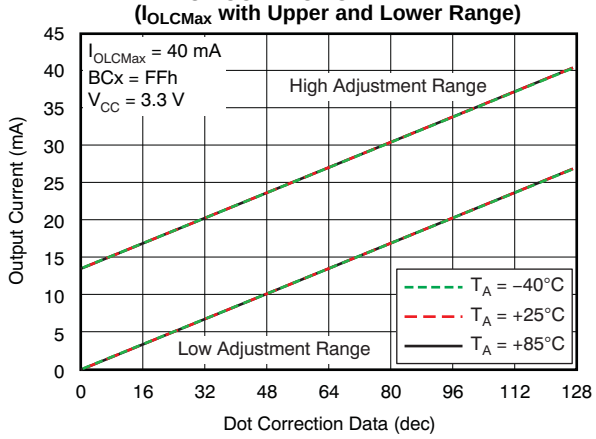


Figure 37.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V_{CC} = 3.3 V, unless otherwise noted.

GLOBAL BRIGHTNESS CONTROL LINEARITY (I_{OLCMax} with Upper Range)

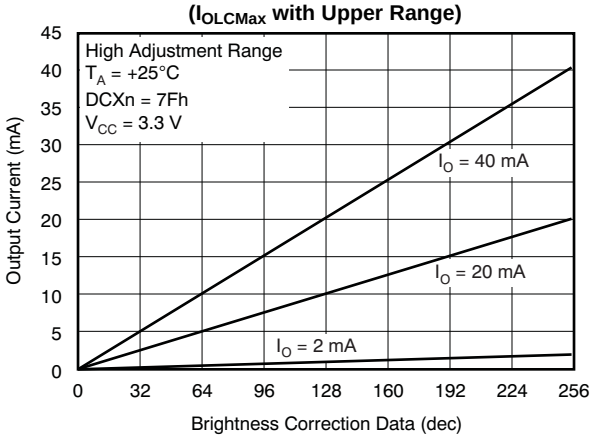


Figure 38.

GLOBAL BRIGHTNESS CONTROL LINEARITY (Ambient Temperature with Upper Range)

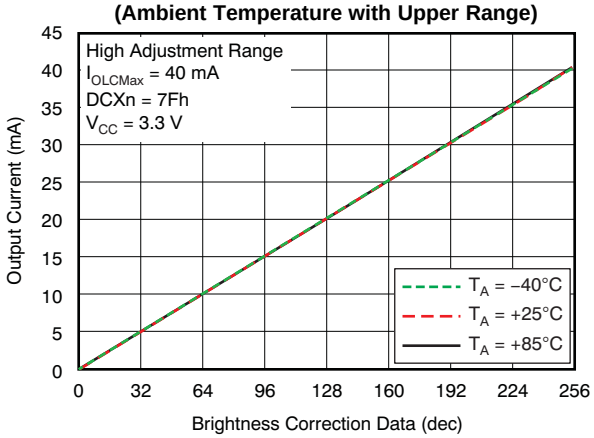


Figure 39.

CONSTANT-CURRENT OUTPUT VOLTAGE WAVEFORM

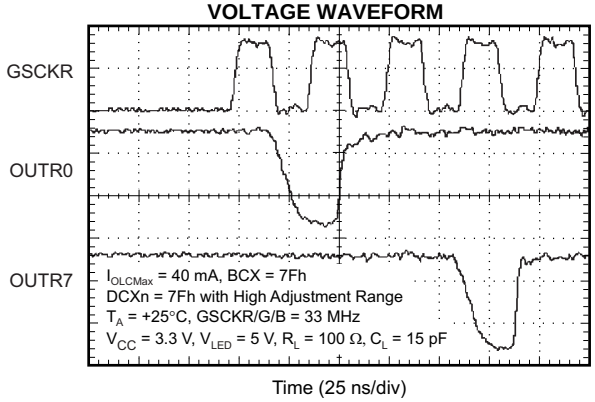


Figure 40.

DETAILED DESCRIPTION

MAXIMUM CONSTANT SINK CURRENT VALUE

The TLC5951 maximum constant sink current value for each channel, I_{OLCMax}, is determined by an external resistor, R_{IREF}, placed between R_{IREF} and GND. The R_{IREF} resistor value is calculated with Equation 1.

$$R_{IREF}\ (k\Omega) = \frac{V_{IREF}\ (V)}{I_{OLCMax}\ (mA)} \times 40 \quad (1)$$

Where:

V_{IREF} = the internal reference voltage on IREF (1.20 V, typically)

I_{OLCMax} is the largest current for each output. Each output sinks the I_{OLCMax} current when it is turned on, the dot correction is set to the maximum value of 7Fh (127d), and the global brightness control data are set to the maximum value of FFh (255d). Each output sink current can be reduced by lowering the output dot correction or brightness control value.

R_{IREF} must be between 1.2 kΩ and 24 kΩ to keep I_{OLCMax} between 40 mA (typ) and 2mA (typ); the output may be unstable when I_{OLCMax} is set lower than 2 mA. Output currents lower than 2 mA can be achieved by setting I_{OLCMax} to 2 mA or higher and then using dot correction and global brightness control to lower the output current.

Figure 14 and Table 2 show the constant sink current versus external resistor, R_{IREF}, characteristics. Multiple outputs can be tied together to increase the constant-current capability. Different voltages can be applied to each output.

Table 2. Maximum Constant Current Output versus External Resistor Value

I_{OLCMax} (mA, Typical)	R_{IREF} (kΩ)
40	1.2
35	1.371
30	1.6
25	1.92
20	2.4
15	3.2
10	4.8
5	9.6
2	24

DOT CORRECTION (DC) FUNCTION

The TLC5951 has the capability to adjust the output current of each channel (OUTR0-OUTR7, OUTG0-OUTG7, OUTB0-OUTB7) individually. This function is called dot correction (DC). The DC function allows the brightness and color deviations of LEDs connected to each output to be individually adjusted. Each output DC is programmed with a 7-bit word for each channel output. Each channel output current is adjusted with 128 steps within one of two adjustment ranges. The dot correction high adjustment range allows the output current to be adjusted from 33.3% to 100% of the maximum output current, I_{OLCMax}. The dot correction low adjustment range allows the output current to be adjusted from 0% to 66.7% of I_{OLCMax}. The range control bits in the function control latch select the high or low adjustment range. Equation 2 and Equation 3 calculate the actual output current as a function of R_{IREF}, DC value, adjustment range, and brightness control value. There are three range control bits that control the DC adjustment range for three groups of outputs: OUTR0-OUTR7, OUTG0-OUTG7, and OUTB0-OUTB7. DC data are programmed into the TLC5951 via the serial interface.

When the IC is powered on, the DC data in the 216-bit common shift register and data latch contain random data. Therefore, DC data must be written to the DC latch before turning the constant-current output on. Additionally, XBLNK should be low when the device turns on to prevent the outputs from turning on before the proper grayscale values can be written. All constant-current outputs are off when XBLNK is low.

GLOBAL BRIGHTNESS CONTROL (BC) FUNCTION

The TLC5951 has the capability to adjust the output current of each color group simultaneously. This function is called global brightness control (BC). The global brightness control for each of the three color groups, (OUTR0-OUTR7, OUTG0-OUTG7, and OUTB0-OUTB7), is programmed with a separate 8-bit word. The BC of each group is adjusted with 256 steps from 0% to 100%. 0% corresponds to 0 mA. 100% corresponds to the maximum output current programmed by R_{IREF} and each output DC value. Note that even though the BC value for all color groups are identical, the output currents can be different if the DC values are different. Equation 2 and Equation 3 calculate the actual output current as a function of R_{IREF}, DC adjustment range, and brightness control value. BC data are programmed into the TLC5951 via the serial interface.

When the IC is powered on, the BC data in the 216-bit common shift register and data latch contain random data. Therefore, BC data must be written to the BC latch before turning the constant-current output on. Additionally, XBLNK should be low when the device turns on to prevent the outputs from turning on before the proper grayscale values can be written. All constant-current outputs are off when XBLNK is low.

Equation 2 determines the output sink current for each color group when the dot correction high adjustment range is chosen.

$$I_{OUT}\,(mA) = \left[\frac{1}{3}\,I_{OLCMax}\,(mA) + \frac{2}{3}\,I_{OLCMax}\,(mA) \times \left[\frac{DC}{127}\right]\right] \times \left[\frac{BC}{255}\right] \quad (2)$$

Equation 3 determines the output sink current for each color group when the dot correction low adjustment range is chosen.

$$I_{OUT}\,(mA) = \left[\frac{2}{3}\,I_{OLCMax}\,(mA) \times \left[\frac{DC}{127}\right]\right] \times \left[\frac{BC}{255}\right] \quad (3)$$

Where:

I_{OLCMax} = the maximum channel current for each channel determined by R_{IREF}

DC = the decimal dot correction value for the output. This value ranges between 0 and 127.

BC = the decimal brightness control value for the output color group. This value ranges between 0 and 255.

Table 3. Output Current versus DC Data and I_{OLCMax} with Dot Correction High Adjustment Range (BC Data = FFh)

DC DATA (Binary)	DC DATA (Decimal)	DC DATA (Hex)	BC DATA (Hex)	PERCENTAGE OF I_{OLCMax} (%)	I_{OUT}, mA (I_{OLCMax} = 40 mA)	I_{OUT}, mA (I_{OLCMax} = 2 mA)
000 0000	0	00	FF	33.3	13.33	0.67
000 0001	1	01	FF	33.9	13.54	0.68
000 0010	2	02	FF	34.4	13.75	0.69
—	—	—	—	—	—	—
111 1101	125	7D	FF	99.0	39.58	1.98
111 1110	126	7E	FF	99.5	39.79	1.99
111 1111	127	7F	FF	100.0	40.00	2.00

Table 4. Output Current versus DC Data and I_{OLCMax} with Dot Correction Low Adjustment Range (BC Data = FFh)

DC DATA (Binary)	DC DATA (Decimal)	DC DATA (Hex)	BC DATA (Hex)	PERCENTAGE OF I_{OLCMax} (%)	I_{OUT}, mA (I_{OLCMax} = 40 mA)	I_{OUT}, mA (I_{OLCMax} = 2 mA)
000 0000	0	00	FF	0	0	0
000 0001	1	01	FF	0.5	0.21	0.01
000 0010	2	02	FF	1.0	0.42	0.01
—	—	—	—	—	—	—
111 1101	125	7D	FF	65.6	26.25	1.31
111 1110	126	7E	FF	66.1	26.46	1.32
111 1111	127	7F	FF	66.7	26.67	1.33

Table 5. Output Current versus BC Data and I_{OLCMax} with Dot Correction High Adjustment Range (DC Data = 7Fh)

BC DATA (Binary)	BC DATA (Decimal)	BC DATA (Hex)	DC DATA (Hex)	PERCENTAGE OF I_{OLCMax} (%)	I_{OUT}, mA (I_{OLCMax} = 40 mA)	I_{OUT}, mA (I_{OLCMax} = 2 mA)
000 0000	0	00	7F	0	0	0
000 0001	1	01	7F	0.4	0.16	0.01
000 0010	2	02	7F	0.8	0.31	0.02
—	—	—	—	—	—	—
111 1101	253	FD	7F	99.2	39.69	1.98
111 1110	254	FE	7F	99.6	39.84	1.99
111 1111	255	FF	7F	100.0	40.00	2.00

Table 6. Output Current versus BC Data, DC Data, and I_{OLCMax} with Dot Correction High Adjustment Range

BC DATA (Hex)	BC DATA (Decimal)	DC DATA (Hex)	DC DATA (Decimal)	PERCENTAGE OF I_{OLCMax} (%)	I_{OLCMax} = 40 mA (mA, Typical)	I_{OLCMax} = 2 mA (mA, Typical)
00	0	20	32	0	0	0
—	—	—	—	—	—	—
33	51	20	32	10.02	4.01	0.2
—	—	—	—	—	—	—
80	128	20	32	25.16	10.06	0.5
—	—	—	—	—	—	—
CC	204	20	32	40.10	16.04	0.8
—	—	—	—	—	—	—
FF	255	20	32	50.13	13.33	1.0

GRAYSCALE (GS) FUNCTION (PWM CONTROL)

The TLC5951 can adjust the brightness of each output channel using a pulse width modulation (PWM) control scheme. The use of 12 bits per channel results in 4096 brightness steps, from 0% up to 100% brightness. The grayscale circuitry is duplicated for each of the three color groups.

The PWM operation for each color group is controlled by a 12-bit GS counter. Three GS counters are implemented to control each of the three color outputs, OUTR0-OUTR7, OUTG0-OUTG7, and OUTB0-OUTB7. Each counter increments on each rising edge of the grayscale reference clock (GSCKR, GSCKG, or GSCKB). The falling edge of XBLNK resets the three counter values to '0'. The grayscale counter values are held at '0' while XBLNK is low, even if the GS clock input is toggled high and low. Pulling XBLNK high enables the GS clock. The first rising edge of a GS clock after XBLNK goes high increments the corresponding grayscale counter by one and switches on all outputs with a non-zero GS value programmed into the GS latch. Each additional rising edge on a GS clock increases the corresponding GS counter by one.

The GS counters keep track of the number of clock pulses from the respective GS clock inputs (GSCKR, GSCKG, and GSCKB). Each output stays on while the counter is less than or equal to the programmed grayscale value. Each output turns off at the rising edge of the GS counter value when the counter is larger than the output grayscale latch value.

Equation 4 calculates each output (OUTRn/Gn/Bn) on-time (t_{OUT_ON}):

$$t_{OUTON}\ (ns) = T_{GSCLKR/G/B}\ (ns) \times GSn \quad (4)$$

Where:

$T_{GSCKR/G/B}$ = one period of GS clock for the color

GSn = the programmed grayscale value for OUTRn/Gn/Bn (GSn = 0d to 4095d)

When new GS data are latched into the GS data latch with the rising edge on GSLAT during a PWM cycle, the GS data latch registers are immediately updated. This latching can cause the outputs to turn on or off unexpectedly. For proper operation, GS data should only be latched into the IC at the end of a display period when XBLNK is low. Table 7 summarizes the GS data value versus the output on-time duty cycle.

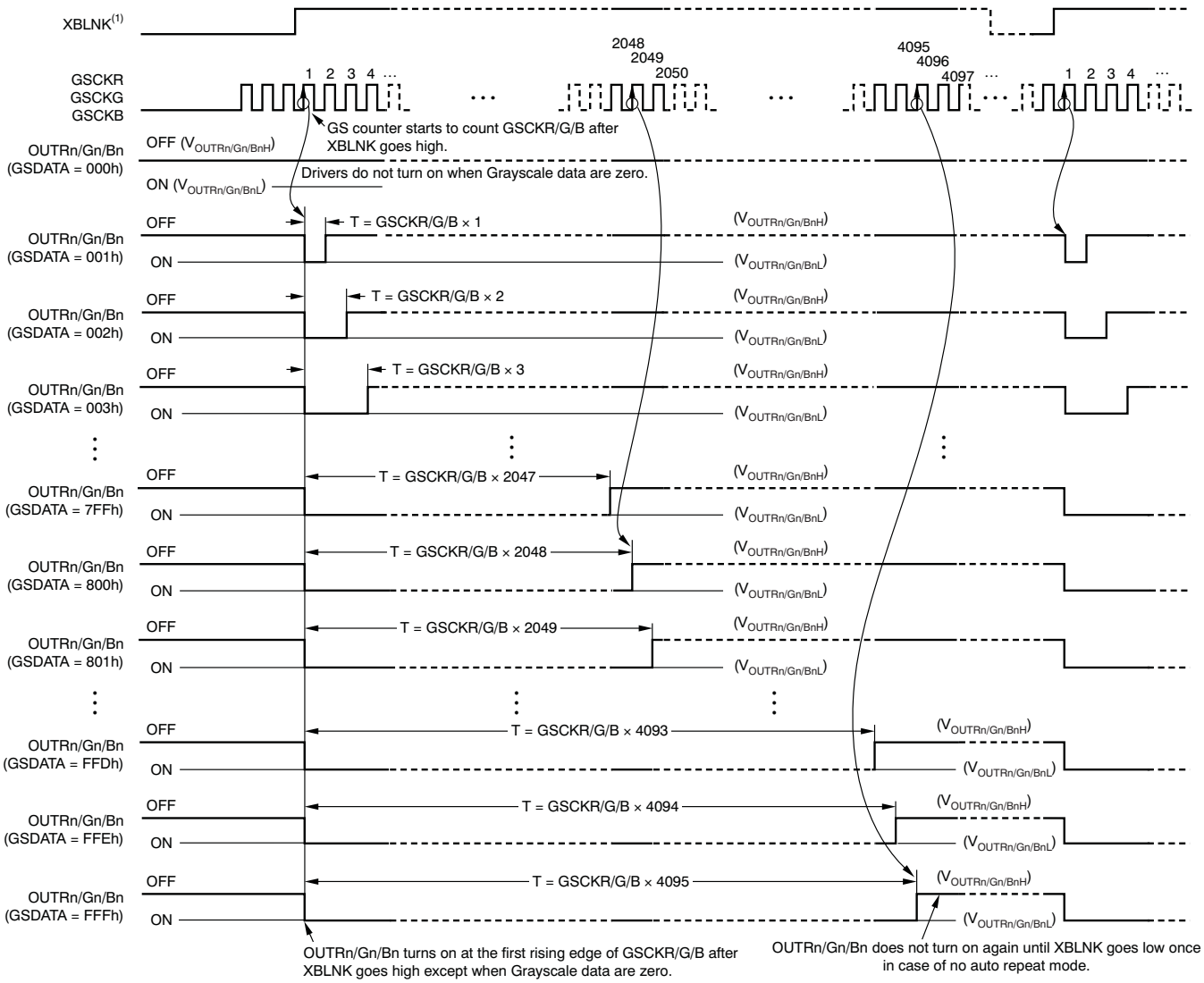
When the IC is powered up, the 288-bit common shift register and GS data latch contain random data. Therefore, GS data must be written to the GS latch before turning the constant-current output on. Additionally, XBLNK should be low when the device is powered up to prevent the outputs from turning on before the proper GS values are programmed into the registers. All constant-current outputs are off when XBLNK is low.

If there are any unconnected outputs (OUTRn, OUTGn, and OUTBn), including LEDs in a failed short or failed open condition, the GS data corresponding to the unconnected output should be set to '0' before turning on the LEDs. Otherwise, the VCC supply current (I_{VCC}) increases while that constant-current output is programmed to be on.

Table 7. Output Duty Cycle and On-Time versus GS Data

GS DATA (Binary)	GS DATA (Decimal)	GS DATA (Hex)	OUTPUT ON-TIME DUTY CYCLE (%)	OUTPUT ON-TIME (33-MHz GS Clock) (ns)
0000 0000 0000	0	000	0	0
0000 0000 0001	1	001	0.02	30
0000 0000 0010	2	002	0.05	61
—	—	—	—	—
0111 1111 1111	2047	7FF	49.99	62030
1000 0000 0000	2048	800	50.01	62061
1000 0000 0001	2049	801	50.04	62091
—	—	—	—	—
1111 1111 1101	4093	FFD	99.95	124030
1111 1111 1110	4094	FFE	99.98	124061
1111 1111 1111	4095	FFF	100	124091

PWM Counter 12-Bit Mode Without Auto Repeat



(1) The internal blank signal is generated when GSLAT is input for GS data with display timing reset enabled. Also, the signal is generated at 4096th GSCKR/G/B when the auto repeat mode is enabled. XBLNK can be connected to VCC when the display timing reset or auto repeat is enabled.

Figure 41. PWM Operation 1

PWM Counter 8-, 10-, or 12-Bit Mode Without Auto Repeat

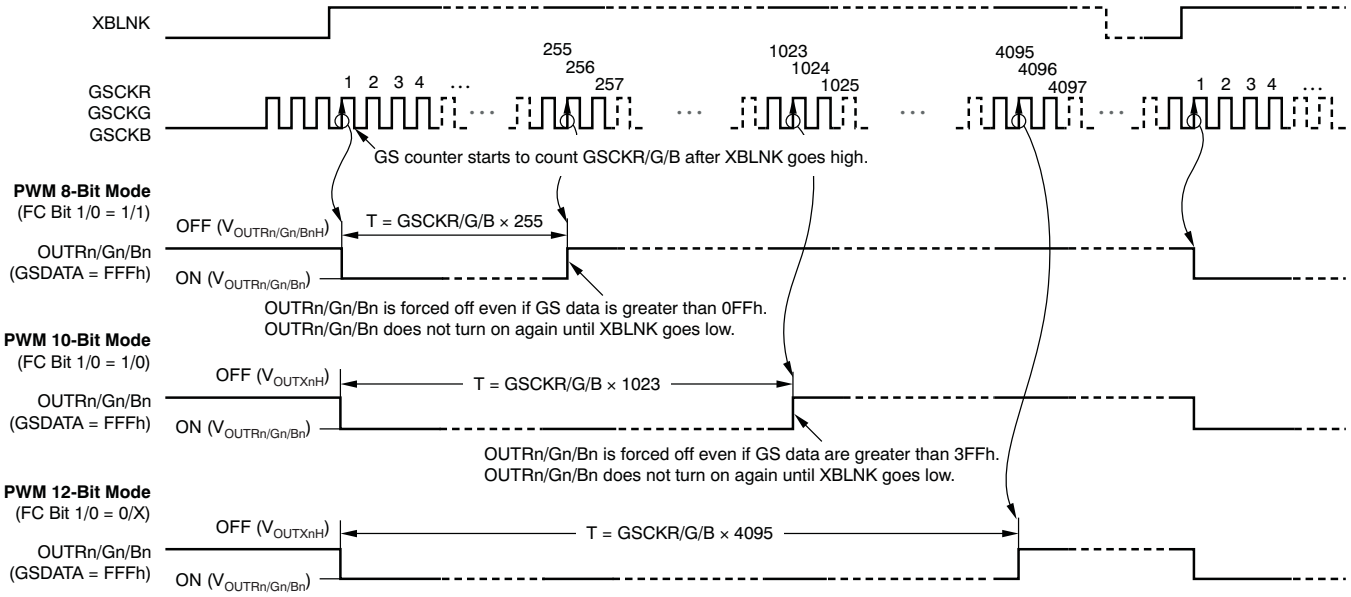


Figure 42. PWM Operation 2

PWM Counter 8-, 10-, or 12-Bit Mode With Auto Repeat

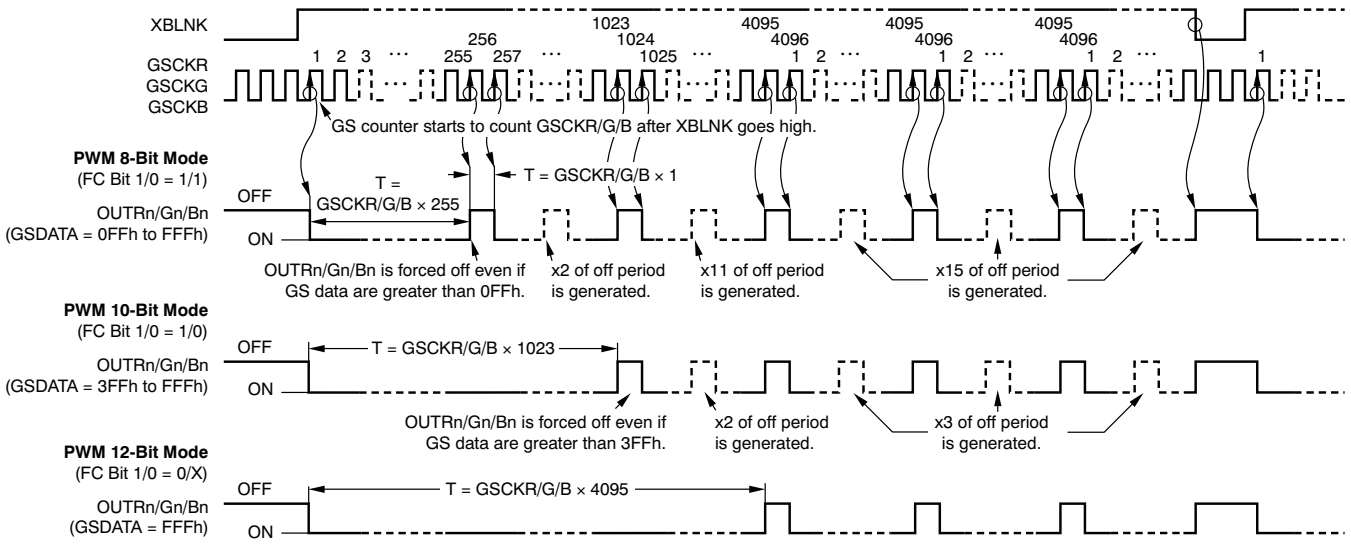


Figure 43. PWM Operation 3

REGISTER AND DATA LATCH CONFIGURATION

The TLC5951 has two data latches to store information: the grayscale (GS) data latch and the DC/BC/FC/UD data latch. The GS data latch can be written as 288-bit data through GSSIN with GSSCK. The DC/BC/FC/UD data latch can be written as data through DCSIN with DCSCK. Also, DC/BC/FC data can be written to the DC/BC/FC/UD data latch through GSSIN with GSSCK. UD data are written to the upper 17 bits of the 216-bit DC/BC/FC/UD shift register at the same time. The data in the DC/BC/FC/UC data latch can be read via GSSOUT with GSSCK. Figure 44 shows the grayscale shift register and data latch configuration.

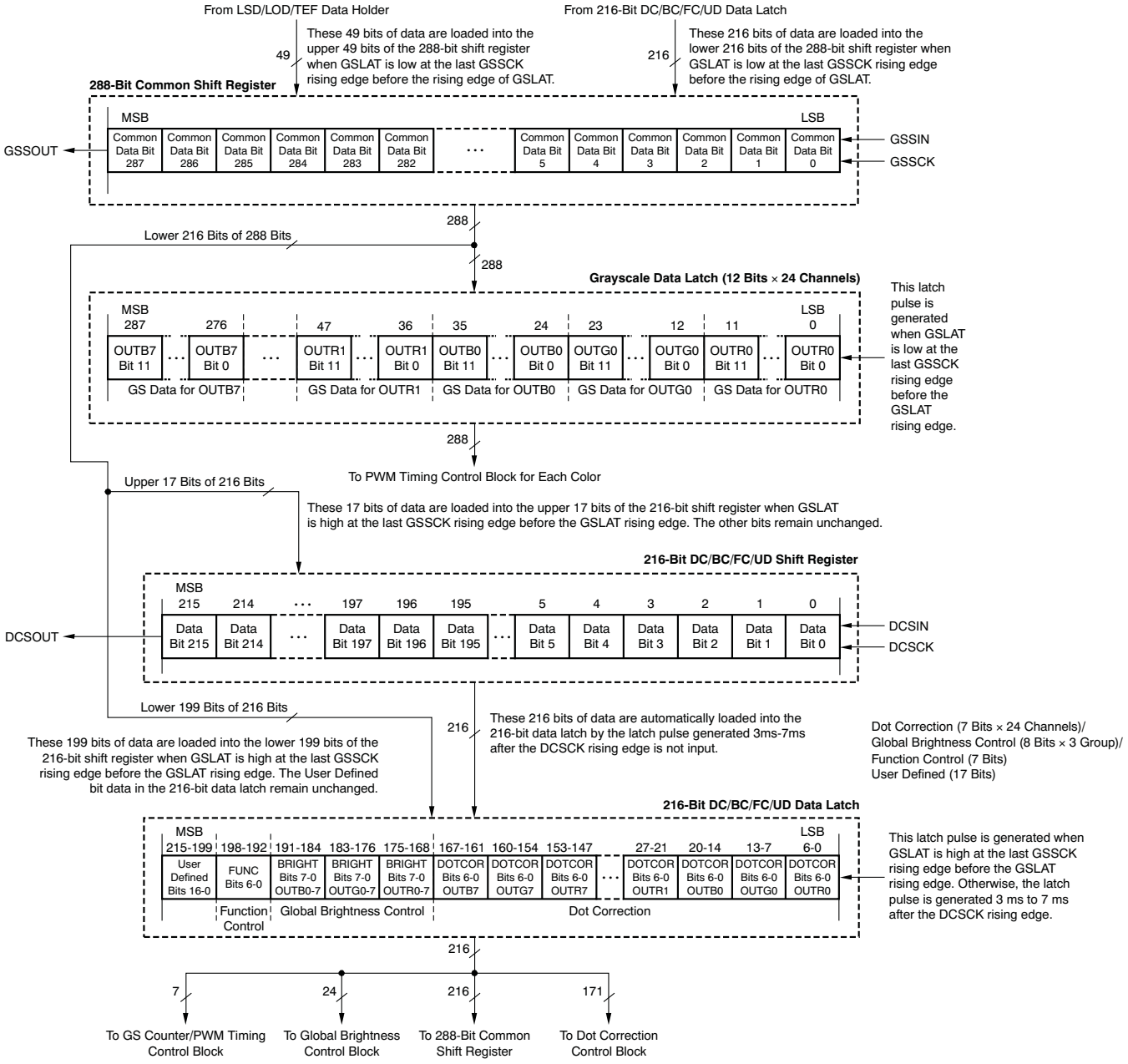


Figure 44. Grayscale Shift Register and Data Latch Configuration

288-Bit Common Shift Register

The 288-bit common shift register is used to shift data from the GSSIN pin into the TLC5951. The data shifted into this register are used for grayscale data, global brightness control, and dot correction data. The register LSB is connected to GSSIN and the MSB is connected to GSSOUT. On each GSSCK rising edge, the data on GSSIN are shifted into the register LSB and all 288 bits are shifted towards the MSB. The register MSB is always connected to GSSOUT.

The level of GSLAT at the last GSSCK before the GSLAT rising edge determines which latch the data are transferred into. When GSLAT is low at the last GSSCK rising edge, all 288 bits are latched into the grayscale data latch. When GSLAT is high at the last GSSCK rising edge, bits 0-198 are copied to bits 0-198 in the DC/BC/FC/UD data latch and bits 199-215 are copied to bits 199-215 in the 216-bit DC/BC/FC/UD shift register at the GSLAT rising edge. To avoid data from being corrupted, the GSLAT rising edge must be input more than 7 ms after the last DCSCK for a DC/BC/FC/UD data write. When the IC powers on, the 288-bit common shift register contains random data.

Grayscale Data Latch

The grayscale (GS) data latch is 288 bits long. This latch contains the 12-bit PWM grayscale value for each of the TLC5951 constant-current outputs. The PWM grayscale values in this latch set the PWM on-time for each constant-current driver. See Table 7 for the on-time duty of each GS data bit. Figure 45 shows the shift register and latch configuration. Refer to Figure 10 for the timing diagram for writing data into the GS shift register and latch.

Data are latched from the 288-bit common shift register into the GS data latch at the rising edge of the GSLAT pin. The conditions for latching data into this register are described in the *288-Bit Common Shift Register* section. When data are latched into the GS data latch, the new data are immediately available on the constant-current outputs. For this reason, data should only be latched when XBLNK is low. If data are latched with XBLNK high, the outputs may turn on or off unexpectedly.

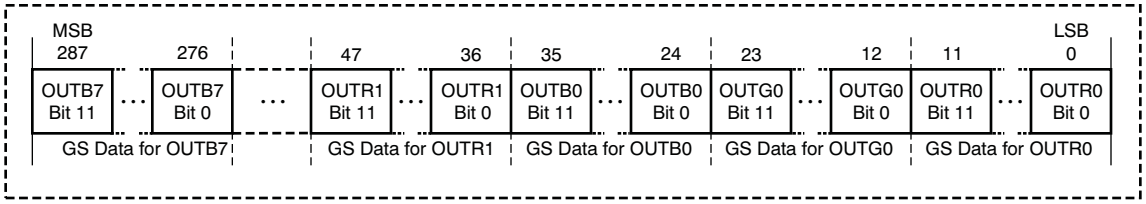


Figure 45. Grayscale Data Latch Configuration

When the IC powers on, the grayscale data latch contains random data. Therefore, grayscale data must be written to the 288-bit common shift register and latched into the GS data latch before turning on the constant-current outputs. XBLNK should be low when powering on the TLC5951 to force all outputs off until the internal registers can be programmed. All constant-current outputs are forced off when XBLNK is low. The data bit assignment is shown in Table 8.

Table 8. Grayscale Data Bit Assignment

BITS	DATA	BITS	DATA
11-0	OUTR0	155-144	OUTR4
23-12	OUTG0	167-156	OUTG4
35-24	OUTB0	179-168	OUTB4
47-36	OUTR1	191-180	OUTR5
59-48	OUTG1	203-192	OUTG5
71-60	OUTB1	215-204	OUTB5
83-72	OUTR2	227-216	OUTR6
95-84	OUTG2	239-228	OUTG6
107-96	OUTB2	251-240	OUTB6
119-108	OUTR3	263-252	OUTR7
131-120	OUTG3	275-264	OUTG7
143-132	OUTB3	287-276	OUTB7

DC/BC/FC/UD Shift Register

The 216-bit DC/BC/FC/UD shift register is used to shift data from the DSSIN pin into the TLC5951. The data shifted into this register are used for the dot correction (DC), global brightness control (BC), function control (FC), and user-defined (UD) data latches. Each of these latches is described in the following sections. The register LSB is connected to DCSIN and the MSB is connected to DCSOUT. On each DCSCK rising edge, the data on DCSIN are shifted into the register LSB and all 216 bits are shifted towards the MSB. The register MSB is always connected to DCOUT. When the IC is powered on, the 216-bit DC/BC/FC/UD shift register contains random data.

DC/BC/FC/UD Data Latch

The 216-bit DC/BC/FC/UD data latch contains dot correction (DC) data, global brightness control (BC) data, function control (FC) data, and user-defined (UD) data. Data can be written into this latch from the DC/BC/FC/UD shift register. Furthermore, DC/BC/FC data can be written into this latch from the 288-bit common shift register. At this time, UD data are written to bits 199-215 in the 216-bit DC/BC/FC/UD shift register data latch. When the IC is powered on, the DC/BC/FC/UD data latch contains random data.

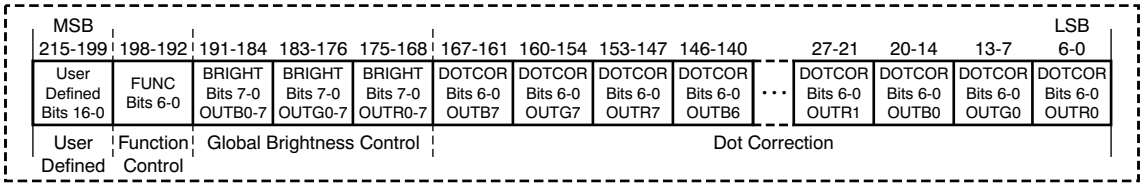


Figure 46. DC/BC/FC/UD Data Latch Configuration

Dot Correction Data Latch

The dot correction (DC) data latch is 168 bits long. The DC data latch consists of bits 0-167 in the DC/BC/FC/UD data latch. This latch contains the 7-bit DC value for each of the TLC5951 constant-current outputs. Each DC value individually adjusts the output current for each constant-current driver. As explained in the *Dot Correction (DC) Function* section, the DC values are used to adjust the output current from 0% to 66.7% of the maximum value when the dot correction low adjustment range is selected and from 33.3% to 100% of the maximum value when the dot correction high adjustment range is selected. The adjustment range is selected by the range control bits in the function control latch.

Table 3 and Table 4 show how the DC data affect the percentage of the maximum current each output. See Figure 46 for the DC data latch configuration. Figure 11 illustrates the timing diagram for writing data from the GS data path into the shift registers and latches. Figure 12 illustrates the timing diagram for writing data from the DC data path into the shift registers and DC latches. DC data are automatically latched from the DC/BC/FC/UD shift register into the DC data latch with an internal latch signal. The internal latch signal is generated in 3 ms to 7 ms after the last DCSCK rising edge.

When the IC powers on, the DC data latch contains random data. Therefore, DC data must be written into the TLC5951 and latched into the DC data latch before turning on the constant-current outputs. XBLNK should be low when powering on the TLC5951 to force all outputs off until the internal registers can be programmed. All constant-current outputs are forced off when XBLNK is low. The data bit assignment is shown in Table 9.

Table 9. Dot Correction Data Bit Assignment

BITS	DATA	BITS	DATA
6-0	OUTR0	90-84	OUTR4
13-7	OUTG0	97-91	OUTG4
20-14	OUTB0	104-98	OUTB4
27-21	OUTR1	111-105	OUTR5
34-28	OUTG1	118-112	OUTG5
41-35	OUTB1	125-119	OUTB5
48-42	OUTR2	132-126	OUTR6
55-49	OUTG2	139-133	OUTG6
62-56	OUTB2	146-140	OUTB6
69-63	OUTR3	153-147	OUTR7
76-70	OUTG3	160-154	OUTG7
83-77	OUTB3	167-161	OUTB7

Global Brightness Control Data Latch

The global brightness control (BC) data latch is 24 bits long. The BC data latch consists of bits 168-191 in the DC/BC/FC/UD data latch.

The data of the BC data latch are used to adjust the constant-current values for eight channel constant-current drivers of each color group. The current can be adjusted from 0% to 100% of each output current adjusted by brightness control with 8-bit resolution. Table 5 describes the percentage of the maximum current for each brightness control data.

When the IC is powered on, the data in the BC data latch are not set to a specific default value. Therefore, brightness control data must be written to the BC latch before turning on the constant-current output. The data bit assignment is shown in Table 10.

Table 10. Data Bit Assignment

BITS	GLOBAL BRIGHTNESS CONTROL DATA BITS 7-0
175-168	OUTR0-OUTR7 group
183-176	OUTG0-OUTG7 group
191-184	OUTB0-OUTB7 group

Function Control Data Latch

The function control (FC) data latch is 7 bits in length and is used to select the dot correction adjustment range, grayscale counter mode, enabling of the auto display repeat, and display timing reset function. When the IC is powered on, the data in the FC latch are not set to a specific default value. Therefore, function control data must be written to the FC data latch before turning on the constant current output.

Table 11. Data Bit Assignment

BIT	DESCRIPTION
192	Dot correction adjustment range for the RED color output (0 = lower range, 1 = higher range). When this bit is '0', dot correction can control the range of constant current by 0% to 66.7% (typ) of the maximum current set by an external resistor. This mode only operates the output for the red LED driver group. When this bit is '1', dot correction can control the range of constant current by 33.3% (typ) to 100% of the maximum current set by an external resistor.
193	Dot correction adjustment range for the GREEN color output (0 = lower range, 1 = higher range). When this bit is '0', dot correction can control the range of constant current by 0% to 66.7% (typ) of the maximum current set by an external resistor. This mode only operates the output for the green LED driver group. When this bit is '1', dot correction can control the range of constant current by 33.3% (typ) to 100% of the maximum current set by an external resistor.
194	Dot correction adjustment range for the BLUE color output (0 = lower range, 1 = higher range). When this bit is '0', dot correction can control the range of constant current by 0% to 66.7% (typ) of the maximum current set by an external resistor. This mode only operates the output for the blue LED driver group. When this bit is '1', dot correction can control the range of constant current by 33.3% (typ) to 100% of the maximum current set by an external resistor.
195	Auto display repeat mode (0 = disabled, 1 = enabled). When this bit is '0', the auto repeat function is disabled. Each output driver is turned on and off once after XBLNK goes high. When this bit is '1', each output driver is repeatedly toggled on/off every 4096th grayscale clock without the XBLNK level changing when the GS counter is configured as a 12-bit mode. If the GS counter is configured as a 10-bit mode, the outputs continue to cycle on/off every 1024th grayscale clock. If the GS counter is set to the 8-bit mode, the output on/off repetition cycles every 256th grayscale clock.
196	Display timing reset mode (0 = disabled, 1 = enabled). When this bit is '1', the GS counter is reset to '0' and all outputs are forced off at the GSLAT rising edge for a GS data write. This function is identical to the low pulse of the XBLNK signal when input. Therefore, the XBLNK signal is not needed to control from a display controller. PWM control starts again from the next input GSCKR/G/B rising edge. When this bit is '0', the GS counter is not reset and no outputs are forced off even if a GSLAT rising edge is input. In this mode, the XBLNK signal should be input after the PWM control of all LED are finished. Otherwise, the PWM control might be not exact.
198, 197	Grayscale counter mode select, bits 1-0. The grayscale counter mode is selected by the setting of bits 1 and 0. Table 12 shows the GS counter mode.

Table 12. GS Counter Mode Truth Table

GRAYSCALE COUNTER MODE		FUNCTION MODE
BIT 1	BIT 0	
0	X (don't care)	12-bit counter mode (maximum output on-time = 4095 × GS clock)
1	0	10-bit counter mode (maximum output on-time = 1023 × GS clock)
1	1	8-bit counter mode (maximum output on-time = 255 × GS clock)

The grayscale data latch bit length is always 288 bits in any grayscale counter mode. All constant-current outputs are forced off at the 256th grayscale clock in the 8-bit mode even if all grayscale data are FFFh. In 10-bit mode, all outputs are forced off at 1024th grayscale clock even if all grayscale data are FFFh.

User-Defined Data Latch

The user-defined (UD) data latch is 17 bits in length and is not used for any device functionality. However, these data can be used for communication between a controller connected to DCSIN and another controller connected to GSSIN. When the IC is powered on, the data in the UD latch are not set to a specific default value.

Table 13. Data Bit Assignment

BITS	USER-DEFINED DATA BITS
215-199	16-0

STATUS INFORMATION DATA (SID)

Status information data (SID) are 288 bits in length and are read-only data. SID consists of the LED open detection (LOD) error, LED short detection (LSD), thermal error flag (TEF), and the data in the DC/BC/FC/UD data latch. The SID are shifted out onto GSSOUT with the GSSCK rising edge after GSLAT is input for a GS data write. These SID are loaded into the 288-bit common shift register after data in the 288-bit common shift register are copied to the data latch.

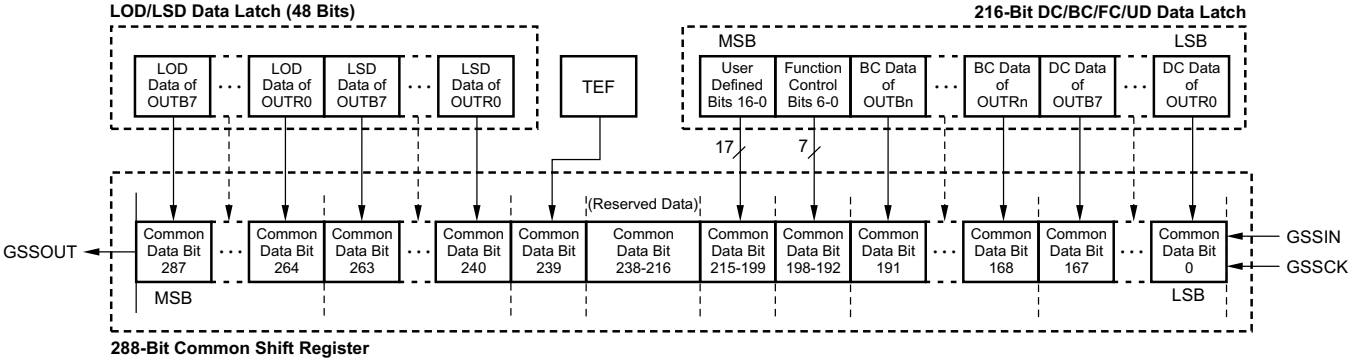


Figure 47. DC/BC/FC Data Load Assignment

Table 14. Data Bit Assignment

BITS	DESCRIPTION
6-0	Dot correction data bits 6-0 for OUTR0
13-7	Dot correction data bits 6-0 for OUTG0
20-14	Dot correction data bits 6-0 for OUTB0
27-21	Dot correction data bits 6-0 for OUTR1
34-28	Dot correction data bits 6-0 for OUTG1
41-35	Dot correction data bits 6-0 for OUTB1
48-42	Dot correction data bits 6-0 for OUTR2
55-49	Dot correction data bits 6-0 for OUTG2
62-56	Dot correction data bits 6-0 for OUTB2
69-63	Dot correction data bits 6-0 for OUTR3
76-70	Dot correction data bits 6-0 for OUTG3
83-77	Dot correction data bits 6-0 for OUTB3
90-84	Dot correction data bits 6-0 for OUTR4
97-91	Dot correction data bits 6-0 for OUTG4
104-98	Dot correction data bits 6-0 for OUTB4
111-105	Dot correction data bits 6-0 for OUTR5
118-112	Dot correction data bits 6-0 for OUTG5
125-119	Dot correction data bits 6-0 for OUTB5
132-126	Dot correction data bits 6-0 for OUTR6
139-133	Dot correction data bits 6-0 for OUTG6
146-140	Dot correction data bits 6-0 for OUTB6
153-147	Dot correction data bits 6-0 for OUTR7
160-154	Dot correction data bits 6-0 for OUTG7
167-161	Dot correction data bits 6-0 for OUTB7
175-168	Global brightness control data bits 7-0 for OUTR0-OUTR7 group
183-176	Global brightness control data bits 7-0 for OUTG0-OUTG7 group
191-184	Global brightness control data bits 7-0 for OUTB0-OUTB7 group
198-192	Function control data bits 6-0
215-199	User-defined data bits 16-0
238-216	Reserved for TI test
239	Thermal error flag (TEF) 1 = High temperature condition, 0 = Normal temperature condition
247-240	LED short detection (LSD) data for OUTR7-OUTR0 1 = LED is short, 0 = Normal operation
255-248	LSD data for OUTG7-OUTG0 1 = LED is short, 0 = Normal operation
263-256	LSD data for OUTB7-OUTB0 1 = LED is short, 0 = Normal operation
271-264	LED open detection (LOD) data for OUTR7-OUTR0 1 = LED is open or connected to GND, 0 = Normal operation
279-272	LOD data for OUTG7-OUTG0 1 = LED is open or connected to GND, 0 = Normal operation
287-280	LOD data for OUTB7-OUTB0 1 = LED is open or connected to GND, 0 = Normal operation

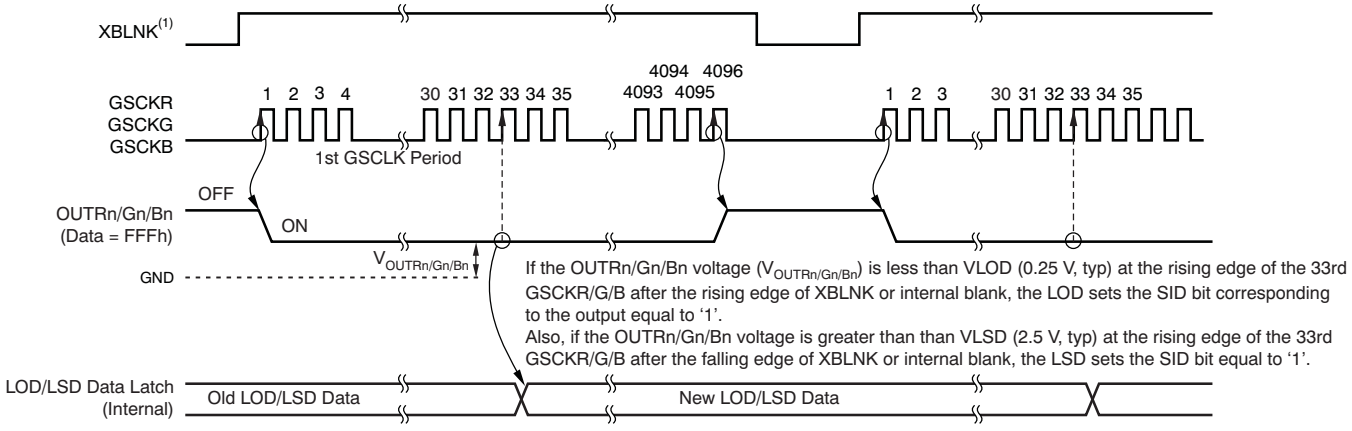
CONTINUOUS BASE LOD, LSD, AND TEF

The LOD/LSD data are updated at the rising edge of the 33rd GSCKR/G/B pulse after XBLNK goes high and the data are retained until the next 33rd GSCKR/G/B. LOD/LSD data are valid when GS data are equal to or higher than 20h (32d). If GS data are less than 20h (32d), LOD/LSD data are not valid and must be ignored. A '1' in an LOD bit indicates an open LED or shorted LED to GND with a low-impedance condition for the corresponding output. A '0' indicates normal operation. A '1' in an LSD bit indicates a shorted LED condition for the corresponding output. A '0' indicates normal operation. When the device is powered on, LOD/LSD data do not show correct values. Therefore, LOD/LSD data must be read from the 33rd GSCKR/G/B pulse input after XBLNK goes high.

The TEF bit indicates that the device temperature is too high. The TEF flag also indicates that the device has turned off all drivers to avoid damage by overheating the device. A '1' in the TEF bit means that the device temperature has exceeded the detect temperature threshold (T_{TEF}) and all outputs are turned off. A '0' in the TEF bit indicates normal operation with normal temperature conditions. The device automatically turns the drivers back on when the device temperature decreases to less than (T_{TEF} – T_{HYST}). Table 15 shows a truth table for LOD/LSD and TEF.

Table 15. LOD/LSD/TEF Truth Table

SID DATA	CONDITION		
	LED OPEN DETECTION (LODn)	LED SHORT DETECTION (LSDn)	THERMAL ERROR FLAG (TEF)
0	LED is not opened ($V_{OUTRn/Gn/Bn} > V_{LOD}$)	LED is not shorted ($V_{OUTRn/Gn/Bn} \le V_{LSD}$)	Device temperature is lower than high-side detect temperature (Temperature $\le T_{TEF}$)
1	LED is open or shorted to GND ($V_{OUTRn/Gn/Bn} \le V_{LOD}$)	LED is shorted between anode and cathode or shorted to higher voltage side ($V_{OUTRn/Gn/Bn} > V_{LSD}$)	Device temperature is higher than high-side detect temperature and driver is forced off (Temperature > T_{TEF})

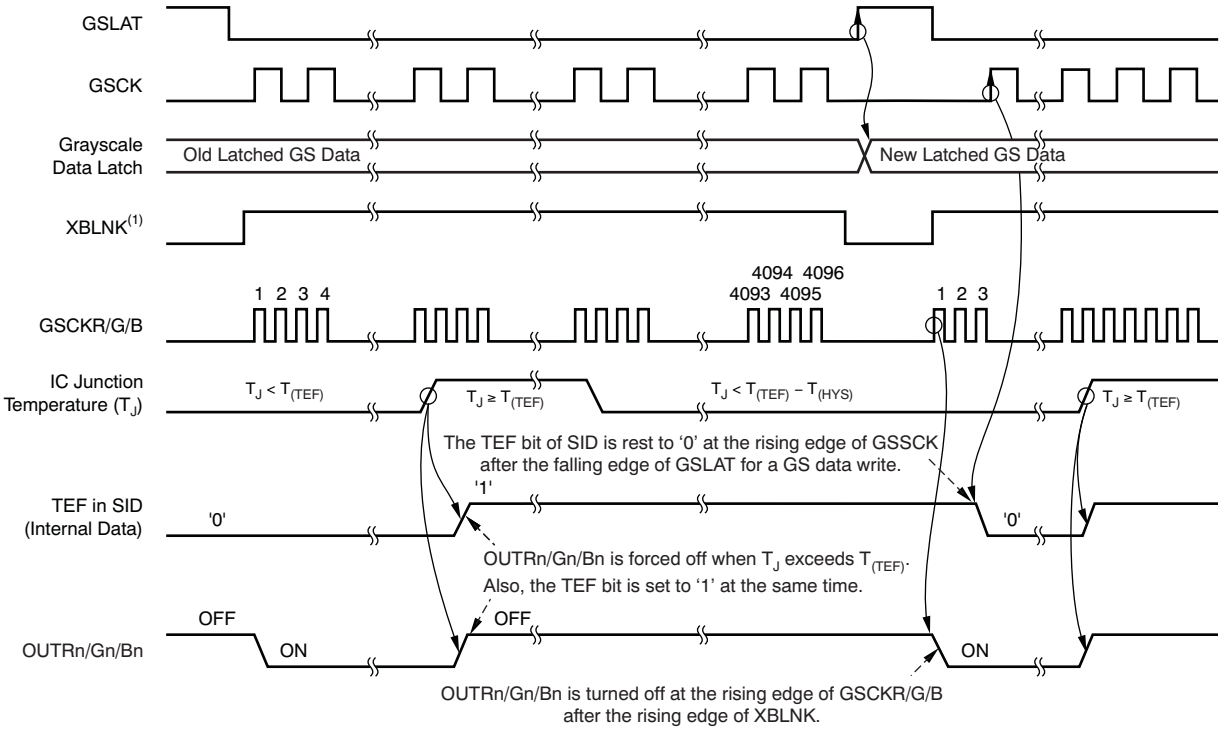


(1) The internal blank signal is generated when GSLAT is input for GS data with display timing reset enabled. Also, the signal is generated at the 4096th GSCK when auto repeat mode is enabled. XBLNK can be connected to VCC when the display timing reset or auto repeat is enabled.

Figure 48. LED Open Detection (LOD) LED Shorted Detection Data Update Timing

THERMAL SHUTDOWN AND THERMAL ERROR FLAG

The thermal shutdown (TSD) function turns off all constant-current outputs on the IC when the junction temperature (T_J) exceeds the threshold (T_{TEF} = +163°C, typ) and sets the thermal error flag (TEF) to '1'. All outputs are latched off when TEF is set to '1' and remain off until the next grayscale cycle after XBLNK goes high and the junction temperature drops below (T_{TEF} – T_{HYST}). TEF remains as '1' until GSLAT is input with low temperature. TEF is set to '0' once the junction temperature drops below (T_{TEF} – T_{HYST}), but the output does not turn on until the first GSCKR/G/B in the next display period even if TEF is set to '0'.



(1) The following internal signal also works to turn the constant outputs on as same as XBLNK inputting. The internal blank signal is generated when GSLAT is input for GS data with display timing reset enabled. Also, the signal is generated at the 4096th GSCKR/G/B when auto repeat mode is enabled. XBLNK can be connected to VCC when the display timing reset or auto repeat is enabled.

Figure 49. TEF/TSD Timing

NOISE REDUCTION

Large surge currents may flow through the IC and the board on which the device is mounted if all 24 outputs turn on simultaneously at the start of each grayscale cycle. These large current surges could induce detrimental noise and electromagnetic interference (EMI) into other circuits. The TLC5951 turns the outputs on in a series delay for each group independently to provide a circuit soft-start feature. The output current sinks are grouped into four groups in each color group. For example, for the RED color output, the first grouped outputs that are turned on/off are OUTR0 and OUTR4. The second grouped outputs that are turned on/off are OUTR1 and OUTR5. The third grouped outputs are OUTR2 and OUTR6 and the fourth grouped outputs are OUTR3 and OUTR7. Each grouped output is turned on and off sequentially with a small delay between groups. However, each color output on and off is controlled by the color grayscale clock.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (August 2013) to Revision D — **Page**

- Added ΔI_{OLC5} and ΔI_{OLC6} parameters to Electrical Characteristics table 5
- Added footnote 6 to footnote 9 in Electrical Characteristics table 5

Changes from Revision B (December 2009) to Revision C — **Page**

- Changed AC Characteristics, T_{WH0}/T_{WL0} parameter associated pin names 3
- Updated Figure 10 14
- Updated Figure 11 15
- Updated Figure 14 17
- Updated Figure 40 21
- Updated Figure 47 33
- Changed description of *Continuous Base LOD, LSD, and TEF* section 35

Changes from Revision A (April 2009) to Revision B — **Page**

- Changed product status from mixed to production data 1
- Changed TLC5951 RHA package status to production data 2
- Deleted footnote 2 from *Ordering Information* table 2
- Changed test conditions of t_{D8} in *Switching Characteristics* table 7
- Deleted footnote 1 from RHA pinout 9
- Changed header for second column in Table 10 31
- Changed description for bits 175-168, 183-176, and 191-184 in Table 14 34

Changes from Original (March 2009) to Revision A — **Page**

- Changed T_{SU3} minimum specification to 40 ns in the *Recommended Operating Conditions* table 3
- Changed V_O minimum specification to maximum specification in the *Recommended Operating Conditions* table 3
- Changed I_{OH} minimum specification to maximum specification in the *Recommended Operating Conditions* table 3
- Changed I_{OL} minimum specification to maximum specification in the *Recommended Operating Conditions* table 3
- Changed I_{OLC} minimum specification to maximum specification in the *Recommended Operating Conditions* table 3
- Changed $f_{CLK\ (SCLK)}$ minimum specification to maximum specification in the *Recommended Operating Conditions* table 3
- Changed $f_{CLK\ (GSCKR/G/B)}$ minimum specification to maximum specification in the *Recommended Operating Conditions* table 3
- Changed I_{CC2} typical value to 6 mA in the *Electrical Characteristics* table 4
- Changed I_{CC3} typical value to 12 mA and maximum value to 27 mA in the *Electrical Characteristics* table 4
- Changed I_{CC4} typical value to 21 mA and maximum value to 55 mA in the *Electrical Characteristics* table 4
- Changed ΔI_{OLC2} typical value to ±1% in the *Electrical Characteristics* table 4
- Changed ΔI_{OLC3} typical value to ±0.5% in the *Electrical Characteristics* table 4
- Changed t_{R0} typical value to 6 ns in the *Switching Characteristics* table 7
- Changed t_{F0} typical value to 6 ns in the *Switching Characteristics* table 7
- Changed fourth paragraph of *Maximum Constant Sink Current Value* section to reference correct graph 22
- Changed DC function adjustment range description to reflect proper adjustment range for each control in *Dot Correction (DC) Function* section 22

- Changed *brightness control* to *dot correction data* in *288-Bit Common Shift Register* section 29
- Corrected number of bits contained within the DC/BC/FC/UD shift register in the *DC/BC/FC/UD Shift Register* section 30
- Corrected typo about which bits are written in the *DC/BC/FC/UD Data Latch* section 30
- Corrected percentage of adjustment rage selected in the *Dot Correction Data Latch* section 30
- Deleted second paragraph of *Status Information Data (SID)* section 33
- Updated LOD bit = '1' condition description in the *Continuous Base LOD, LSD, and TEF* section 35

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC5951DAP	ACTIVE	HTSSOP	DAP	38	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5951	Samples
TLC5951DAPR	ACTIVE	HTSSOP	DAP	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5951	Samples
TLC5951RHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC 5951	Samples
TLC5951RHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC 5951	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

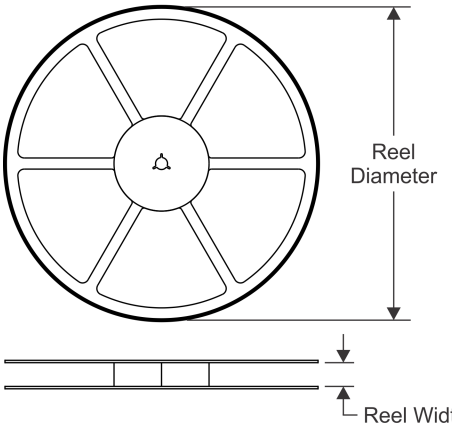
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

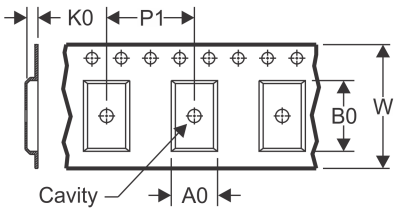
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

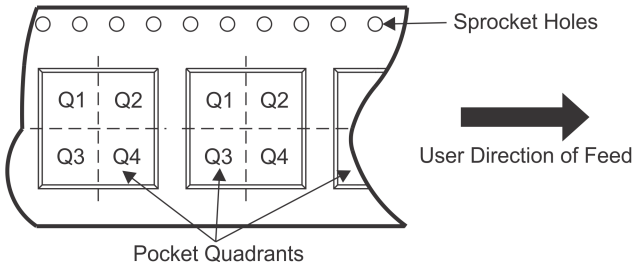


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

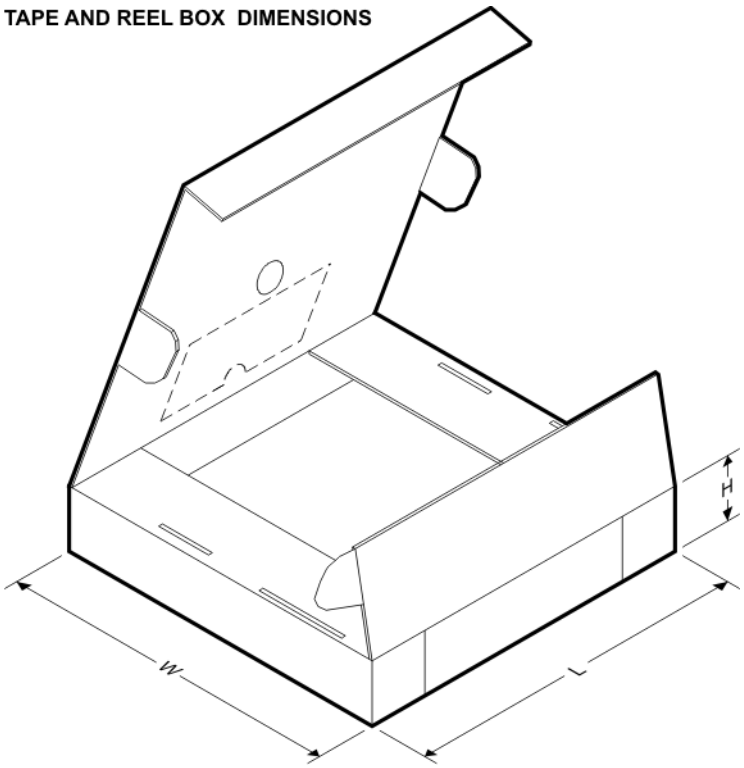
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5951RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TLC5951RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

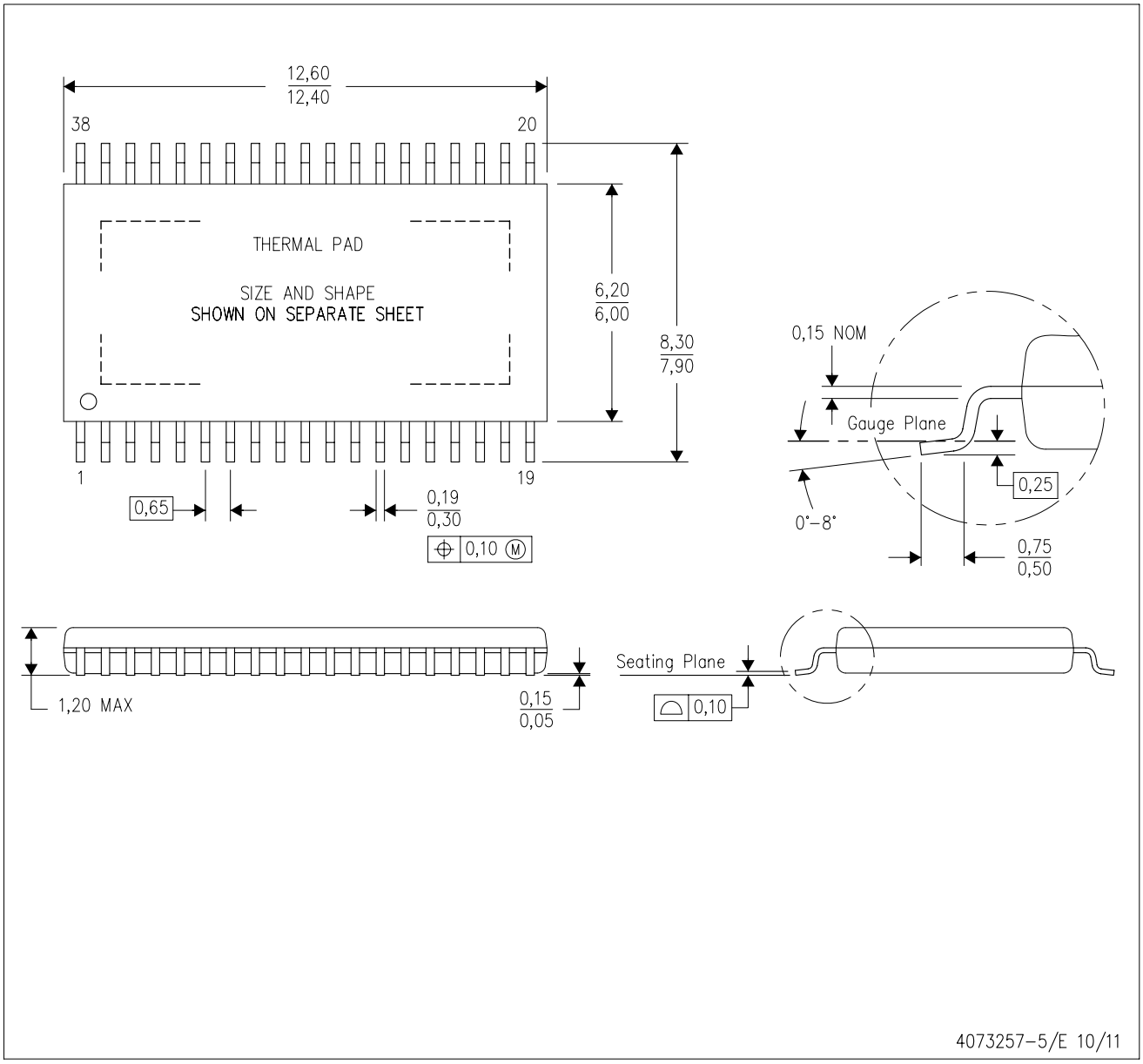
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5951RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
TLC5951RHAT	VQFN	RHA	40	250	210.0	185.0	35.0

DAP (R–PDSO–G38) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153 Variation DDT–1.

PowerPAD is a trademark of Texas Instruments.

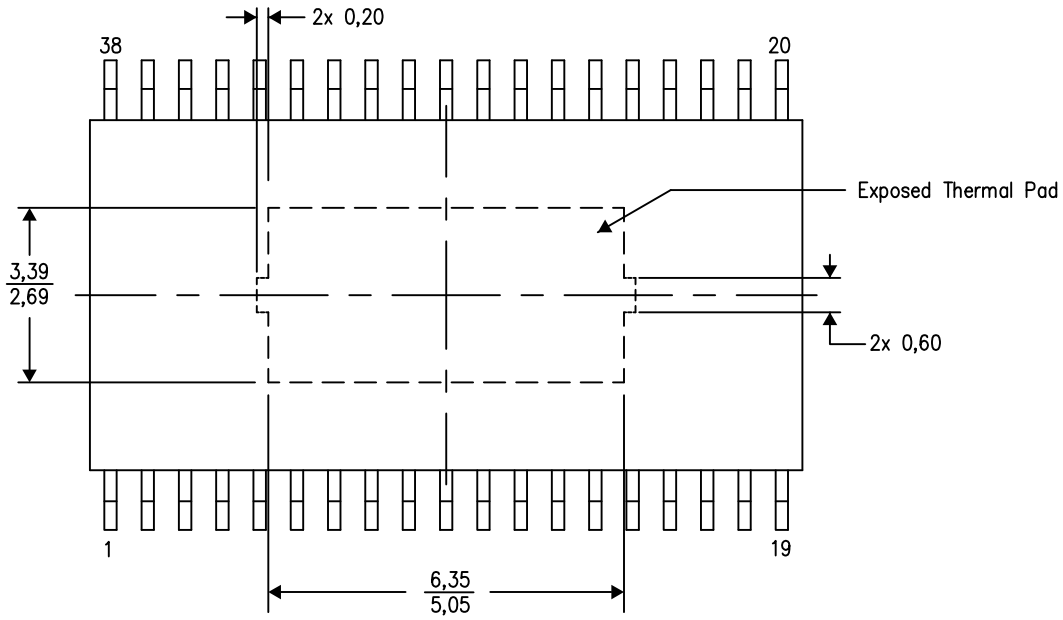
DAP (R–PDSO–G38) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

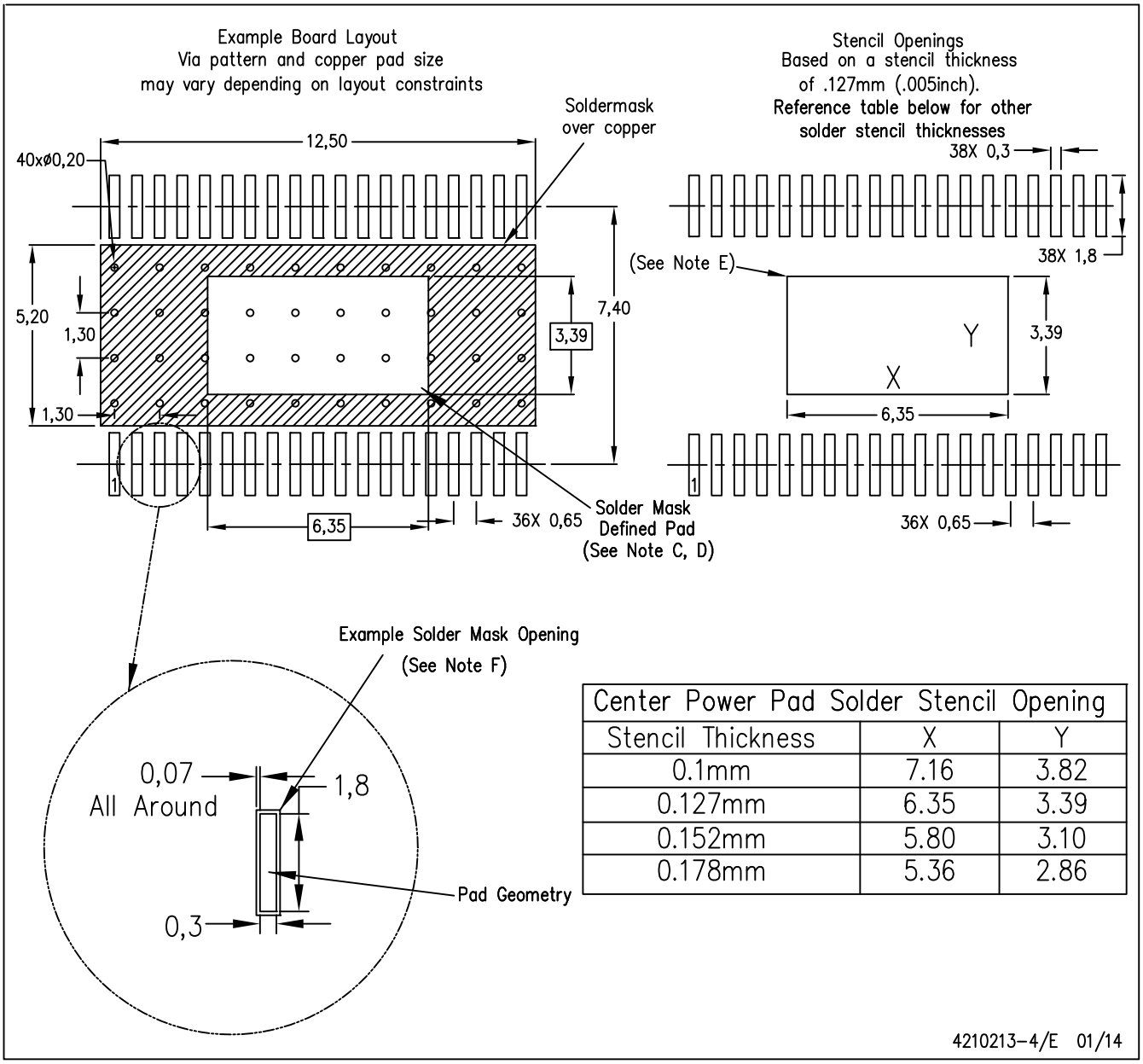
Exposed Thermal Pad Dimensions

4206319–7/M 09/13

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

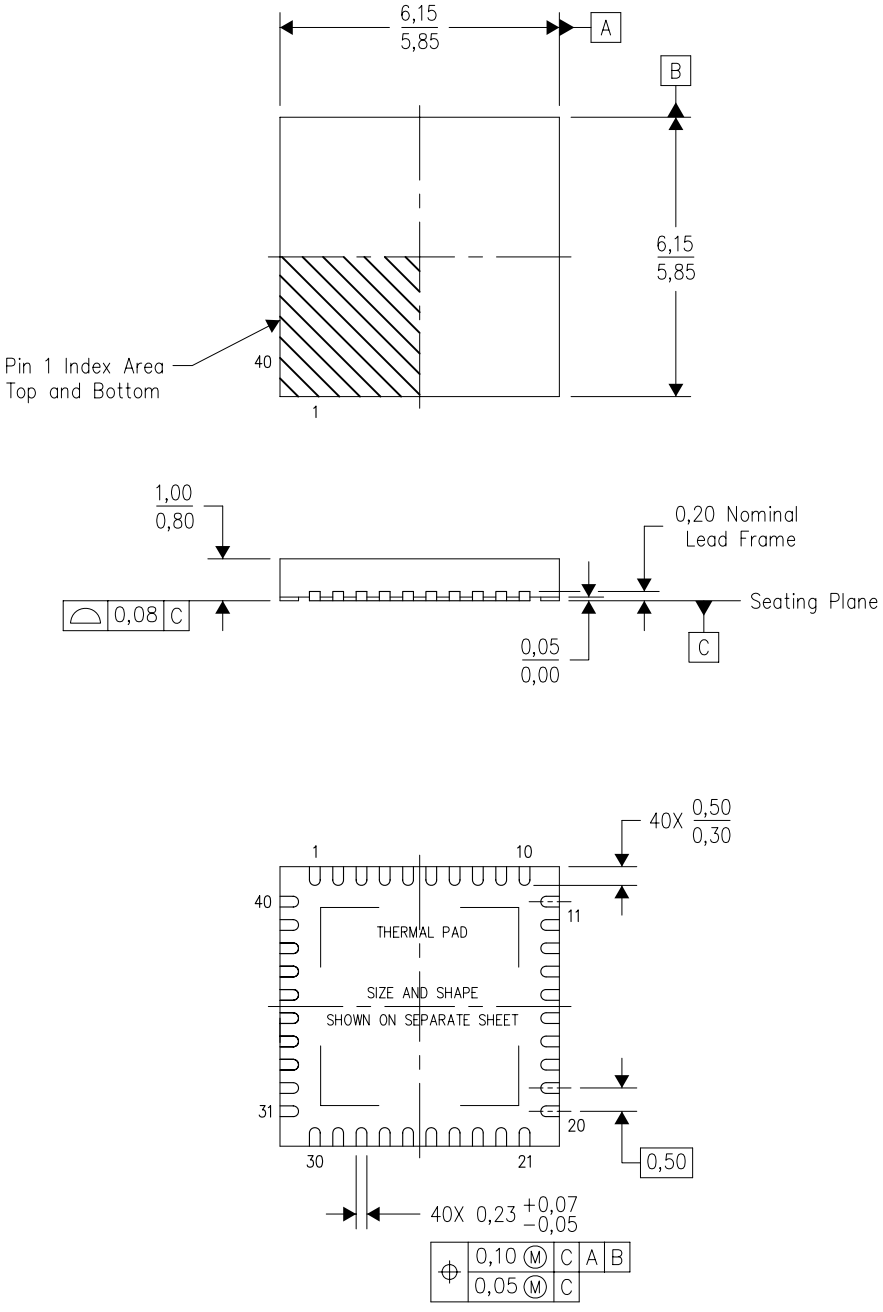
DAP (R–PDSO–G38) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	7.16	3.82
0.127mm	6.35	3.39
0.152mm	5.80	3.10
0.178mm	5.36	2.86

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
F. Contact the board fabrication site for recommended soldermask tolerances.

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



Bottom View

4204276/E 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220 variation VJJD–2.

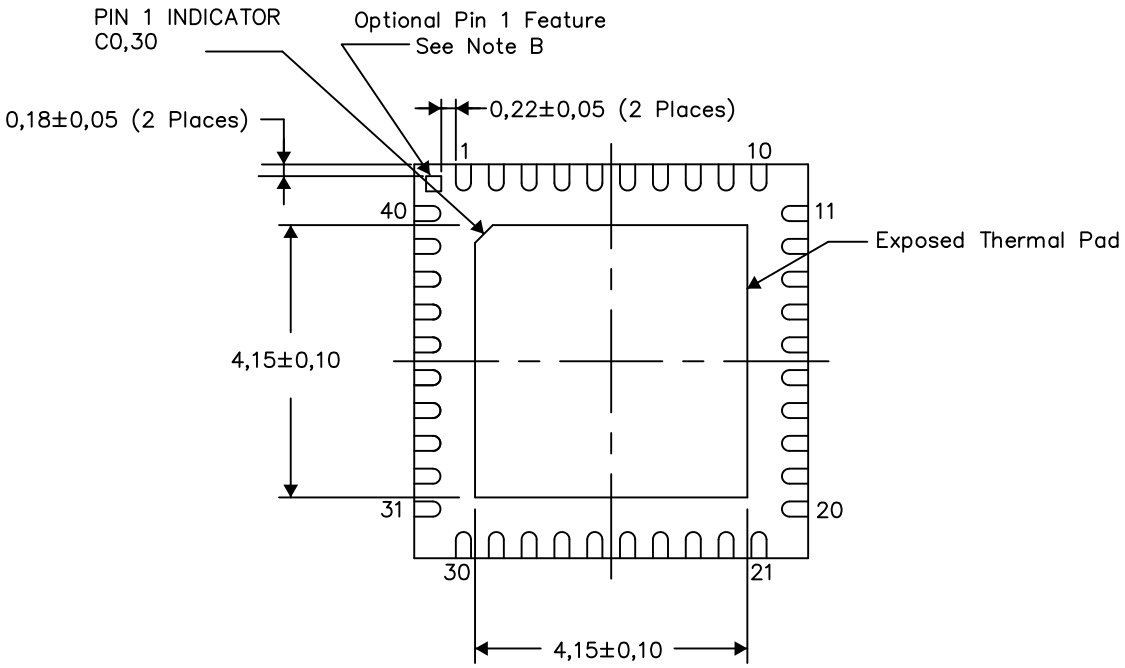
RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

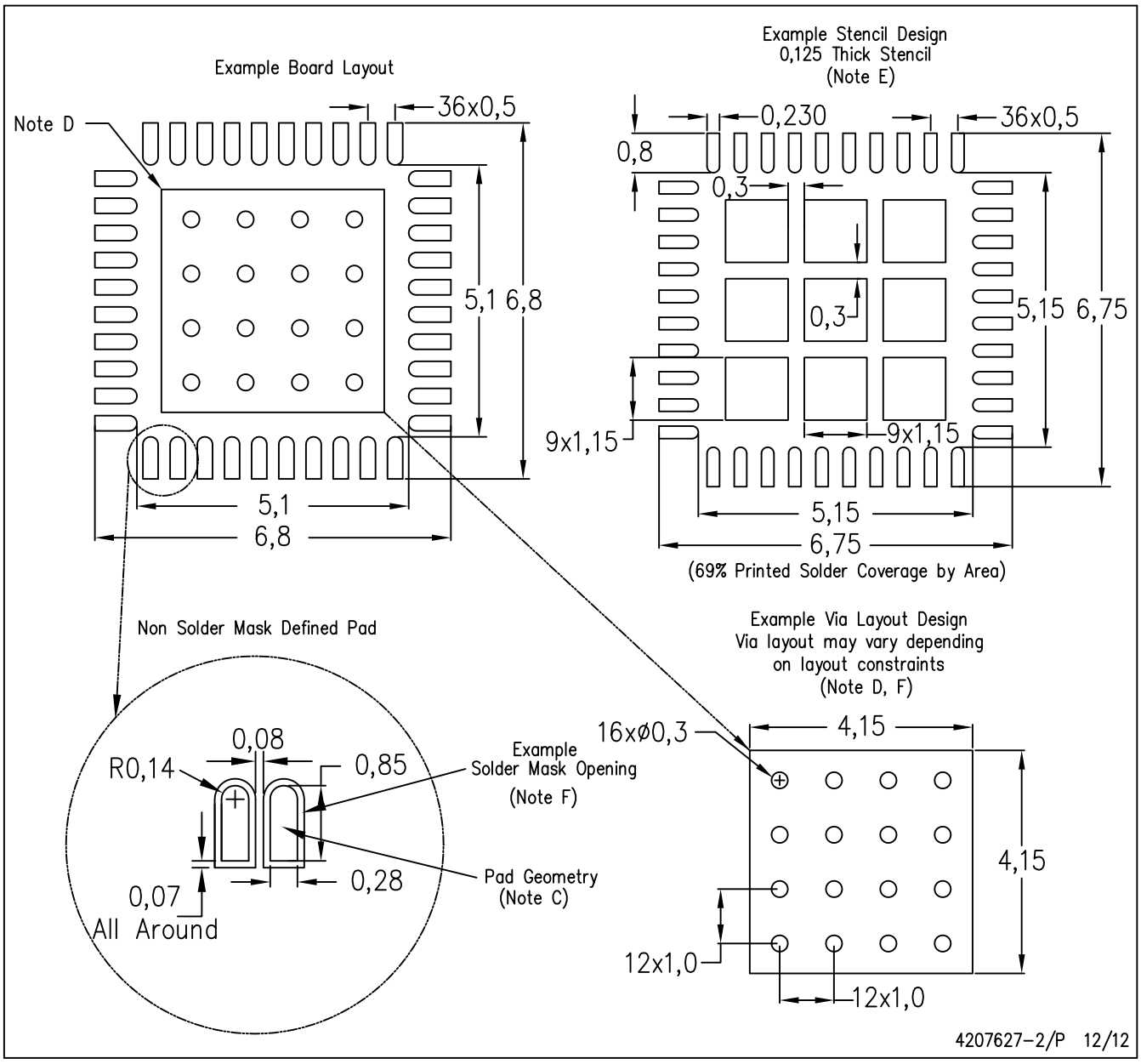
Exposed Thermal Pad Dimensions

4206355–2/U 12/12

NOTES: A. All linear dimensions are in millimeters

B. The Pin 1 Identification mark is an optional feature that may be present on some devices In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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