

2N7002BKV

60 V, 340 mA dual N-channel Trench MOSFET

Rev. 2 — 22 September 2010

Product data sheet

1. Product profile

1.1 General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in an ultra small SOT666 Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Logic-level compatible
- Very fast switching
- Trench MOSFET technology
- ESD protection up to 2 kV
- AEC-Q101 qualified

1.3 Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DS}	drain-source voltage	$T_{amb} = 25 ^{\circ}C$	-	-	60	V
V_{GS}	gate-source voltage	T _{amb} = 25 °C	-	-	±20	V
I _D	drain current	T_{amb} = 25 °C; V_{GS} = 10 V	[1] -	-	340	mA
R _{DSon}	drain-source on-state resistance	$T_j = 25 ^{\circ}\text{C};$ $V_{GS} = 10 \text{V};$ $I_D = 500 \text{mA}$	-	1	1.6	Ω

^[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².



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2. Pinning information

Table 2. **Pinning** Simplified outline Pin **Symbol** Description 1 S1 source 1 2 G1 gate 1 3 D2 drain 2 4 S2 source 2 5 G2 gate 2 6 D1 drain 1

017aaa055

Graphic symbol

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
2N7002BKV	-	plastic surface-mounted package; 6 leads	SOT666

4. Marking

Table 4. Marking codes

3	
Type number	Marking code
2N7002BKV	ZG

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

		• • • • • • • • • • • • • • • • • • • •	•		
Symbol	Parameter	Conditions	Min	Max	Unit
Per trans	sistor				
V_{DS}	drain-source voltage	T _{amb} = 25 °C	-	60	V
V_{GS}	gate-source voltage	T _{amb} = 25 °C	-	±20	V
I _D	drain current	V _{GS} = 10 V	<u>[1]</u>		
		T _{amb} = 25 °C	-	340	mA
		T _{amb} = 100 °C	-	240	mA
I _{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \le 10$ μs	-	1.2	Α

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 Table 5.
 Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
P _{tot}	total power dissipation	$T_{amb} = 25 ^{\circ}C$	[2] -	350	mW
			<u>[1]</u> -	410	mW
		T _{sp} = 25 °C	-	1140	mW
Source-di	rain diode				
Is	source current	T _{amb} = 25 °C	<u>[1]</u> -	340	mA
ESD max	imum rating				
V_{ESD}	electrostatic discharge voltage	human body model	[3] _	2000	V
Per devic	e				
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	525	mW
Tj	junction temperature			150	°C
T _{amb}	ambient temperature		-55	+150	°C
T _{stg}	storage temperature		-65	+150	°C
· · · · · · · · · · · · · · · · · · ·			·	•	·

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [3] Measured between all pins.

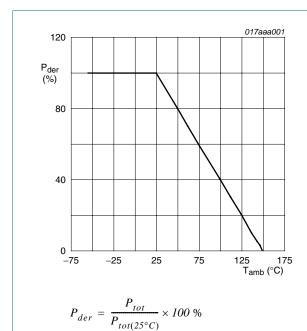
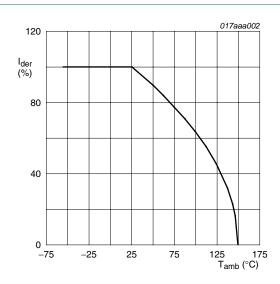


Fig 1. Normalized total power dissipation as a function of ambient temperature

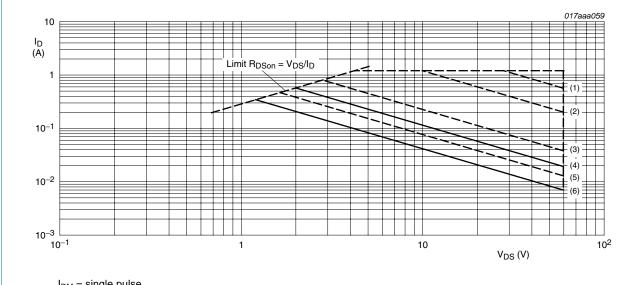


$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$

Fig 2. Normalized continuous drain current as a function of ambient temperature

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I_{DM} = single pulse

- (1) $t_p = 100 \mu s$
- (2) $t_p = 1 \text{ ms}$
- (3) $t_p = 10 \text{ ms}$
- (4) DC; $T_{sp} = 25 \, ^{\circ}C$
- (5) $t_p = 100 \text{ ms}$
- (6) DC; $T_{amb} = 25 \, ^{\circ}C$; drain mounting pad 1 cm²

Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

Thermal characteristics

Table 6. **Thermal characteristics**

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Per transis	stor					
$R_{th(j-a)}$ thermal resistance from junction to ambient	thermal resistance from	in free air	<u>[1]</u> -	315	360	K/W
		[2] _	265	305	K/W	
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	110	K/W
Per device						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	<u>[1]</u> -	-	240	K/W

^[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

^[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².

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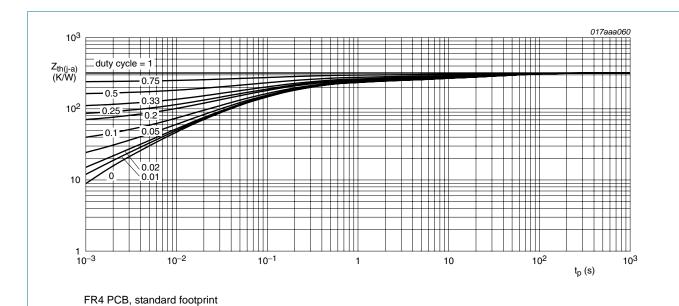
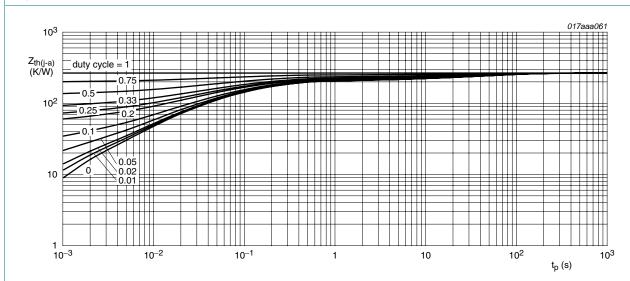


Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 1 cm²

Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

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7. Characteristics

Table 7. Characteristics

 $T_i = 25$ °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	racteristics					
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10 \ \mu A; \ V_{GS} = 0 \ V$	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 250 \ \mu A; \ V_{DS} = V_{GS}$	1.1	1.6	2.1	V
I _{DSS}	drain leakage current	$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}$				
		T _j = 25 °C	-	-	1	μΑ
		T _j = 150 °C	-	-	10	μΑ
I _{GSS}	gate leakage current	$V_{GS} = \pm 20 \text{ V}; V_{DS} = 0 \text{ V}$	-	-	10	μΑ
R _{DSon}	drain-source on-state resistance		<u>[1]</u>			
		$V_{GS} = 5 \text{ V}; I_D = 50 \text{ mA}$	-	1.3	2	Ω
		$V_{GS} = 10 \text{ V}; I_D = 500 \text{ mA}$	-	1	1.6	Ω
9fs	forward transconductance	$V_{DS} = 10 \text{ V}; I_D = 200 \text{ mA}$	[1] _	550	-	mS
Dynamic (characteristics					
Q _{G(tot)}	total gate charge	I _D = 300 mA;	-	0.5	0.6	nC
Q_{GS}	gate-source charge	V _{DS} = 30 V; - V _{GS} = 4.5 V	-	0.2	-	nC
Q_{GD}	gate-drain charge	VGS = 4.5 V	-	0.1	-	nC
C _{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 10 \text{ V};$	-	33	50	pF
Coss	output capacitance	f = 1 MHz	-	7	-	pF
C _{rss}	reverse transfer capacitance		-	4	-	pF
t _{d(on)}	turn-on delay time	V _{DD} = 50 V;	-	5	10	ns
t _r	rise time	$R_L = 250 \Omega;$	-	6	-	ns
t _{d(off)}	turn-off delay time	$-V_{GS} = 10 \text{ V};$ $R_G = 6 \Omega$	-	12	24	ns
t _f	fall time		-	7	-	ns
Source-dr	ain diode					
V _{SD}	source-drain voltage	$I_S = 115 \text{ mA}; V_{GS} = 0 \text{ V}$	0.47	0.75	1.1	V

^[1] Pulse test: $t_p \le 300~\mu s;~\delta \le 0.01.$

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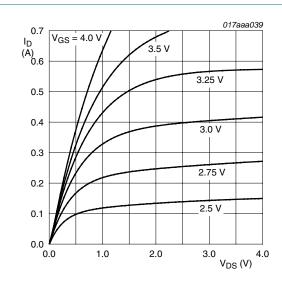
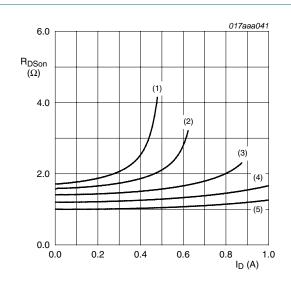


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



T_{amb} = 25 °C

 $T_{amb} = 25 \, ^{\circ}C$

(1) $V_{GS} = 3.25 \text{ V}$

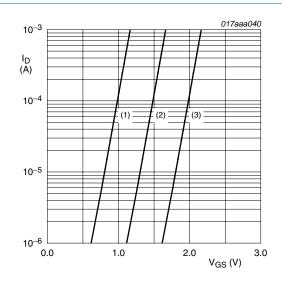
(2) $V_{GS} = 3.5 \text{ V}$

(3) $V_{GS} = 4 V$

(4) $V_{GS} = 5 \text{ V}$

(5) $V_{GS} = 10 \text{ V}$

Fig 8. Drain-source on-state resistance as a function of drain current; typical values



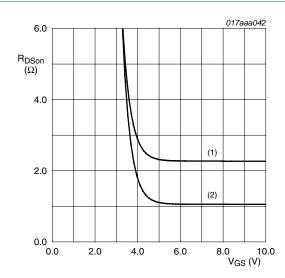
 T_{amb} = 25 °C; V_{DS} = 5 V

(1) minimum values

(2) typical values

(3) maximum values

Fig 7. Sub-threshold drain current as a function of gate-source voltage



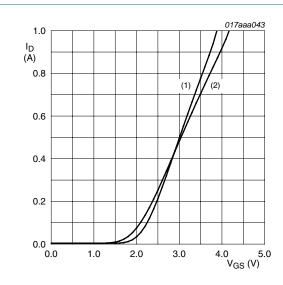
 $I_D = 500 \text{ mA}$

(1) $T_{amb} = 150 \, ^{\circ}C$

(2) $T_{amb} = 25 \, ^{\circ}C$

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

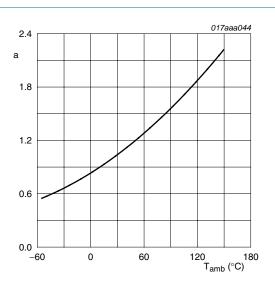
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$$V_{DS} > I_D \times R_{DSon}$$

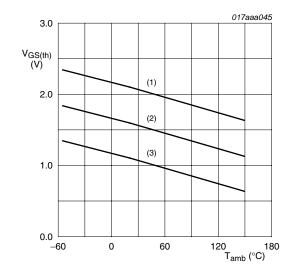
- (1) $T_{amb} = 25 \, ^{\circ}C$
- (2) $T_{amb} = 150 \, ^{\circ}C$

Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

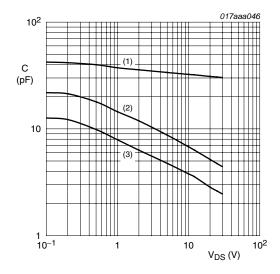
Fig 11. Normalized drain-source on-state resistance as a function of ambient temperature; typical values



 $I_D = 0.25 \text{ mA}; V_{DS} = V_{GS}$

- (1) maximum values
- (2) typical values
- (3) minimum values

Fig 12. Gate-source threshold voltage as a function of ambient temperature

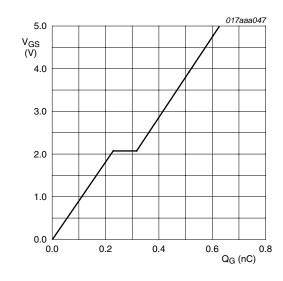


 $f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$

- (1) C_{iss}
- (2) C_{oss}
- (3) C_{rss}

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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 I_D = 300 mA; V_{DD} = 6 V; T_{amb} = 25 °C

Fig 14. Gate-source voltage as a function of gate charge; typical values

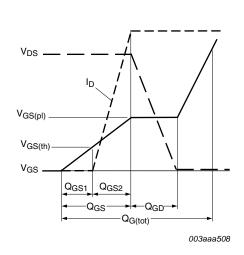
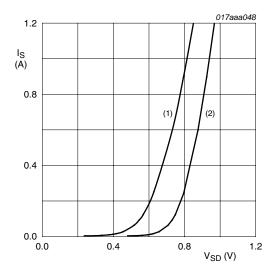


Fig 15. Gate charge waveform definitions



 $V_{GS} = 0 V$

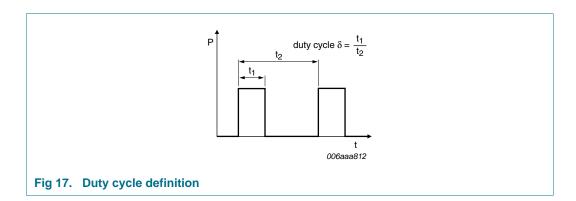
(1) $T_{amb} = 150 \, ^{\circ}C$

(2) $T_{amb} = 25 \, ^{\circ}C$

Fig 16. Source current as a function of source-drain voltage; typical values

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8. Test information



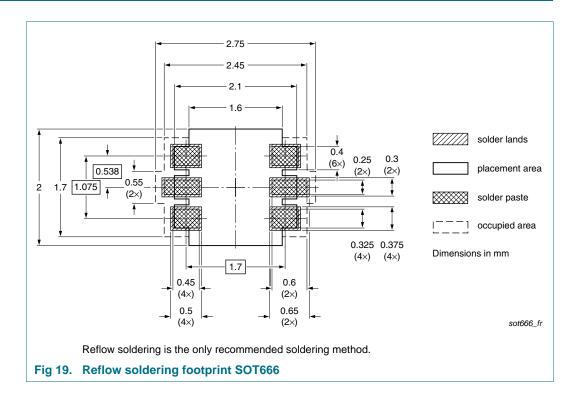
9. Package outline

SOT666 Plastic surface-mounted package; 6 leads - A Х pin 1 index С - w M A detail X 2 mm scale **DIMENSIONS (mm are the original dimensions)** UNIT Ε D Α bp С e₁ H_{E} L_p у 0.6 0.27 1.7 1.5 1.7 1.5 0.3 0.1 0.18 1.3 1.0 0.5 0.17 0.08 1.1 REFERENCES **EUROPEAN** OUTLINE ISSUE DATE VERSION JEDEC **PROJECTION** IEC JEITA 04-11-08 SOT666 06-03-16

Fig 18. Package outline SOT666

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10. Soldering



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11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
2N7002BKV v.2	20100922	Product data sheet	-	2N7002BKV v.1
Modifications:	• Table 6 "The	ning": graphic symbol ame ermal characteristics": typo ermal characteristics": typo	for $R_{th(j-sp)}$ maximum va	lue per transistor amended ue per device amended
2N7002BKV v.1	20100610	Product data sheet	-	-

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12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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