



20-MHz, Low-Noise, 1.8-V, RRI/O, CMOS Operational Amplifier With Shutdown

Check for Samples: [OPA322-Q1](#), [OPA322S-Q1](#), [OPA2322-Q1](#), [OPA2322S-Q1](#), [OPA4322-Q1](#), [OPA4322S-Q1](#)

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
 - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
 - Device HBM ESD Classification Level H3A
 - Device CDM ESD Classification Level C5
- Gain Bandwidth: 20 MHz
- Low Noise: 8.5 nV/ $\sqrt{\text{Hz}}$ at 1 kHz
- Slew Rate: 10 V/ μs
- Low THD+N: 0.0005%
- Rail-to-Rail I/O
- Offset Voltage: 2 mV (max)
- Supply Voltage: 1.8 V to 5.5 V
- Supply Current: 1.5 mA/ch
 - Shutdown: 0.1 μA /ch
- Unity-Gain Stable
- Small Packages:
 - SOT23, DFN, MSOP, TSSOP

APPLICATIONS

- Automotive
- Sensor Signal Conditioning
- Consumer Audio
- Multi-Pole Active Filters
- Control-Loop Amplifiers
- Communications
- Security
- Scanners

DESCRIPTION

The OPA322-Q1 family consists of single, dual, and quad-channel CMOS operational amplifiers featuring low noise and rail-to-rail inputs/outputs optimized for low-power, single-supply applications. Specified over a wide supply range of 1.8 V to 5.5 V, and with a low quiescent current of only 1.5 mA per channel, these devices are well-suited for power-sensitive applications.

The combination of very low noise (8.5 nV/ $\sqrt{\text{Hz}}$ at 1 kHz), high gain-bandwidth (20 MHz), and fast slew rate (10 V/ μs) make the OPA322-Q1 family ideal for a wide range of applications, including signal conditioning and sensor amplification requiring high gains. Featuring low THD+N, the OPA322-Q1 family is also excellent for consumer audio applications, particularly for single-supply systems.

The OPAx322S-Q1 models include a shutdown mode allowing the amplifiers to switch from normal operation to a standby current that is typically less than 0.1 μA .

The OPA322-Q1 (single version) is available in SOT23-5 and SOT23-6, whereas the OPA2322 (dual version) comes in MSOP-8, MSOP-10, SO-8, and DFN-8 packages. The quad versions OPA4322 come in TSSOP-14 and TSSOP-16 packages. The specification on all versions is for operation from –40°C to 125°C.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range, unless otherwise noted.

		OPA322-Q1, OPA322S-Q1, OPA2322-Q1, OPA2322S-Q1, OPA4322-Q1, OPA4322S-Q1	UNIT
Supply voltage, $V_S = (V+) - (V-)$		6	V
Signal input pins	Voltage ⁽²⁾	$(V-) - 0.5$ to $(V+) + 0.5$	V
	Current ⁽²⁾	± 10	mA
Output short-circuit current ⁽³⁾		Continuous	mA
Operating temperature, T_A		-40 to 125	°C
Storage temperature, T_{stg}		-65 to 150	°C
Junction temperature, T_J		150	°C
ESD ratings	Human-body model (HBM) AEC-Q100 Classification Level H3A	4	kV
	Charged-device model (CDM) AEC-Q100 Classification Level C5	1000	V

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute-maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.

THERMAL INFORMATION: OPA322-Q1

THERMAL METRIC ⁽¹⁾		OPA322-Q1	OPA322S-Q1	UNIT
		DBV	DBV	
		5 PINS	6 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	219.3	177.5	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	107.5	108.9	°C/W
θ_{JB}	Junction-to-board thermal resistance	57.5	27.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.4	13.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	56.9	26.9	°C/W
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

THERMAL INFORMATION: OPA2322-Q1

THERMAL METRIC ⁽¹⁾		OPA2322-Q1			OPA2322S-Q1	UNIT
		D	DRG	DGK	DGS	
		8 PINS	8 PINS	8 PINS	10 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	122.6	50.6	174.8	171.5	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	67.1	54.9	43.9	43.0	°C/W
θ_{JB}	Junction-to-board thermal resistance	64.0	25.2	95.0	91.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.2	0.6	2.0	1.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	63.4	25.3	93.5	89.9	°C/W
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	5.7	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

THERMAL INFORMATION: OPA4322-Q1

THERMAL METRIC ⁽¹⁾		OPA4322-Q1	OPA4322S-Q1	UNIT
		PW	PW	
		14 PINS	16 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	109.8	105.9	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	34.9	28.1	°C/W
θ_{JB}	Junction-to-board thermal resistance	52.5	51.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.2	0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	51.8	50.4	°C/W
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

ELECTRICAL CHARACTERISTICS: $V_S = 1.8\text{ V to }5.5\text{ V}$, or $\pm 0.9\text{ V to } \pm 2.75\text{ V}$

Boldface limits apply over the specified temperature range, $T_A = -40^\circ\text{C to }125^\circ\text{C}$.

At $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, $V_{OUT} = V_S / 2$, and $\overline{\text{SHDN}}_X = V_{S+}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA322-Q1, OPA322S-Q1, OPA2322-Q1, OPA2322S-Q1, OPA4322-Q1, OPA4322S-Q1			UNIT
			MIN	TYP	MAX	
OFFSET VOLTAGE						
Input offset voltage	V _{OS}			0.5	2	mV
versus Temperature	dV _{OS} /dT	V _S = 5.5 V		1.8	6	μV/°C
versus Power supply	PSR	V _S = 1.8 V to 5.5 V		10	50	μV/V
Over temperature		V _S = 1.8 V to 5.5 V		20	65	μV/V
Channel separation		At 1 kHz		130		dB
INPUT VOLTAGE						
Common-mode voltage range	V _{CM}		(V−) − 0.1		(V+) + 0.1	V
Common-mode rejection ratio	CMRR	(V−) − 0.1 V < V _{CM} < (V+) + 0.1 V	90	100		dB
Over temperature			90			dB
INPUT BIAS CURRENT						
Input bias current	I _B			±0.2	±10	pA
Over temperature		T _A = −40°C to 85°C			±50	pA
		OPA322-Q1, OPA322S-Q1, T _A = −40°C to 125°C			±800	pA
		OPA2322, OPA2322S, T _A = −40°C to 125°C			±600	pA
		OPA4322, OPA4322S, T _A = −40°C to 125°C			±400	pA
Input offset current	I _{OS}			±0.2	±10	pA
Over temperature		T _A = −40°C to 85°C			±50	pA
		T _A = −40°C to 125°C			±600	pA
NOISE						
Input voltage noise		f = 0.1 Hz to 10 Hz		2.8		μV _{PP}
Input voltage noise density	e _n	f = 1 kHz		8.5		nV/√Hz
		f = 10 kHz		7		nV/√Hz
Input current noise density	i _n	f = 1 kHz		0.6		fA/√Hz
INPUT CAPACITANCE						
Differential				5		pF
Common-mode				4		pF
OPEN-LOOP GAIN						
Open-loop voltage gain	A _{OL}	0.1 V < V _O < (V+) − 0.1 V, R _L = 10 kΩ	100	130		dB
		0.1 V < V _O < (V+) − 0.1 V, R _L = 10 kΩ	94			dB
Phase margin	PM	V _S = 5 V, C _L = 50 pF		47		Degrees
FREQUENCY RESPONSE V _S = 5.0 V, C _L = 50 pF						
Gain bandwidth product	GBP	Unity gain		20		MHz
Slew rate	SR	G = 1		10		V/μs
Settling time	t _S	To 0.1%, 2-V step, G = 1		0.25		μs
		To 0.01%, 2-V step, G = 1		0.32		μs
Overload recovery time		V _{IN} × G > V _S		100		ns
Total harmonic distortion + noise ⁽¹⁾	THD+N	V _O = 4 V _{PP} , G = 1, f = 10 kHz, R _L = 10 kΩ		0.0005		%
		V _O = 2 V _{PP} , G = 1, f = 10 kHz, R _L = 600 Ω		0.0011		%

(1) Third-order filter; bandwidth = 80 kHz at -3 dB

ELECTRICAL CHARACTERISTICS: $V_S = 1.8\text{ V}$ to 5.5 V , or $\pm 0.9\text{ V}$ to $\pm 2.75\text{ V}$ (continued)

Boldface limits apply over the specified temperature range, $T_A = -40^\circ\text{C}$ to 125°C .

At $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, $V_{OUT} = V_S / 2$, and $\overline{\text{SHDN}}_X = V_{S+}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA322-Q1, OPA322S-Q1, OPA2322-Q1, OPA2322S-Q1, OPA4322-Q1, OPA4322S-Q1			UNIT
			MIN	TYP	MAX	
OUTPUT						
Voltage output swing from both rails	V _O	R _L = 10 kΩ		10	30	mV
Over temperature		R _L = 10 kΩ			40	mV
Short-circuit current	I _{SC}	V _S = 5.5 V		±65		mA
Capacitive load drive	C _L		See Typical Characteristics			
Open-loop output resistance	R _O	I _O = 0 mA, f = 1 MHz		90		Ω
POWER SUPPLY						
Specified voltage range	V _S		1.8		5.5	V
Quiescent current per amplifier	I _Q	I _O = 0 mA, V _S = 5.5 V				
OPA322-Q1, OPA322S-Q1		I _O = 0 mA, V _S = 5.5 V		1.6	1.9	mA
Over temperature		I _O = 0 mA, V _S = 5.5 V			2	mA
OPA2322-Q1, OPA2322S-Q1		I _O = 0 mA, V _S = 5.5 V		1.5	1.75	mA
Over temperature		I _O = 0 mA, V _S = 5.5 V			1.85	mA
OPA4322-Q1, OPA4322S-Q1		I _O = 0 mA, V _S = 5.5 V		1.4	1.65	mA
Over temperature		I _O = 0 mA, V _S = 5.5 V			1.75	mA
Power-on time		V _{S+} = 0 V to 5 V, to 90% I _Q level		28		μs
SHUTDOWN ⁽²⁾ V _S = 1.8 V to 5.5 V						
Quiescent current, per amplifier	I _{QSD}	All amplifiers disabled, $\overline{\text{SHDN}} = V_{S-}$		0.1	0.5	μA
High voltage (enabled)	V _{IH}	Amplifier enabled	(V+) - 0.1			V
Low voltage (disabled)	V _{IL}	Amplifier disabled			(V-) + 0.1	V
Amplifier enable time (full shutdown) ⁽³⁾	t _{ON}	Full shutdown; G = 1, V _{OUT} = 0.9 × V _S / 2 ⁽⁴⁾		10		μs
Amplifier enable time (partial shutdown) ⁽³⁾	t _{ON}	Partial shutdown; G = 1, V _{OUT} = 0.9 × V _S / 2 ⁽⁴⁾		6		μs
Amplifier disable time ⁽³⁾	t _{OFF}	G = 1, V _{OUT} = 0.1 × V _S / 2		3		μs
$\overline{\text{SHDN}}$ pin input bias current (per pin)		V _{IH} = 5 V		0.13		μA
		V _{IL} = 0 V		0.04		μA
TEMPERATURE						
Specified range			-40		125	°C
Operating range			-40		150	°C

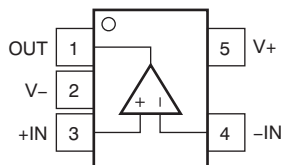
(2) Ensured by design and characterization; not production tested.

(3) The definition of disable time (t_{OFF}) and enable time (t_{ON}) is the time interval between the 50% point of the signal applied to the $\overline{\text{SHDN}}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.

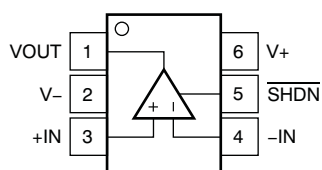
(4) Full shutdown refers to the dual OPA2322S-Q1 having both channels A and B disabled ($\overline{\text{SHDN}}_A = \overline{\text{SHDN}}_B = V_{S-}$) and the quad OPA4322S-Q1 having all channels A to D disabled ($\overline{\text{SHDN}}_{A/B} = \overline{\text{SHDN}}_{C/D} = V_{S-}$). Partial shutdown exercises only one $\overline{\text{SHDN}}$ pin; in this mode, the internal biasing and oscillator remain operational and the enable time is shorter.

PIN CONFIGURATIONS

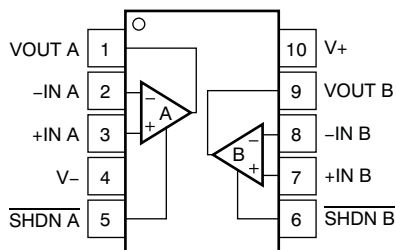
DBV PACKAGE
SOT23-5
(TOP VIEW)



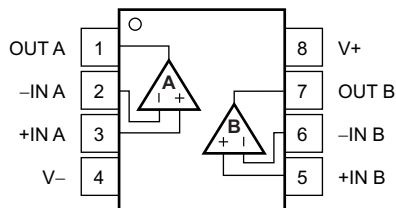
DBV PACKAGE
SOT23-6
(TOP VIEW)



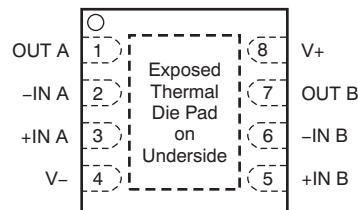
DGS PACKAGE
MSOP-10
(TOP VIEW)



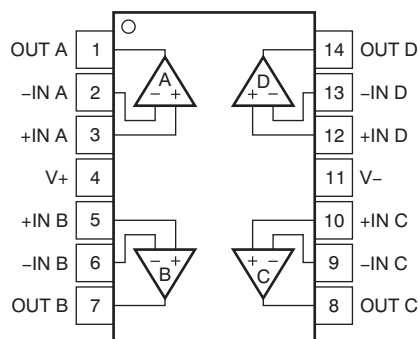
D, DGK PACKAGES
SO-8, MSOP-8
(TOP VIEW)



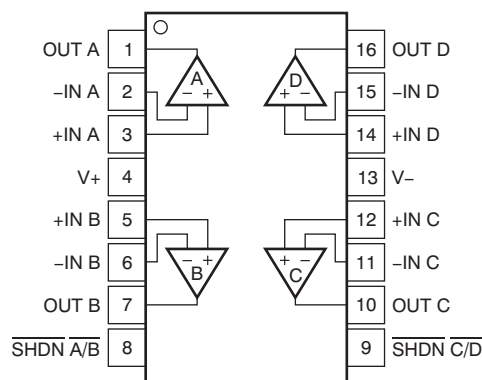
DRG PACKAGE⁽¹⁾⁽²⁾
DFN-8
(TOP VIEW)



PW PACKAGE
TSSOP-14
(TOP VIEW)



PW PACKAGE
TSSOP-16
(TOP VIEW)



- (1) Connect thermal pad to V-.
- (2) Pad size: 2 mm × 1.2 mm.

TYPICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = \text{mid-supply}$, and $R_L = 10\text{ k}\Omega$, unless otherwise noted.

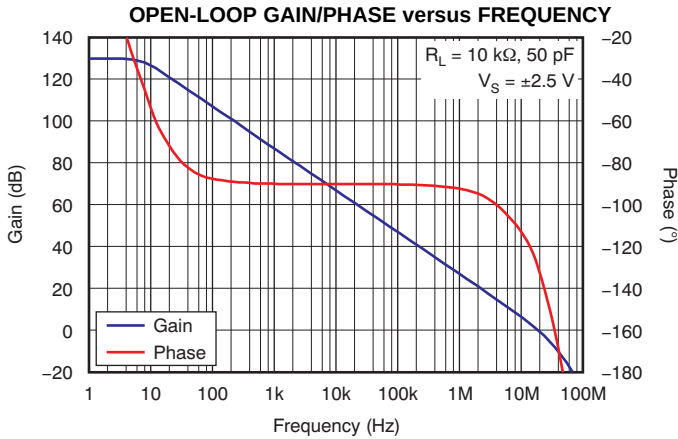


Figure 1.

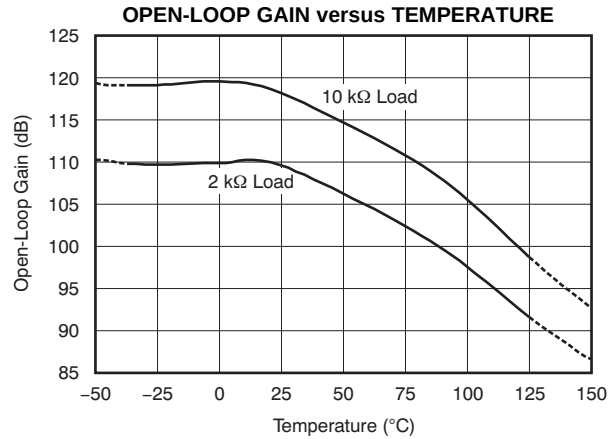


Figure 2.

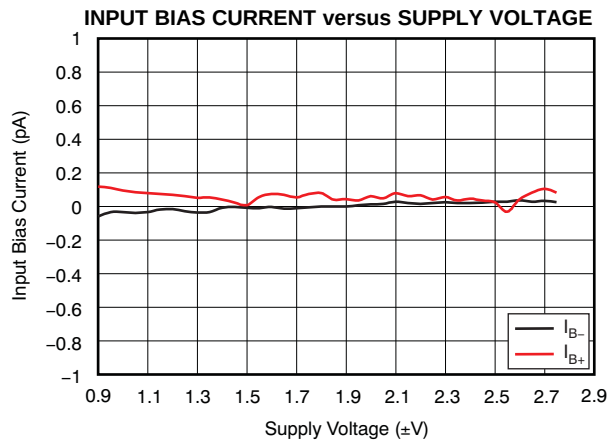


Figure 3.

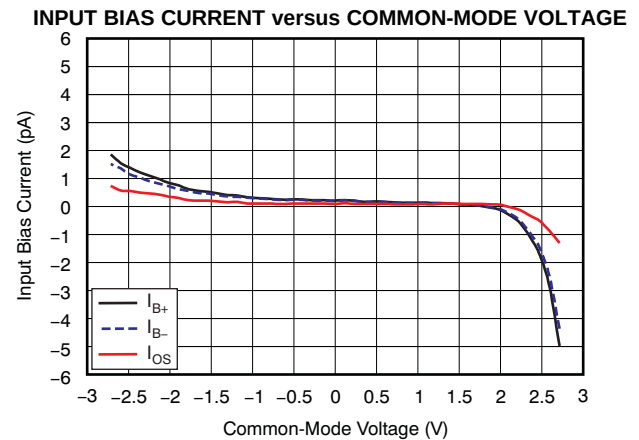


Figure 4.

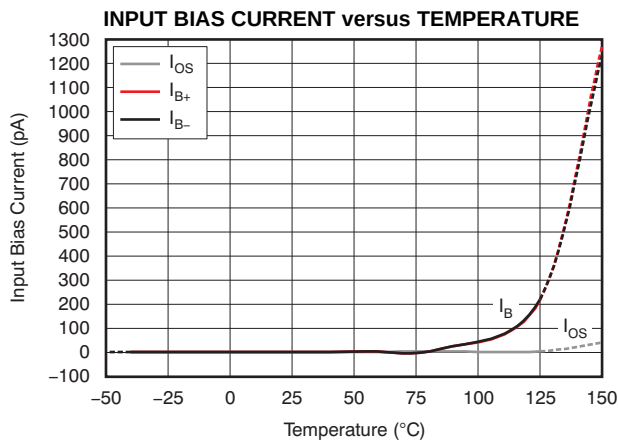


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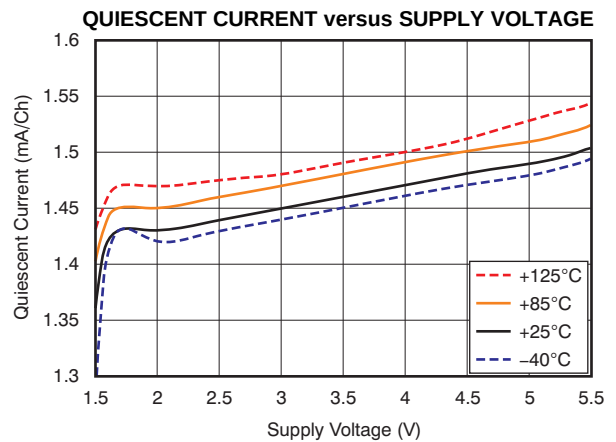


Figure 6.

TYPICAL CHARACTERISTICS (continued)

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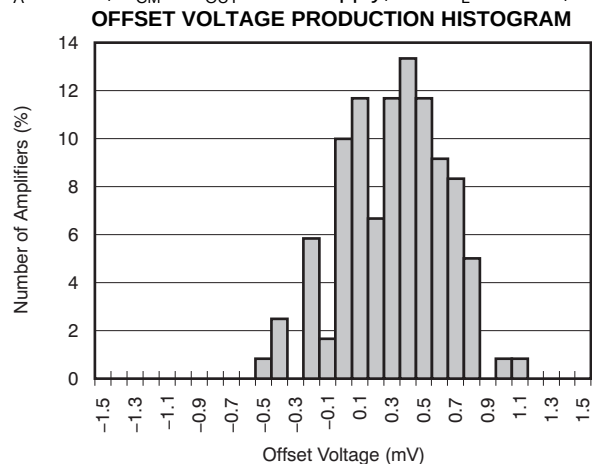


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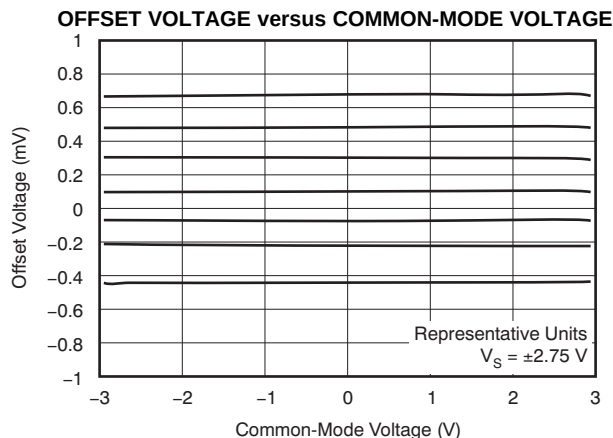


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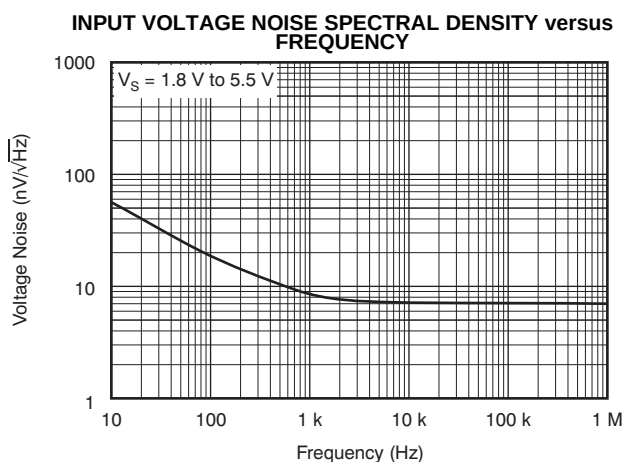


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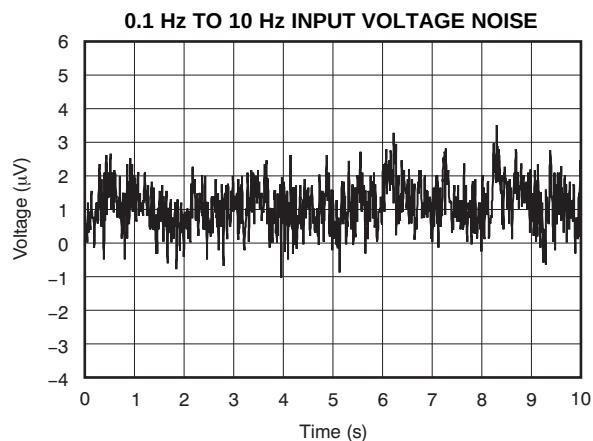


Figure 10.

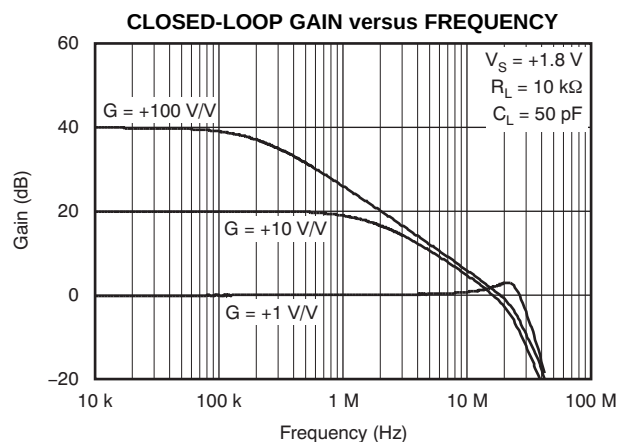


Figure 11.

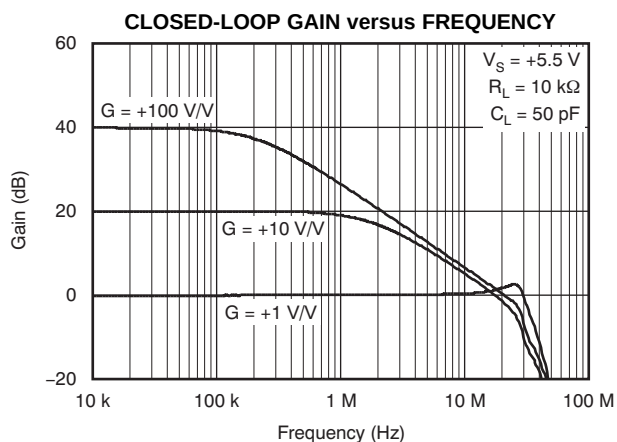


Figure 12.

TYPICAL CHARACTERISTICS (continued)

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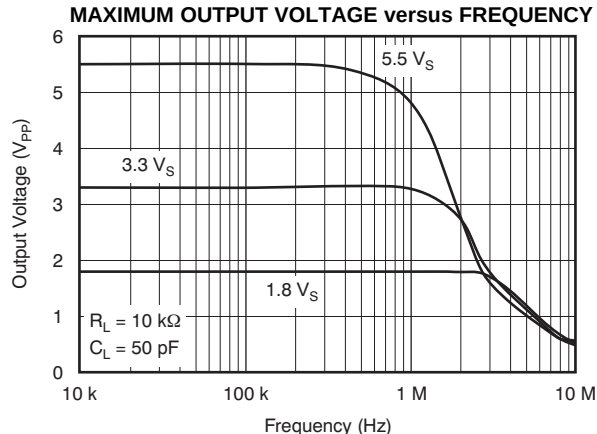


Figure 13.

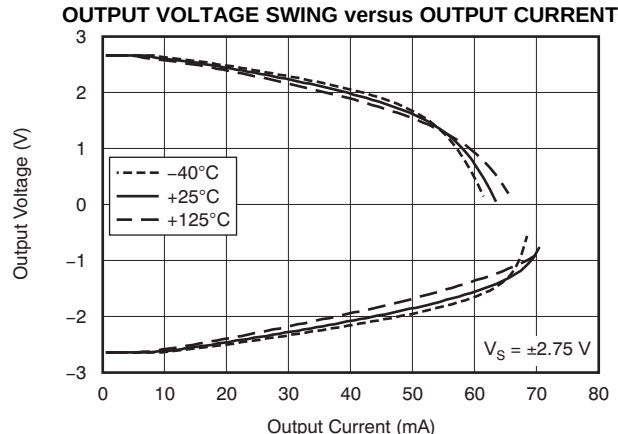


Figure 14.

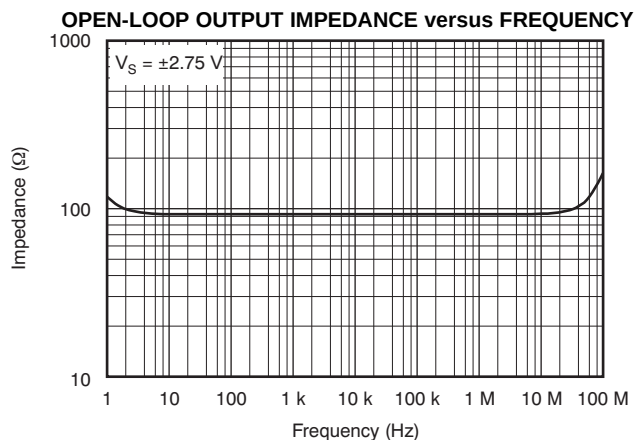


Figure 15.

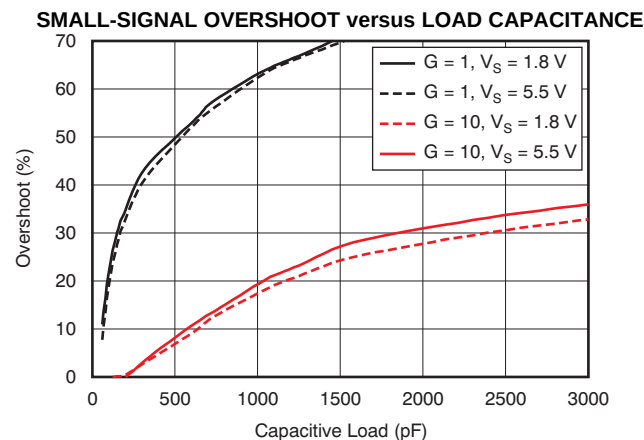


Figure 16.

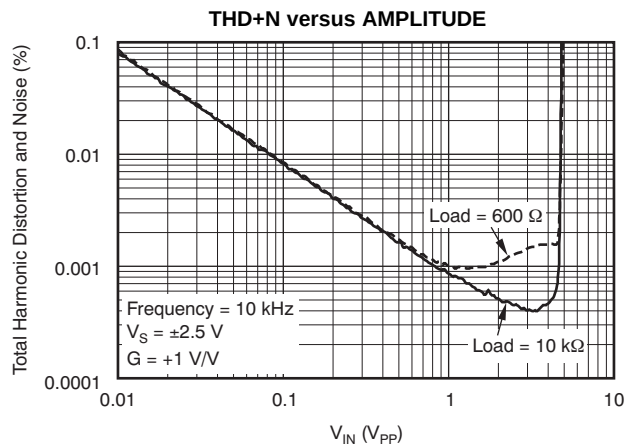


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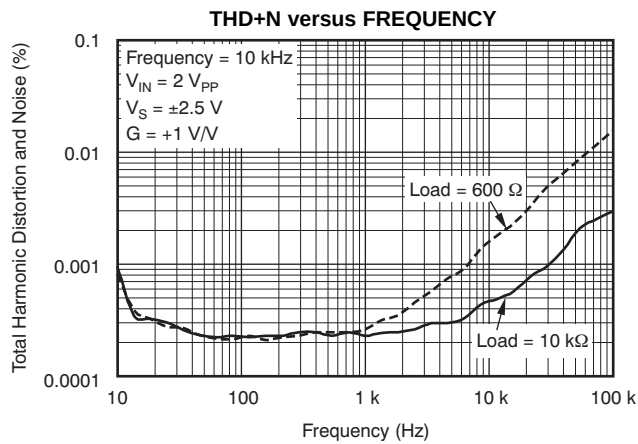


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = \text{mid-supply}$, and $R_L = 10\text{ k}\Omega$, unless otherwise noted.

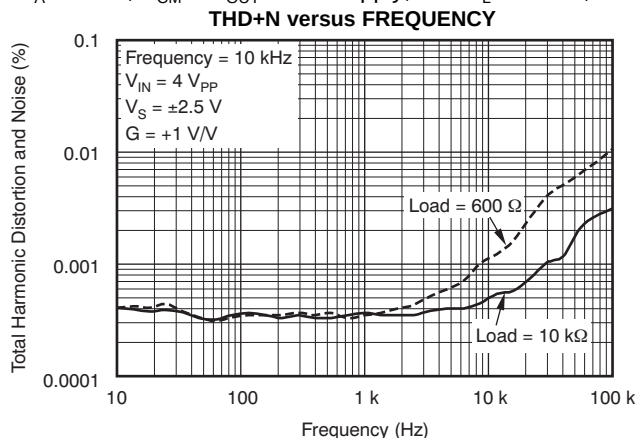


Figure 19.

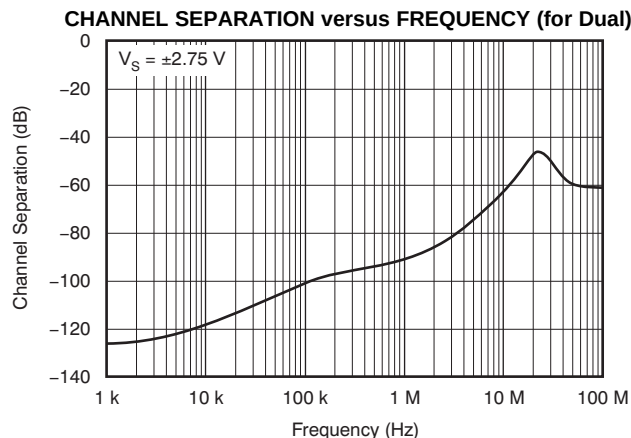


Figure 20.

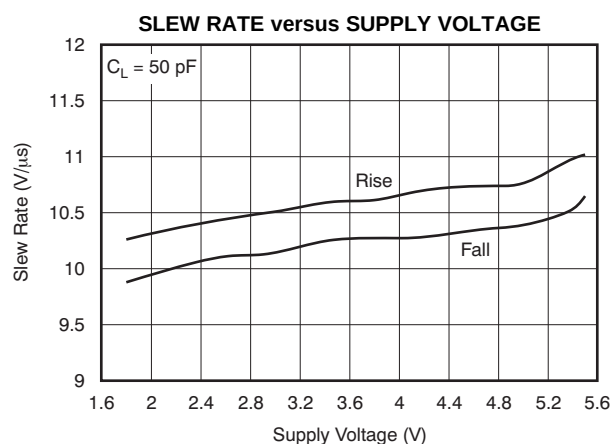


Figure 21.

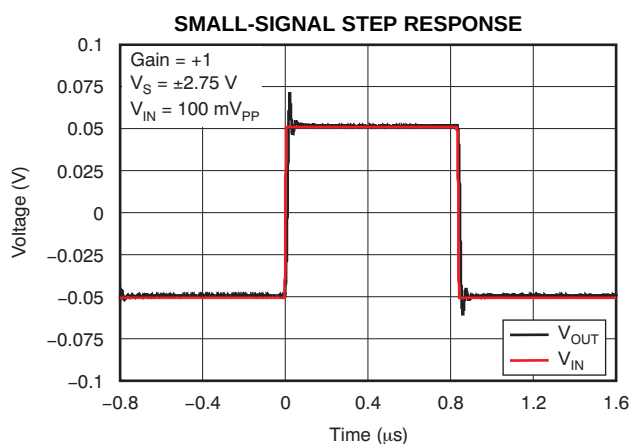


Figure 22.

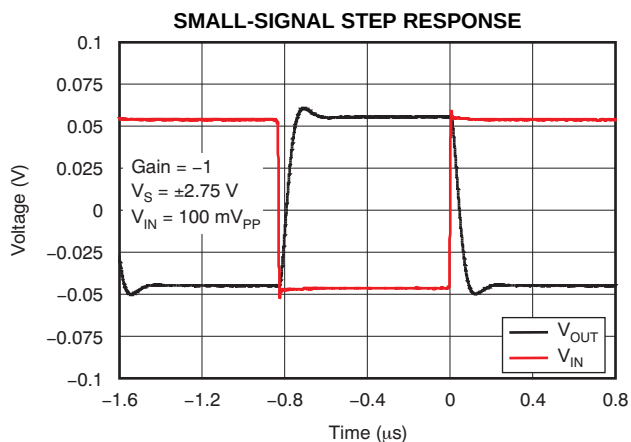


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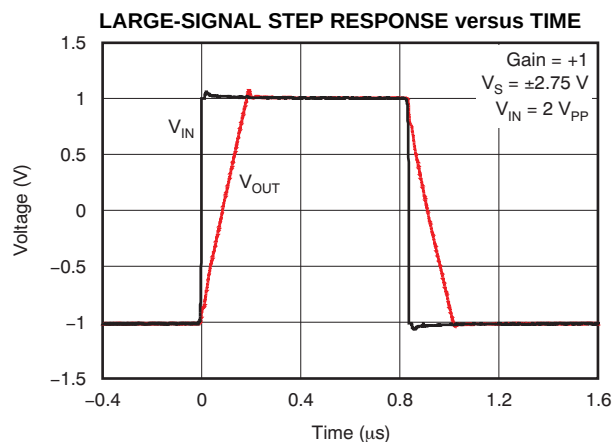


Figure 24.

TYPICAL CHARACTERISTICS (continued)

At $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = \text{mid-supply}$, and $R_L = 10\text{ k}\Omega$, unless otherwise noted.

CMRR AND PSRR versus FREQUENCY

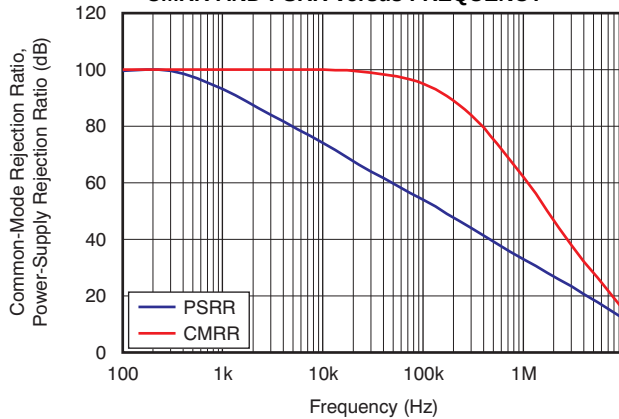


Figure 25.

TURN-OFF TRANSIENT

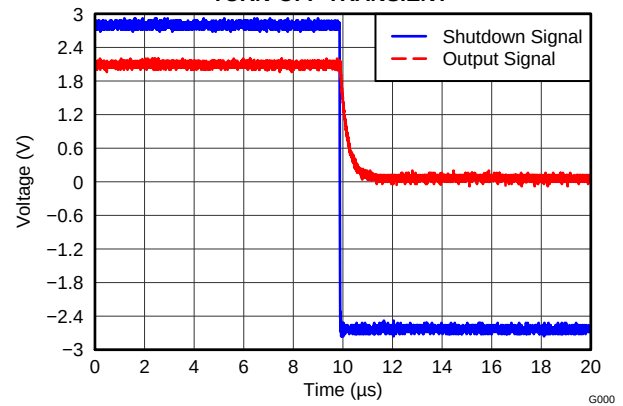


Figure 26.

TURN-ON TRANSIENT

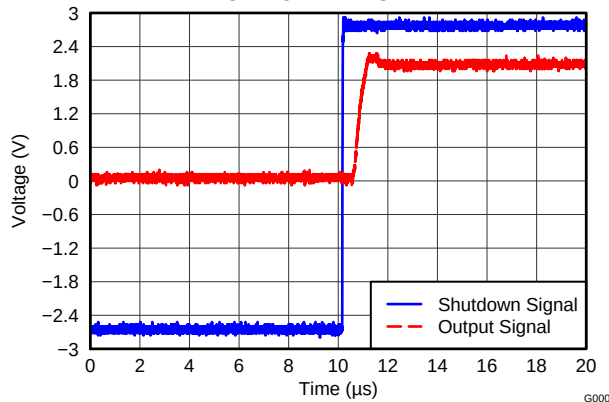


Figure 27.

**TURN-ON AND TURN-OFF TRANSIENT 5.5V
(High Supply)**

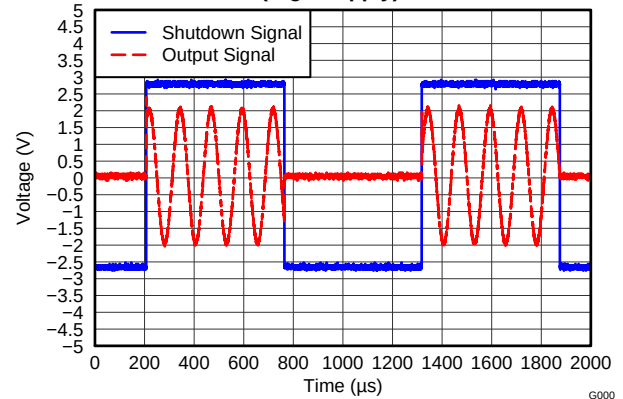


Figure 28.

**TURN-ON AND TURN-OFF TRANSIENT 1.8V
(Low Supply)**

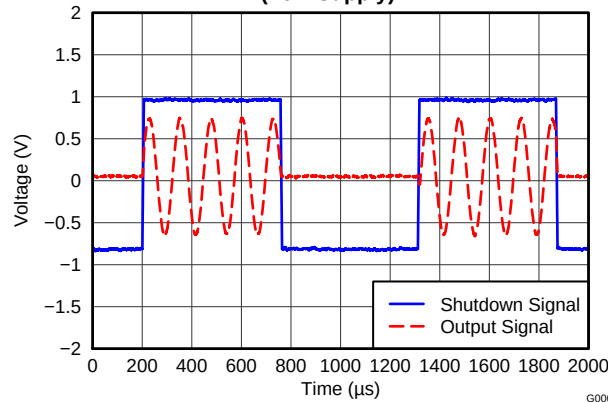


Figure 29.

APPLICATION INFORMATION

OPERATING VOLTAGE

The OPA322-Q1 family of operational amplifiers are unity-gain stable and can operate on a single-supply voltage (1.8 V to 5.5 V), or a split-supply voltage (± 0.9 V to ± 2.75 V), making them highly versatile and easy to use. The power-supply pins should have local bypass ceramic capacitors (typically 0.001 μ F to 0.1 μ F). The specifications of these amplifiers fully apply from 1.8 V to 5.5 V and over the extended temperature range of -40°C to 125°C . Parameters that can exhibit variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#).

INPUT AND ESD PROTECTION

The OPA322-Q1 incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit input overdrive protection, as long as the current is limited to 10 mA as stated in the [Absolute Maximum Ratings](#) table. Many input signals are inherently current-limited to less than 10 mA; therefore, there is no need for a limiting resistor. [Figure 30](#) shows how one may add a series input resistor (R_S) to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input; keep the value minimal in noise-sensitive applications.

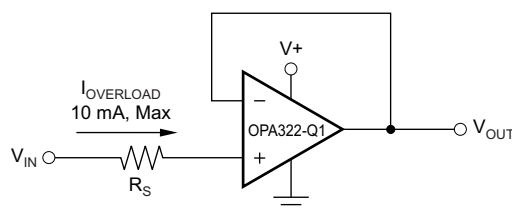


Figure 30. Input Current Protection

PHASE REVERSAL

The design of the OPA322-Q1 operational amplifiers is for immunity to phase reversal when the input pins exceed the supply voltages, therefore providing further in-system stability and predictability. [Figure 31](#) shows the input voltage exceeding the supply voltage without any phase reversal.

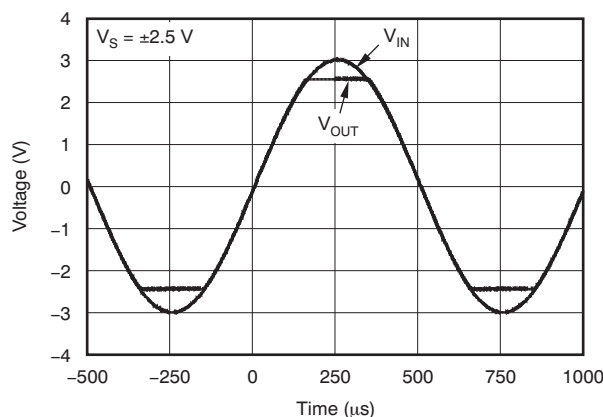
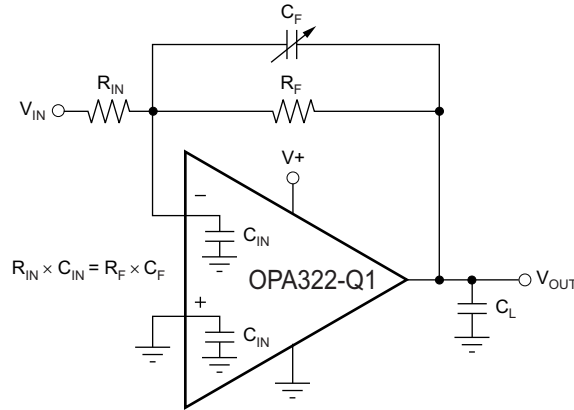


Figure 31. No Phase Reversal

FEEDBACK CAPACITOR IMPROVES RESPONSE

For optimum settling time and stability with high-impedance feedback networks, it may be necessary to add a feedback capacitor across the feedback resistor, R_F , as shown in Figure 32. This capacitor compensates for the zero created by the feedback network impedance and the OPA322-Q1 input capacitance (and any parasitic layout capacitance). The effect becomes more significant with higher-impedance networks.



NOTE: Where C_{IN} is equal to the OPA322-Q1 input capacitance (approximately 9 pF) plus any parasitic layout capacitance.

Figure 32. Feedback Capacitor Improves Dynamic Performance

TI suggests the use of a variable capacitor for the feedback capacitor, because input capacitance may vary between operational amplifiers and layout capacitance is difficult to determine. For the circuit shown in Figure 32, choose the value of the variable feedback capacitor so that the input resistance times the input capacitance of the OPA322-Q1 (typically 9 pF) plus the estimated parasitic layout capacitance equals the feedback capacitor times the feedback resistor:

$$R_{IN} \times C_{IN} = R_F \times C_F$$

where:

C_{IN} is equal to the OPA322-Q1 input capacitance (sum of differential and common-mode) plus the layout capacitance.

Adjust the capacitor value until optimum performance is obtained.

EMI SUSCEPTIBILITY AND INPUT FILTERING

Operational amplifiers vary in susceptibility to electromagnetic interference (EMI). If conducted EMI enters the device, the dc offset observed at the amplifier output may shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although EMI can affect all operational amplifier pin functions, the input pins are likely to be the most susceptible. The OPA322-Q1 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. The input filter provides both common-mode and differential-mode filtering. The filter design is for a cutoff frequency of approximately 580 MHz (–3 dB), with a rolloff of 20 dB per decade.

OUTPUT IMPEDANCE

The open-loop output impedance of the OPA322-Q1 common-source output stage is approximately 90 Ω . Connecting the operational amplifier with feedback significantly reduces this value by the loop gain. For each decade rise in the closed-loop gain, the loop gain is reduced by the same amount, which results in a ten-fold increase in effective output impedance. While the OPA322-Q1 output impedance remains very flat over a wide frequency range, at higher frequencies the output impedance rises as the open-loop gain of the operational amplifier drops. However, at these frequencies the output also becomes capacitive as a result of parasitic capacitance. This characteristic, in turn, prevents the output impedance from becoming too high, which can cause stability problems when driving large capacitive loads. As mentioned previously, the OPA322-Q1 has excellent capacitive load-drive capability for an operational amplifier with its bandwidth.

CAPACITIVE LOAD AND STABILITY

The OPA322-Q1 design is for use in applications where driving a capacitive load is required. As with all operational amplifiers, there may be specific instances where the OPA322-Q1 can become unstable. The particular operational amplifier circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation. An operational amplifier in the unity-gain (1 V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to become unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the operational amplifier output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, the OPA322-Q1 remains stable with a pure capacitive load up to approximately 1 nF.

The equivalent series resistance (ESR) of some very large capacitors ($C_L > 1 \mu\text{F}$) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains, as shown in Figure 33. One technique for increasing the capacitive load-drive capability of the amplifier operating in unity gain is to insert a small resistor (R_S), typically 10Ω to 20Ω , in series with the output, as shown in Figure 34.

This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. A possible problem with this technique is the creation of a voltage divider with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing. The error contributed by the voltage divider, however, may be insignificant. For instance, with a load resistance, $R_L = 10 \text{ k}\Omega$ and $R_S = 20 \Omega$, the gain error is only about 0.2%. However, when R_L is decreased to 600Ω , which the OPA322-Q1 is able to drive, the error increases to 7.5%.

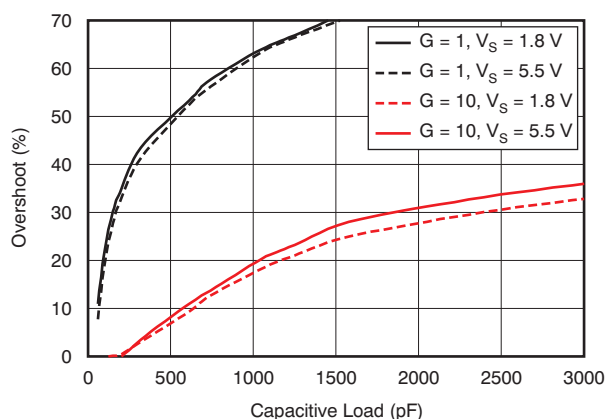


Figure 33. Small-Signal Overshoot versus Capacitive Load (100-mV_{pp} Output Step)

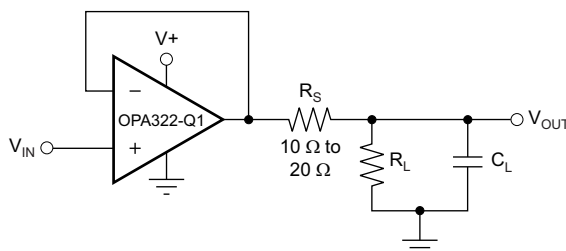


Figure 34. Improving Capacitive Load Drive

OVERLOAD RECOVERY TIME

Overload recovery time is the time required for the output of the amplifier to come out of saturation and recover to the linear region. Overload recovery is particularly important in applications with a requirement for small-signal amplification in the presence of large transients. Figure 35 and Figure 36 show the positive and negative overload recovery times of the OPA322-Q1, respectively. In both cases, the time elapsed before the OPA322-Q1 comes out of saturation is less than 100 ns. In addition, the symmetry between the positive and negative recovery times allows excellent signal rectification without distortion of the output signal.

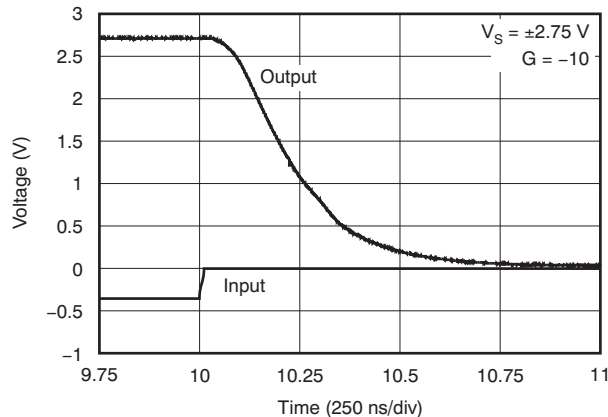


Figure 35. Positive Recovery Time

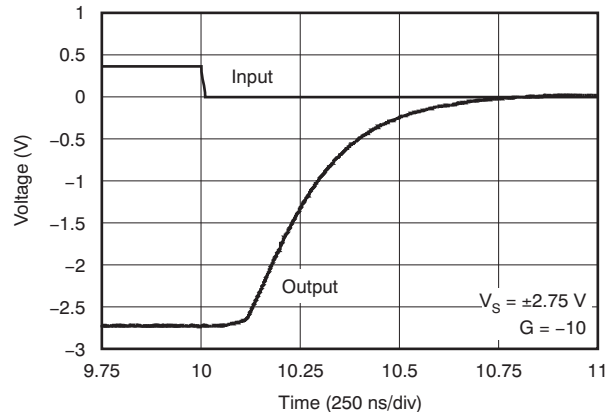


Figure 36. Negative Recovery Time

SHUTDOWN FUNCTION

The reference for the SHDN (enable) pin function of the OPAx322S-Q1 is to the negative supply voltage of the operational amplifier. A logic-level high enables the operational amplifier. The definition of a valid logic high is voltage $[(V+) - 0.1 \text{ V}]$, up to $(V+)$, applied to the SHDN pin. The definition of a valid logic low is $[(V-) + 0.1 \text{ V}]$, down to $(V-)$, applied to the enable pin. The maximum allowed voltage applied to SHDN is 5.5 V with respect to the negative supply, independent of the positive supply voltage. Drive this pin or connect it either to a valid high or low voltage; do not leave it as an open circuit.

The logic input is a high-impedance CMOS input. Control of dual operational amplifier versions is independent, and that of quad operational amplifier versions is in pairs with logic inputs. For battery-operated applications, use of this feature may greatly reduce the average current and extend battery life. The enable time is 10 μs for full shutdown of all channels; disable time is 3 μs . When disabled, the output assumes a high-impedance state. This architecture allows the OPAx322S-Q1 to operate as a *gated* amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time (t_{OFF}) depends on loading conditions and increases with increased load resistance. Ensuring shutdown (disable) within a specific shutdown time requires the specified 10-k Ω load to mid-supply ($V_S / 2$). Using the OPAx322S-Q1 without a load significantly increases the resulting turn-off time.

GENERAL LAYOUT GUIDELINES

The OPA322-Q1 is a wideband amplifier. To realize the full operational performance of the device, follow good high-frequency printed circuit board (PCB) layout practices. Connect the bypass capacitors between each supply pin and ground as close to the device as possible. Design the bypass capacitor traces for minimum inductance.

LEADLESS DFN PACKAGE

The OPA2322-Q1 uses the DFN style package (also known as SON), which is a QFN with contacts on only two sides of the package bottom. This leadless package maximizes PCB space and offers enhanced thermal and electrical characteristics through an exposed pad. One of the primary advantages of the DFN package is its low height (0.8 mm).

DFN packages are physically small, and have a smaller routing area. Additionally, they offer improved thermal performance, reduced electrical parasitics, and a pinout scheme that is consistent with other commonly-used packages (such as SO and MSOP). The absence of external leads also eliminates bent-lead issues.

Standard PCB-assembly techniques allow for easy mounting of the DFN package. See the application reports, [QFN/SON PCB Attachment \(SLUA271\)](#) and [Quad Flatpack No-Lead Logic Packages \(SCBA017\)](#), both available for download at www.ti.com. **Connect the exposed leadframe die pad on the bottom of the DFN package to the most-negative potential (V-).** The dimension of the exposed thermal die pad is 2 mm × 1,2 mm and is centered.

APPLICATION EXAMPLES

ACTIVE FILTER

The OPA322-Q1 is well-suited for active filter applications that require a wide-bandwidth, fast-slew-rate, low-noise, single-supply operational amplifier. [Figure 37](#) shows a 500-kHz, second-order, low-pass filter using the multiple-feedback (MFB) topology. The component selection provides a maximally-flat Butterworth response. Beyond the cutoff frequency, rolloff is –40 dB/decade. The Butterworth response is ideal for applications that require predictable gain characteristics, such as the anti-aliasing filter used in front of an ADC.

One point to observe when considering the MFB filter is its inverted output, relative to the input. If this inversion is not required, or not desired, a one can achieve a noninverting output through one of these options:

1. Adding an inverting amplifier
2. Adding an additional second-order MFB stage
3. Using a noninverting filter topology, such as the Sallen-Key (shown in [Figure 38](#)).

One can quickly accomplish MFB and Sallen-Key, low-pass and high-pass filter synthesis using TI's [FilterPro™](#) program. This software is available as a free download at www.ti.com.

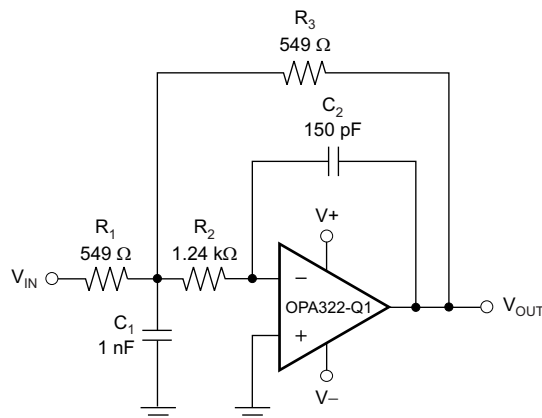


Figure 37. Second-Order Butterworth 500-kHz Low-Pass Filter

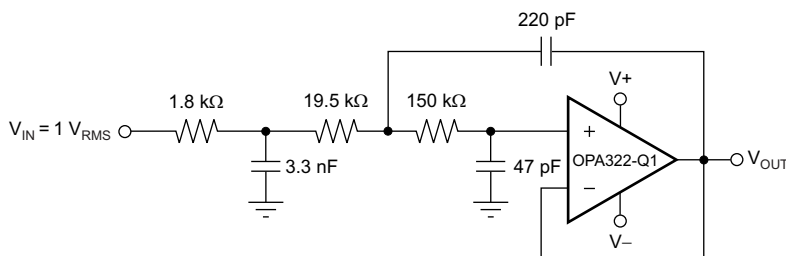


Figure 38. OPA322-Q1 Configured as a Three-Pole, 20-kHz, Sallen-Key Filter

REVISION HISTORY

Changes from Original (June 2013) to Revision A	Page
• Changed from Product Preview to Production Data	1
• Removed ordering information table	2
• Changed input bias current max over temp limit from ± 400 to ± 600	4
• Changed input offset current max over temp limit from ± 400 to ± 600	4
• Changed max voltage output swing from both rails from 20 to 30.	5
• Changed max over temperature limit from 30 to 40.	5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2322AQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OVDQ	Samples
OPA4322AQPWQ1	PREVIEW	TSSOP	PW	14	90	TBD	Call TI	Call TI	-40 to 125		
OPA4322AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	4322AQ1	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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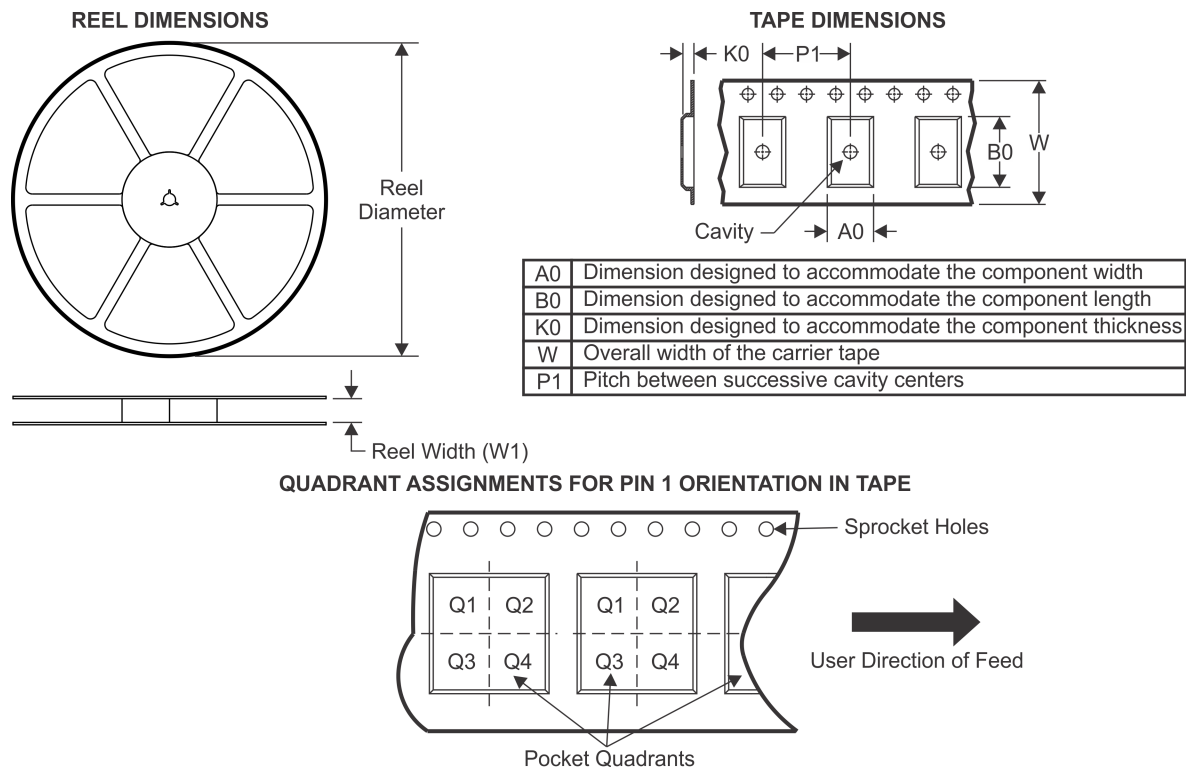
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OTHER QUALIFIED VERSIONS OF OPA2322-Q1, OPA4322-Q1 :

- Catalog: [OPA2322](#), [OPA4322](#)

NOTE: Qualified Version Definitions:

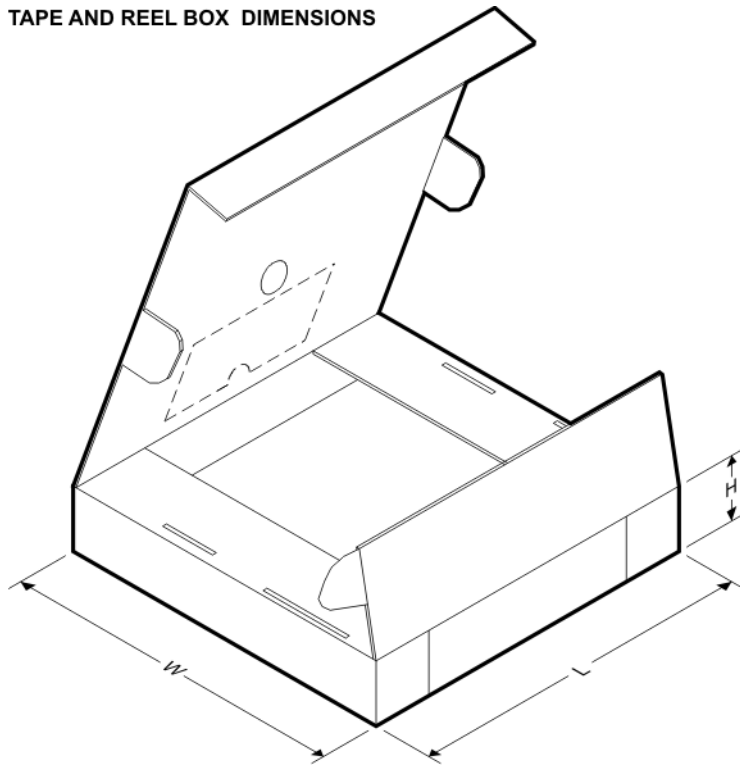
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2322AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

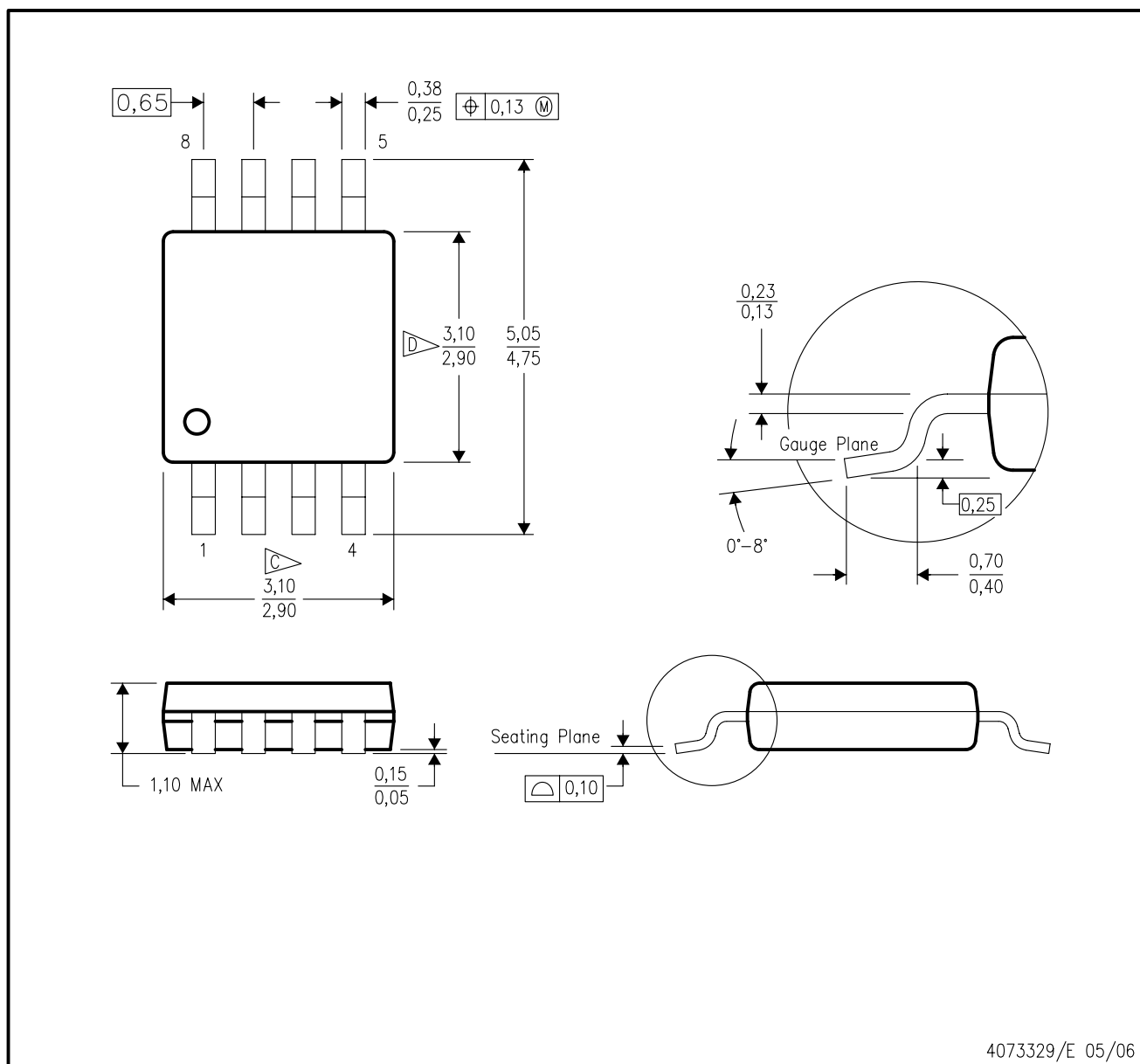


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2322AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0

D GK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

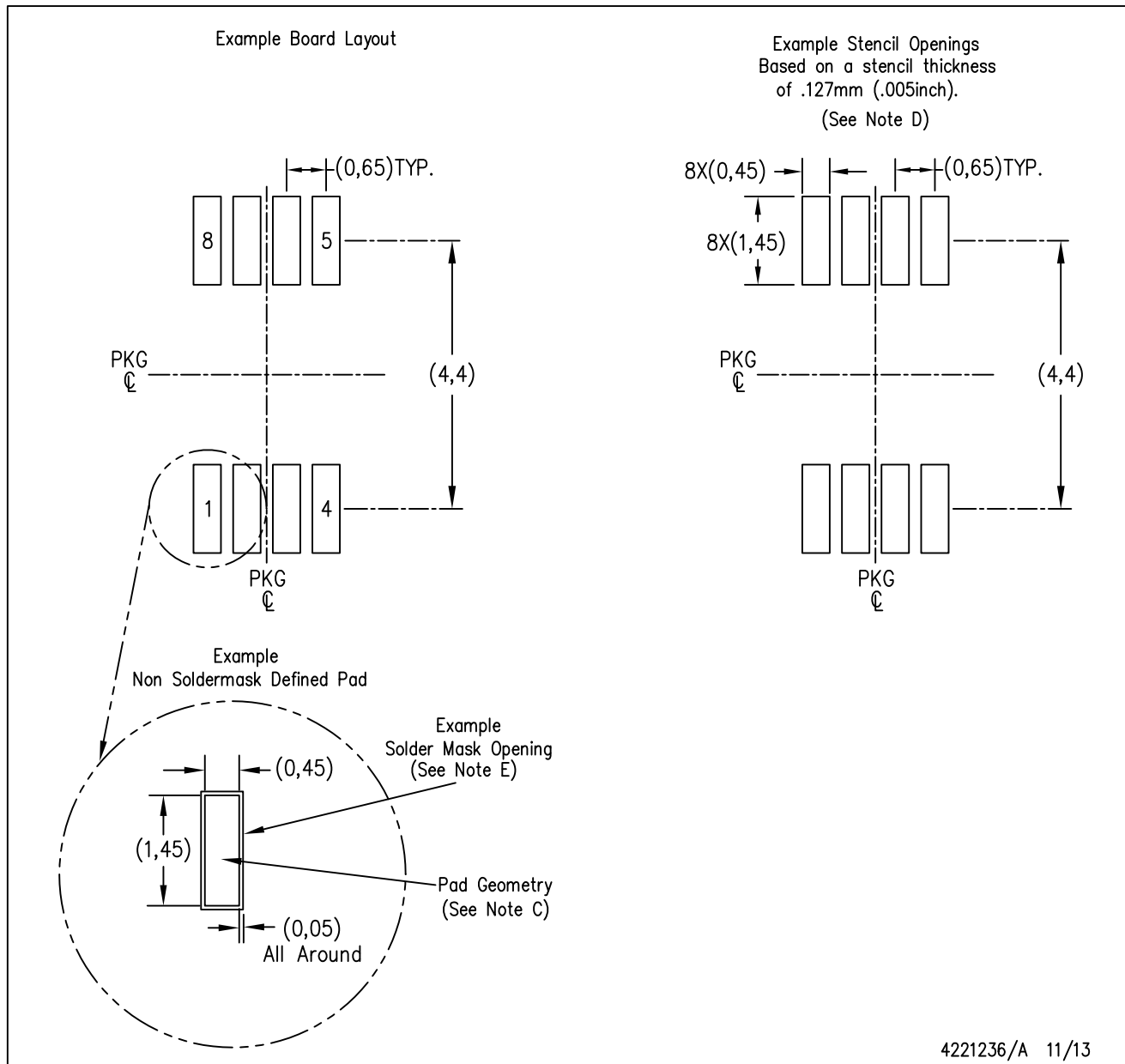


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- ☒ C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- ☐ D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8)

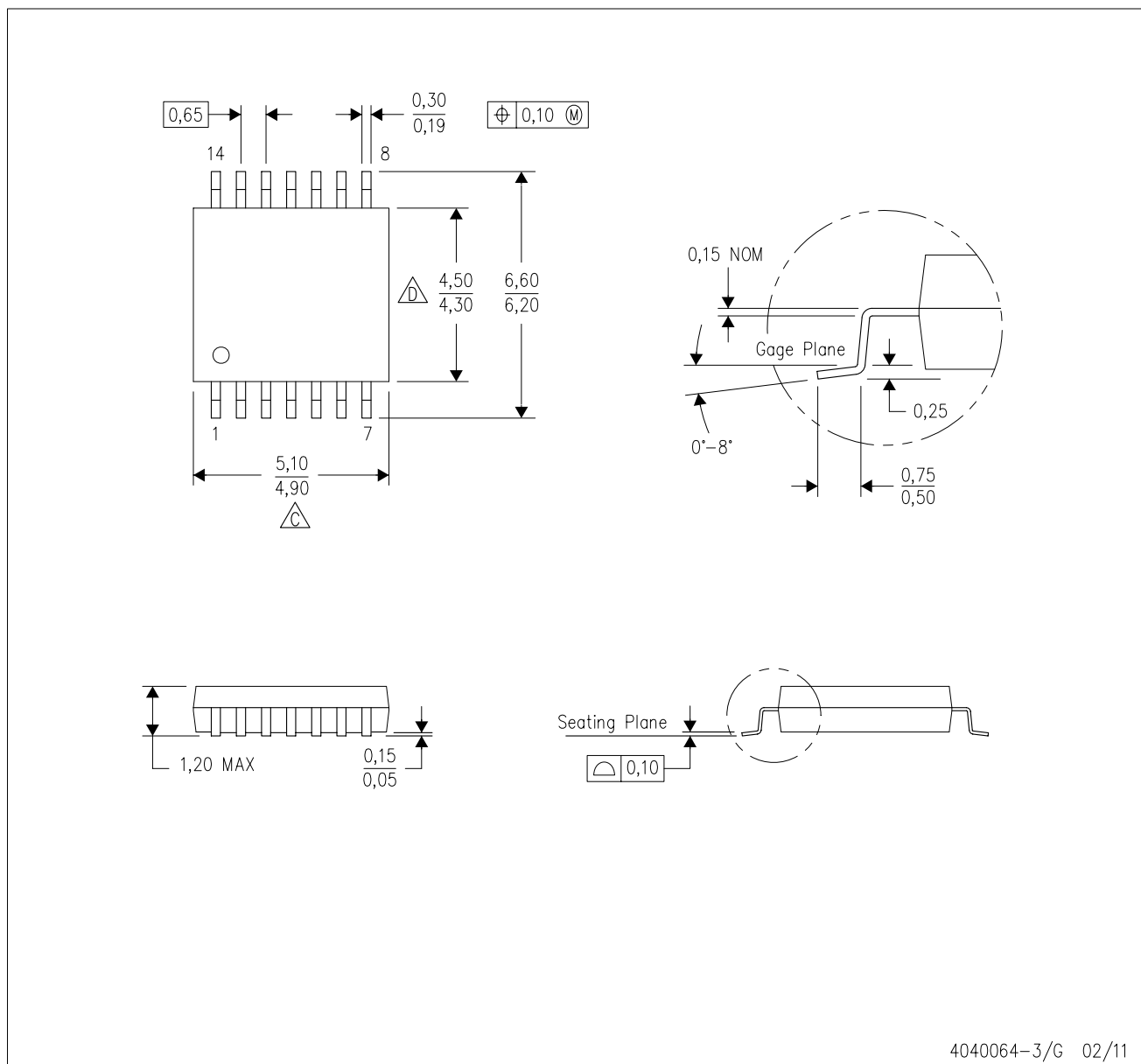
PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
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 - This drawing is subject to change without notice.
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 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

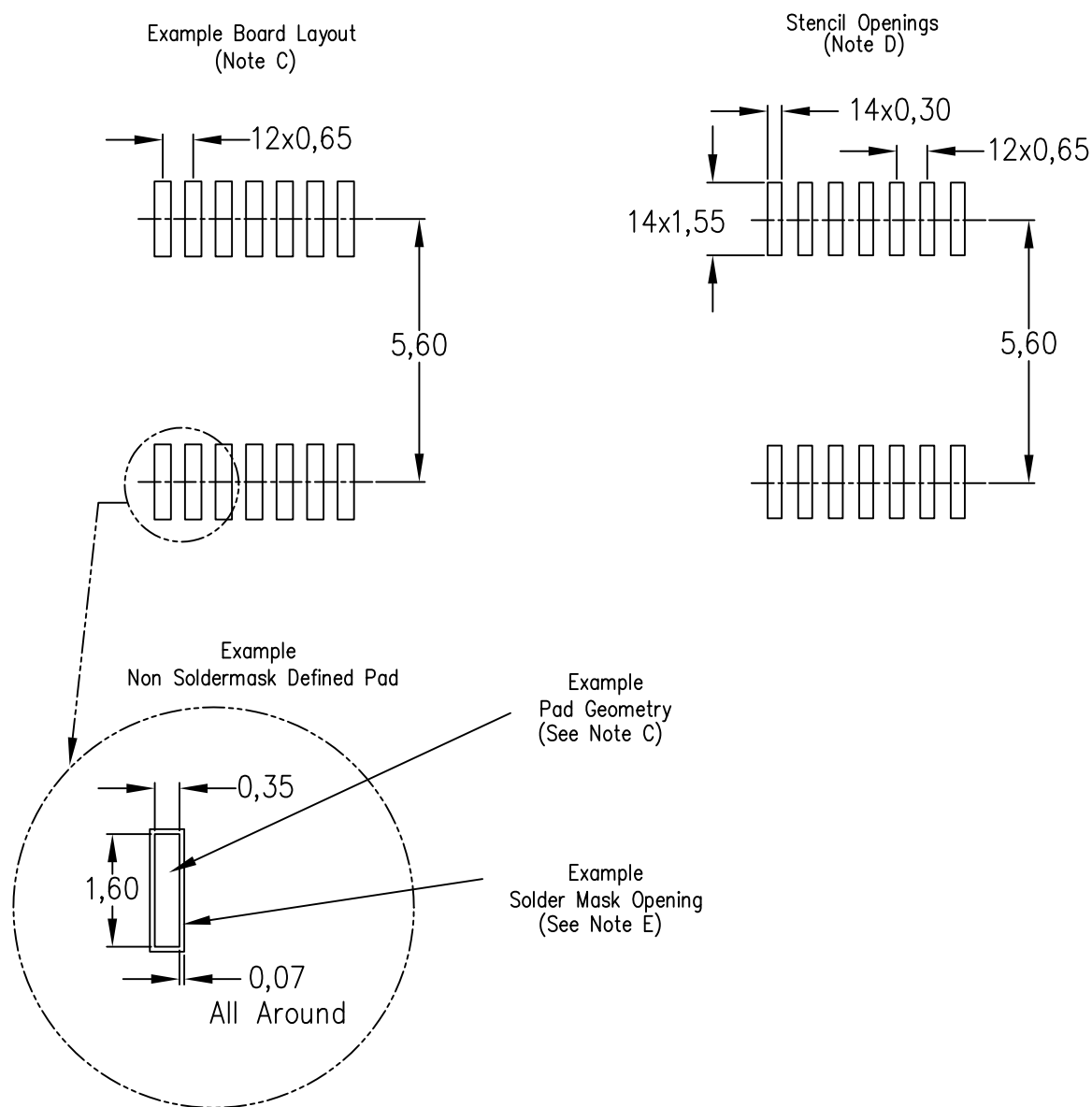


4040064-3/G 02/11

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 - B. This drawing is subject to change without notice.
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 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
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 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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