CP2000DC54-PE Compact Power Line DC/DC Converter

Input: -40 to -72Vdc; Outputs: ±54 Vdc @ 2000W; 5 Vdc @ 4W

Applications

- 48Vdc distributed power architectures
- Power over Ethernet
- Routers/Switches
- VoIP/Soft Switches
- LAN/WAN/MAN applications
- File servers
- Indoor wireless
- Telecommunications equipment
- Enterprise Networks
- SAN/NAS/iSCSI applications
- Advanced workstations

Features

- Compact 1-RU form factor providing 22 W/in3
- Input Current < 60A at 40 Vdc input
- Programmable output voltage from 44V to 58 Vdc,
- Output defaulted to 54V
- RS485[1] and PMBus compliant dual I^2C serial bus communications
- Designed to IEEE802.3af Compliance, 2250 output*** isolation to chassis/signals for POE applications. (see ordering info)
- DC Output over-voltage and over-current protection
- DC Input over-voltage and under-voltage protection
- Over-temperature warning and protection
- Redundant, parallel operation with active load sharing and isolated redundant +5V Aux power, isolated signals and I^2C communications
- Remote ON/OFF
- Hot insertion/removal (hot plug)
- Four front panel LED indicators
- UL* Recognized to UL60950-1, CAN/ CSA† C22.2 No. 60950-1, and VDE‡ 0805-1 Licensed to IEC60950-1
- CE mark meets 2006/95/EC directive §
- Internal variable-speed fan control
- RoHS 5 compliant
- POE compliant to IEEE802.3af

Description

The CP2000DC54-PE DC/DC Converter, also called a Power Entry Module (PEM) in the Compact Power Line platform is specifically designed to operate as an integral part of a complete distributed power system. The high-density, front-to-back airflow PEM is designed for minimal space utilization and is highly expandable for future growth. It is provided with many features including PoE isolation, and dual-redundant I^2C communications busses that allow it to be used in a broad range of applications. These signals and the 5V auxiliary supply are isolated from the main output and frame ground. The flexible feature set makes this Power Entry Module an excellent choice for applications requiring modular dc-to-dc bulk intermediate voltages, such as in distributed power.

* UL is a registered trademark of Underwriters Laboratories, Inc.
† CSA is a registered trademark of Canadian Standards Association.
‡ VDE is a trademark of Verband Deutscher Elektrotechniker e.V.
§ This product is intended for integration into end-user equipment. All the required procedures for CE marking of end-user equipment should be followed. (The CE mark is placed on selected products.)
** ISO is a registered trademark of the International Organization of Standards.

[1] Introduced in 2011

imagination at work

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Electrical Specifications

Input					
Parameter	**Min**	**Typ**	**Max**	**Units**	**Notes**
Operating Voltage	-40		-72	Vdc	
Low Input Shutdown of Main output	-38.5	-39	-39.5	Vdc	
Input Turn-ON of both Outputs	-43	-43.5	-44	Vdc	
Reverse Input Voltage	The module shall not be damaged				
Idling Power Output OFF Output ON			35 60	W	5Vdc output at no-load Both outputs at no-load
Input Current			60	Adc	At input voltages > 40Vdc
Cold Start Inrush Current			60	Adc	Measured at 25°C for all line conditions. Does not include X-capacitor charging spike
Efficiency	88 82	90 84		%	From 75% to 100% of full load For loads > 25% of full load
Holdup Time	8			ms	Minimum Vin = 48Vdc, output at ½ Full Load, output can droop down to -40Vdc
Ride Through	8			ms	
Input Capacitance			25	µF	

Main Output					
Parameter	**Min**	**Typ**	**Max**	**Units**	**Notes**
Maximum Output Power			2000	W	At voltages > 54Vdc
Output Voltage Setpoint		54		Vdc	Output floats with respect to frame ground.
Voltage Regulation Set Point at 50% FL Set Point Tolerance Set Point Regulation Droop Regulation Droop Accuracy	 -0.5 -1 -5	 54 1 	 0.5 1 5	 Vdc % % Vdc %	 Resets to factory setting if power is removed All conditions (temp, line, drift) Linear from 1 to 39 A. All conditions (temp, line, drift)
Output Voltage Range	44		58	Vdc	Set either by I²C, or analog margining.
Output Current	0.1		37	A	At 54Vdc. Below 0.1A the module meets its regulation requirements.
Reverse (sink) output current			0.5	A	Isolation function provided
Active Current Share	-5		5	%FL	Single-wire connection. Loads > 25%FL
Passive Current Share	-15		+15	%FL	Between modules without the single wire connection. Loads > 25%FL
Output Ripple (5 to 20MHz) RMS Peak-to-Peak			 250 500	 mVrms mVpk-pk	 Measured with 20MHz bandwidth under any condition of loading. Minimum load is 1A.
External Bulk Load Capacitance	0		5,000	µF	External capacitance can be increased but the power supply will not meet its turn-ON rise time requirement.

CP2000DC54-PE series dc-dc converter

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Electrical Specifications (continued)

Output (continued)					
Parameter	**Min**	**Typ**	**Max**	**Units**	**Notes**
Turn-On Delay Rise Time[2] Overshoot		 5 500	 5	 s ms %	Monotonic Turn_On after detection of valid DC input voltage. Measured from 30% to 100% of Vnom.
Restart Shutdown Delay		20		S	Shutdown is delayed during a re-start in order to guarantee restart of multiple paralleled modules.
Load Step Response ΔI ΔV Response Time		 2.0 2	 50 	 %FL Vdc ms	ΔI/Δt slew rate 1A/µs. Settling time to within regulation requirements.
Overload[3] Current Limit Shutdown	 38.9		 43 39	 Adc Vdc	 Fold-down. Default state – hiccup mode
System Start-up	A 20 second shutdown delay is implemented to allow modules to be plugged in one at a time. During this time fold-down occurs but the module will not shut down below 39Vdc.				
Over-voltage Delayed Instantaneous Latchoff			 60 65	 Vdc Vdc	 200msec delayed shutdown implemented. Latched shutdown without hiccup.
	Three restart attempts are implemented within a one minute window prior to a latched shutdown when Vout < 65Vdc. Beyond 1 minute the counter restarts				
Over-temperature Warning Shutdown	 20	5		 °C °C	Implemented prior to commencement of an OT shutdown Below the maximum rating of the device being protected
Auto-recoverable	Temperature hysteresis of approximately 10°C provided between shutdown and restart.				

Auxiliary Output					
Parameter	**Min**	**Typ**	**Max**	**Units**	**Notes**
ON when the input voltage is	-26		-72	Vdc	
Output Voltage Setpoint		5.2		Vdc	Isolated from the main output to meet POE requirements. 50mA dedicated for powering adjacent PEMs during a fault. 700mA available for external use.
Output Current	0.005		0.75	A	
Overall Regulation	-5		+5	%	
Ripple and Noise		50	100 25	mVpk-pk mVrms	20MHz bandwidth. Measured across a 1µF tantalum and a 0.1µF ceramic capacitor
Over-voltage Clamp			7	Vdc	
Over-current Limit	110		175	%FL	
Isolation from the main output	2250			Vdc	
Isolation from frame ground	50			Vdc	A 1MΩ noise suppression resistor is connected between Logic_GRD and Frame_GRD.

[2] Below -5°C the rise time is approximately 5 minutes to protect bulk capacitors in the unit

[3] Hiccup performance attempts automatic recovery from an overload shutdown with approximately a 90% off-time duty cycle. The duty cycle varies periodically in order to guarantee multi-module recovery synchronization. Latchoff can be chosen via software instead of the default hiccup. Recovery from a latchoff requires ENABLING, or software commanding OFF followed by an ON after a 2 second delay.

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Mechanical, Environmental and EMC Specifications

Dimensions (nominal)	
Length (in./mm)	13.85 / 351.8
Width (in./mm)	4.00 / 101.6
Height (in./mm)	1.66 / 42.2
Weight (lb/kg)	4.6 / 2.1

Environmental					
Parameter	**Min**	**Typ**	**Max**	**Units**	**Notes**
Ambient Temperature Operating Ambient Derating Power Derating[2]	-5[4]	 1	 45 1	 °C °C %/°C	 Air inlet from sea level to 5,000 feet. Per 1,000 feet above 5,000 feet. Up to 55°C
Storage Temperature	-40		85	°C	
Humidity	5		95	%	Relative humidity, non-condensing
Shock and Vibration Operational Test Test Levels Drop and Tip Over					 IEC 68-2 IEC 721-3-2 IEC 68-2-31
Earthquake Rating	4			Zone	Per Telcordia GR-63-CORE, all floors, when installed in CP Shelf.

EMC, Performance					
Parameter	**Min**	**Typ**	**Max**	**Units**	**Notes**
Radiated Emissions[5]	FCC and CISPR22 (EN55022) - Class A[3]				
Conducted Emissions - dc	Telcordia GR-1089-CORE and CISPR22 (EN55022) - Class A				
ESD	Error free per EN/IEC 61000-4-2 Level 4 (8 kV contact discharge, 15 kV air discharge).				
Radiated Immunity	Error free per EN/IEC 61000-4-3 Level 3 (10 V/m).				
Differential mode surge			100	Vdc	ANSI T1.315, No errors
Differential mode surge transient			1000	Vdc	No errors. IEEE C62.41 defined pulse transient
Common mode surge (1.2/50µs pulse)			1000	Vdc	
Conducted Immunity	Error free per EN/IEC 61000-4-6 Level 3 (10Vrms).				
Reliability (calculated)		400,000		Hours	At ambient of 25°C at full load per Telcordia SR-332, Reliability Prediction for Electronic Equipment, Method I Case III.
Isolation Input-Chassis/Signals Input-Output/Signals Output-Chassis/Signals Main-Aux Outputs	 1700 2250 2250 2250			Vdc	 Per EN60950. Per IEEE802.3af.
Service Life		10		Years	25°C ambient, full load excluding fans.
Acoustic Noise		55		dBA	Noise is proportional to fan speed, load and ambient temperature.

[4] Designed to start at an ambient as low as -40°C, but may not meet operational limits until above -5°C.

[5] Radiated emissions compliance was met using a Lineage Power shelf. This shelf includes output common and differential mode capacitors that assist in meeting compliance.

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Status and Control

The PEM provides two means for monitor/control: analog or I²C.

Details of analog controls are provided in this data sheet under Signal Definitions. GE Energy will provide separate application notes on the I²C protocol for users to interface to the CPL PEMs. Contact your local GE Energy representative for details.

Hot Plug

When rapidly extracting and reinserting modules care should be taken to allow for discharging the internal bias supply so that a predictable restart could be achieved. The way to ensure that the circuit sufficiently discharges is to observe the spinning of the fans after an extraction. The unit should not be reinserted until the fans stop spinning.

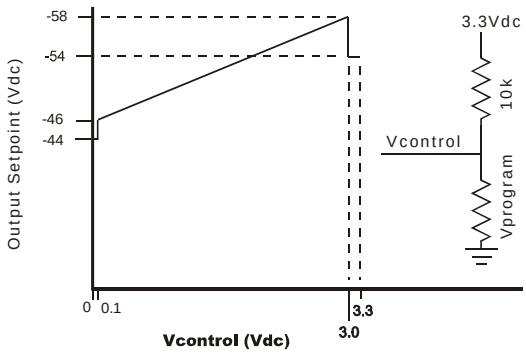
Without bleeding down internal bias the module may remember its last assigned address and may not configure itself properly if reinserted into another slot.

Control Definitions

All signals are referenced to Logic_GRD unless otherwise noted. See the Signal Definitions Table at the end of this document for further description of all the signals.

Control Signals

Margining: Set point of the PEM can be changed via this input pin. Programming can be either a voltage source or a resistance divider. The margining pin is connected to 3.3Vdc via a 10kΩ resistor inside the PEM. See graphs below.



An open circuit on this pin reverts the voltage level back to the original setting.

Software commanded margining overrides the hardware set point indefinitely or until the default setting is reinstated for example if input power and bias power have been removed from the module.

Module Present Signal: This signal has dual functionality. It can be used to alert the system when a module is inserted. A 500Ω resistor is present in series between this signal and Logic_GRD. An external pull-up should not raise the voltage on the pin above 0.25Vdc. Above 1Vdc, the write_protect feature of the EEPROM is enabled.

Protocol Select: Establishes the communications mode of the power supply, between analog/I²C and RS485 modes. For RS485, connect 10kΩ pull-down resistor to 54_OUT(-DC).

Enable: On/Off control when I²C communications are utilized as configured by the Protocol pin. This pin must be pulled low to turn **ON** the power supply. The power supply will turn **OFF** if either the **Enable** or the **ON/OFF** pin is released. This signal is referenced to Logic_GRD.

ON/OFF: This is a short pin utilized for hot-plug applications to ensure that the power supply turns **OFF** before the power pins are disengaged. It also ensures that the power supply turns **ON** only after the power pins have been engaged. Must be connected to V_OUT (-DC).

Status Signals

Power_OK: This signal is HI when the main output is present and goes LO when the main output is not present.

I_limit: This signal is HI when the main output is not in current limit and goes LO when current limit has activated.

Alert #: I²C interrupt signal.

Fault: This signal goes LO for any failure that requires PEM replacement. Some of these faults may be due to:

- Fan failure
- Over-temperature condition
- Over-temperature shutdown
- Over-voltage shutdown
- Internal PEM Fault

Digital Feature Descriptions

PMBus™ compliance: The power supply is fully compliant to the Power Management Bus (PMBus™) rev1.2 requirements with the following exceptions:

The power supply continuously updates its STATUS and ALARM registers to the latest state in order to capture the 'present' state of the power supply. There are a number of indicators, such as those indicating a communications fault (PEC error, data error) that do not get cleared until specifically instructed by the host controller sending a clear_faults command. A 'bit' indicator notifies the user if the STATUS and ALARM registers changed since the last 'read' by the host controller.

For example, if a voltage surge causes a momentary shutdown for over voltage the power supply will automatically restart if the 'auto_restart' feature is invoked. During the momentary shutdown the power supply issues an Alert# indicating to the system controller that a status change has occurred. If the system controller reads back the STATUS and ALARM registers while the power supply is shut down it will get the correct fault condition. However, inquiry of the state of the power supply after the restart event would indicate that the power supply is functioning correctly. The STATUS and ALARM indicators did not freeze at the original shutdown state and so the reason for the original Alert# is erased. The restart 'bit' would be set to indicate that an event has occurred.

The power supply also clears the STATUS and ALARM registers after a successful read back of the information in these registers, with the exception of communications error alarms. This automated process improves communications efficiency since the host controller does not have to issue another clear_faults command to clear these registers.

Dual, redundant buses: Two independent I²C lines provide true communications bus redundancy and allow two independent controllers to sequentially control the power supply. For example, a short or an open connection in one of the I²C lines does not affect communications capability on the other I²C line. Failure of a 'master' controller does not affect the power supplies and the second 'master' can take over control at any time.

Using the PCA9541 multiplexer: Transition between the two I²C lines is provided by the PCA9541 I²C/01 master selector multiplexer, which, upon start-up, connects channel 0. Applications using only a single I²C line can immediately start talking across the bus without first requiring to reconfigure the multiplexer.

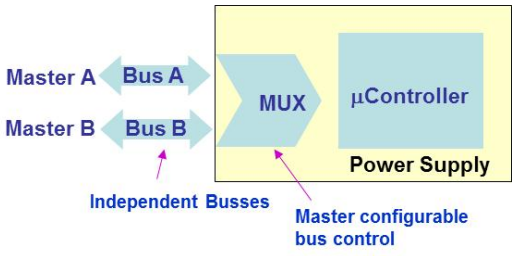


Diagram showing the dual I²C bus system.

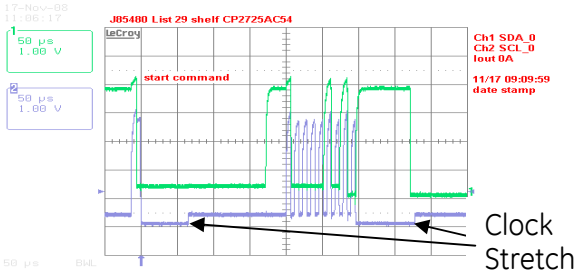
Control can be taken over at any time by a specific 'master' even during data transmission to the other 'master'. The 'master' needs to be able to handle incomplete transmissions in the multi-master environment in case switching should commence in the middle of data transmission.

Master/Slave: The 'host controller' is always the MASTER. Power supplies are always SLAVES. SLAVES cannot initiate communications or toggle the Clock. SLAVES also must respond expeditiously at the command of the MASTER as required by the clock pulses generated by the MASTER.

Clock stretching: The 'slave' µController inside the power supply may initiate clock stretching if it is busy and it desires to delay the initiation of any further communications. During the clock stretch the 'slave' may keep the clock LO until it is ready to receive further instructions from the host controller. The maximum clock stretch interval is 25ms.

The host controller needs to recognize this clock stretching, and refrain from issuing the next clock signal, until the clock line is released, or it needs to delay the next clock pulse beyond the clock stretch interval of the power supply.

Note that clock stretching can only be performed after completion of transmission of the 9th ACK bit, the exception being the START command.



Example waveforms showing clock stretching.

Communications speed: Both 100kHz and 400kHz clock rates are supported. The power supplies default to the 100kHz clock rate.

Packet Error Checking: The power supply will not respond to commands without the trailing PEC. The integrity of communications is compromised if packet error correction is not employed. There are many functional features, including turning OFF the main output, that require validation to ensure that the correct command is executed.

PEC is a CRC-8 error-checking byte, based on the polynomial $C(x) = x^8 + x^2 + x + 1$, in compliance with PMBus™ requirements. The calculation is based in all message bytes, including the originating write address and command bytes preceding read instructions. The PEC is appended to the message by the device that supplied the last byte.

SMBusAlert#: The power supply can issue SMBAlert# driven from either its internal micro controller (µC) or from the PCA9541 I²C bus master selector. That is, the SMBAlert# signal of the internal µC funnels through the PCA9541 master selector that buffers the SMBAlert# signal and splits the signal to the two SMBAlert# signal pins exiting the power supply. In addition, the PCA9541 signals its own SMBAlert#

request to either of the two SMBAlert# signals when required.

Non-supported commands: Non supported commands are flagged by setting the appropriate STATUS bit and issuing an SMBAlert# to the 'host' controller.

Data out-of-range: The power supply validates data settings and sets the data out-of-range bit and SMBAlert# if the data is not within acceptable range.

SMBAlert# triggered by the µC: The µC driven SMBAlert# signal informs the 'master/host' controller that either a STATE or ALARM change has occurred. Normally this signal is HI. The signal will change to its LO level if the power supply has changed states and the signal will be latched LO until the power supply receives a 'clear' instruction as outlined below. If the alarm state is still present after the 'clear_faults' command has been received, then the signal will revert back into its LO level again and will latch until a subsequent 'clear' signal is received from the host controller.

The signal will be triggered for any state change, including the following conditions;

- VIN under or over voltage
- Vout under or over voltage
- IOUT over current
- Over Temperature warning or fault
- Fan Failure
- Communication error
- PEC error
- Invalid command
- Internal faults

The power supply will clear the SMBusAlert# signal (release the signal to its HI state) upon the following events:

- Completion of a 'read_status' instruction
- Receiving a CLEAR_FAULTS command
- The main output recycled (turned OFF and then ON) via the ENABLE signal pin
- The main output recycled (turned OFF and then ON) by the OPERATION command

SMBAlert# triggered by the PCA9541: If clearing the Alert# signal via the clear_faults or read back fails, then reading back the Alert# status of the PCA9541 will be necessary followed by clearing of the PCA9541 Alert#.

The PCA9541 can issue an Alert# even when single bus operation is selected where the bus master selector has not been used or addressed. This may occur because the default state of the PCA9541/01 integrated circuit issues Alert# to both i^2C lines for all possible transitioning states of the device. For example, a RESET caused by a glitch would cause the Alert# to be active.

If the PCA9541 is not going to be used in a specific application (such as when only a single I^2C line is utilized), it is imperative that interrupts from the PCA9541 are de-activated by the host controller. To de-activate the interrupt registers the PCA9541 the 'master' needs to address the PCA9541 in the 'write' mode, the interrupt enable (IE) register needs to be accessed and the interrupt masks have to be set to HI '1'. (Note: do not mask bit 0 which transmits Alert# from the power supply). This command setting the interrupt enable register of the PCA9541 is shown below;

Start	Unit Address								ACK
1	7	6	5	4	3	2	1	0	1
S	1	1	1	0	A2	A1	A0	0	A

Command Code	ACK	IE Register	Stop
8	1	8	
0x00	A	0x0E	P

There are two independent interrupt enable (IE) registers, one for each controller channel (I^2C-0 and I^2C-1). The interrupt register of each channel needs to be configured independently. That is, channel I^2C-0 cannot configure the IE register of I^2C-1 or vise-versa.

This command has to be initiated to the PC9541 only once after application of power to the device. However, every time a restart occurs the PCA9541 has to be reconfigured since its default state is to issue Alert# for changes to its internal status.

If the application did not configure the interrupt enable register the Alert# line can be cleared (de-activated), if it has been activated by the PCA9541, by reading back the data from the interrupt status registers (Istat).

Refer to the PCA9541 data sheet for further information on how to communicate to the PCA9541 multiplexer.

Please note that the PCA9541 does not support Packet Error Checking (PEC).

Re-initialization: The I^2C code is programmed to re-initialize if no activity is detected on the bus for 5 seconds. Re-initialization is designed to guarantee that the I^2C µController does not hang up the bus. Although this rate is longer than the timing requirements specified in the SMBus specification, it had to be extended in order to ensure that a re-initialization would not occur under normal transmission rates. During the few µseconds required to accomplish re-initialization the I^2C µController may not recognize a command sent to it. (i.e. a start condition).

Global broadcast: This is a powerful command because it can instruct all power supplies to respond simultaneously in one command. But it does have a serious disadvantage. Only a single power supply needs to pull down the ninth *acknowledge* bit. To be certain that each power supply responded to the global instruction, a *READ* instruction should be executed to each power supply to verify that the command properly executed. The GLOBAL BROADCAST command should only be executed for write instructions to slave devices.

Note: The PCA9541 i2c master selector does not respond to the GLOBAL BROADCAST command.

Read back delay: The power supply issues the SMBAlert # notification as soon as the first state change occurred. During an event a number of different states can be transitioned to before the final event occurs. If a read back is implemented rapidly by the host a successive SMBAlert# could be triggered by the transitioning state of the power supply. In order to avoid successive SMBAlert# s and read back and also to avoid reading a transitioning state, it is prudent to wait more than 2 seconds after the receipt of an SMBAlert# before executing a read back. This delay will

ensure that only the final state of the power supply is captured.

Successive read backs: Successive read backs to the power supply should not be attempted at intervals faster than every one second. This time interval is sufficient for the internal processors to update their data base so that successive reads provide fresh data.

Device ID: Address bits A2, A1, A0 set the specific address of the power supply. The least significant bit x (LSB) of the address byte configures write [0] or read [1] events. In a ***write*** command the system instructs the power supply. In a ***read*** command information is being accessed from the power supply.

	Address Bit							
	7	6	5	4	3	2	1	0
PCA9541	1	1	1	0	A2	A1	A0	R/W
Micro controller	1	0	0	0	A2	A1	A0	R/W
External EEPROM	1	0	1	0	A2	A1	A0	R/W
Global Broadcast	0	0	0	0	0	0	0	0
	MSB							LSB

The **Global Broadcast** instruction executes a simultaneous ***write*** instruction to all power supplies. A ***read*** instruction cannot be accessed globally. The three programmable address bits are the same for all I^2C accessible devices within the power supply.

PMBus™ Commands

Standard instruction: Up to two bytes of data may follow an instruction depending on the required data content. Analog data is always transmitted as LSB followed by MSB. PEC is mandatory and includes the address and data fields.

1	8		1	8	1
S	Slave address	Wr	A	Command Code	A

8	1	8	1	8	1	1
Low data byte	A	High data byte	A	PEC	A	P

☐ Master to Slave ☐ Slave to Master
SMBUS annotations; S – Start , Wr – Write, Sr – re-Start, Rd – Read,
A – Acknowledge, NA – not-acknowledged, P – Stop

Direct mode data format: The Direct Mode data format is supported, where y = [mX + b] x 10^R. In the equation, y is the data value from the controller and x is the 'real' value either being set or returned.

For example, to set the output voltage to 50.45V_{DC}, Multiply the desired set point by the m constant, 50.45 x 400 = 20,180. Convert this binary number to its hex equivalent: 20,180b = 0x4ED4. The result is sent LSB=0xD4 first, then MSB=0x4E.

The constants are

FUNCTION	Operation	m	b	R
Output voltage Output voltage shutdown	Write / read	400	0	0
Output Current	read	5	0	0
Temperature	read	1	0	0
Input Voltage	read	1	75	0
Input Power	read	1	0	0
Fan Speed setting (%)	read	1	0	0
Fan speed in RPM	read	100	0	0

PMBus™ Command set:

Command	Hex Code	Data Field	Function
Operation	01	1	Output ON/OFF
Clear_Faults	03	0	Clear Status
Vout_command	21	2	Set Vout
Vout_OV_fault_limit	40	2	Set OV fault limit
Read_status	D0	10	Read Status, V_{out}, I_{out}, T
LEDs test ON	D2	0	Test LEDs
LEDs test OFF	D3	0	
Service_LED_ON	D4	0	Service LED
Service_LED_OFF	D5	0	
Enable_write	D6	0	Enable EEPROM write
Disable_write	D7	0	Disable EEPROM write
Inhibit_restart	D8	0	Latch upon failure
Auto_restart	D9	0	Hiccup
Isolation_test	DA	0	Perform isolation test
Read_input_string	DC	2	Read Vin and Pin
Read_firmware_rev	DD	3	Firmware revisions
Read_run_timer	DE	3	Accumulated ON state
Fan_speed_set	DF	3	Fan speed control
Fan_normal_speed	E0	0	Stop fan control
Read_fan_speed	E1	4	Fan control & speed
Stretch_LO_25ms	E2	0	Production test feature

Command Descriptions

Operation (01h) : By default the Power supply is turned **ON** at power up as long as *ENABLE* is active LO. The Operation command is used to turn the Power Supply ON or OFF via the PMBus. The data byte below follows the OPERATION command.

FUNCTION	DATA BYTE
Unit ON	0x80
Unit OFF	0x00

To **RESET** the power supply cycle the power supply OFF, wait at least 2 seconds, and then turn back ON. All alarms and shutdowns are cleared during a restart.

Clear_faults (03h): This command clears information bits in the STATUS registers, these include:

- Isolation OK
- Isolation test failed
- Restarted OK
- Invalid command
- Invalid data
- PEC error

Vout_Command (21h) : This command is used to change the output voltage of the power supply. Changing the output voltage should be performed simultaneously to all power supplies operating in parallel using the Global Address (Broadcast) feature. If only a single power supply is instructed to change its output, it may attempt to source all the required power which can cause either a power limit or shutdown condition.

Software programming of output voltage overrides the set point voltage configured during power_up. The program no longer looks at the 'margin pin' and will not respond to any hardware voltage setting. The default state cannot be accessed any longer unless power is removed from the DSP.

To properly hot-plug a power supply into a live backplane, the system generated voltage should get re-configured into either the factory adjusted firmware level or the voltage level reconfigured by the margin pin. Otherwise, the voltage state of the plugged in power supply could be significantly different than the powered system.

Voltage margin range: $42V_{DC}$ – 58 V_{DC}.

A voltage programming example: The task: set the output voltage to $50.45V_{DC}$

The constants for voltage programming are: m = 400, b and R = 0. Multiply the desired set point by the m constant, 50.45 x 400 = 20,180. Convert this binary number to its hex equivalent: 20,180b = 4ED4h. Transmit the data LSB first, followed by MSB,
0 x D44Eh.

Vout_OV_fault_limit (40h) : This command sets the Output Overvoltage Shutdown level.

Manufacturer-Specific PMBus™ Commands

Many of the manufacturer-specific commands read back more than two bytes. If more than two bytes of data are returned, the standard SMBus™ Block read is utilized. In this process, the Master issues a Write command followed by the data transfer from the power supply. The first byte of the Block Read data field sends back in hex format the number of data bytes, exclusive of the PEC number, that follows. Analog data is always transmitted LSB followed by MSB. A No-ack following the PEC byte signifies that the transmission is complete and is being terminated by the 'host'.

Read_status (D0h) : This 'manufacturer specific' command is the basic read back returning STATUS and ALARM register data, output voltage, output current, and internal temperature data in a single read.

1	8		1	8	1
S	Slave address	Wr	A	Command Code	A

1	8		1	8	1
Sr	Slave address	Rd	A	Byte count = 9	A

8	1	8	1	8	1
Status-2	A	Status-1	A	Alarm-2	A

8	1	8	1	8	1
Alarm-1	A	Voltage LSB	A	Voltage MSB	A

8	1	8	1	8	1	1
Current	A	Temperature	A	PEC	NA	P

Status and alarm registers

The content and partitioning of these registers is significantly different than the standard register set in the PMBus™ specification. More information is provided by these registers and they are accessed rapidly, at once, using the 'multi parameter' read back scheme of this document. There are a total of four registers. All errors, 0 – normal, 1 – alarm.

Status-2

Bit	Title	Description
7	PEC Error	Mismatch between computed and transmitted PEC. The instruction has not been executed. Clear_Flags resets this register.
6	Will Restart	Restart after a shutdown = 1
5	Invalid Instruction	The instruction is not supported. An ALERT# will be issued. Clear_Flags resets this register.
4	Power Capacity	n/a
3	Isolation test failed	Information only to system controller
2	Restarted ok	Informs HOST that a successful RESTART occurred clearing the status and alarm registers
1	Data out of range	Flag appears until the data value is within range. A clear_flags command does not reset this register until the data is within normal range.
0	Enable pin HI	State of the ENABLE pin, HI = 1 = OFF

Isolation test failed: The 'system controller' has to determine that sufficient capacity exists in the system to take a power supply 'off line' in order to test its isolation capability. Since the power supply cannot determine whether sufficient redundancy is available, the results of this test are provided, but the 'internal fault' flag is not set.

Status-1

Bit	Title	Description
7	spare	
6	Isolation test OK	Isolation test completed successfully.
5	Internal fault	The power supply is faulty
4	Shutdown	
3	Service LED ON	ON = 1
2	External fault	the power supply is functioning OK
1	LEDs flashing	LEDs tested test ON = 1
0	Output ON	ON = 1

Alarm-2

Bit	Title	Description
7	Fan Fault	
6	No primary	No primary detected
5	Primary OT	Primary section OT
4	DC/DC OT	DC/DC section OT
3	Output voltage lower than bus	Internal regulation failure
2	Thermal sensor failed	Internal failure of a temperature sensing circuit
1	5V out_of_limits	Either OVP or OCP occurred
0	Power delivery	a power delivery fault occurred

Power Delivery: The power supply compares its internal sourced current to the current requested by the current share pin. If the difference is > 10A, a fault is issued.

Alarm-1

Bit	Title	Description
7	Unit in power limit	An overload condition that results in constant power
6	Primary fault	Indicates either primary failure or INPUT not present. Used in conjunction with bit-0 and Status_1 bits 2 and 5 to assess the fault.
5	Over temp. shutdown	One of the over_temperature sensors tripped the supply
4	Over temp warning	Temperature is too high, close to shutdown
3	In over current	Shutdown is triggered by low output voltage < 39V_{DC}.
2	Over voltage shutdown	
1	Vout out_of_limits	Indication the output is not within design limits. This condition may or may not cause an output shutdown.
0	Vin out_of_limits	The input voltage is outside design limits

LEDS test ON (D2h) : Will turn-ON simultaneously the four front panel LEDs of the Power supply sequentially 7 seconds ON and 2 seconds OFF until instructed to turn OFF. The intent of this function is to provide visual identification of the power supply being talked to and also to visually verify that the LEDs operate and driven properly by the micro controller.

LEDS test OFF (D3h) : Will turn-OFF simultaneously the four front panel LEDs of the Power supply.

Service LED ON (D4h) : Requests the power supply to ***flash***-ON the Service (ok-to-remove) LED. The ***flash*** sequence is approximately 0.5 seconds ON and 0.5 seconds OFF.

Service LED OFF (D5h) : Requests the power supply to turn OFF the Service (ok-to-remove) LED.

Enable write (D6h) : This command enables write permissions into the upper ¼ of memory locations for the external EEPROM. A write into these locations is normally disabled until commanded through I^2C to permit writing into the protected area. A delay of about 10ms is required from the time the instruction is requested to the time that the power supply actually completes the instruction.

See the FRU-ID section for further information of content written into the EEPROM at the factory.

Disable write (D7h) : This command disables write permissions into the upper ¼ of memory locations for the external EEPROM.

Unit in Power Limit or in Current Limit: When output voltage is > 36V_{DC} the Output LED will continue blinking. When output voltage is < 36V_{DC}, if the unit is in the RESTART mode, it goes into a hiccup. When the unit is ON the output LED is ON, when the unit is OFF the output LED is OFF.

When the unit is in latched shutdown the output LED is OFF.

Inhibit_restart (D8h) : The **Inhibit-restart** command directs the power supply to remain latched off for over_voltage, over_temperature and over_current. The command needs to be sent to the power supply only once. The power supply will remember the INHIBIT instruction as long as internal bias is active.

Restart after a lachoff: To restart after a latch_off either of four restart mechanisms are available. The hardware pin **Enable** may be turned OFF and then ON**.** The unit may be commanded to restart via i2c through the *Operation* command by first turning OFF then turning ON . The third way to restart is to remove and reinsert the unit. The fourth way is to turn OFF and then turn ON ac power to the unit. The fifth way is by changing firmware from **latch off** to **restart.** Each of these commands must keep the power supply in the OFF state for at least 2 seconds, with the exception of changing to **restart**.

A successful restart shall clear all alarm registers, set the **restarted successful** bit of the ***Status_2*** register.

A power system that is comprised of a number of power supplies could have difficulty restarting after a shutdown event because of the non-synchronized behavior of the individual power supplies. Implementing the latch-off mechanism permits a synchronized restart that guarantees the simultaneous restart of the entire system.

A synchronous restart can be implemented by;

1. Issuing a GLOBAL OFF and then ON command to all power supplies,
2. Toggling Off and then ON the ENABLE signal
3. Removing and reapplying input commercial power to the entire system.

The power supplies should be turned OFF for at least 20 – 30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual power supplies.

Auto_restart (D9h) : Auto-restart is the default configuration for overvoltage, overcurrent and overtemperature shutdowns.

However, overvoltage has a unique limitation. An overvoltage shutdown is followed by three attempted restarts, each restart delayed 1 second, within a 1 minute window. If within the 1 minute window three attempted restarts failed, the unit will latch OFF. If within the 1 minute less than 3 shutdowns occurred then the count for latch OFF resets and the 1 minute window starts all over again.

This command resets the power supply into the default auto-restart configuration.

Isolation test (DAh): This command verifies functioning of output OR'ing. At least two paralleled power supplies are required. The host should verify that N+1 redundancy is established. If N+1 redundancy is not established the test can fail. Only one power supply should be tested at a time.

Verifying test completion should be delayed for approximately 30 seconds to allow the power supply sufficient time to properly execute the test.

Failure of the isolation test is not considered a power supply FAULT because the N+1 redundancy requirement cannot be verified. The user must determine whether a true isolation fault indeed exists.

Read input string (DCh) : Reads back the input voltage and input power consumed by the power supply. In order to improve the resolution of the input voltage reading the data is shifted by 75V.

1	7	1	1	8
S	Slave address	Wr	A	Command Code 0xDC

1	1	7	1	1
A	Sr	Slave Address	Rd	A

8	1	8	1
Byte Count = 4	A	Voltage	A

8	1	8	1	8	1	1
Power - LSB	A	Power - MSB	A	PEC	No-ack	P

Read_firmware_rev [0 x DD]: Reads back the firmware revision of all three µC in the power supply.

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code 0xDD	A

1	1	7	1	1	8	1
A	Sr	Slave Address	Rd	A	Byte Count = 4	A

8	1	8	1
Primary micro revision	A	DSP revision	A

8	1	8	1	1
I2c Micro revision	A	PEC	No-ack	P

For example; the read returns one byte for each device (i.e. 0 x 002114h). The sequence is primary micro, DSP, and I²C micro. 0x00 in the first byte indicates that revision information for the primary micro is not supported. The number 21 for the DSP indicates revision 2.1, and the number 14 for the i2c micro indicates revision 1.4.

Read_run_timer [0 x DE]: This command reads back the recorded operational ON state of the power supply in hours. The operational ON state is accumulated from the time the power supply is initially programmed at the factory. The power supply is in the operational ON state both when in standby and when it delivers main output power. Recorded capacity is approximately 10 years of operational state.

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code 0xDE	A

1	7	1	1	8	1
Sr	Slave Address	Rd	A	Byte count = 4	A

8	1	8	1	8	1
Time - LSB	A	Time	A	Time - MSB	A

8	1	1
PEC	No-ack	P

Fan_speed_set (DFh) : This command instructs the power supply to increase the speed of the fan. The transmitted data byte represents the hex equivalent of the duty cycle in percentage, i.e. 100% = 0 x 64h. The command can only increase fan speed, it cannot instruct the power supply to reduce the fan speed below what the power supply requires for internal control.

Fan_normal_speed (E0h): This command returns fan control to the power supply. It does not require a trailing data byte.

Read_Fan_speed (E1h) : Returns the commanded fan speed in percent and the measured fan speed in RPM from the individual fans. Up to 3 fans are supported. If a fan does not exist (units may contain from 1 to 3 fans), or if the command is not supported the unit return 0x00.

1	8	1	8	1
S	Slave address	Wr	A	Command 0xE1	A

1	8	1	8	1
Sr	Slave address	Rd	A	Byte count = 5	A

8	1	8	1	8	1	8	1
Adjustment %	A	Fan-1	A	Fan-2	A	Fan-3	A

8	1	1
PEC	NA	P

Stretch_LO_25ms (E2h) : Command used for production test of the clock stretch feature.

None supported commands or invalid data: The power supply notifies the MASTER if a non-supported command has been sent or invalid data has been received. Notification is implemented by setting the appropriate STATUS and ALARM registers and setting the SMBAlert# flag.

Fault Management

The power supply records faults in the STATUS and ALARM registers above and notifies the *MASTER* controller as described in the **Alarm Notification** section of the non-conforming event.

The STATUS and ALARM registers are continuously updated with the latest event registered by the rectifier monitoring circuits. A *host* responding to an SMBusALERT# signal may receive a different state of the rectifier if the state has changed from the time the SMBusALERT# has been triggered by the rectifier.

The power supply differentiates between **internal faults** that are within the power supply and **external faults** that the power supply protects itself from, such as overload or input voltage out of limits. The FAULT LED, FAULT PIN or i2c alarm is not asserted for EXTERNAL FAULTS. Every attempt is made to annunciate External Faults. Some of these annunciations can be observed by looking at the input LEDs. These fault categorizations are predictive in nature and therefore there is a likelihood that a categorization may not have been made correctly.

Input voltage out of range: The Input LED will continue blinking as long as sufficient power is available to power the LED. If the input voltage is completely gone the Input LED is OFF.

State Change Definition

A **state_change** is an indication that an event has occurred that the MASTER should be aware of. The following events shall trigger a **state_change**;

- Initial power-up of the system when AC gets turned ON . This is the indication from the rectifier that it has been turned ON. Note that the master needs to read the status of each power supply to reset the system_interrupt. If the power supply is back-biased through the 8V_INT or the 5VSTB it will not issue an SMBALERT# when AC power is turned back ON.
- Whenever the power supply gets hot-plugged into a working system. This is the indicator to the system (MASTER) that a new power supply is on line.
- Any changes in the bit patterns of the STATUS and ALARM registers are a STATUS change which triggers the SMBALERT# flag. Note that a host-issued command such as CLEAR_FAULTS will not trigger an SMB

Hot plug procedures

Careful system control is recommended when hot plugging a power supply into a live system. It takes about 15 seconds for a power supply to configure its address on the bus based on the analog voltage levels present on the backplane. If communications are not stopped during this interval, multiple power supplies may respond to specific instructions because the address of the hot plugged power supply always defaults to xxxx000 (depending on which device is being addressed within the power supply) until the power supply configures its address.

The recommended procedure for hot plug is the following: The system controller should be told which power supply is to be removed. The controller turns the service LED ON, thus informing the installer that the identified power supply can be removed from the system. The system controller should then poll the module_present signal to verify when the power supply is re-inserted. It should time out for 15 seconds after this signal is verified. At the end of the time out all communications can resume.

Predictive Failures

Alarm warnings that do not cause a shutdown are indicators of potential future failures of the power supply. For example, if a thermal sensor failed, a warning is issued but an immediate shutdown of the power supply is not warranted.

Another example of potential predictive failure mechanisms can be derived from information such as fan speed when multiple fans are used in the same power supply. If the speed of the fans varies by more than 20% from each other, this is an indication of an impending fan wear out.

The goal is to identify problems early before a protective shutdown would occur that would take the power supply out of service.

External EEPROM

A 64k-bit EEPROM is provided across the I^2C bus. This EEPROM is used for both storing FRU_ID information and for providing a scratchpad memory function for customer use.

Functionally the EEPROM is equivalent to the ST M34D64 part that has its memory partitioned into a *write protected* upper ¼ of memory space and the lower ¾ section that cannot be protected. FRU_ID is written into the *write protected* portion of memory.

Write protect feature: Writing into the upper 1/4 of memory can be accomplished either by hardware or software.

The power supply pulls down the write_protect (Wp) pin to ground via a 500Ω resistor between the 'module_present' signal pin and Logic_GRD (see the Module Present Signal section of Input Signals). Writing into the upper ¼ of memory can be accomplished by pulling HI the module_present pin.

An alternative, and the recommended approach, is to issue the Enable_write command via software.

Page implementation: The external EEPROM is partitioned into 32 byte pages. For a write operation only the starting address is required. The device automatically increments the memory address for each byte of additional data it receives. However, if the 32 byte limit is exceeded the device executes a wrap-around that will start rewriting from the first address specified. Thus byte 33 will replace the first byte written, byte 34 the second byte and so on. One needs to be careful therefore not to exceed the 32 byte page limitation of the device.

CP2000DC54-PE series dc-dc converter

Input: -40Vdc to -72Vdc; Outputs: ±54Vdc @ 2000W; 5Vdc @ 4W

Alarm Table

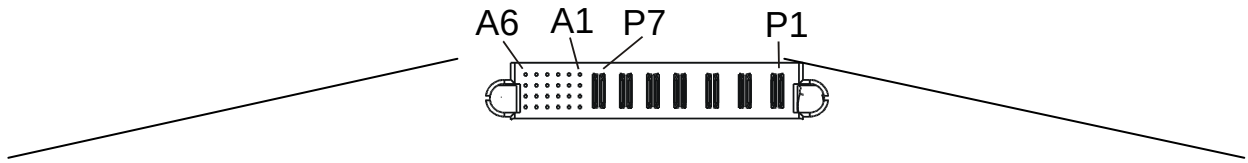
	Power Supply LED State					Monitoring Signals (Referenced to Logic_GRD)				
Condition	**IN OK** Green	**DC OK** Green	**Service** Amber	**Fault** Red		**Fault**	**OTW**	**Power OK**	**I_Limit**	**Module Present**
OK	1	1	0	0		HI	HI	HI	HI	LO
Thermal Alarm (5C before shutdown)	1	1	1	0		HI	LO	HI	HI	LO
Thermal Shutdown	1	0	1	1		LO	LO	LO	HI	LO
Defective Fan	1	0	0	1		LO	HI	LO	HI	LO
Blown Input Fuse in Unit	1	0	0	1		LO	HI	LO	HI	LO
No Input > 8mS (single unit)	0	1	0	0		HI	HI	LO[2]	HI	LO
Input Present but not within limits	0	0	0	0		HI	HI	LO	HI	LO
Input not present (with back bias)	0	0	0	0		HI	HI	LO	HI	LO
Over Voltage Latched Shutdown	1	0	0	1		LO	HI	LO	HI	LO
Over Current	1	Blinks	0	0		HI	HI	LO	LO	LO
Over Current Shutdown	1	0	0	0		HI	HI	LO	LO	LO
Non-catastrophic Internal Failure[1]	1	1	0	1		LO	HI	HI	HI	LO
1 Missing Module (external pull-up)										HI
Standby (remote)	1	0	0	0		HI	HI	LO	HI	LO
Service Request (i²C mode)	1	1	Blinks	0		HI	HI	HI	HI	LO

[1] Any detectable fault condition that does not result in the power supply shutting down. For example, ORing FET failure, boost section out of regulation, etc.

[2] Signal transition from HI to LO is output load dependent

Output Connector

Mating Connector: AMP 1450572-1



	Signal						Output Power		Input Power				
	6	5	4	3	2	1	P7	P6	P5	P4	P3	P2	P1
A	SCL_0	MOD_PRES	Ilimit	LOGIC_GRD	RS 485+	UNIT_ADDR	V_OUT (-DC)	V_OUT (+DC)	CO_RTN Vin (+)		EARTH (GND)	CO_LINE Vin (-)	
B	SCL_1	OTW	Alert#_0	Alert#_1	RS 485-	8V_INT							
C	SDA_0	Margin	Enable	Reset	Ishare	N/C							
D	SDA_1	Fault	5VA	Power_OK	ON/OFF	SHELF_ADDR							

Connector is viewed from the rear positioned inside the power supply.

Signal pins columns 1 and 2 are referenced to V_OUT (-DC). Signal pins columns 3 through 6 are referenced to Logic GRD.

Last-to-make first-to-break pins.

First-to-make last-to-break longest pin implemented in the mating connector.

N/C – no connect pins must be left open. Do not connect these pins to either voltage sources or ground.

Signal Definitions

All hardware alarm signals (Fault, Power_OK, I_Limit, OTW) are open drain FETs. These signals should be pulled HI to either 3.3V or 5V. Maximum sink current 5mA. An active LO signal (< 0.4Vdc) state is referenced to Logic GRD unless otherwise stated. Contact your Lineage Power representative for more details.

Function	Label	Type	Description
Output Enable	Enable	Input	If shorted to LOGIC_GRD, the PEM output is enabled when using I²C mode of operation. May also be toggled to reset a latched OFF PEM.
Output Good	Power_OK	Output	An open drain FET; normally HI, indicating output power is present. Changes to LO when the main output is OFF,
Current Limit	I_Limit	Output	An open drain FET; normally HI, indicating normal operation. Changes to LO when in current limit,
I²C Interrupt	Alert#_0 Alert#_1	Output	Interrupt signal via I²C lines indicating that service is requested from the host controller. This signal pin is pulled up to 3.3V via a 10kΩ resistor and switches to active LO when an interrupt occurs.
PEM Fault	Fault	Output	Indicates that an internal fault exists. An open drain FET; normally HI, changes to LO.
Module Present	MOD_PRES	Output	Used to Indicate presence of PEM.
ON/OFF	ON/OFF	Input	Short pin, connects last and breaks first; used to activate and deactivate output during hot-insertion and extraction, respectively. Ref: V_OUT (-DC)
Margining	Margin	Input	Allows changing of output voltage through an analog voltage input or via resistor divider.
Over-Temperature Warning	OTW	Output	An open drain FET; normally HI, changes to LO approximately 5°C prior to thermal shutdown.
PEM address	Unit_addr	Input	Voltage level addressing of PEMs within a single shelf. Ref: V_OUT (-DC).
Shelf Address	Shelf_addr	Input	Voltage level addressing of PEMs within multiple shelves. Ref: V_OUT (-DC).
Back bias	8V_INT	_	Diode OR'ed 8Vdc drain; used to back bias microprocessors and DSP of failed PEM from operating PEMs. Ref: V_OUT (-DC).
Mux Reset	Reset	Input	Resets the I²C lines to I²C line 0.
Standby power	5VA	Output	5V at 0.75A provided for external use by either adjacent power supplies or the using system.
Current Share	Ishare	-	A single wire interface between each of the power unit forces them to share the load current. Ref: V_OUT (-DC).
I²C Line 0	SCL_0, SDA_0	Input	I²C line 0.
I²C Line 1	SCL_1, SDA_1	Input	I²C line 1.

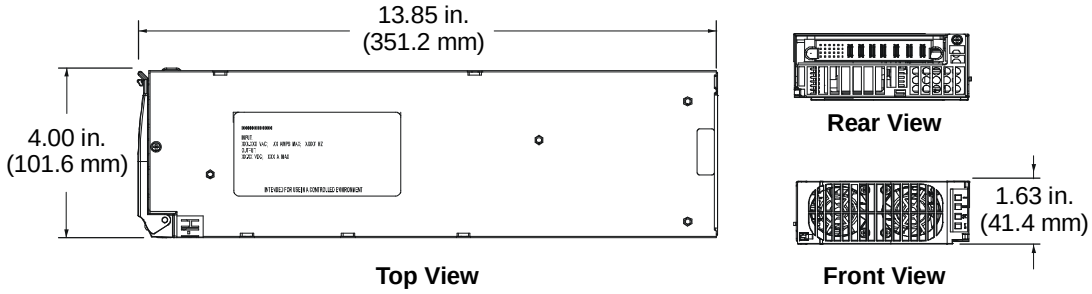
CP2000DC54-PE series dc-dc converter

Input: -40Vdc to -72Vdc; Outputs: ±54Vdc @ 2000W; 5Vdc @ 4W

Front Panel LEDs

	Analog Mode	I²C Mode
	←	**ON:** Input ok **OFF:** Input out of limits →
	←	**ON:** Output ok **Blinking:** Overload →
	Over-temperature Warning	**ON:** Over-temperature Warning **Blinking:** Service
	←	**ON:** Fault →

Dimensions



Ordering Information

Item	Description	Comcode
CP2000DC54-PE	Designed and factory tested to IEEE802.3af POE compliance, Auxiliary Output: 5Vdc at 0.75A.	CC109146692

Consult the 1U shelf data sheet for potential shelf configurations for this module from GE Energy.

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