

30V, N-Channel NexFET™ Power MOSFETs

Check for Samples: [CSD17305Q5A](#)

FEATURES

- Optimized for 5V Gate Drive
- Ultralow Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

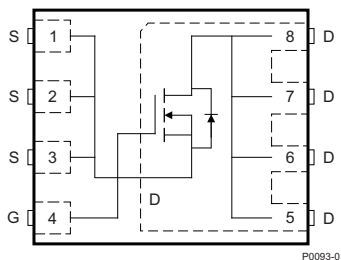
APPLICATIONS

- Notebook Point of Load
- Point-of-Load Synchronous Buck in Networking, Telecom and Computing Systems

DESCRIPTION

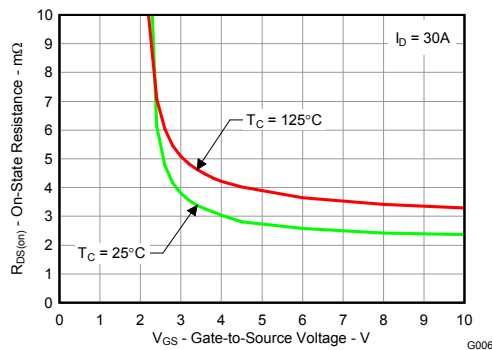
The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications, and optimized for 5V gate drive applications.

Top View



P0093-01

$R_{DS(on)}$ VS V_{GS}



PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	30	V
Q_g	Gate Charge Total (4.5V)	14.1	nC
Q_{gd}	Gate Charge Gate to Drain	3	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 3V$	3.9 mΩ
		$V_{GS} = 4.5V$	2.8 mΩ
		$V_{GS} = 8V$	2.4 mΩ
$V_{GS(th)}$	Threshold Voltage	1.1	V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD17305Q5A	SON 5-mm × 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

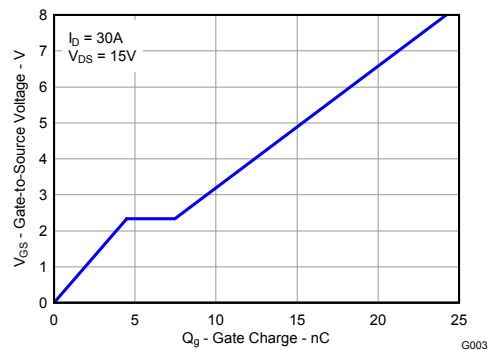
ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	+10 / -8	V
I_D	Continuous Drain Current, $T_C = 25^\circ\text{C}$	100	A
	Continuous Drain Current ⁽¹⁾	29	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ ⁽²⁾	181	A
P_D	Power Dissipation ⁽¹⁾	3.1	W
T_J , T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
E_{AS}	Avalanche Energy, single pulse $I_D = 78A$, $L = 0.1mH$, $R_G = 25\Omega$	304	mJ

(1) Typical $R_{\theta JA} = 40^\circ\text{C/W}$ on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$

GATE CHARGE



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

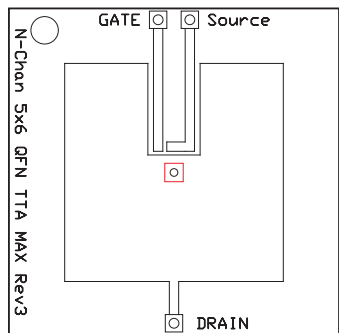
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV _{DSS}	Drain to Source Voltage	V _{GS} = 0V, I _D = 250μA	30			V
I _{DSS}	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = 24V			1	μA
I _{GSS}	Gate to Source Leakage Current	V _{DS} = 0V, V _{GS} = +10/-8V			100	nA
V _{GS(th)}	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	0.9	1.1	1.6	V
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 3V, I _D = 30A		3.9	5.4	mΩ
		V _{GS} = 4.5V, I _D = 30A		2.8	3.6	mΩ
		V _{GS} = 8V, I _D = 30A		2.4	3.4	mΩ
g _{fs}	Transconductance	V _{DS} = 15V, I _D = 30A		139		S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		2000	2600	pF
C _{oss}	Output Capacitance			1100	1430	pF
C _{rss}	Reverse Transfer Capacitance			79	103	pF
R _G	Series Gate Resistance			1	2	Ω
Q _g	Gate Charge Total (4.5V)	V _{DS} = 15V, I _D = 30A		14.1	18.3	nC
Q _{gd}	Gate Charge Gate to Drain			3		nC
Q _{gs}	Gate Charge Gate to Source			4.5		nC
Q _{g(th)}	Gate Charge at V _{th}			2.2		nC
Q _{oss}	Output Charge	V _{DS} = 13.5V, V _{GS} = 0V		27		nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 15V, V _{GS} = 4.5V, I _D = 30A R _G = 2Ω		8.9		ns
t _r	Rise Time			16.5		ns
t _{d(off)}	Turn Off Delay Time			20		ns
t _f	Fall Time			7.9		ns
Diode Characteristics						
V _{SD}	Diode Forward Voltage	I _{SD} = 30A, V _{GS} = 0V		0.85	1	V
Q _{rr}	Reverse Recovery Charge	V _{DD} = 13.5V, I _F = 30A, di/dt = 300A/μs		34		nC
t _{rr}	Reverse Recovery Time			27		ns

THERMAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

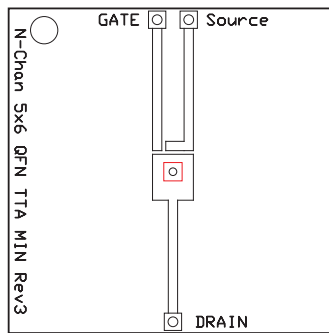
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case ⁽¹⁾			1.3	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ^{(1) (2)}			50	$^\circ\text{C/W}$

- $R_{\theta JC}$ is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch \times 1.5-inch (3.81-cm \times 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



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Max $R_{\theta JA} = 50^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of
2-oz. (0.071-mm thick)
Cu.

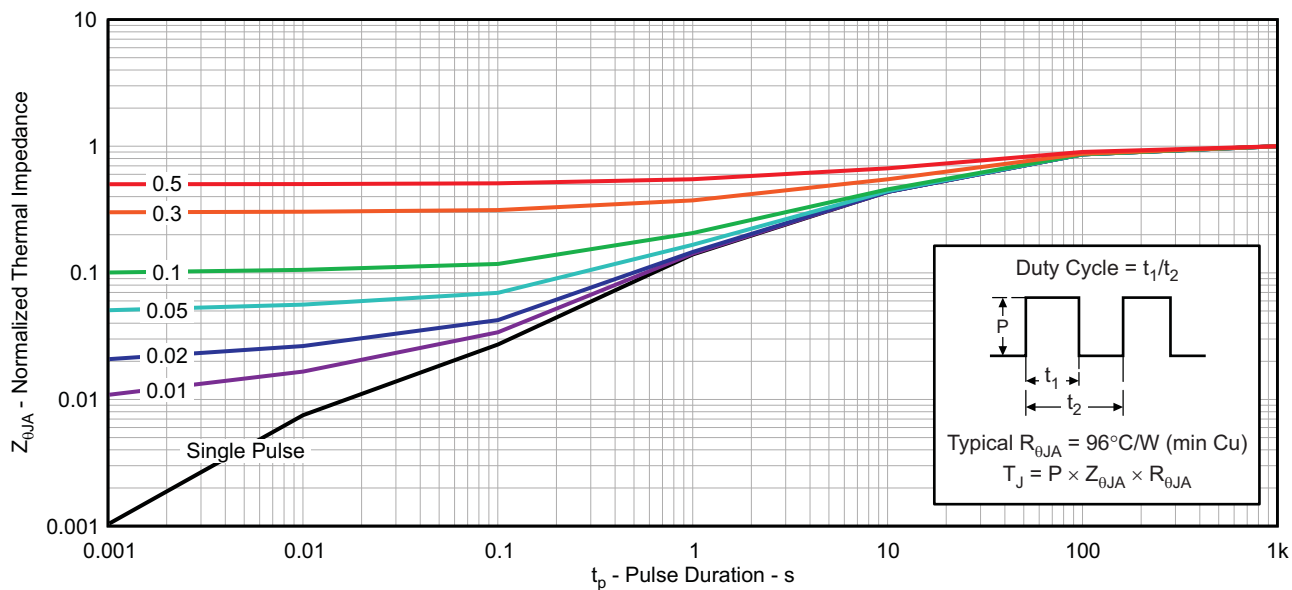


M0137-02

Max $R_{\theta JA} = 120^{\circ}\text{C/W}$
when mounted on a
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)

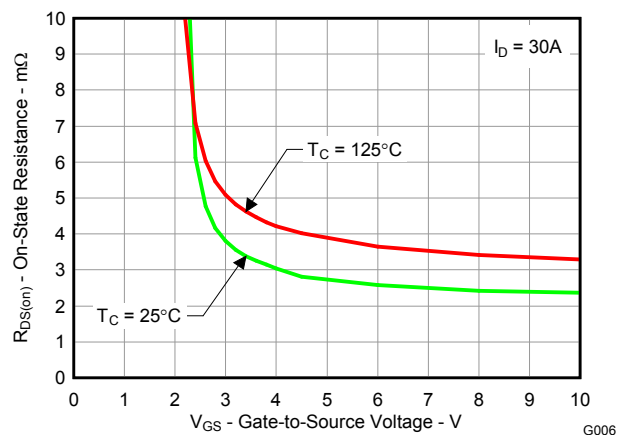
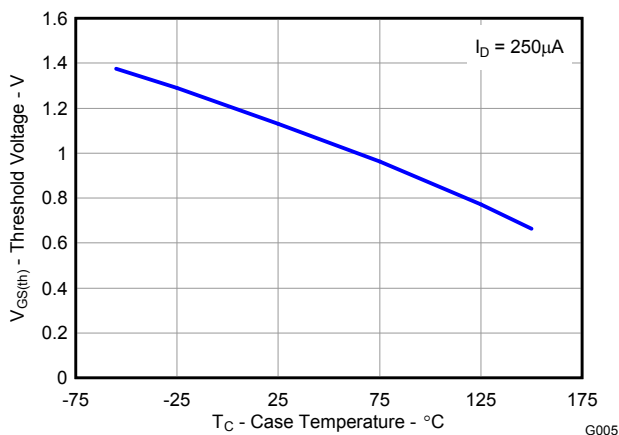
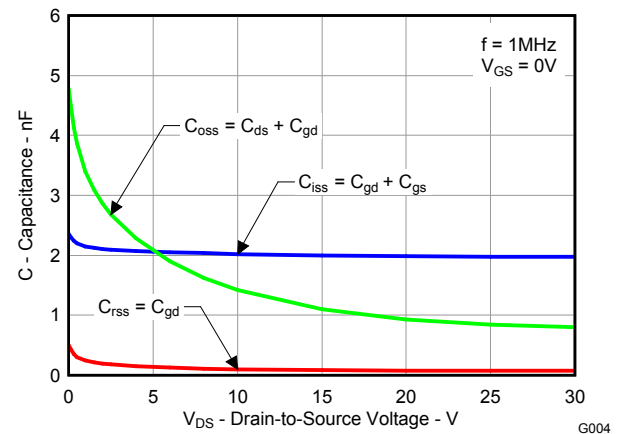
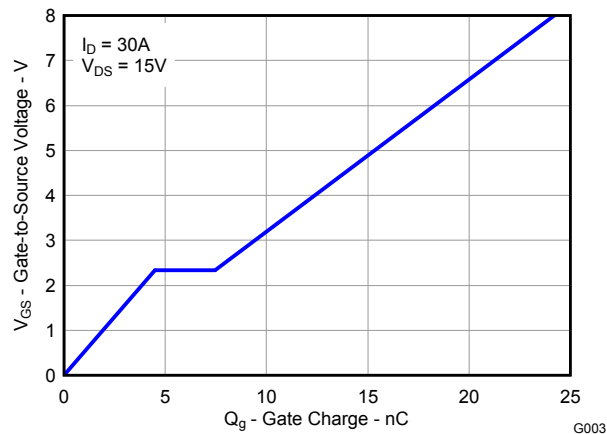
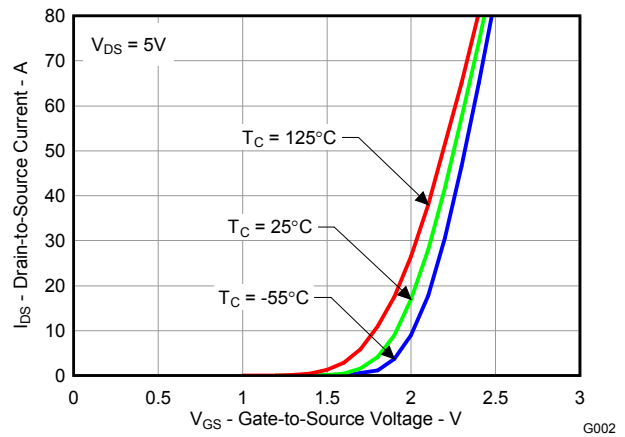
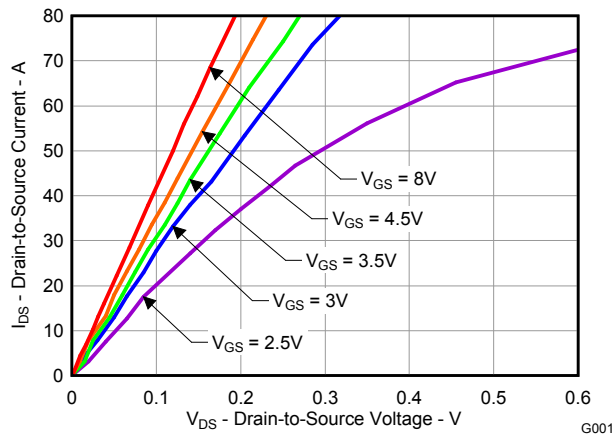


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Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)



TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

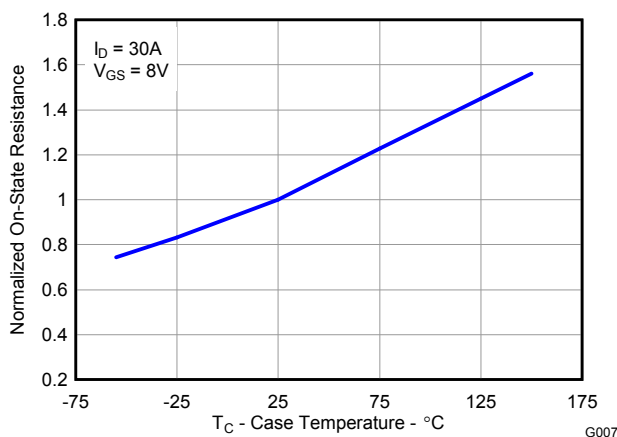


Figure 8. Normalized On-State Resistance vs. Temperature

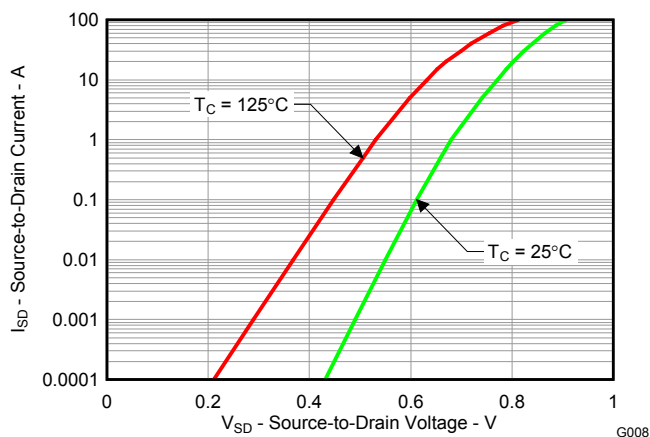


Figure 9. Typical Diode Forward Voltage

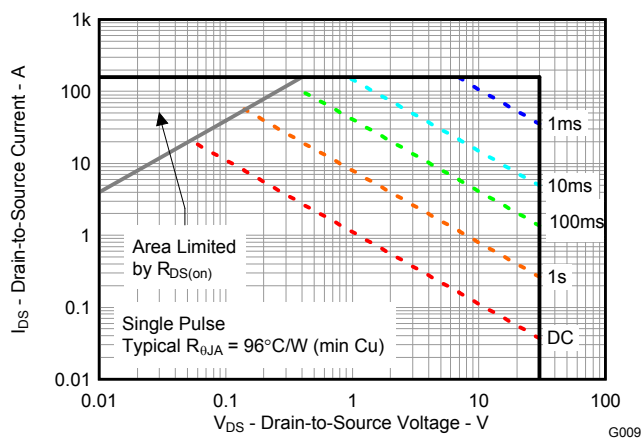


Figure 10. Maximum Safe Operating Area

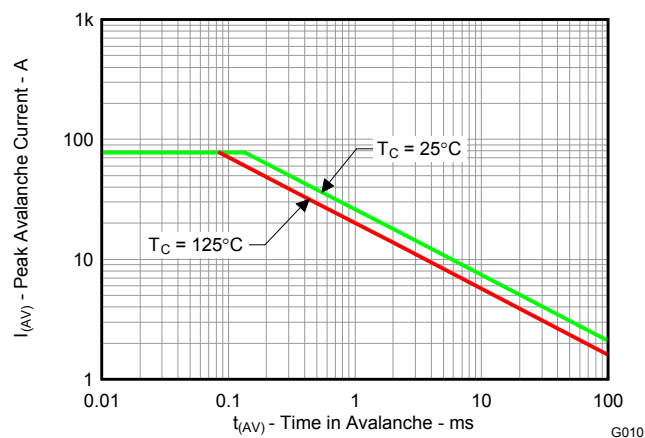


Figure 11. Single Pulse Unclamped Inductive Switching

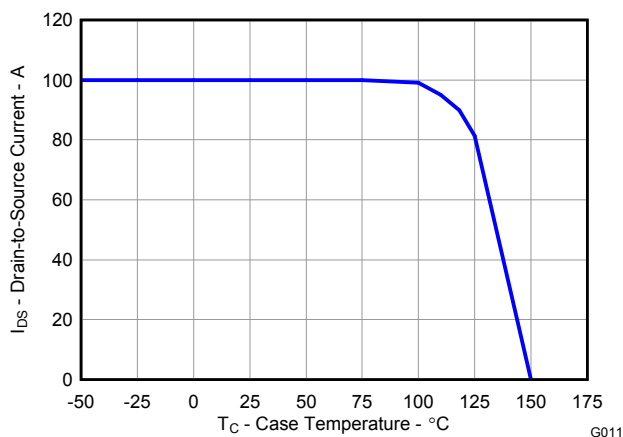
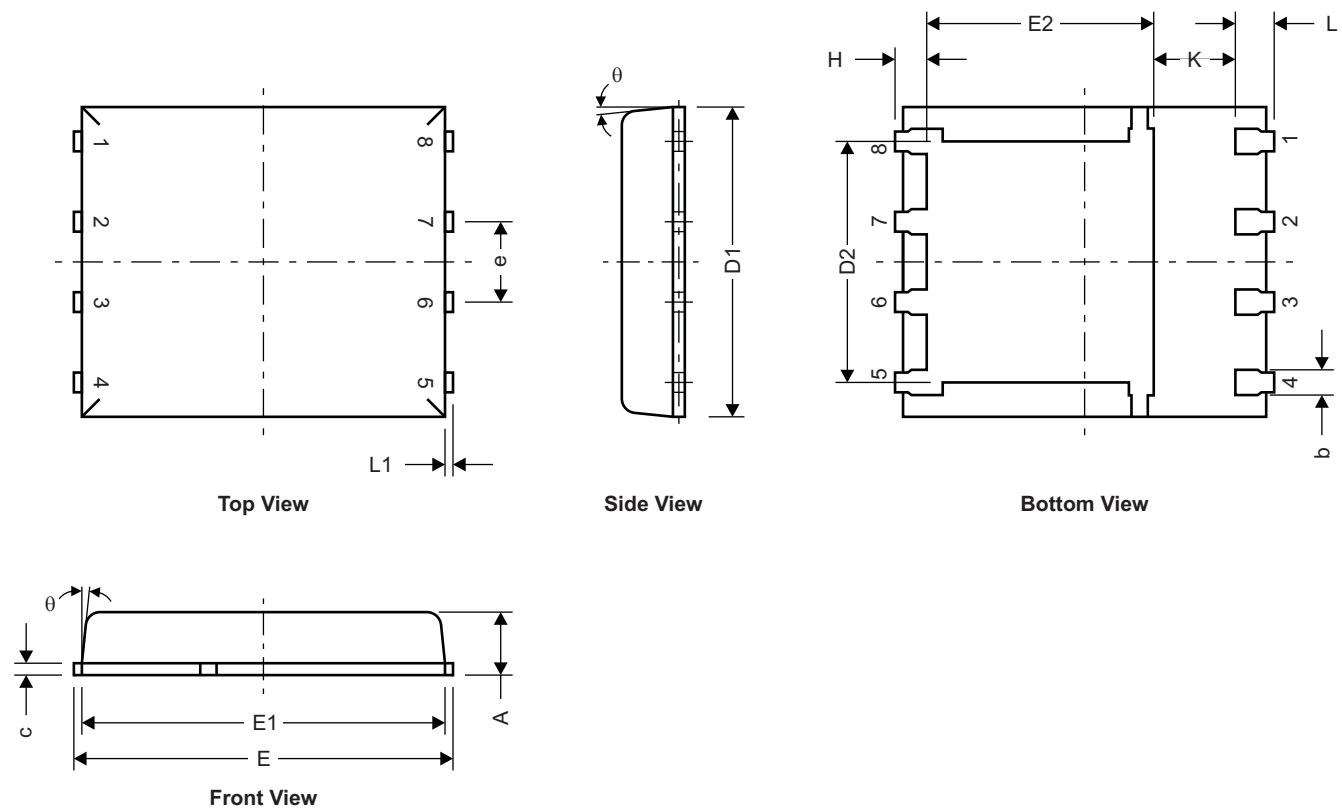


Figure 12. Maximum Drain Current vs. Temperature

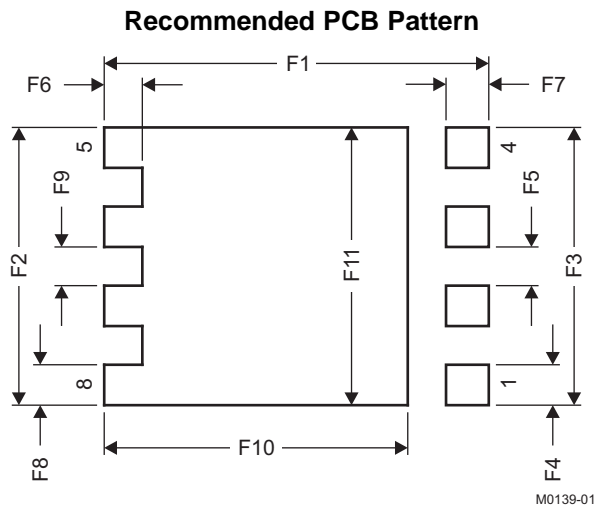
MECHANICAL DATA

Q5A Package Dimensions



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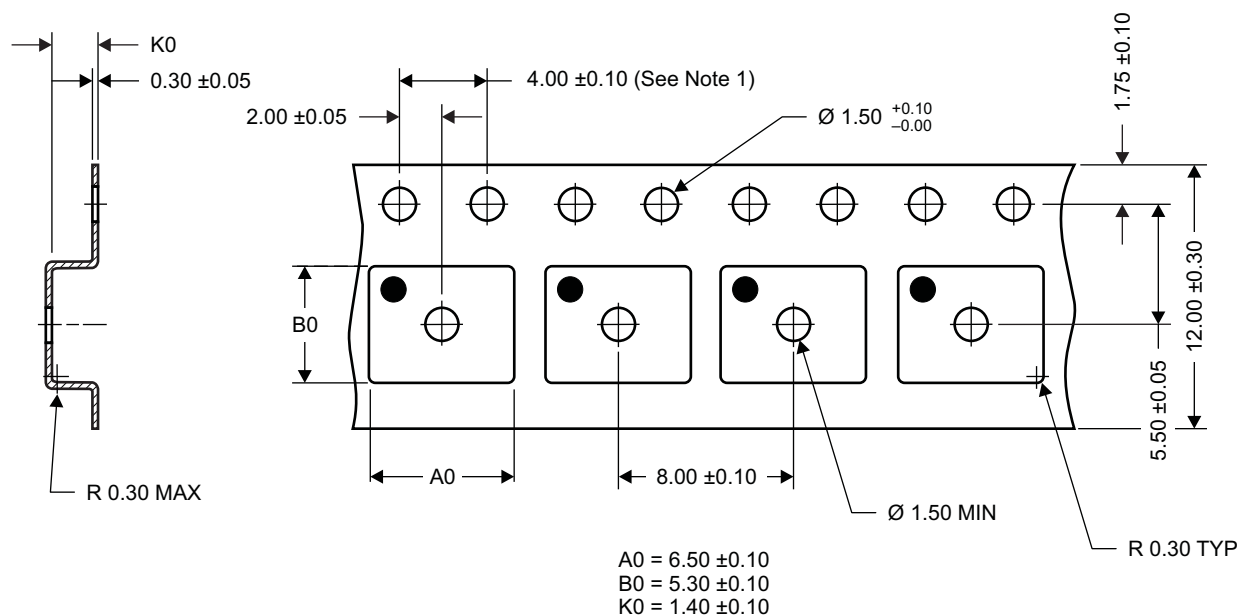
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.17	1.27	1.37
H	0.41	0.56	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
θ	0°		12°



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

Q5A Tape and Reel Information



Notes:

- 10-sprocket hole-pitch cumulative tolerance ± 0.2
- Camber not to exceed 1mm in 100mm, noncumulative over 250mm
- Material: black static-dissipative polystyrene
- All dimensions are in mm (unless otherwise specified)
- A0 and B0 measured on a plane 0.3mm above the bottom of the pocket

REVISION HISTORY

Changes from Original (February 2010) to Revision A	Page
<ul style="list-style-type: none">Updated the Q5A Package Dimensions table. DIM c MAX was 0.30, DIM D2 MAX was 3.96, DIM e MIN was blank MAX was blank, DIM H NOM was 0.51 MAX was 0.61	6
<ul style="list-style-type: none">Deleted Note 6 from the Q5A Tape and Reel Information - "MSL1 260°C (IR and convection) PbF reflow compatible"	7
<ul style="list-style-type: none">Deleted the Package Marking Information section	7

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD17305Q5A	SON	DQJ	8	2500	330.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1
CSD17305Q5A	SON	DQJ	8	2500	330.2	12.4	6.5	5.3	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD17305Q5A	SON	DQJ	8	2500	340.0	340.0	38.0
CSD17305Q5A	SON	DQJ	8	2500	347.0	342.0	55.0

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