CY2305C
CY2309C

3.3 V Zero Delay Clock Buffer

Features

- 10 MHz to 100–133 MHz operating range
- Zero input and output propagation delay
- Multiple low skew outputs
- One input drives five outputs (CY2305C)
- One input drives nine outputs, grouped as 4 + 4 + 1 (CY2309C)
- 50 ps typical cycle-to-cycle jitter (15 pF, 66 MHz)
- Test mode to bypass phase locked loop (PLL) (CY2309C) only, see Select Input Decoding on page 6
- Available in space saving 16-pin 150 Mil small outline integrated circuit (SOIC) or 4.4 mm thin shrunk small outline package (TSSOP) packages (CY2309C), and 8-pin, 150 Mil SOIC package (CY2305C)
- 3.3 V operation
- Commercial, industrial and automotive-A flows available

Functional Description

The CY2305C and CY2309C are die replacement parts for CY2305 and CY2309.

The CY2309C is a low-cost 3.3 V zero delay buffer designed to distribute high speed clocks and is available in a 16-pin SOIC or TSSOP package. The CY2305C is an 8-pin version of the CY2309C. It accepts one reference input and drives out five low skew clocks. The -1H versions of each device operate up to 100–133 MHz frequencies and have higher drive than the -1 devices. All parts have on-chip phase locked loops (PLLs) which lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad.

The CY2309C has two banks of four outputs each that are controlled by the select inputs as shown in the Select Input Decoding on page 6. If all output clocks are not required, Bank B is three-stated. The input clock is directly applied to the outputs by the select inputs for chip and system testing purposes.

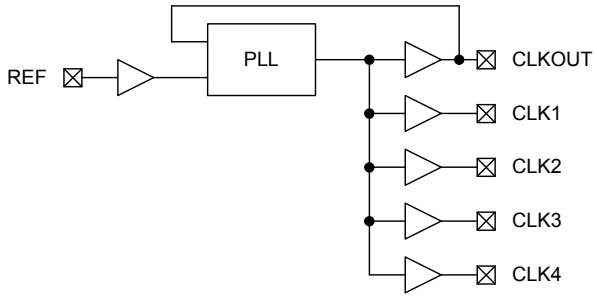
The CY2305C and CY2309C PLLs enter a power down mode when there are no rising edges on the REF input. In this state, the outputs are three-stated and the PLL is turned off. This results in less than 12.0 μA of current draw for commercial temperature devices and 25.0 μA for industrial and automotive-A temperature parts. The CY2309C PLL shuts down in one additional case as shown in the Select Input Decoding on page 6.

In the special case when S2:S1 is 1:0, the PLL is bypassed and REF is output from DC to the maximum allowable frequency. The part behaves as a non-zero delay buffer in this mode and the outputs are not three-stated.

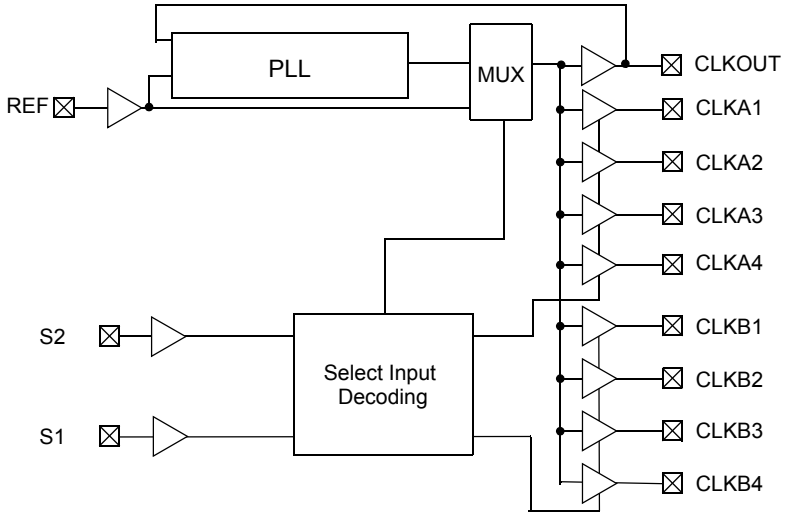
The CY2305C or CY2309C is available in two or three different configurations as shown in the Ordering Information on page 15. The CY2305C-1 or CY2309C-1 is the base part. The CY2305-1H or CY2309-1H is the high drive version of the -1. Its rise and fall times are much faster than the -1.

For a complete list of related documentation, click here.

Logic Block Diagram – CY2305C



Logic Block Diagram – CY2309C



Contents

Pinouts

Figure 1. 8-pin SOIC pinout (Top View)
CY2305C

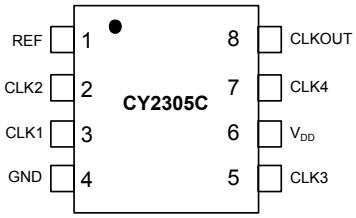
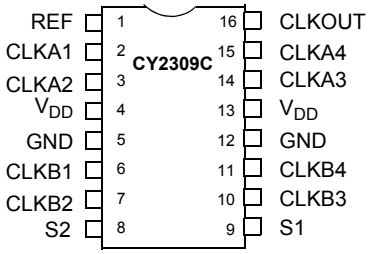


Figure 2. 16-pin SOIC / TSSOP pinout (Top View)
CY2309C



Pin Definitions

8-pin SOIC

Pin	Signal	Description
1	REF [1]	Input reference frequency
2	CLK2 [2]	Buffered clock output
3	CLK1 [2]	Buffered clock output
4	GND	Ground
5	CLK3 [2]	Buffered clock output
6	V_{DD}	3.3 V supply
7	CLK4 [2]	Buffered clock output
8	CLKOUT [2]	Buffered clock output, internal feedback on this pin

Pin Definitions

16-pin SOIC / TSSOP

Pin	Signal	Description
1	REF [1]	Input reference frequency
2	CLKA1 [2]	Buffered clock output, Bank A
3	CLKA2 [2]	Buffered clock output, Bank A
4	V_{DD}	3.3 V supply
5	GND	Ground
6	CLKB1 [2]	Buffered clock output, Bank B
7	CLKB2 [2]	Buffered clock output, Bank B
8	S2 [3]	Select input, bit 2
9	S1 [3]	Select input, bit 1
10	CLKB3 [2]	Buffered clock output, Bank B
11	CLKB4 [2]	Buffered clock output, Bank B
12	GND	Ground
13	V_{DD}	3.3 V supply
14	CLKA3 [2]	Buffered clock output, Bank A
15	CLKA4 [2]	Buffered clock output, Bank A
16	CLKOUT [2]	Buffered output, internal feedback on this pin

Notes
1. Weak pull down.
2. Weak pull down on all outputs.
3. Weak pull ups on these inputs.

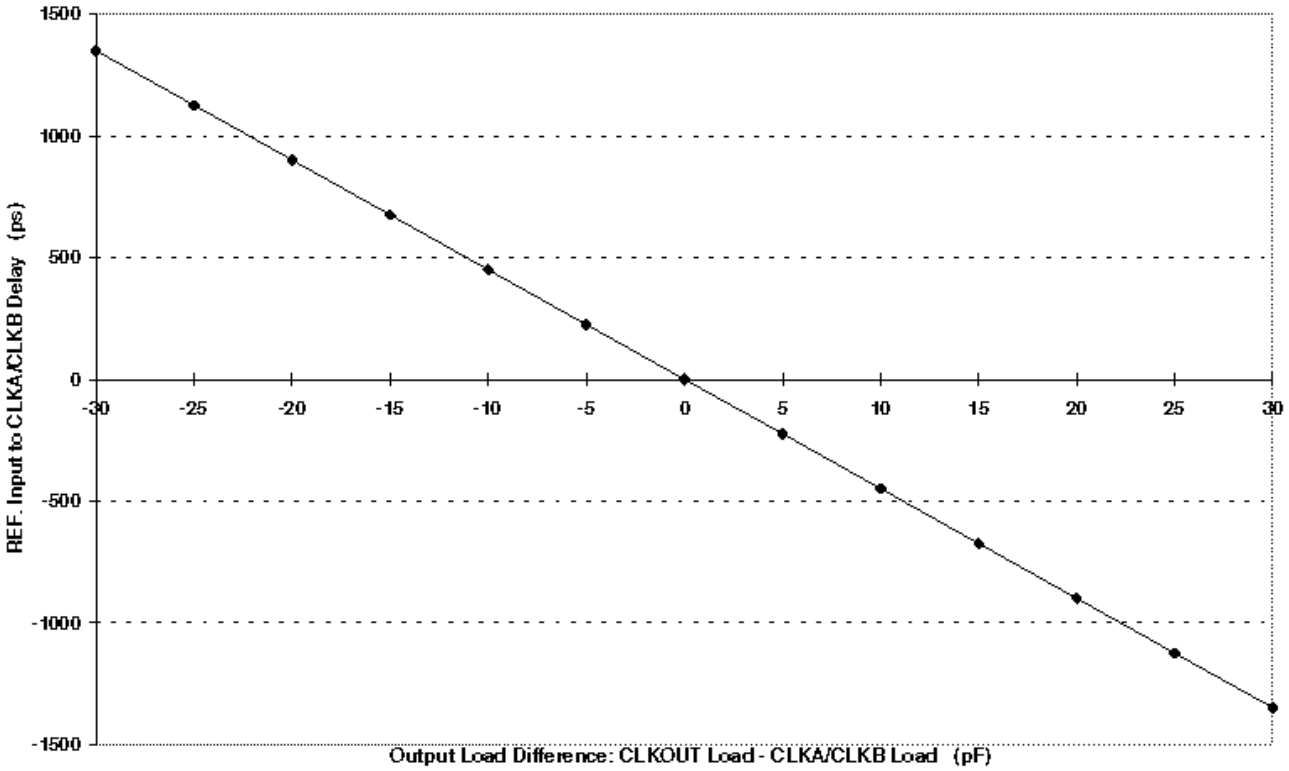
Functional Overview

Select Input Decoding

For CY2309C

S2	S1	CLOCK A1–A4	CLOCK B1–B4	CLKOUT [4]	Output Source	PLL Shutdown
0	0	Three state	Three state	Driven	PLL	N
0	1	Driven	Three state	Driven	PLL	N
1	0	Driven	Driven	Driven	Reference	Y
1	1	Driven	Driven	Driven	PLL	N

Figure 3. REF. Input to CLKA/CLKB Delay vs. Loading Difference between CLKOUT and CLKA/CLKB pins



Zero Delay and Skew Control

All outputs must be uniformly loaded to achieve Zero Delay between the input and output. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input or output delay.

For applications requiring zero input or output delay, all outputs including CLKOUT are equally loaded. Even if CLKOUT is not used, it must have a capacitive load equal to that on other outputs for obtaining zero input or output delay.

For zero output to output skew, all outputs must be loaded equally.

Even if CLKOUT is not used, it must have a capacitive load, equal to that on other outputs, for obtaining zero input-output delay. If input to output delay adjustments are required, use Figure 3 to calculate loading differences between the CLKOUT pin and other outputs.

Note

4. This output is driven and has an internal feedback for the PLL. The load on this output is adjusted to change the skew between the reference and output.

Absolute Maximum Conditions

Supply voltage to ground potential .....–0.5 V to +4.6 V
DC input voltage (Except REF) .....–0.5 V to V_{DD} + 0.5 V
DC input voltage REF .....–0.5 V to V_{DD} + 0.5 V

Storage temperature ..... –65 °C to +150 °C
Junction temperature ..... 150 °C
Static discharge voltage
(per MIL-STD-883, Method 3015) .....> 2,000 V

Operating Conditions

Operating Conditions Table for CY2305CSXC-XX and CY2309CSXC-XX Commercial Temperature devices.

Parameter	Description	Min	Max	Unit
V_{DD}	Supply voltage	3.0	3.6	V
T_A	Operating temperature (ambient temperature)	0	70	°C
C_L	Load capacitance, below 100 MHz	–	30	pF
C_L	Load capacitance, from 100 MHz to 133 MHz	–	10	pF
C_{IN}	Input capacitance	–	7	pF
t_{PU}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps are monotonic)	0.05	50	ms

Operating Conditions

Operating Conditions Table for CY2305CSXI-XX, CY2305CSXA-XX and CY2309CSXI-XX Industrial / Automotive-A Temperature devices.

Parameter	Description	Min	Max	Unit
V_{DD}	Supply voltage	3.0	3.6	V
T_A	Operating temperature (ambient temperature)	–40	85	°C
C_L	Load capacitance, below 100 MHz	–	30	pF
C_L	Load capacitance, from 100 MHz to 133 MHz	–	10	pF
C_{IN}	Input capacitance	–	7	pF
t_{PU}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps are monotonic)	0.05	50	ms

Electrical Characteristics

Electrical Characteristics Table for CY2305CSXC-XX and CY2309CSXC-XX Commercial Temperature devices.

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW voltage [5]		–	0.8	V
V_{IH}	Input HIGH voltage [5]		2.0	–	V
I_{IL}	Input LOW current	V_{IN} = 0 V	–	50	µA
I_{IH}	Input HIGH current	V_{IN} = V_{DD}	–	100	µA
V_{OL}	Output LOW voltage [6]	I_{OL} = 8 mA (–1) I_{OH} = 12 mA (–1H)	–	0.4	V
V_{OH}	Output HIGH voltage [6]	I_{OH} = –8 mA (–1) I_{OL} = –12 mA (–1H)	2.4	–	V
I_{DD} (PD mode)	Power-down supply current	REF = 0 MHz	–	12	µA
I_{DD}	Supply current	Unloaded outputs at 66.67 MHz, SEL inputs at V_{DD}	–	32	mA

Electrical Characteristics

Electrical Characteristics Table for CY2305CSXI-XX, CY2305CSXA-XX and CY2309CSXI-XX Industrial / Automotive-A Temperature devices.

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW voltage [5]		–	0.8	V
V_{IH}	Input HIGH voltage [5]		2.0	–	V
I_{IL}	Input LOW current	V_{IN} = 0 V	–	50	µA
I_{IH}	Input HIGH current	V_{IN} = V_{DD}	–	100	µA
V_{OL}	Output LOW voltage [6]	I_{OL} = 8 mA (–1) I_{OH} =12 mA (–1H)	–	0.4	V
V_{OH}	Output HIGH voltage [6]	I_{OH} = –8 mA (–1) I_{OL} = –12 mA (–1H)	2.4	–	V
I_{DD} (PD mode)	Power-down supply current	REF = 0 MHz	–	25	µA
I_{DD}	Supply current	Unloaded outputs at 66.67 MHz, SEL inputs at V_{DD}	–	35	mA

Notes
5. REF input has a threshold voltage of V_{DD}/2.
6. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Characteristics

Switching Characteristics Table for CY2305CSXC-1 and CY2309CSXC-1 Commercial Temperature devices. All parameters are specified with loaded outputs.

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
t_1	Output frequency	30 pF load 10 pF load	10 10	–	100 133.33	MHz MHz
t_{DC}	Output duty cycle [7] = $t_2 \div t_1$	Measured at 1.4 V, F_{out} > 50 MHz	40	50	60	%
		Measured at 1.4 V, $F_{out} \leq 50$ MHz	45	50	55	%
t_3	Rise time [7]	Measured between 0.8 V and 2.0 V	–	–	2.25	ns
t_4	Fall time [7]	Measured between 0.8 V and 2.0 V	–	–	2.25	ns
t_5	Output-to-output skew [7]	All outputs equally loaded	–	–	200	ps
t_{6A}	Delay, REF rising edge to CLKOUT rising edge [7]	Measured at $V_{DD}/2$	–	0	±350	ps
t_{6B}	Delay, REF rising edge to CLKOUT rising edge [7]	Measured at $V_{DD}/2$. Measured in PLL Bypass mode, CY2309C device only.	1	5	8.7	ns
t_7	Device-to-device skew [7]	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	–	0	700	ps
t_J	Cycle-to-cycle jitter, peak [7]	Measured at 66.67 MHz, loaded outputs	–	50	175	ps
t_{LOCK}	PLL lock time [7]	Stable power supply, valid clock presented on REF pin	–	–	1.0	ms

Note
7. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Characteristics

Switching Characteristics Table for CY2305CSXC-1H and CY2309CSXC-1H Commercial Temperature devices. All parameters are specified with loaded outputs.

Parameter	Description	Description	Min	Typ	Max	Unit
t_1	Output frequency	30-pF load 10-pF load	10 10	–	100 133.33	MHz MHz
t_{DC}	Output duty cycle [8] = $t_2 \div t_1$	Measured at 1.4 V, F_{out} > 50 MHz	40	50	60	%
		Measured at 1.4 V, $F_{out} \leq 50$ MHz	45	50	55	%
t_3	Rise time [8]	Measured between 0.8 V and 2.0 V	–	–	1.5	ns
t_4	Fall time [8]	Measured between 0.8 V and 2.0 V	–	–	1.5	ns
t_5	Output-to-output skew [8]	All outputs equally loaded	–	–	200	ps
t_{6A}	Delay, REF rising edge to CLKOUT rising edge [8]	Measured at $V_{DD}/2$	–	0	±350	ps
t_{6B}	Delay, REF rising edge to CLKOUT rising edge [8]	Measured at $V_{DD}/2$. Measured in PLL Bypass mode, CY2309C device only.	1	5	8.7	ns
t_7	Device-to-device skew [8]	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	–	0	700	ps
t_8	Output slew rate [8]	Measured between 0.8 V and 2.0 V using Test circuit #2	1	–	–	V/ns
t_J	Cycle-to-cycle jitter, peak [8]	Measured at 66.67 MHz, loaded outputs	–	–	175	ps
t_{LOCK}	PLL lock time [8]	Stable power supply, valid clock presented on REF pin	–	–	1.0	ms

Note
8. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Characteristics

Switching Characteristics Table for CY2305CSXI-1, CY2305CSXA-1, and CY2309CSXI-1 Industrial Temperature devices. All parameters are specified with loaded outputs.

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
t_1	Output frequency	30 pF load 10 pF load	10 10	–	100 133.33	MHz MHz
t_{DC}	Output duty cycle [9] = $t_2 \div t_1$	Measured at 1.4 V, F_{out} > 50 MHz	40	50	60	%
		Measured at 1.4 V, $F_{out} \leq$ 50 MHz	45	50	55	%
t_3	Rise time [9]	Measured between 0.8 V and 2.0 V	–	–	2.25	ns
t_4	Fall time [9]	Measured between 0.8 V and 2.0 V	–	–	2.25	ns
t_5	Output-to-output skew [9]	All outputs equally loaded	–	–	200	ps
t_{6A}	Delay, REF rising edge to CLKOUT rising edge [9]	Measured at $V_{DD}/2$	–	0	±350	ps
t_{6B}	Delay, REF rising edge to CLKOUT rising edge [9]	Measured at $V_{DD}/2$. Measured in PLL Bypass mode, CY2309C device only.	1	5	8.7	ns
t_7	Device-to-device skew [9]	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	–	0	700	ps
t_J	Cycle-to-cycle jitter, peak [9]	Measured at 66.67 MHz, loaded outputs	–	50	175	ps
t_{LOCK}	PLL lock time [9]	Stable power supply, valid clock presented on REF pin	–	–	1.0	ms

Note
9. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching characteristics

Switching Characteristics Table for CY2305CSXI-1H, CY2305CSXA-1H and CY2309CSXI-1H Industrial / Automotive-A Temperature devices. All parameters are specified with loaded outputs.

Parameter	Description	Description	Min	Typ	Max	Unit
t_1	Output frequency	30 pF load 10 pF load	10 10	–	100 133.33	MHz MHz
t_{DC}	Output duty cycle [10] = $t_2 \div t_1$	Measured at 1.4 V, F_{out} > 50 MHz	40	50	60	%
		Measured at 1.4 V, $F_{out} \leq$ 50 MHz	45	50	55	%
t_3	Rise time [10]	Measured between 0.8 V and 2.0 V	–	–	1.5	ns
t_4	Fall time [10]	Measured between 0.8 V and 2.0 V	–	–	1.5	ns
t_5	Output-to-output skew [10]	All outputs equally loaded	–	–	200	ps
t_{6A}	Delay, REF rising edge to CLKOUT rising edge [10]	Measured at $V_{DD}/2$	–	0	±350	ps
t_{6B}	Delay, REF rising edge to CLKOUT rising edge [10]	Measured at $V_{DD}/2$. Measured in PLL Bypass mode, CY2309C device only.	1	5	8.7	ns
t_7	Device-to-device skew [10]	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	–	0	700	ps
t_8	Output slew rate [10]	Measured between 0.8 V and 2.0 V using Test circuit #2	1	–	–	V/ns
t_J	Cycle-to-cycle jitter, peak [10]	Measured at 66.67 MHz, loaded outputs	–	–	175	ps
t_{LOCK}	PLL lock time [10]	Stable power supply, valid clock presented on REF pin	–	–	1.0	ms

Note
10. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Waveforms

Figure 4. Duty Cycle Timing

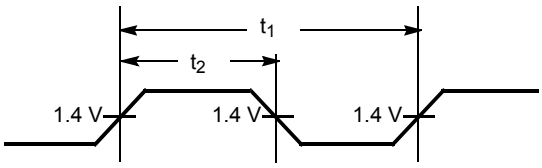


Figure 5. All Outputs Rise/Fall Time

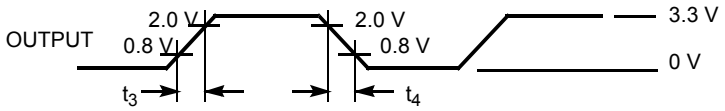


Figure 6. Output-Output Skew

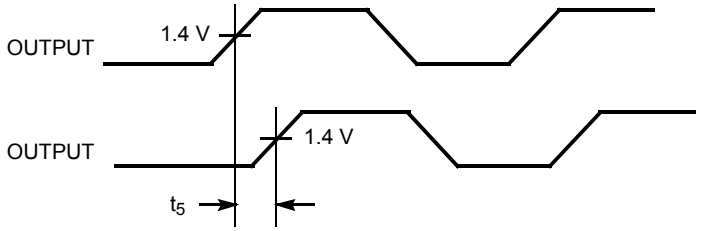


Figure 7. Input-Output Propagation Delay

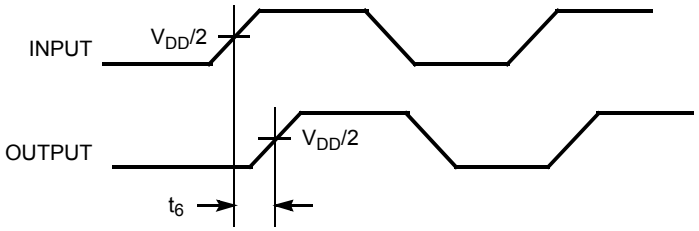
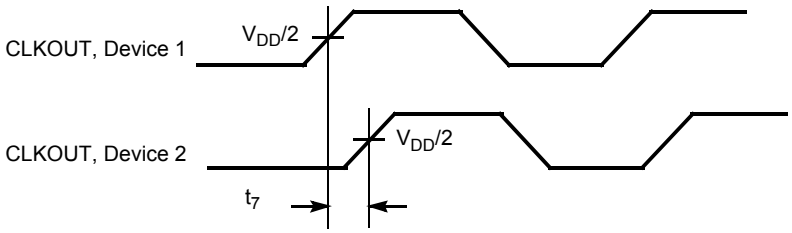
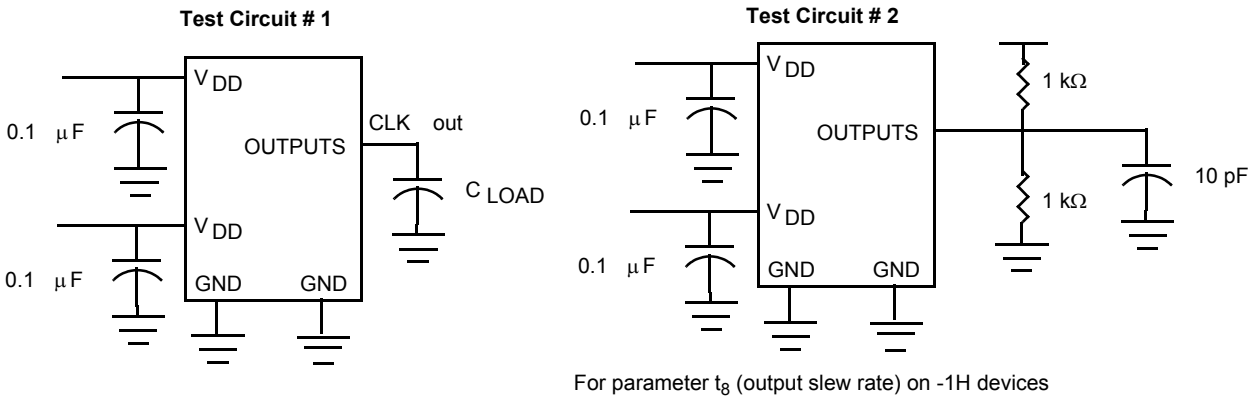


Figure 8. Device-Device Skew



Test Circuits

Figure 9. Test Circuits

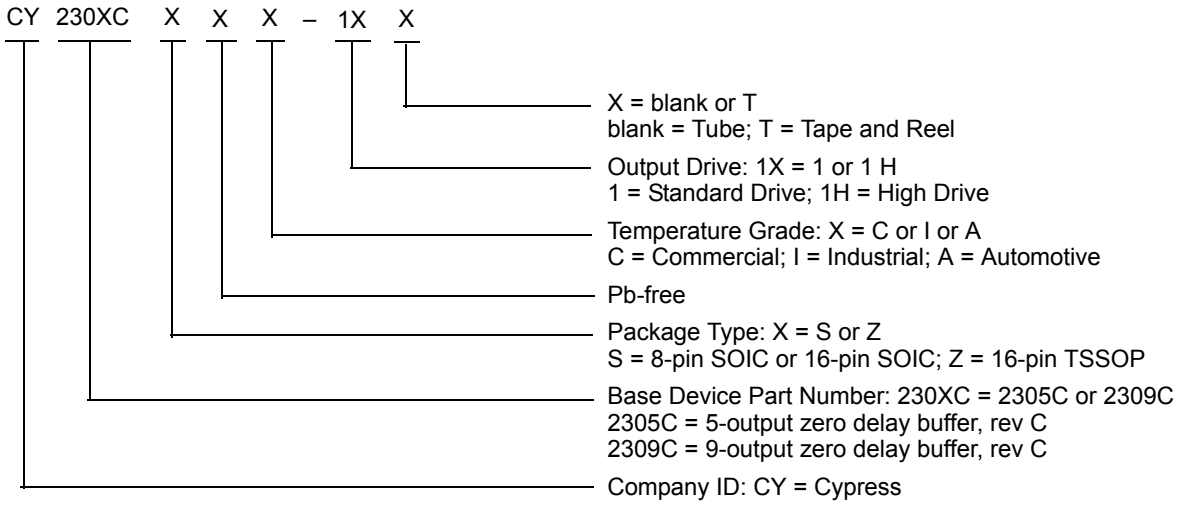


For parameter t_8 (output slew rate) on -1H devices

Ordering Information

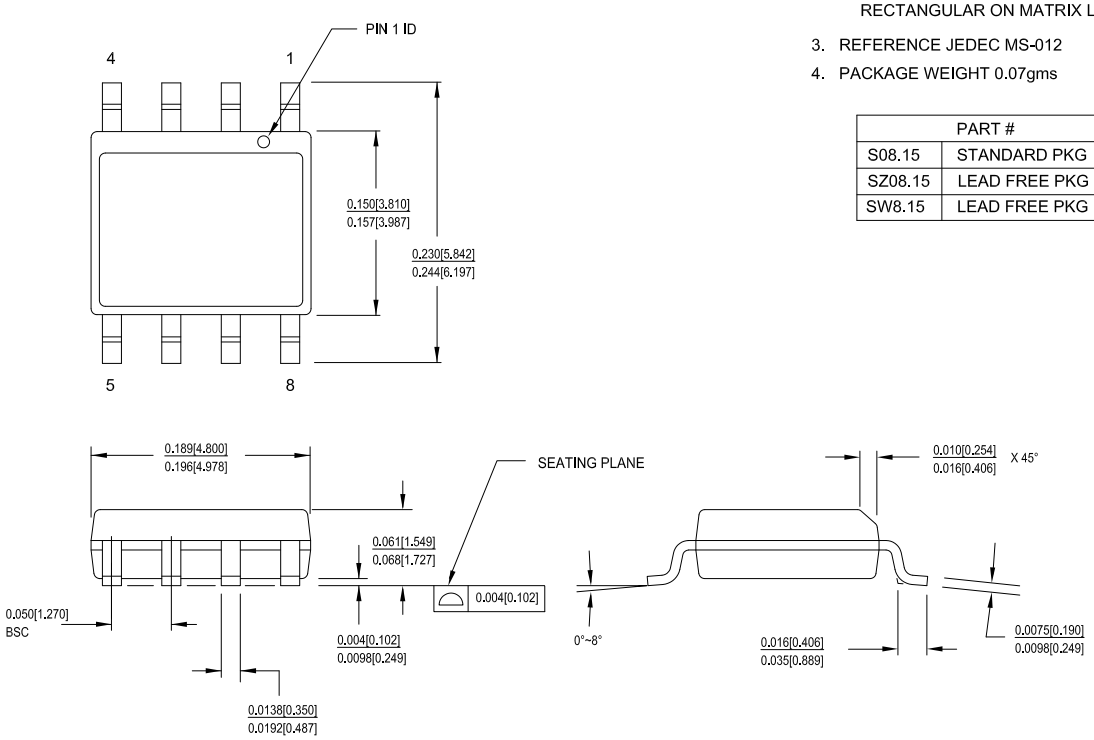
Ordering Code	Package Type	Operating Range
Pb-free - CY2305C		
CY2305CSXC-1	8-pin SOIC (150 Mil)	Commercial
CY2305CSXC-1T	8-pin SOIC (150 Mil) – Tape and Reel	Commercial
CY2305CSXC-1H	8-pin SOIC (150 Mil)	Commercial
CY2305CSXC-1HT	8-pin SOIC (150 Mil) – Tape and Reel	Commercial
CY2305CSXI-1	8-pin SOIC (150 Mil)	Industrial
CY2305CSXI-1T	8-pin SOIC (150 Mil) – Tape and Reel	Industrial
CY2305CSXI-1H	8-pin SOIC (150 Mil)	Industrial
CY2305CSXI-1HT	8-pin SOIC (150 Mil) – Tape and Reel	Industrial
CY2305CSXA-1H	8-pin SOIC (150 Mil)	Automotive-A
CY2305CSXA-1HT	8-pin SOIC (150 Mil) – Tape and Reel	Automotive-A
Pb-free - CY2309C		
CY2309CSXC-1	16-pin SOIC (150 Mil)	Commercial
CY2309CSXC-1T	16-pin SOIC (150 Mil) – Tape and Reel	Commercial
CY2309CSXC-1H	16-pin SOIC (150 Mil)	Commercial
CY2309CSXC-1HT	16-pin SOIC (150 Mil) – Tape and Reel	Commercial
CY2309CSXI-1	16-pin SOIC (150 Mil)	Industrial
CY2309CSXI-1T	16-pin SOIC (150 Mil) – Tape and Reel	Industrial
CY2309CSXI-1H	16-pin SOIC (150 Mil)	Industrial
CY2309CSXI-1HT	16-pin SOIC (150 Mil) – Tape and Reel	Industrial
CY2309CZXC-1	16-pin TSSOP (4.4 mm)	Commercial
CY2309CZXC-1T	16-pin TSSOP (4.4 mm) – Tape and Reel	Commercial
CY2309CZXC-1H	16-pin TSSOP (4.4 mm)	Commercial
CY2309CZXC-1HT	16-pin TSSOP (4.4 mm) – Tape and Reel	Commercial
CY2309CZXI-1	16-pin TSSOP (4.4 mm)	Industrial
CY2309CZXI-1T	16-pin TSSOP (4.4 mm) – Tape and Reel	Industrial
CY2309CZXI-1H	16-pin TSSOP (4.4 mm)	Industrial
CY2309CZXI-1HT	16-pin TSSOP (4.4 mm) – Tape and Reel	Industrial

Ordering Code Definitions



Package Diagrams

Figure 10. 8-pin SOIC (150 Mils) S0815/SZ815/SW815 Package Outline, 51-85066



1. DIMENSIONS IN INCHES[MM] MIN.
   MAX.
2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #	
S08.15	STANDARD PKG
SZ08.15	LEAD FREE PKG
SW8.15	LEAD FREE PKG

51-85066 *F

Package Diagrams *(continued)*

Figure 11. 16-pin SOIC (150 Mil) S16.15/SZ16.15 Package Outline, 51-85068

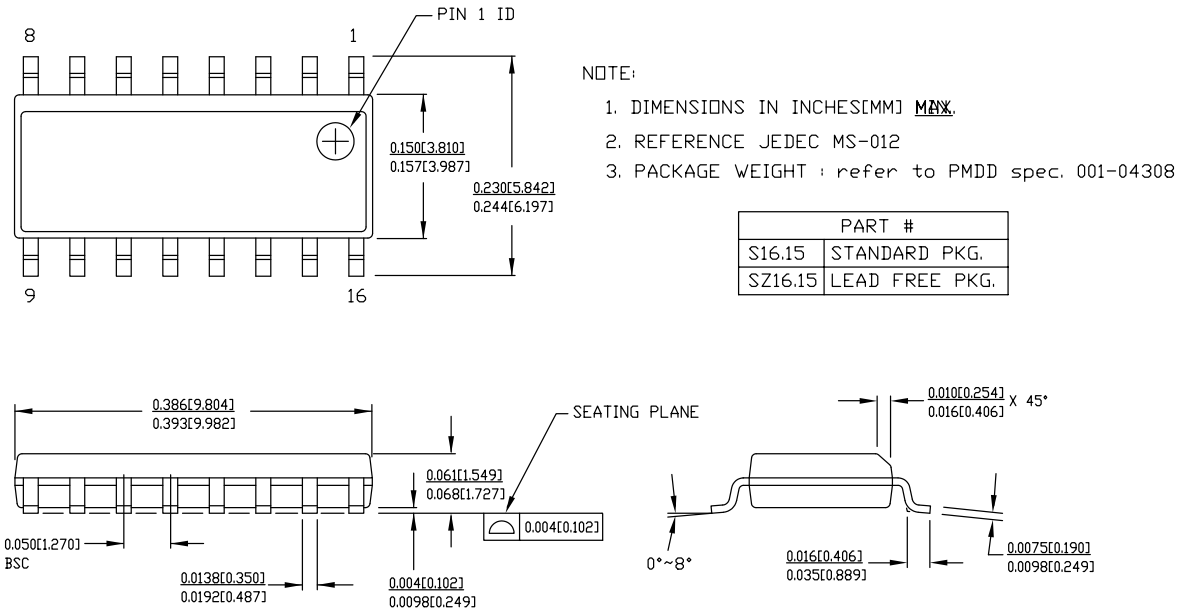
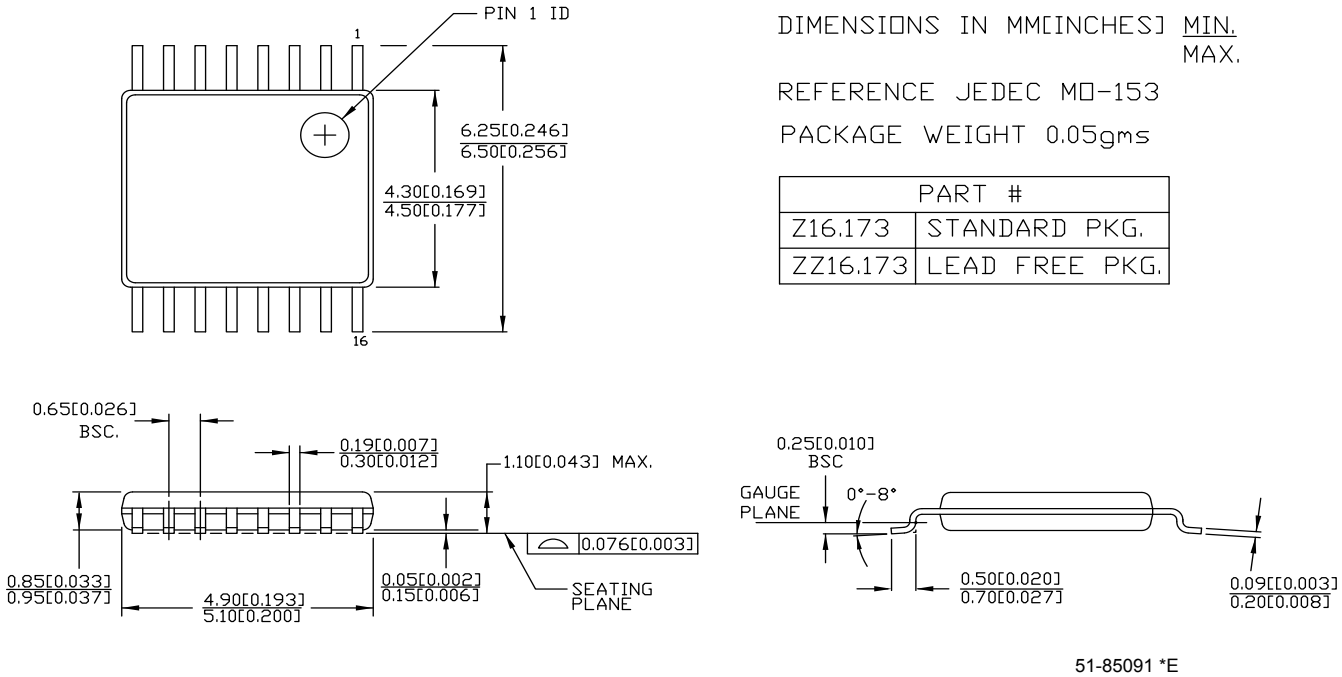


Figure 12. 16-pin TSSOP (4.40 mm Body) Z16.173/ZZ16.173 Package Outline, 51-85091



Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
PLL	Phase Locked Loop
SOIC	Small Outline Integrated Circuit
TSSOP	Thin Shrunk Small Outline Package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kHz	kilohertz
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
ns	nanosecond
pF	picofarad
ps	picosecond
V	volt

Document History Page

Document Title: CY2305C/CY2309C, 3.3 V Zero Delay Clock Buffer Document Number: 38-07672				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	224421	See ECN	RGL	New data sheet
*A	268571	See ECN	RGL	Added bullet for 5 V tolerant inputs in the features
*B	276453	See ECN	RGL	Minor Change: Moved one sentence from the features to the Functional Description
*C	303063	See ECN	RGL	Updated data sheet as per characterization data
*D	318315	See ECN	RGL	Data sheet rewrite
*E	344815	See ECN	RGL	Minor Error: Corrected the header of all the AC/DC tables with the right part numbers.
*F	127988938	See ECN	KVM	Changed title from ,low Cost 3.3 V Zero Delay Buffer to 3.3 V Zero Delay Clock Buffer Specified the VIL minimum value to -0.3 V Specified the VIH maximum value to VDD + 0.3 V Changed DC Input Voltage (REF) maximum value in Absolute Maximum section Removed references to 5 V tolerant inputs (pages 1 and 2) Removed Pentium compatibility reference Added CY2305C block diagram Added ,peak to the jitter specifications Changed typical jitter from 75 ps to 50 ps for standard drive devices For standard drive devices, tightened rise/fall times from 2.5 ns to 2.25 ns Tightened cycle-to-cycle jitter from 200 ps to 175 ps Tightened output-to-output skew from 250 ps to 200 ps
*G	1561504	See ECN	KVM / NSI / AESA	Added CY2305C Automotive-A grade devices Extended duty cycle specs to cover entire frequency range Changed from Preliminary to Final
*H	2558537	08/27/08	KVM / AESA	Added CY2305CSXA-1 and CY2305CSXA-1T parts in Ordering Information table under Pb-free CY2305C
*I	2901743	03/30/2010	VIVG	Updated Package Diagrams. Added Ordering Code Definitions Added Sales, Solutions, and Legal Information URLs.
*J	3080990	11/10/2010	BASH	Modified pin diagram of Figure 1. Updated as per new template Added Acronyms and Units of Measure table Added TOC
*K	3160535	02/03/2011	BASH	Removed min value of V_{IL} and max value of V_{IH} from Electrical Characteristics Table on page 6 and page 7. Removed Prune parts CY2305CSXA-1 and CY2305CSXA-1T from the datasheet.
*L	3822852	11/27/2012	PURU	Updated Select Input Decoding (Added Figure 3 only, no edits). Updated Zero Delay and Skew Control (Minor edits). Updated Package Diagrams: spec 51-85091 – Changed revision from *C to *D. spec 51-85068 – Changed revision from *C to *E. spec 51-85066 – Changed revision from *D to *E.
*M	4201564	11/25/2013	CINM	Updated Package Diagrams: spec 51-85066 – Changed revision from *E to *F. Updated in new template. Completing Sunset Review.

Document History Page *(continued)*

Document Title: CY2305C/CY2309C, 3.3 V Zero Delay Clock Buffer Document Number: 38-07672				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
*N	4578443	11/25/2014	TAVA	Added related documentation hyperlink in page 1. Updated package diagram.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC® Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Community | Forums | Blogs | Video | Training

Technical Support

cypress.com/go/support

AMEYA360
Components Supply Platform

Authorized Distribution Brand :

Website :

Welcome to visit www.ameya360.com

Contact Us :

- ### Address :

  401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
  Minhang District, Shanghai , China

- ### Sales :

  Direct +86 (21) 6401-6692

  Email amall@ameya360.com

  QQ 800077892

  Skype ameyasales1 ameyasales2

- ### Customer Service :

  Email service@ameya360.com

- ### Partnership :

  Tel +86 (21) 64016692-8333

  Email mkt@ameya360.com