LMV7271/LMV7275/LMV7272 Single & Dual, 1.8V Low Power Comparators with Rail-to-Rail Input

Check for Samples: LMV7271

FEATURES

- (V_S = 1.8V, T_A = 25°C, Typical values unless specified).
- Single or Dual Supplies
- Ultra low supply current 9µA per channel
- Low input bias current 10nA
- Low input offset current 200pA
- Low guaranteed V_{OS} 4mV
- Propagation delay 880ns (20mV overdrive)
- Input common mode voltage range 0.1V beyond rails
- LMV7272 is available in DSBGA package

APPLICATIONS

- Mobile communications
- Laptops and PDA's
- Battery powered electronics
- General purpose low voltage applications

DESCRIPTION

The LMV727X are rail-to-rail input low power comparators, which are characterized at supply voltage 1.8V, 2.7V and 5.0V. They consume only 9uA supply current per channel while achieving a 800ns propagation delay.

The LMV7271/LMV7275 (single) are available in SC70 and SOT-23 packages. The LMV7272 (dual) is available in DSBGA package. With these tiny packages, the PC board area can be significantly reduced. They are ideal for low voltage, low power and space critical designs.

The LMV7271/LMV7272 both feature a push-pull output stage which allows operation with minimum power consumption when driving a load. The LMV7275 features an open drain output stage that allows for wired-OR configurations. The open drain output also offers the advantage of allowing the output to be pulled to any voltage up to 5.5V, regardless of the supply voltage of the LMV7275.

The LMV727X are built with Texas Instruments' advance submicron silicon-gate BiCMOS process. They all have bipolar inputs for improved noise performance and CMOS outputs for rail-to-rail output swing.

Typical Circuit

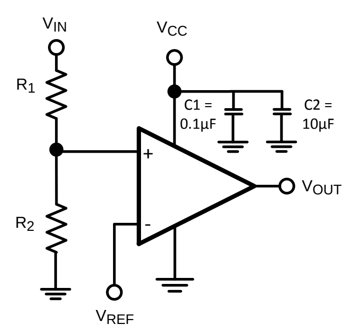


Figure 1. Threshold Detector

Part Number	Single/Dual	Package	Output
LMV7271	Single	SC70, SOT-23	Push/Pull
LMV7272	Dual	DSBGA	Push/Pull
LMV7275	Single	SC70, SOT-23	Open Drain

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance	2KV (3)
	200V (4)
V_{IN} Differential	±Supply Voltage
Supply Voltage (V^+ - V^-)	6V
Voltage at Input/Output pins	V^+ +0.1V, V^- −0.1V
Soldering Information	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (5)	+150°C

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(2) **If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.**
(3) Human body model, 1.5kΩ in series with 100pF.
(4) Machine Model, 0Ω in series with 200pF.
(5) Typical values represent the most likely parametric norm.

Operating Ratings (1)

Supply Voltage Range	1.8V to 5.5V
Temperature Range (2)	−40°C to +85°C
Package Thermal Resistance (2)	
SOT-23	325°C/W
SC70	265°C/W
8-Bump DSBGA	220°C/W

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

1.8V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 1.8V, V^- = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage			0.3	4 **6**	mV
TC V_{OS}	Input Offset Temperature Drift	V_{CM} = 0.9V (3)		20		uV/°C
I_B	Input Bias Current			10		nA
I_{OS}	Input Offset Current			200		pA
I_S	Supply Current	LMV7271/LMV7275		9	12 **14**	µA
		LMV7272		18	25 **28**	µA

(1) All limits are guaranteed by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Offset Voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

1.8V Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 1.8V, V^- = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)	Units
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0.9V (LMV7271/LMV7272 only)	3.5	6		mA
		Sinking, V_O = 0.9V	4	6		
V_{OH}	Output Voltage High (LMV7271/LMV7272 only)	I_O = 0.5mA	1.7	1.74		V
		I_O = 1.5mA	1.47	1.63		
V_{OL}	Output Voltage Low	I_O = −0.5mA		52	100	mV
		I_O = −1.5mA		166	220	
V_{CM}	Input Common Mode Voltage Range	CMRR > 45 dB			1.9	V
			−0.1			V
CMRR	Common Mode Rejection Ratio	0 < V_{CM} < 1.8V	46	78		dB
PSRR	Power Supply Rejection Ratio	V^+ = 1.8V to 5V	55	80		dB
$I_{LEAKAGE}$	Output Leakage Current	V_O = 1.8V (LMV7275 only)		2		pA

1.8V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 1.8V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2 and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)	Units
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 20mV Load = 50pF//5kΩ		880		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ		570		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 20mV Load = 50pF//5kΩ		1100		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ		800		ns

(1) Machine Model, 0Ω in series with 200pF.
(2) All limits are guaranteed by testing or statistical analysis.

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage			0.3	4 **6**	mV
TC V_{OS}	Input Offset Temperature Drift	V_{CM} = 1.35V (3)		20		µV/°C
I_B	Input Bias Current			10		nA
I_{OS}	Input offset Current			200		pA
I_S	Supply Current	LMV7271/LMV7275		9	13 **15**	µA
		LMV7272		18	25 **28**	µA
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 1.35V (LMV7271/LMV7272 only)	10	15		mA
		Sinking, V_O = 1.35V	10	15		

(1) Machine Model, 0Ω in series with 200pF.
(2) All limits are guaranteed by testing or statistical analysis.
(3) Offset Voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

2.7V Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OH}	Output Voltage High (LMV7271/LMV7272 only)	I_O = 0.5mA	2.63	2.66		V
		I_O = 2.0mA	2.48	2.55		
V_{OL}	Output Voltage Low	I_O = −0.5mA		50	70	mV
		I_O = −2mA		155	220	
V_{CM}	Input Common Voltage Range	CMRR > 45dB			2.8	V
			−0.1			V
CMRR	Common Mode Rejection Ratio	0 < V_{CM} < 2.7V	46	78		dB
PSRR	Power Supply Rejection Ratio	V^+ = 1.8V to 5V	55	80		dB
$I_{LEAKAGE}$	Output Leakage Current	V_O = 2.7V (LMV7275 only)		2		pA

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2 and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)	Units
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 20mV Load = 50pF//5kΩ		1200		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ		810		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 20mV Load = 50pF//5kΩ		1300		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ		860		ns

(1) Machine Model, 0Ω in series with 200pF.
(2) All limits are guaranteed by testing or statistical analysis.

5.0V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage			0.3	4 **6**	mV
TC V_{OS}	Input Offset Temperature Drift	V_{CM} = 2.5V (3)		20		µV/°C
I_B	Input Bias Current			10		nA
I_{OS}	Input Offset Current			200		pA
I_S	Supply Current	LMV7271/LMV7275		10	14 **16**	µA
		LMV7272		20	27 **30**	µA
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 2.5V (LMV7271/LMV7272 only)	18	34		mA
		Sinking, V_O = 2.5V	18	34		
V_{OH}	Output Voltage High (LMV7271/LMV7272 only)	I_O = 0.5mA	4.93	4.96		V
		I_O = 4.0mA	4.675	4.77		

(1) Machine Model, 0Ω in series with 200pF.
(2) All limits are guaranteed by testing or statistical analysis.
(3) Offset Voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

5.0V Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OL}	Output Voltage Low	I_O = −0.5mA		27	70	mV
		I_O = −4.0mA		225	315	
V_{CM}	Input Common Voltage Range	CMRR > 45dB			5.1	V
			−0.1			
CMRR	Common Mode Rejection Ratio	0 < V_{CM} < 5.0V	46	78		dB
PRSS	Power Supply Rejection Ratio	V^+ = 1.8V to 5V	55	80		dB
$I_{LEAKAGE}$	Output Leakage Current	V_O = 5V (LMV7275 only)		2		pA

5.0V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5.0V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2 and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)	Units
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 20mV Load = 50pF//5kΩ		2100		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ		1380		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 20mV Load = 50pF//5kΩ		1800		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ		1100		ns

(1) Machine Model, 0Ω in series with 200pF.
(2) All limits are guaranteed by testing or statistical analysis.

CONNECTION DIAGRAMS

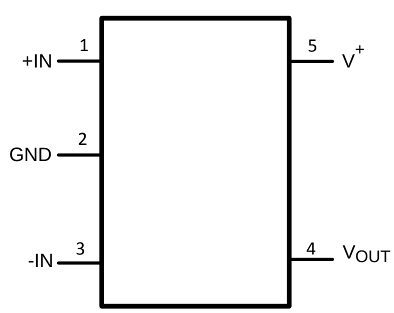


Figure 2. 5-Pin SOT-23/SC70 (LMV7271/LMV7275) (Top View)

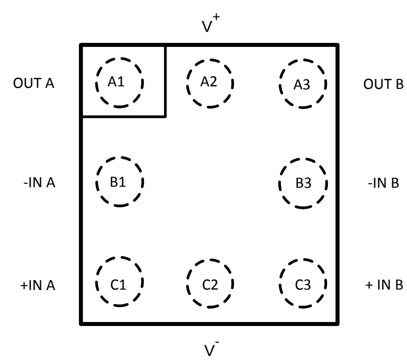


Figure 3. 8-Bump DSBGA (LMV7272) (bump side down)

TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, Unless otherwise specified).

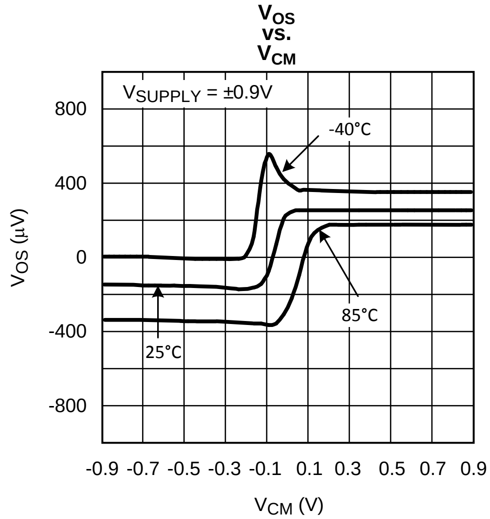


Figure 4.

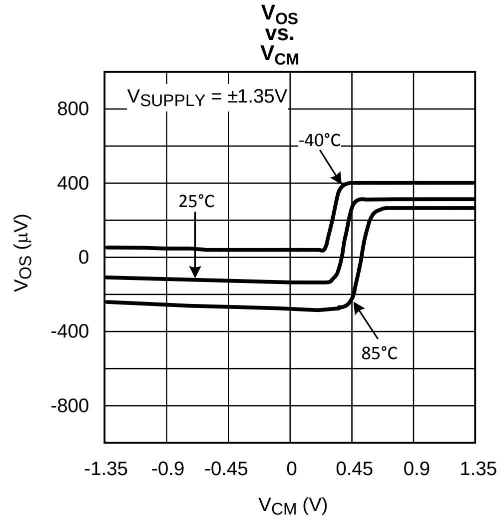


Figure 5.

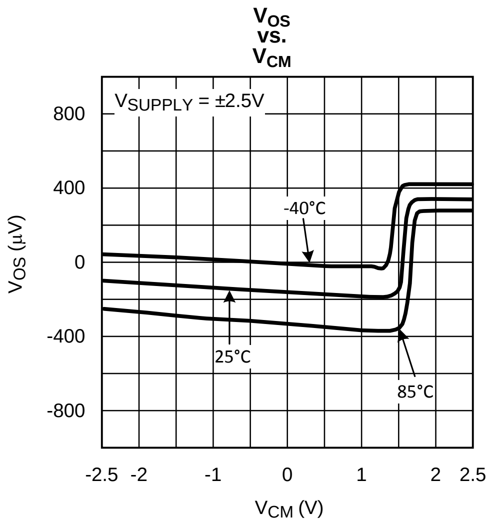


Figure 6.

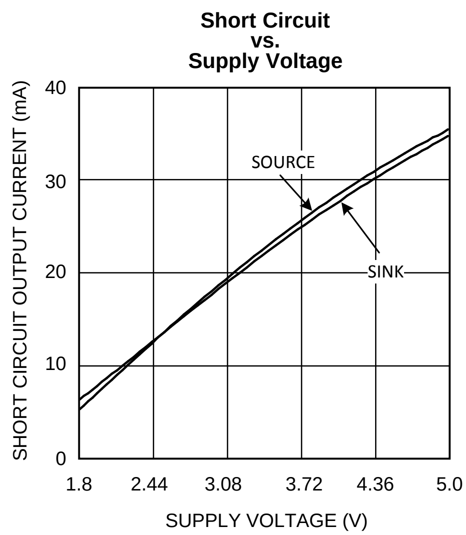


Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(T_A = 25°C, Unless otherwise specified).

Supply Current vs. Supply Voltage (LMV7271)

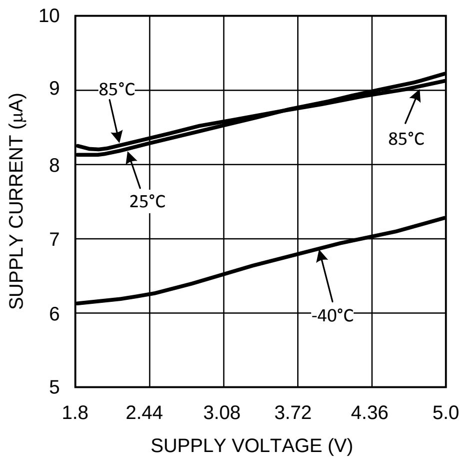


Figure 8.

Supply Current vs. Supply Voltage (LMV7272)

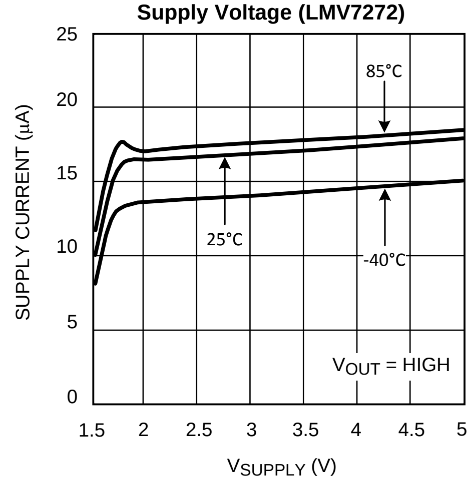


Figure 9.

Supply Current vs. Supply Voltage (LMV7272)

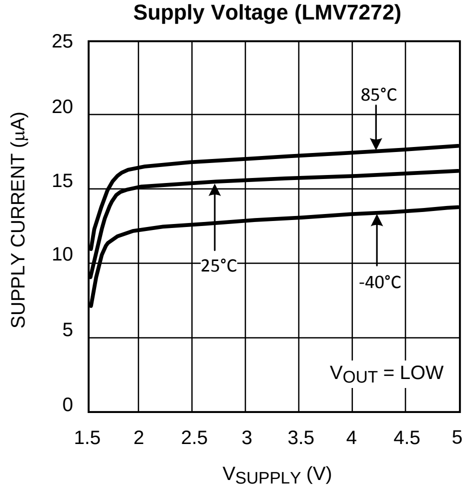


Figure 10.

Output Positive Swing vs. V_{SUPPLY}

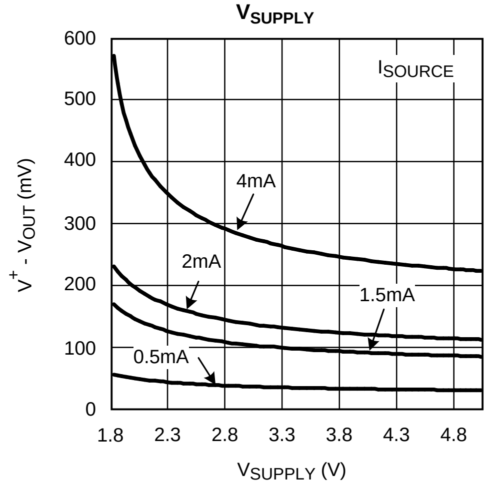


Figure 11.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(T_A = 25°C, Unless otherwise specified).

Output Negative Swing vs. V_{SUPPLY}

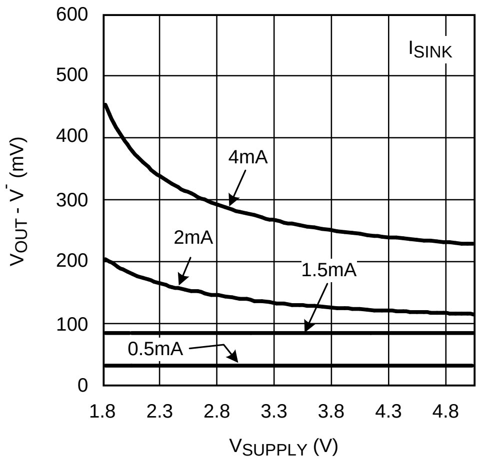


Figure 12.

Output Positive Swing vs. I_{SOURCE}

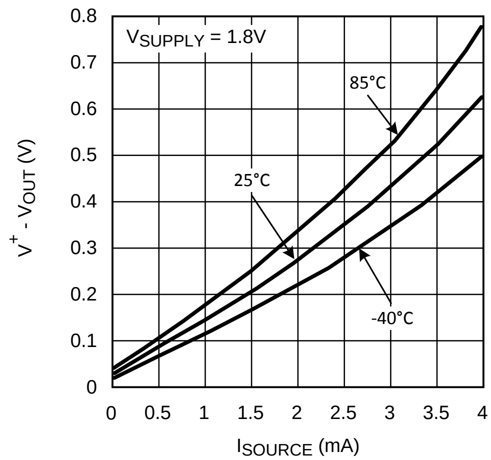


Figure 13.

Output Negative Swing vs. I_{SINK}

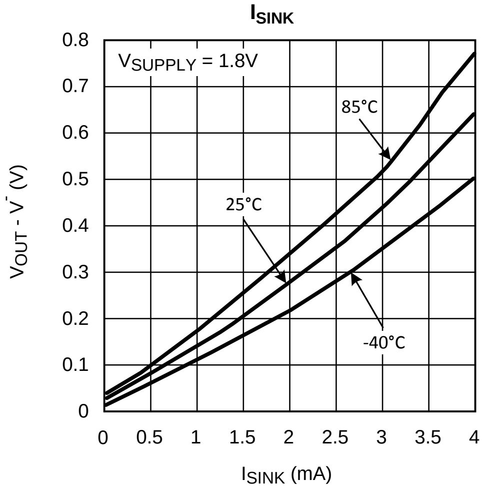


Figure 14.

Output Positive Swing vs. I_{SOURCE}

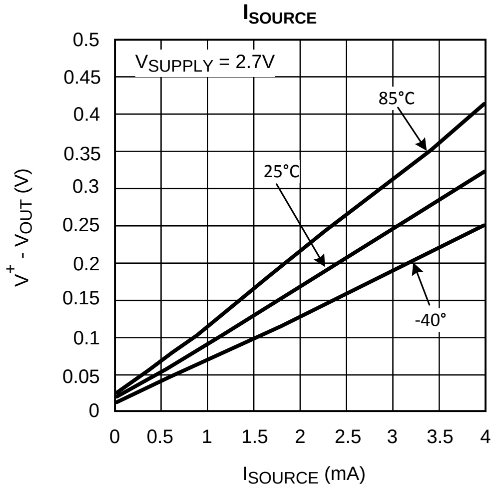


Figure 15.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(T_A = 25°C, Unless otherwise specified).

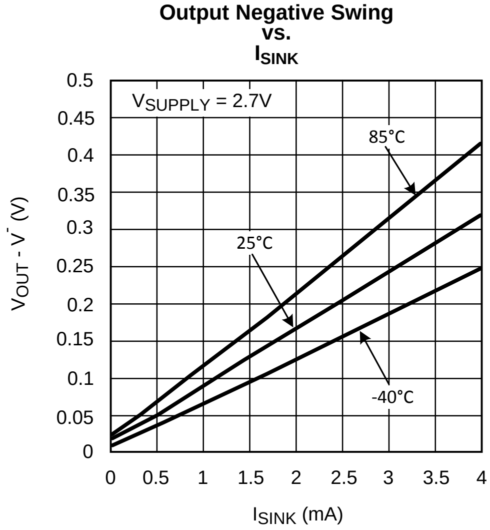


Figure 16.

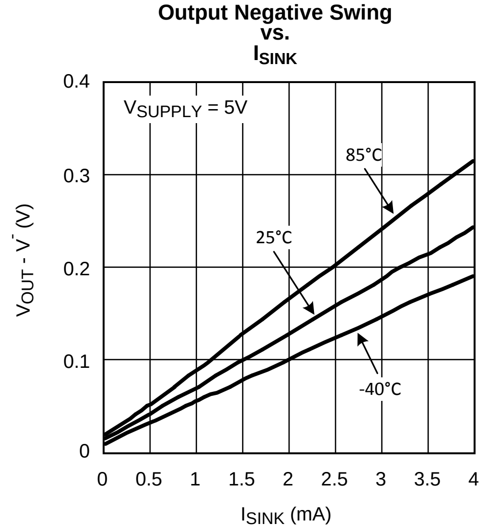


Figure 17.

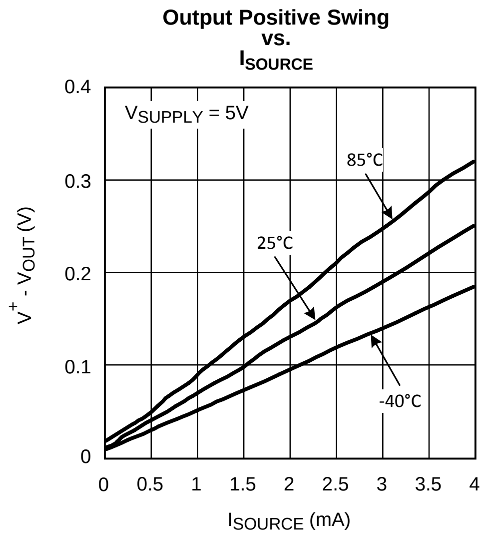


Figure 18.

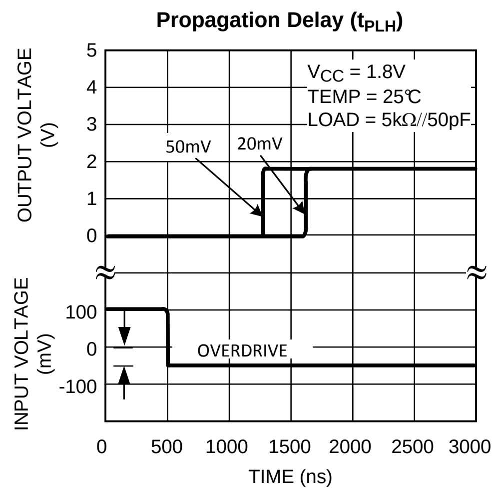


Figure 19.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(T_A = 25°C, Unless otherwise specified).

Propagation Delay (t_{PHL})

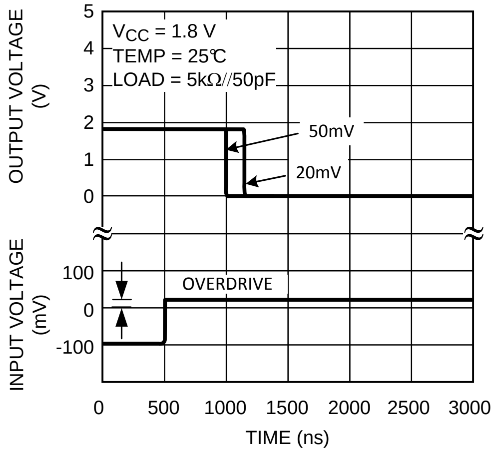


Figure 20.

Propagation Delay (t_{PLH})

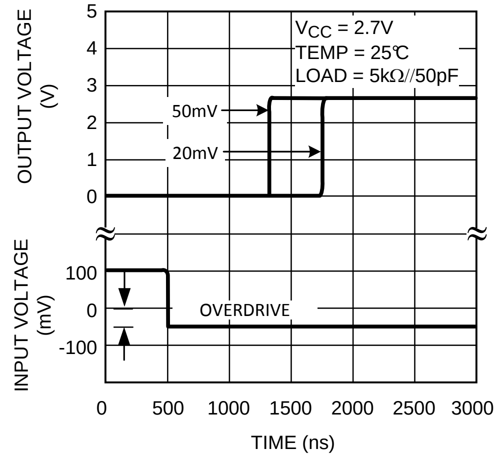


Figure 21.

Propagation Delay (t_{PHL})

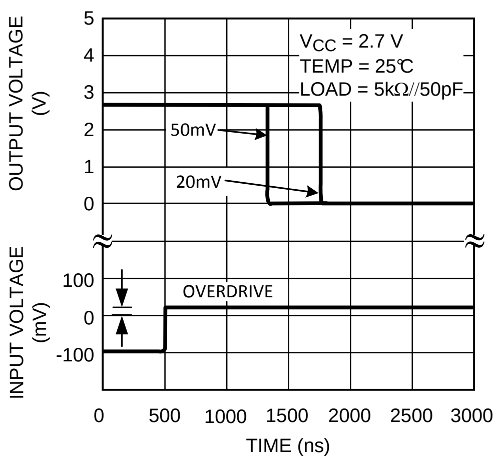


Figure 22.

Propagation Delay (t_{PLH})

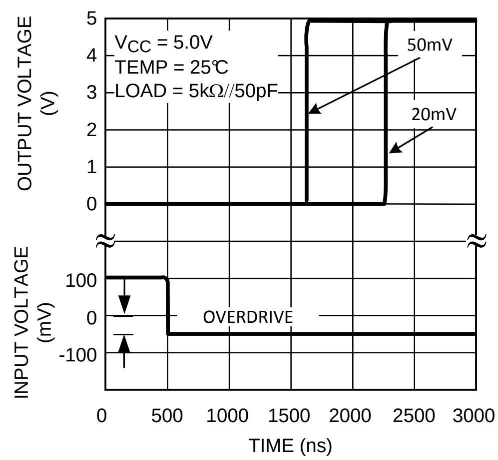


Figure 23.

Propagation Delay (t_{PHL})

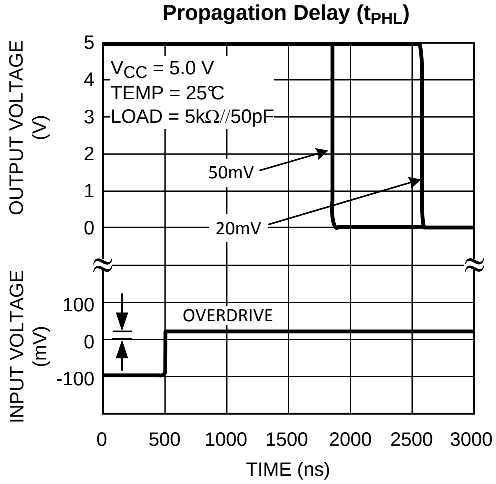


Figure 24.

t_{PHL} vs. Overdrive

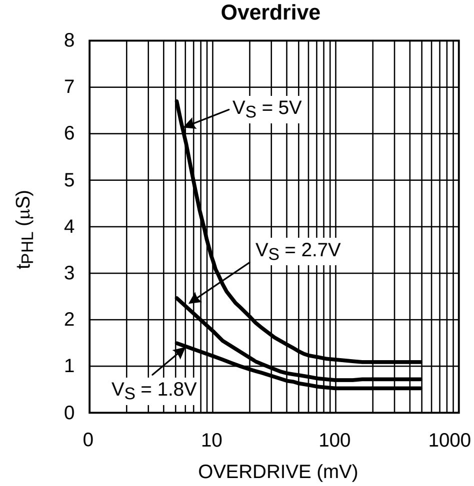


Figure 25.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(T_A = 25°C, Unless otherwise specified).

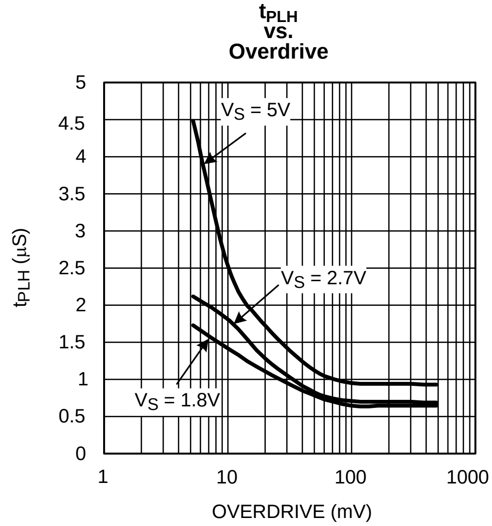


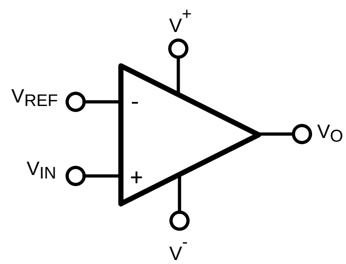
Figure 26.

APPLICATION NOTES

BASIC COMPARATOR

A comparator is often used to convert an analog signal to a digital signal. As shown in Figure 28, the comparator compares an input voltage (V_{IN}) to a reference voltage (V_{REF}). If V_{IN} is less than V_{REF}, the output (V_O) is low. However, if V_{IN} is greater than V_{REF}, the output voltage (V_O) is high.

Figure 27. LMV7271



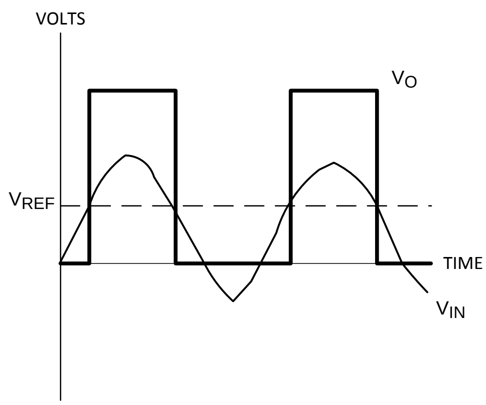


Figure 28. LMV7271 Basic Comparator

RAIL-TO-RAIL INPUT STAGE

The LMV727X has an input common mode voltage range (V_{CM}) of −0.1V below the V^- to 0.1V above V^+. This is achieved by using paralleled PNP and NPN differential input pairs. When the V_{CM} is near V^+, the NPN pair is on and the PNP pair is off. When the V_{CM} is near V^-, the NPN pair is off and the PNP pair is on. The crossover point between the NPN and PNP input stages is around 950mV from V^+. Since each input stage has its own offset voltage (V_{OS}), the V_{OS} of the comparator becomes a function of the V_{CM}. See curves for V_{OS} vs. V_{CM} in Typical Performance Characteristics section. In application design, it is recommended to keep the V_{CM} away from the crossover point to avoid problems. The wide input voltage range makes LMV727X ideal in power supply monitoring circuits, where the comparators are used to sense signals close to ground and power supplies.

OUTPUT STAGE

The LMV7271 and LMV7272 have a push-pull output stage. This output stage keeps the total system power consumption to the absolute minimum. The only current consumed is the low supply current and the current going directly into the load. When the output switches, both PMOS and NMOS at the output stage are on at the same time for a very short time. This allows current to flow directly between V^+ and V^- through output transistors. The result is a short spike of current (shoot-through current) drawn from the supply and glitches in the supply voltages. The glitches can spread to other parts of the board as noise. To prevent the glitches in supply lines, power supply bypass capacitors must be installed. See section for supply bypassing in the Application Notes for details.

HYSTERESIS

It is a standard procedure to use hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier of its own noise.

Inverting Comparator with Hysteresis

The inverting comparator with hysteresis requires a three resistor network that is referenced to the supply voltage V_{CC} of the comparator (Figure 29). When V_{IN} at the inverting input is less than V_A, the voltage at the non-inverting node of the comparator ($V_{IN} < V_A$), the output voltage is high (for simplicity assume V_O switches as high as V_{CC}). The three network resistors can be represented as $R_1||R_3$ in series with R_2. The lower input trip voltage V_{A1} is defined as

$$V_{A1} = \frac{V_{CC}\, R_2}{(R_1||R_3) + R_2} \tag{1}$$

When V_{IN} is greater than V_A ($V_{IN} > V_A$), the output voltage is low and very close to ground. In this case the three network resistors can be presented as $R_2//R_3$ in series with R_1. The upper trip voltage V_{A2} is defined as

$$V_{A2} = \frac{V_{CC}\, (R_2||R_3)}{R_1 + (R_2||R_3)} \tag{2}$$

The total hysteresis provided by the network is defined as

$$\Delta V_A = V_{A1} - V_{A2} \tag{3}$$

A good typical value of ΔV_A would be in the range of 5 to 50mV. This is easily obtained by choosing R_3 as 1000 to 100 times ($R_1||R_2$) for 5V operation, or as 300 to 30 times ($R_1||R_2$) for 1.8V operation.

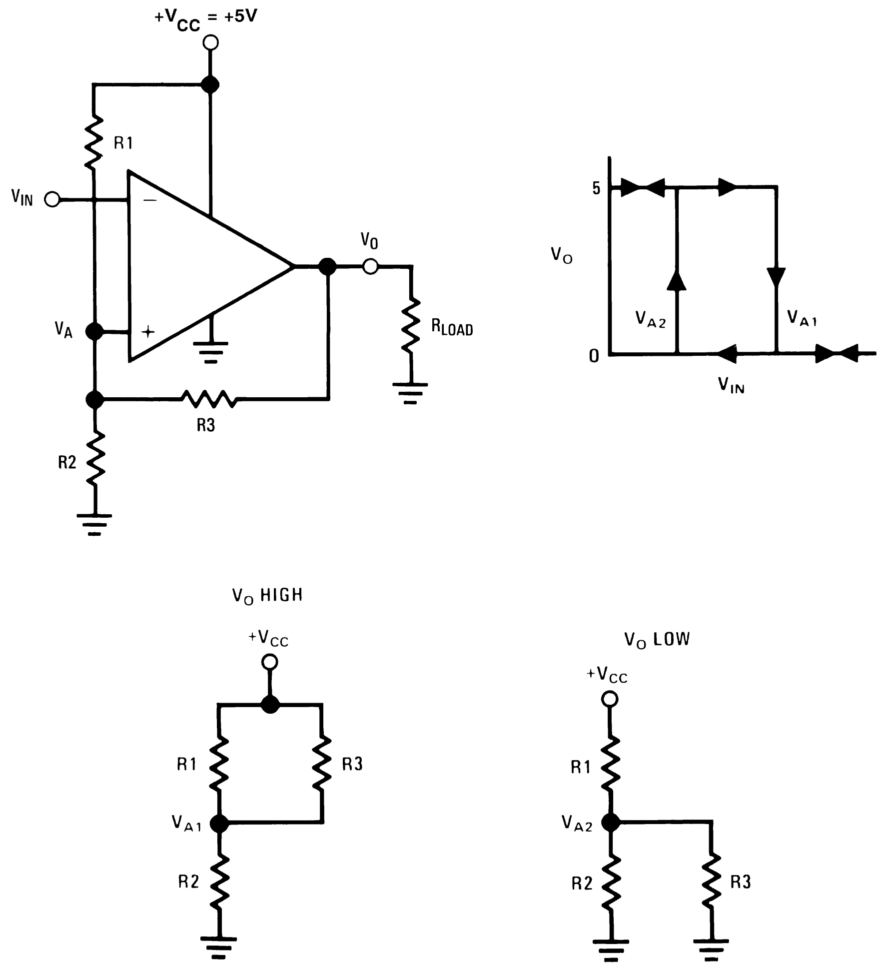


Figure 29. Inverting Comparator with Hysteresis

Non-Inverting Comparator with Hysteresis

A non-inverting comparator with hysteresis requires a two resistor network, and a voltage reference (V_{REF}) at the inverting input (Figure 30). When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise up to V_{IN1}, where V_{IN1} is calculated by

$$V_{in1} = \frac{V_{ref}(R_1 + R_2)}{R_2} \tag{4}$$

When V_{IN} is high, the output is also high. To make the comparator switch back to its low state, V_{IN} must equal V_{REF} before V_A will again equal V_{REF}. V_{IN} can be calculated by:

$$V_{in2} = \frac{V_{ref}(R_1 + R_2) - V_{CC}R_1}{R_2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}.

$$\Delta V_{IN} = V_{CC}R_1/R_2 \tag{6}$$

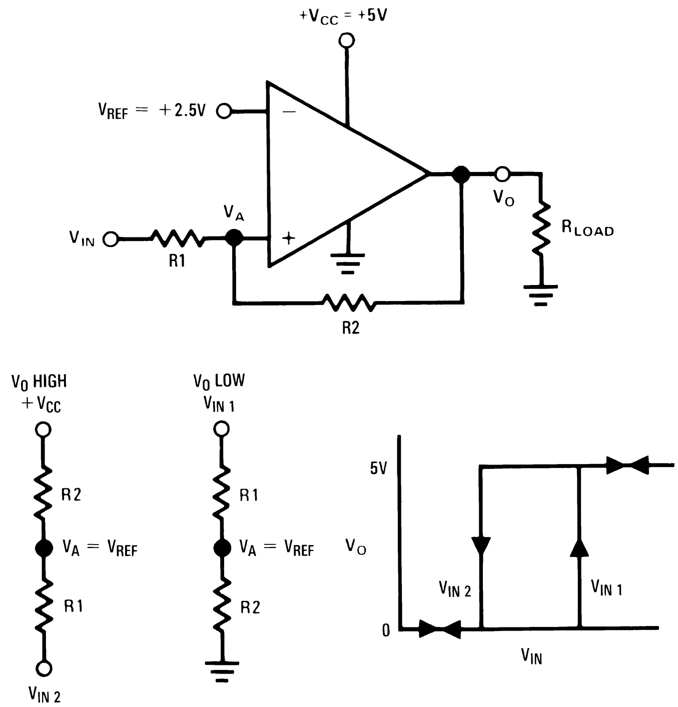


Figure 30. Non-Inverting Comparator with Hysteresis

CIRCUIT TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

Feedback to almost any pin of a comparator can result in oscillation. In addition, when the input signal is a slow voltage ramp or sine wave, the comparator may also burst into oscillation near the crossing point. To avoid oscillation or instability, PCB layout should be engineered thoughtfully. Several precautions are recommended:

1. Power supply bypassing is critical, and will improve stability and transient response. Resistance and inductance from power supply wires and board traces increase power supply line impedance. When supply current changes, the power supply line will move due to its impedance. Large enough supply line shift will cause the comparator to mis-operate. To avoid problems, a small bypass capacitor, such as 0.1uF ceramic, should be placed immediately adjacent to the supply pins. An additional 6.8μF or greater tantalum capacitor should be placed at the point where the power supply for the comparator is introduced onto the board. These capacitors act as an energy reservoir and keep the supply impedance low. In dual supply application, a 0.1μF capacitor is recommended to be placed across V^+ and V^- pins.
2. Keep all leads short to reduce stray capacitance and lead inductance. It will also minimize any unwanted coupling from any high-level signals (such as the output). The comparators can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Try to avoid a long loop which could act as an inductor (coil).
3. It is a good practice to use an unbroken ground plane on a printed circuit board to provide all components with a low inductive ground connection. Make sure ground paths are low-impedance where heavier currents are flowing to avoid ground level shift. Preferably there should be a ground plane under the component.
4. The output trace should be routed away from inputs. The ground plane should extend between the output and inputs to act as a guard. This can be achieved by running a topside ground plane between the output and inputs. A typical PCB layout is shown in Figure 31.

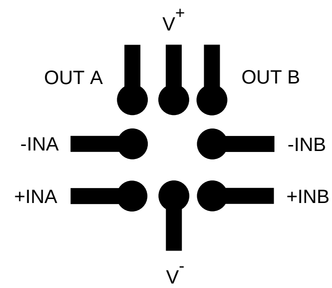


Figure 31. Typical PCB Layout

5. When the signal source is applied through a resistive network to one input of the comparator, it is usually advantageous to connect the other input with a resistor with the same value, for both DC and AC consideration. Input traces should be laid out symmetrically if possible.
6. All pins of any unused comparators should be tied to the negative supply.

DSBGA LIGHT SENSITIVITY

Exposing the DSBGA device to direct sunlight will cause mis-operation of the device. Light sources such as Halogen lamps can also affect electrical performance if brought near to the device. The wavelengths, which have the most detrimental effect, are reds and infrareds.

DSBGA MOUNTING

The DSBGA package requires specific mounting techniques, which are detailed in Application Note AN-1112 (SNVA009).

LMV7272 DSBGA to DIP Conversion Board

To facilitate characterization and testing, a DSBGA to DIP conversion board, LMV7272TLCONV, is available. It is a 2-layer board, with the LMV7272 mounted on the bottom layer, and a capacitor (C1, between the positive and negative supplies) added to the top layer.

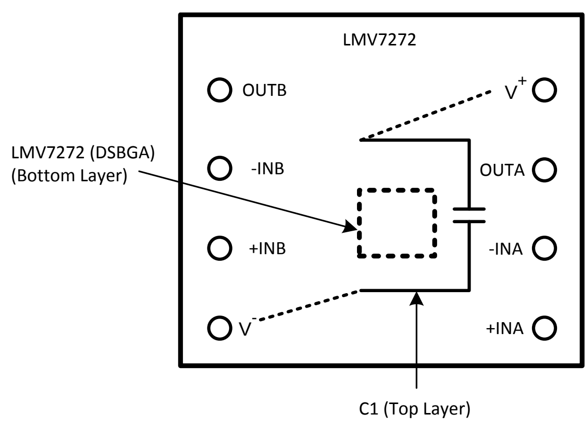


Figure 32. LMV7272TLCONV Diagram

Typical Applications

UNIVERSAL LOGIC LEVEL SHIFTER

The output of LMV7275 is an unconnected drain of an NMOS device, which can be pulled up, through a resistor, to any desired output level within the permitted power supply range. Hence, the following simple circuit works as a universal logic level shifter, pulling up the signal to the desired level.

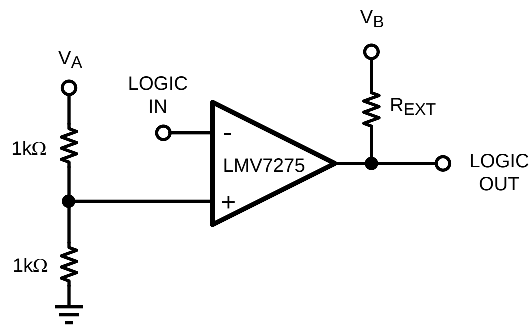


Figure 33. Logic Level Shifter

POSITIVE PEAK DETECTOR

A positive peak detect circuit is basically a comparator operated in a unity gain follower configuration, with a capacitor as a load to maintain the highest voltage. A diode is added at the output to prevent the capacitor from discharging through the pull-up resistor, and a 1MΩ resistor added in parallel to the capacitor to provide a high impedance discharge path. When the input V_{IN} increases, the inverting input of the comparator follows it, thus charging the capacitor. When it decreases, the cap discharges through the 1MΩ resistor. The decay time can be modified by changing the resistor. The output should be accessed through a follower circuit to prevent loading.

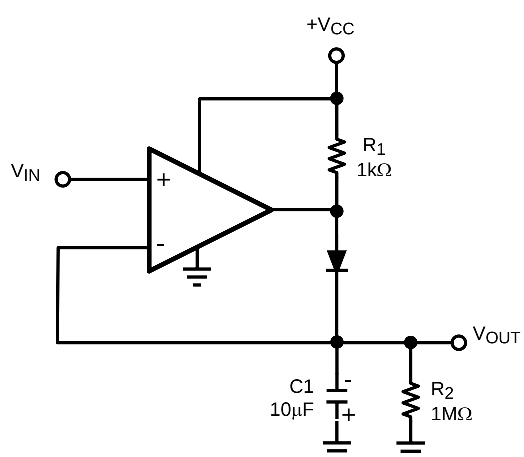


Figure 34. Positive Peak Detector

OR'ING THE OUTPUT

Since the output is an unconnected NMOS drain, many drains can be tied together, pulled up to V_{DD} by a single resistor to provide an output OR'ing function. If any of the comparator outputs is pulled low the output V_O goes down.

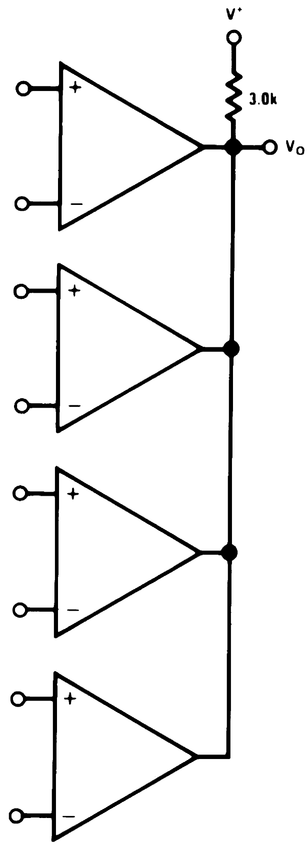


Figure 35. OR’ing the Outputs

NEGATIVE PEAK DETECTOR

For the negative detector, the output transistor of the comparator acts as a low impedance current sink. Since there is no pull-up resistor, the only discharge path will be the 1MΩ resistor and any load impedance used. Decay time is changed by varying the 1MΩ resistor.

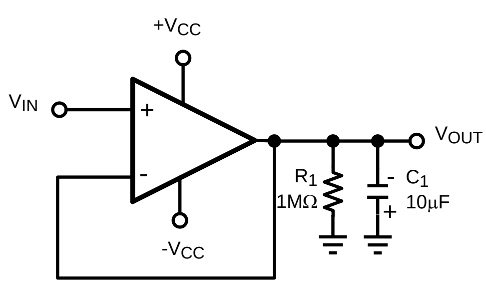


Figure 36. Negative Peak Detector

SQUARE WAVE GENERATOR

A typical application for a comparator is as a square wave oscillator. The circuit below generates a square wave whose period is set by the RC time constant of the capacitor $C_1$and resistor R_4. The maximum frequency is limited by the large signal propagation delay of the comparator, and by the capacitive loading at the output, which limits the output slew rate.

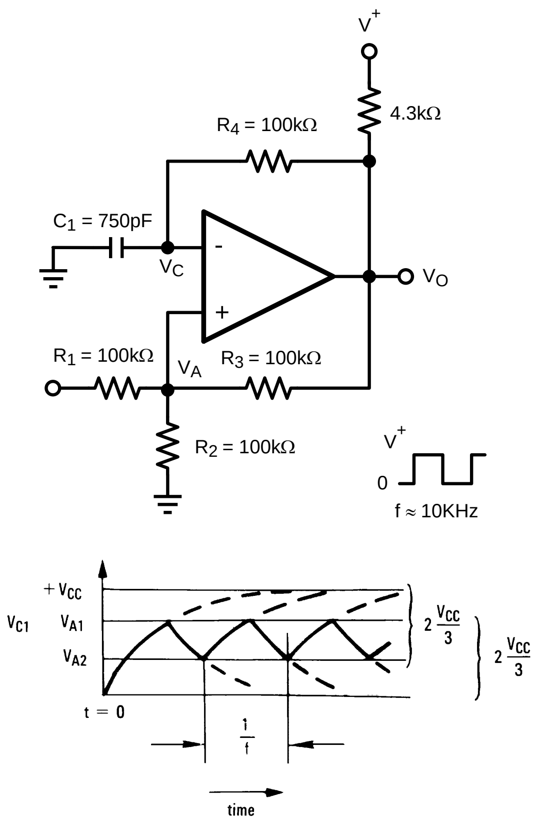


Figure 37. Squarewave Oscillator

To analyze the circuit, consider it when the output is high. That implies that the inverted input (V_C) is lower than the non-inverting input (V_A). This causes the C_1 to get charged through $R_{4,}$ and the voltage V_C increases till it is equal to the non-inverting input. The value of V_A at this point is

$$V_{A1} = \frac{V_{CC}.R_2}{R_2 + R_1||R_3} \tag{7}$$

If $R_1 = R_2 = R_3$, then $V_{A1} = 2V_{CC}/3$

At this point the comparator switches pulling down the output to the negative rail. The value of V_A at this point is

$$V_{A2} = \frac{V_{CC}\,(R_2||R_3)}{R_1 + (R_2||R_3)} \tag{8}$$

If $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$

The capacitor C_1 now discharges through R_4, and the voltage V_C decreases till it is equal to V_{A2}, at which point the comparator switches again, bringing it back to the initial stage. The time period is equal to twice the time it takes to discharge C_1 from $2V_{CC}/3$ to $V_{CC}/3$, which is given by R_4C_1.ln2. Hence the formula for the frequency is:

$F = 1/(2 \cdot R_4 \cdot C_1 \cdot \ln 2)$

REVISION HISTORY

Changes from Revision G (February 2013) to Revision H	Page
• Changed layout of National Data Sheet to TI format	19

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV7271MF	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	C25A	
LMV7271MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C25A	Samples
LMV7271MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C25A	Samples
LMV7271MG	NRND	SC70	DCK	5	1000	TBD	Call TI	Call TI	-40 to 85	C34	
LMV7271MG/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C34	Samples
LMV7271MGX/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C34	Samples
LMV7272TL/NOPB	ACTIVE	DSBGA	YZR	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C 01	Samples
LMV7272TLX/NOPB	ACTIVE	DSBGA	YZR	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C 01	Samples
LMV7275MF	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	C26A	
LMV7275MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C26A	Samples
LMV7275MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C26A	Samples
LMV7275MG	NRND	SC70	DCK	5	1000	TBD	Call TI	Call TI	-40 to 85	C35	
LMV7275MG/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C35	Samples
LMV7275MGX/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C35	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

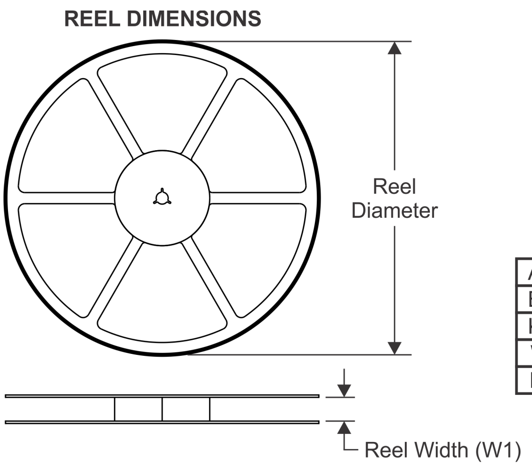
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

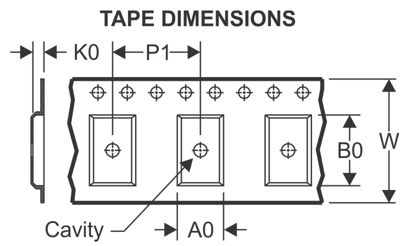
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

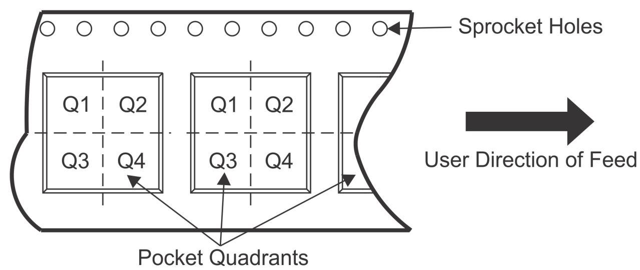
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

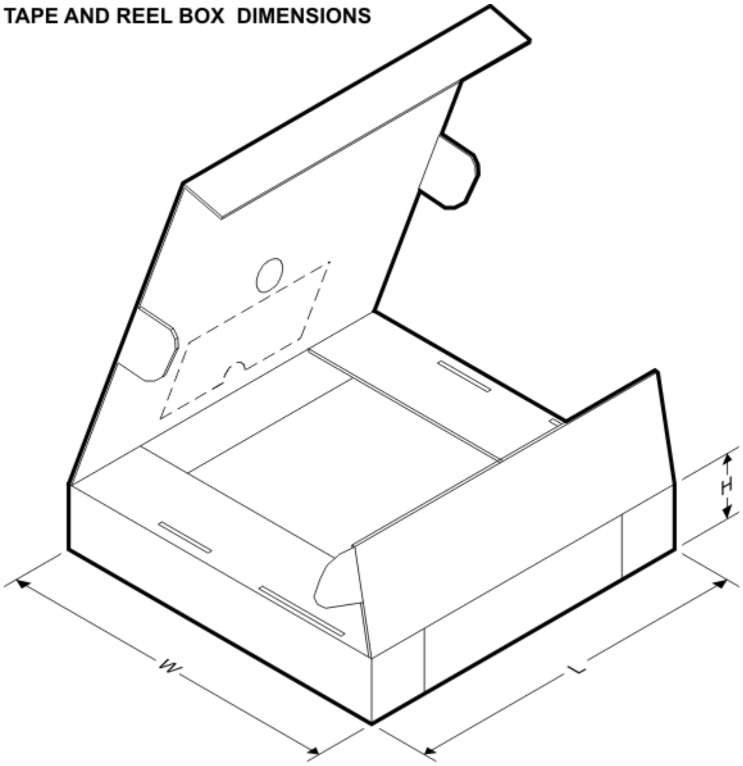
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV7271MF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7271MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7271MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7271MG	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7271MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7271MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7272TL/NOPB	DSBGA	YZR	8	250	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1
LMV7272TLX/NOPB	DSBGA	YZR	8	3000	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1
LMV7275MF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7275MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7275MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7275MG	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7275MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7275MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

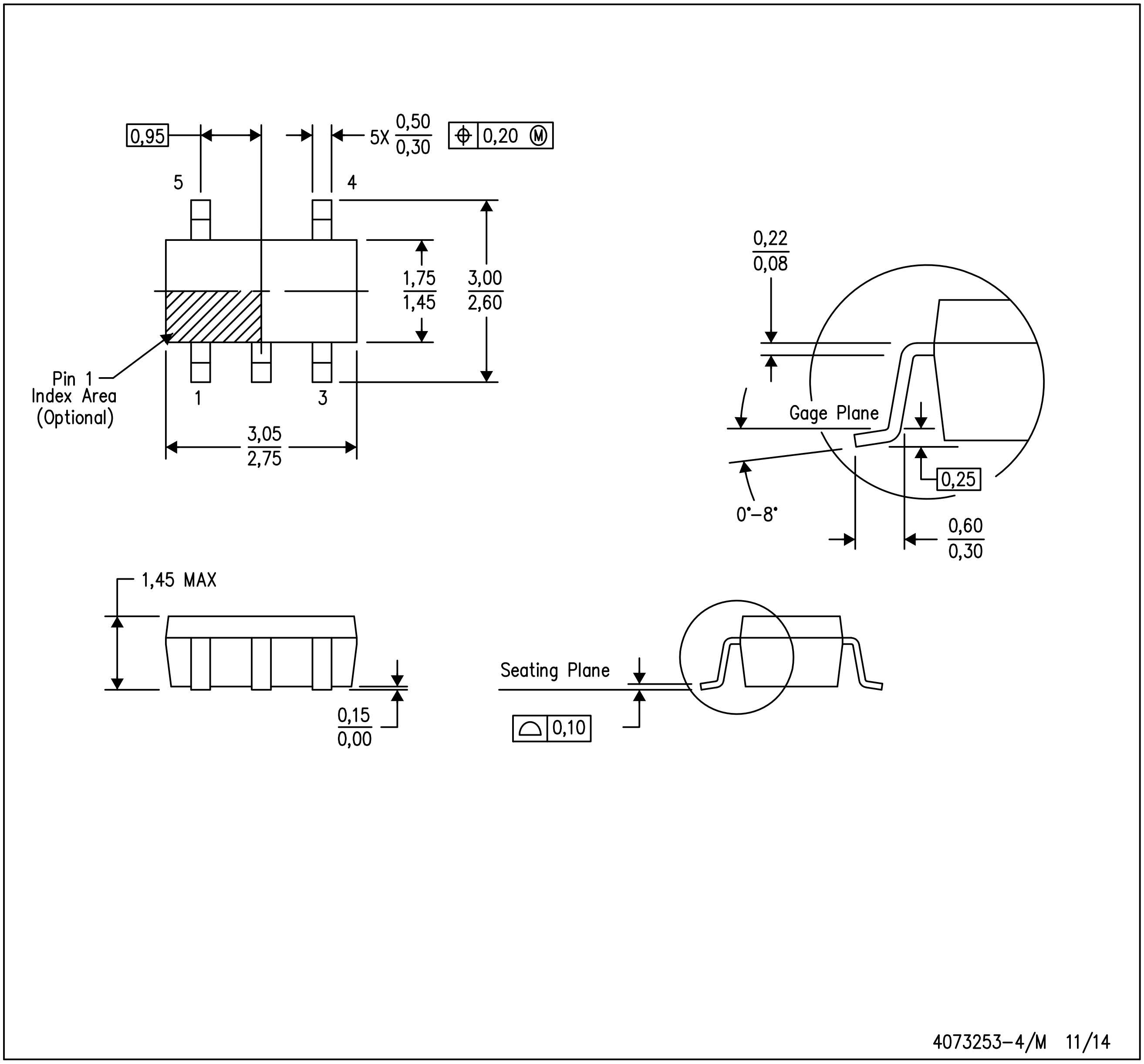
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

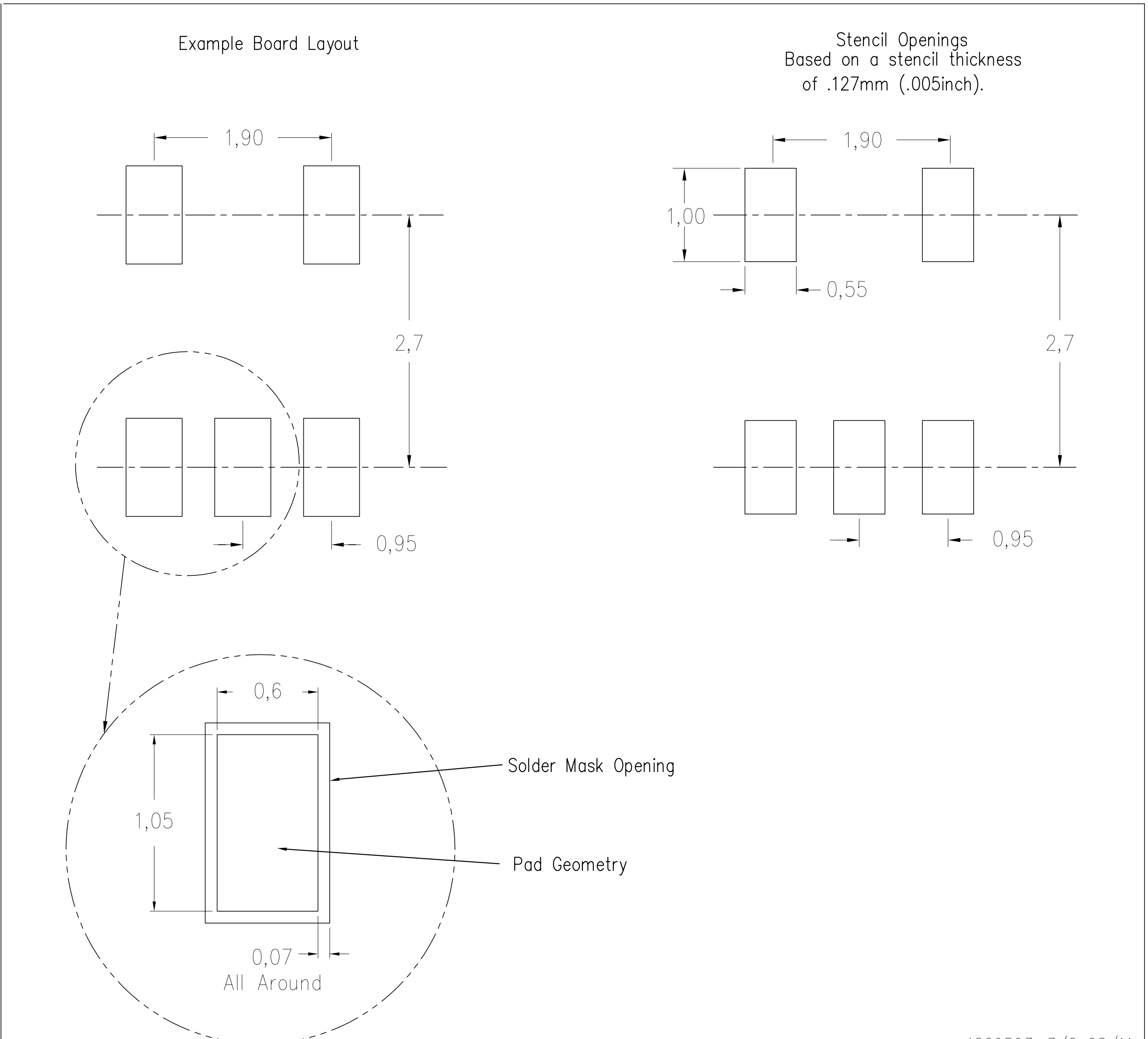
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV7271MF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV7271MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV7271MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV7271MG	SC70	DCK	5	1000	210.0	185.0	35.0
LMV7271MG/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV7271MGX/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LMV7272TL/NOPB	DSBGA	YZR	8	250	210.0	185.0	35.0
LMV7272TLX/NOPB	DSBGA	YZR	8	3000	210.0	185.0	35.0
LMV7275MF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV7275MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV7275MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV7275MG	SC70	DCK	5	1000	210.0	185.0	35.0
LMV7275MG/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV7275MGX/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE

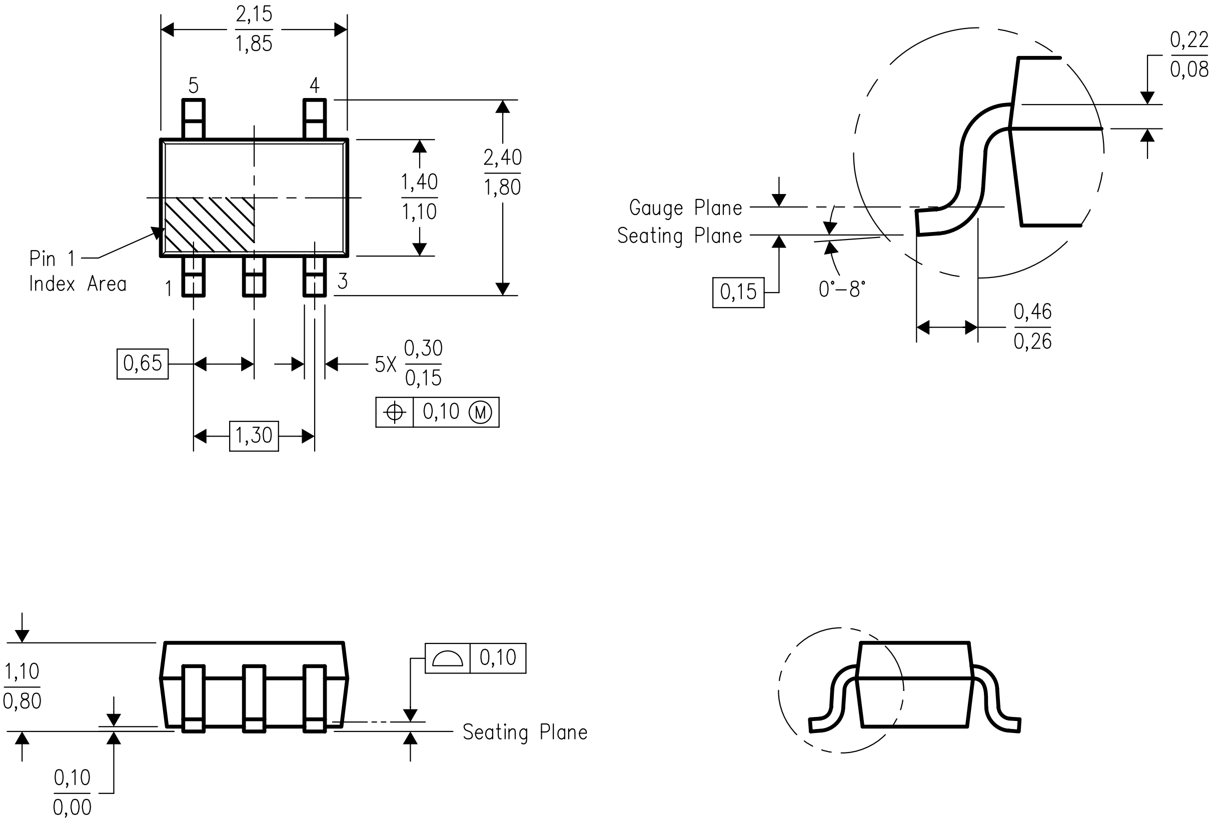


4209593–3/C 08/11

NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

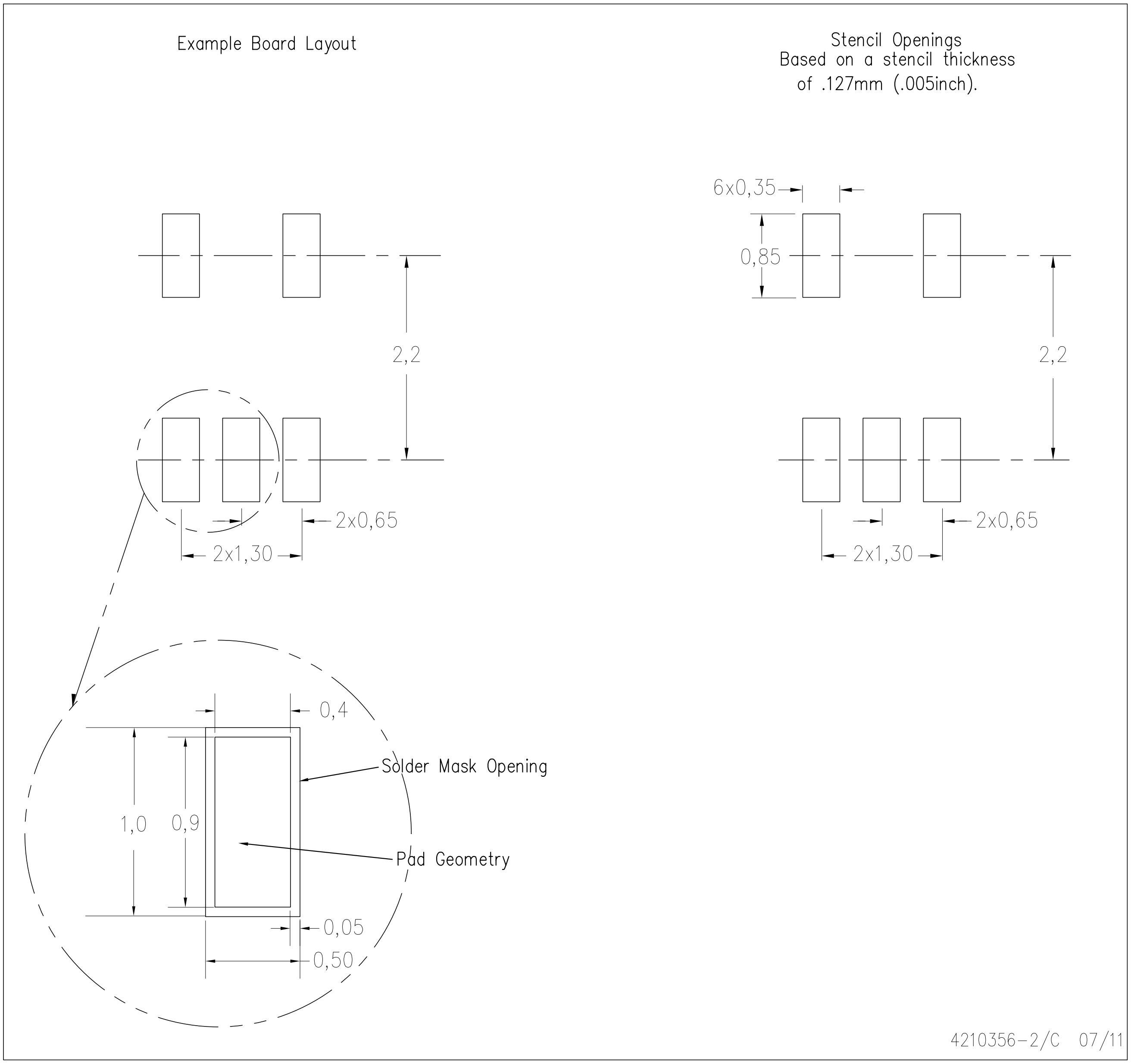
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

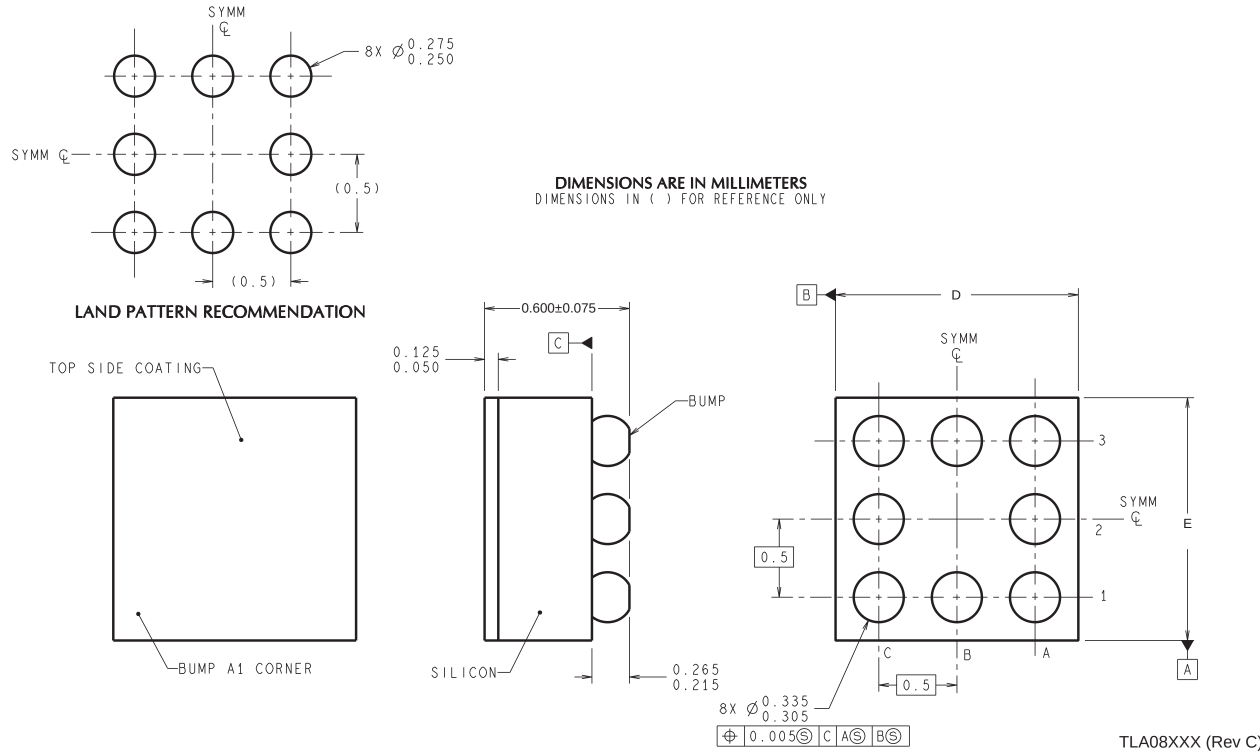
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R-PDSO-G5) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

YZR0008



D: Max = 1.55 mm, Min = 1.489 mm

E: Max = 1.55 mm, Min = 1.489 mm

4215045/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

AMEYA360
Components Supply Platform

Authorized Distribution Brand :

Website :

Welcome to visit www.ameya360.com

Contact Us :

- Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
Minhang District, Shanghai , China

- Sales :

Direct +86 (21) 6401-6692

Email amall@ameya360.com

QQ 800077892

Skype ameyasales1 ameyasales2

- Customer Service :

Email service@ameya360.com

- Partnership :

Tel +86 (21) 64016692-8333

Email mkt@ameya360.com