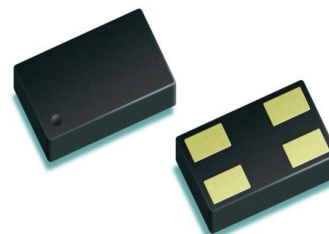


RF ESD Protection Diodes

- ESD protection of RF antenna / interfaces or ultra high speed data lines acc. to:
IEC61000-4-2 (ESD): ± 20 kV (air / contact)
IEC61000-4-4 (EFT): 40 A (5/50 ns)
IEC61000-4-5 (surge): 10 A (8/20 μ s)
- Very low line capacitance: 0.8 pF @ 1 GHz
(0.4 pF per diode)
- Ultra low series inductance: 0.4 nH per diode
- Very low clamping voltage
- Ultra small leadless package 1.2 x 0.8 x 0.39 mm
- Pb-free (RoHS compliant) package



Applications in anti-parallel configuration

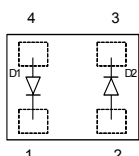
- For low RF signal levels without superimposed DC voltage: e.g. GPS, XM-Radio, Sirius, DVB, DMB, DAB, Remote Keyless Entry

Applications in rail-to-rail configuration

- For high RF signal levels or low RF signal levels with superimposed DC voltage: e.g. HDMI, S-ATA, Gbit Ethernet
- For more technical details on ESD and Antenna protection please refer to Application Note No.103 on www.infineon.com/tvsdiodes



ESD0P8RFL



Type	Package	Configuration	Marking
ESD0P8RFL	TSLP-4-7	anti-parallel	E8

Maximum Ratings at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Value	Unit
ESD contact discharge ¹⁾	V_{ESD}	20	kV
Peak pulse current ($t_p = 8 / 20 \mu\text{s}$) ²⁾	I_{pp}	10	A
Operating temperature range	T_{op}	-55...150	$^\circ\text{C}$
Storage temperature	T_{stg}	-65...150	

Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Characteristics -					
Reverse working voltage ³⁾	V _{RWM}	-	-	50	V
Reverse current ³⁾ V _R = 50 V	I _R	-	-	100	nA
Forward clamping voltage ²⁾ I _{PP} = 10 A	V _{FC}	-	12	15	V
Line capacitance ⁴⁾ V _R = 0 V, f = 1 GHz	C _T	-	0.8	-	pF
Series inductance (per diode)	L _S	-	0.4	-	nH

¹⁾ V_{ESD} according to IEC61000-4-2, only valid in anti-parallel or rail-to-rail connection.

Please refer to the application examples.

²⁾ I_{pp} according to IEC61000-4-5, only valid in anti-parallel or rail-to-rail connection.

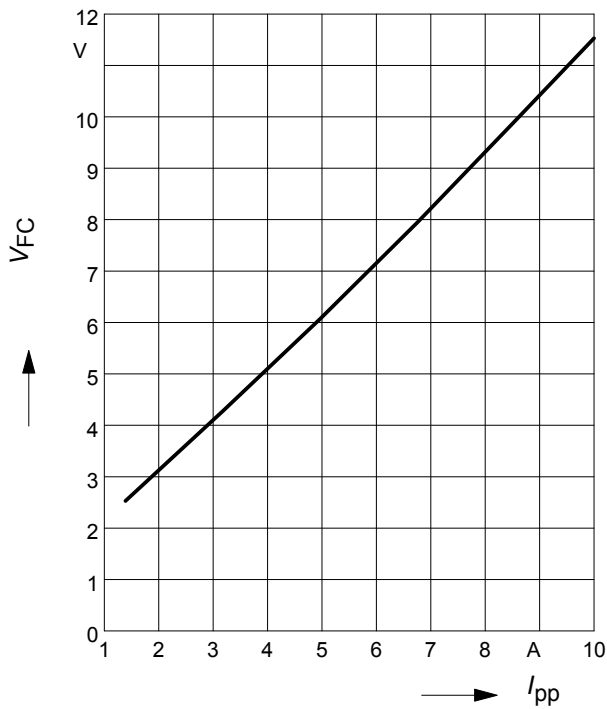
Please refer to the application examples.

³⁾Only valid in rail-to-rail configuration with $V_{\text{CC}} \geq V_{\text{RWM}}$

⁴⁾Total capacitance line to ground (2 diodes in parallel)

Forward clamping voltage $V_{FC} = f(I_{PP})$

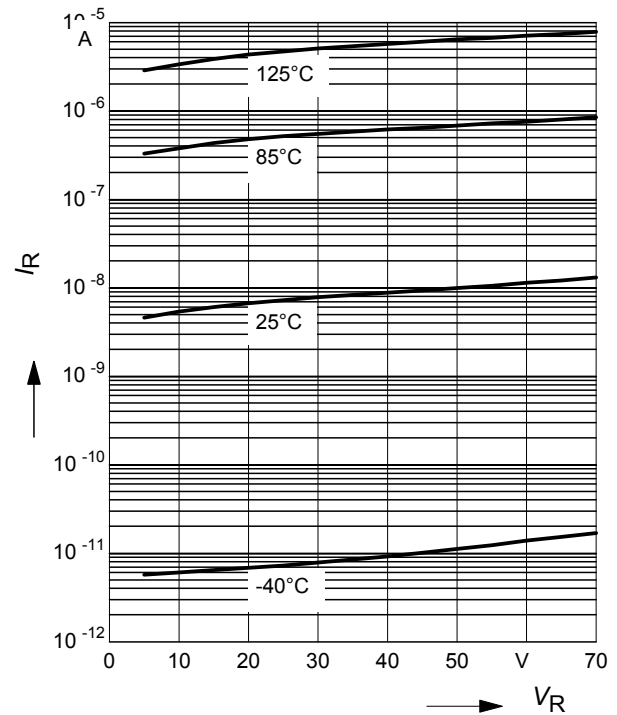
$t_p = 8 / 20 \mu s$



Reverse current $I_R = f(V_R)$

$T_A = \text{Parameter}$

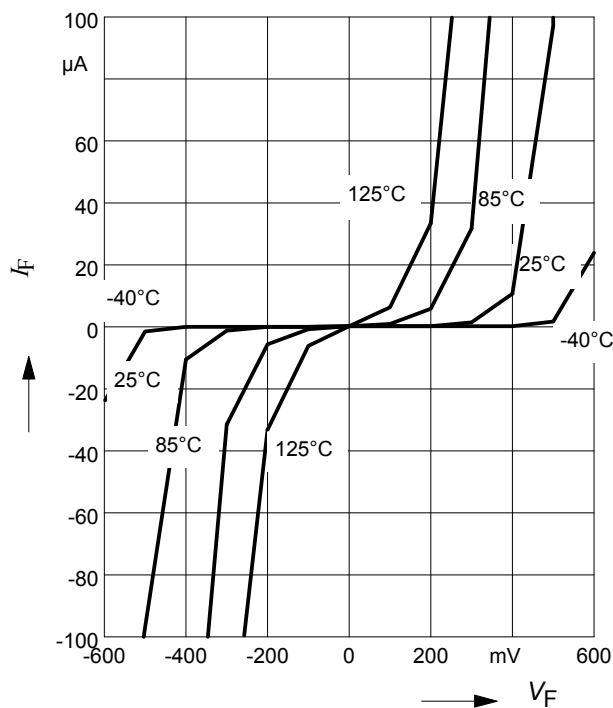
leakage in rail-to-rail configuration



Forward current $I_F = f(V_F)$

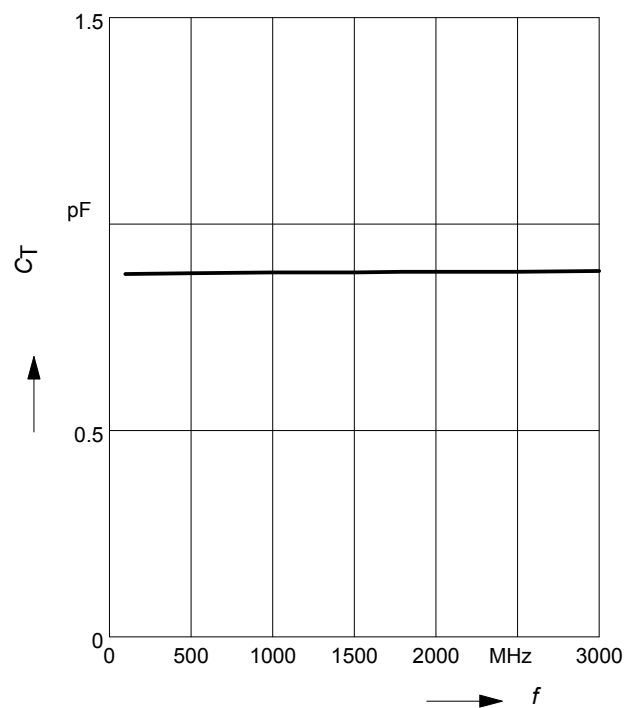
$T_A = \text{Parameter}$

leakage in anti-parallel configuration



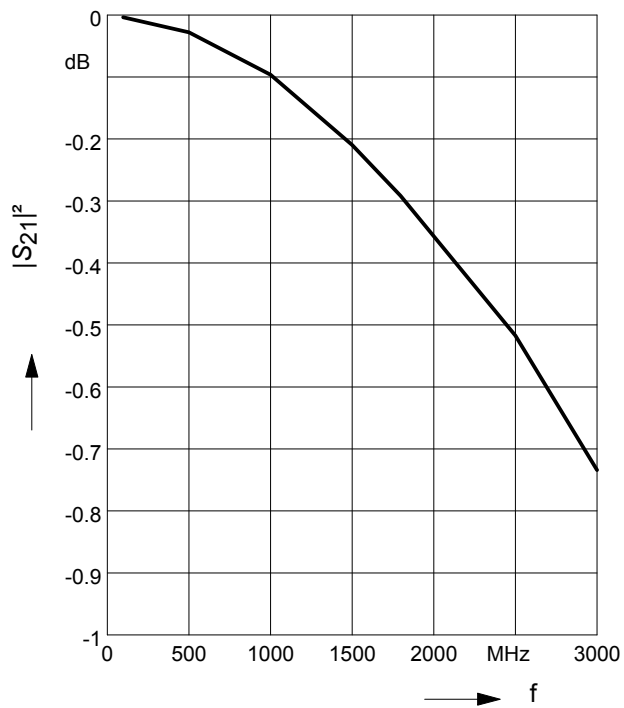
Line capacitance $C_T = f(f)$

$V_R = 0 V$



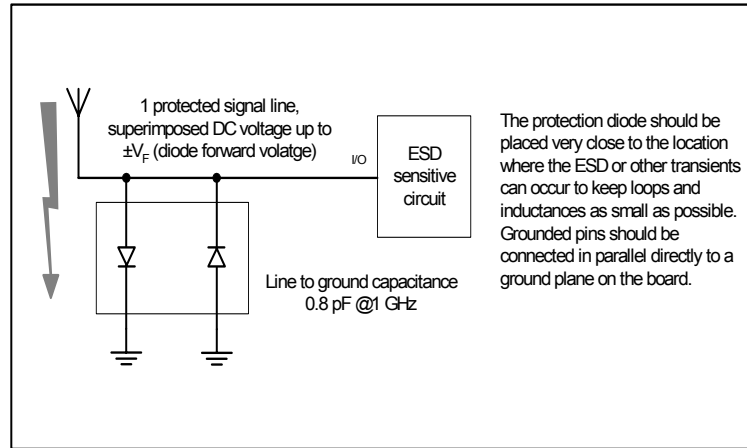
Insertion loss $I_L = -|S_{21}|^2 = f(f)$

$V_R = 0 \text{ V}$, $Z = 50 \Omega$



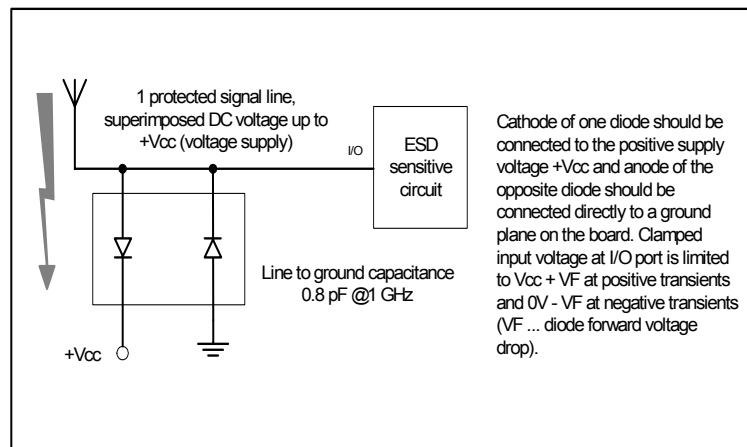
1. Application example

1 RF signal channel, anti-parallel configuration,
please refer also to Application Note No.103



2. Application example

1 RF signal channel, rail-to-rail configuration



Technical drawing of a 2x2 grid of holes. The drawing shows a rectangular plate with four holes arranged in a square pattern. The dimensions and tolerances are as follows:

- Overall width: $4 \times 0.25 \pm 0.035$ (labeled 1¹⁾)
- Overall height: $4 \times 0.35 \pm 0.035$ (labeled 1¹⁾)
- Distance between hole centers (pitch): 0.8 ± 0.05
- Distance from the left edge to the first hole center: 0.45 ± 0.05
- Distance from the bottom edge to the first hole center: 0.75 ± 0.05
- Distance from the right edge to the last hole center: 1.2 ± 0.05
- The holes are numbered 1, 2, 3, and 4 in a clockwise direction starting from the bottom-left.

☒ Stencil apertures

Technical drawing of a mechanical part. The main view shows a rectangular part with a width of 4 and a height of 8. There are four circular features arranged in a 2x2 grid, with a center-to-center distance of 1.45 between adjacent circles. A dimension of 1.05 is shown from the left edge to the center of the first circle. A detail view on the right shows a cross-section of a pin with a diameter of 0.5. A label 'Pin 1 marking' points to the first circle in the grid.

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