USB-Charging Port Controller and Power Switch With Load Detection

Check for Samples: TPS2546-Q1

FEATURES

- **AEC-Q100 Qualified**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C5**
- **Operating Range: 4.5 V to 5.5 V**
- **Automatic SDP and CDP Switching for Devices that do Not Connect to CDP Ports**
- **D+/D– CDP and DCP Modes per USB Battery Charging Specification 1.2**
- **D+/D– Shorted Mode per Chinese Telecommunication Industry Standard YD/T 1591-2009**
- **Automatically Selects Charge Mode in Non-BC1.2 Devices**
  - **D+/D– Divider Modes 2 / 2.7 V and 2.7 / 2 V**
  - **D+/D– 1.2 V Mode**
- **Supports Sleep-Mode Charging and Wake Up by Mouse and Keyboard**
- **Load Detection in S4 and S5 States Supports Intelligent Power Management**
- **73-mΩ (typ) High-Side MOSFET**
- **Adjustable Current-Limit up to 3 A (typ)**
- **Max Device Current**
  - **2 µA When Device Disabled**
  - **270 µA When Device Enabled**
- **Drop-In and BOM Compatible with TPS2543**
- **16-Pin WQFN (3 × 3) Package**

APPLICATIONS

- **Automotive**
- **USB Ports (Host and Hubs)**
- **Notebook and Desktop PCs**
- **Universal Wall-Charging Adapters**

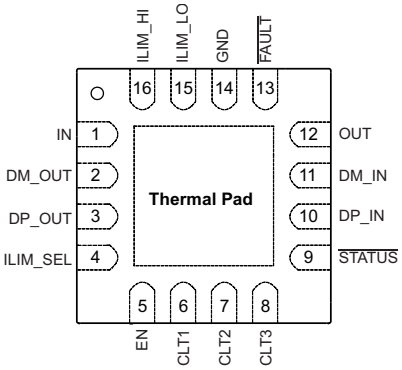
DESCRIPTION

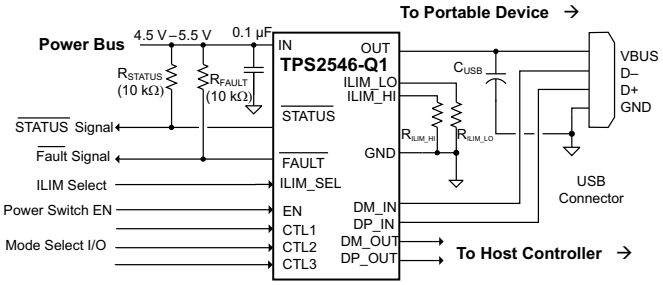
The TPS2546-Q1 device is a USB-charging port controller and power switch with an integrated USB 2.0 high-speed data-line (D+ and D–) switch. The TPS2546-Q1 provides the electrical signatures on D+ and D– to support charging schemes as described in the FEATURES of this data sheet. Texas Instruments tests the charging of popular mobile phones, tablets, and media devices with the TPS2546-Q1 device to ensure compatibility with both BC1.2 compliant and non-BC1.2 compliant devices.

In addition to charging popular devices, the TPS2546-Q1 device also supports two distinct power-management features: power wake and port-power management (PPM) through the $\overline{\text{STATUS}}$ pin. Power wake allows for power supply control in S4 or S5 charging and provides PPM with the ability to manage port power in a multiport application. Additionally, system wakeup (from S3) with a mouse or keyboard (at both low speed and full speed) is fully supported by the TPS2546-Q1 device.

The TPS2546-Q1 73-mΩ power-distribution switch is intended for applications where heavy capacitive loads and short circuits are encountered. Two programmable current thresholds provide flexibility for setting current limits and load detect thresholds.

TPS2546-Q1 RTE PACKAGE AND TYPICAL APPLICATION DIAGRAM





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range, voltages are referenced to GND (unless otherwise noted)

			MIN	MAX	UNIT
Voltage range	IN, EN, ILIM_LO, ILIM_HI, $\overline{\text{FAULT}}$, $\overline{\text{STATUS}}$, ILIM_SEL, CTL1, CTL2, CTL3, OUT		–0.3	7	V
	IN to OUT		–7	7	
	DP_IN, DM_IN, DP_OUT, DM_OUT		–0.3	(IN + 0.3) or 5.7	
Input clamp current	DP_IN, DM_IN, DP_OUT, DM_OUT			±20	mA
Continuous current in SDP or CDP mode	DP_IN to DP_OUT or DM_IN to DM_OUT			±100	mA
Continuous current in BC1.2 DCP mode	DP_IN to DM_IN			±50	mA
Continuous output current	OUT			Internally limited	
Continuous output sink current	$\overline{\text{FAULT}}$, $\overline{\text{STATUS}}$			25	mA
Continuous output source current	ILIM_LO, ILIM_HI			Internally limited	mA
Electrostatic discharge rating	HBM	AEC-Q100 Classificaiton Level H2		2	kV
	CDM	AEC-Q100 Classificaiton Level C5		750	V
Operating junction temperature, T_J			–40	Internally limited	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS2546-Q1 RTE (16 PIN)	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	53.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	51.4	
θ_{JB}	Junction-to-board thermal resistance	17.2	
ψ_{JT}	Junction-to-top characterization parameter	3.7	
ψ_{JB}	Junction-to-board characterization parameter	20.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	3.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

voltages are referenced to GND (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage, IN	4.5	5.5	V
	Input voltage, logic-level inputs, EN, CTL1, CTL2, CTL3, ILIM_SEL	0	5.5	V
	Input voltage, data line inputs, DP_IN, DM_IN, DP_OUT, DM_OUT	0	V_{IN}	V
V_{IH}	High-level input voltage, EN, CTL1, CTL2, CTL3, ILIM_SEL	1.8		V
V_{IL}	Low-level input voltage, EN, CTL1, CTL2, CTL3, ILIM_SEL		0.8	V
	Continuous current, data line inputs, SDP or CDP mode, DP_IN to DP_OUT, DM_IN to DM_OUT		±30	mA
	Continuous current, data line inputs, BC1.2 DCP mode, DP_IN to DM_IN		±15	mA
I_{OUT}	Continuous output current, OUT	0	2.5	A
	Continuous output sink current, $\overline{\text{FAULT}}$, $\overline{\text{STATUS}}$	0	10	mA
R_{ILIM_XX}	Current-limit set resistors	16.9	750	kΩ
T_J	Operating virtual junction temperature	–40	125	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted: $-40 \le T_J \le 125°C$, $4.5\ V \le V_{IN} \le 5.5\ V$, $V_{EN} = V_{IN}$, $V_{ILIM\_SEL} = V_{IN}$, $V_{CTL1} = V_{CTL2} = V_{CTL3} = V_{IN}$. $R_{\overline{FAULT}} = R_{\overline{STATUS}} = 10\ k\Omega$, $R_{ILIM\_HI} = 20\ k\Omega$, $R_{ILIM\_LO} = 80.6\ k\Omega$. Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH						
$R_{DS(on)}$	On resistance(1)	$T_J = 25°C$, $I_{OUT} = 2\ A$		73	84	mΩ
		$-40°C \le T_J \le 85°C$, $I_{OUT} = 2\ A$		73	105	
		$-40°C \le T_J \le 125°C$, $I_{OUT} = 2\ A$		73	120	
t_r	OUT voltage rise time	$V_{IN} = 5\ V$, $C_L = 1\ \mu F$, $R_L = 100\ \Omega$ (see Figure 23 and Figure 24)	0.7	1	1.6	ms
t_f	OUT voltage fall time		0.2	0.35	0.5	
t_{on}	OUT voltage turn-on time	$V_{IN} = 5\ V$, $C_L = 1\ \mu F$, $R_L = 100\ \Omega$ (see Figure 23 and Figure 25)		2.7	4	ms
t_{off}	OUT voltage turn-off time			1.7	3	
I_{REV}	Reverse leakage current	$V_{OUT} = 5.5\ V$, $V_{IN} = V_{EN} = 0\ V$, $-40 \le T_J \le 85°C$, Measure I_{OUT}			2	µA
DISCHARGE						
R_{DCHG}	OUT discharge resistance		400	500	630	Ω
t_{DCHG_L}	Long OUT discharge hold time	Time $V_{OUT} < 0.7\ V$ (see Figure 26)	1.3	2	2.9	s
t_{DCHG_S}	Short OUT discharge hold time	Time $V_{OUT} < 0.7\ V$ (see Figure 26)	205	310	450	ms
EN, ILIMSEL, CTL1, CTL2, CTL3 INPUTS						
	Input pin rising logic threshold voltage		1	1.35	1.70	V
	Input pin falling logic threshold voltage		0.85	1.15	1.45	V
	Hysteresis(2)			200		mV
	Input current	Pin voltage = 0 V or 5.5 V	–0.5		0.5	µA
ILIMSEL CURRENT LIMIT						
I_{OS}	OUT short circuit current limit(1)	$V_{ILIM\_SEL} = 0\ V$, $R_{ILIM\_LO} = 210\ k\Omega$	205	240	275	mA
		$V_{ILIM\_SEL} = 0\ V$, $R_{ILIM\_LO} = 80.6\ k\Omega$	575	625	680	
		$V_{ILIM\_SEL} = 0\ V$, $R_{ILIM\_LO} = 22.1\ k\Omega$	2120	2275	2430	
		$V_{ILIM\_SEL} = V_{IN}$, $R_{ILIM\_HI} = 20\ k\Omega$	2340	2510	2685	
		$V_{ILIM\_SEL} = V_{IN}$, $R_{ILIM\_HI} = 16.9\ k\Omega$	2770	2970	3170	
t_{IOS}	Response time to OUT short circuit(2)	$V_{IN} = 5.0\ V$, $R = 0.1\ \Omega$, lead length = 2 inches (see Figure 27)		1.5		µs
SUPPLY CURRENT						
I_{IN_OFF}	Disabled IN supply current	$V_{EN} = 0\ V$, $V_{OUT} = 0\ V$, $-40 \le T_J \le 85°C$		0.1	2	µA
I_{IN_ON}	Enabled IN supply current	$V_{CTL1} = V_{CTL2} = V_{IN}$, $V_{CTL3} = 0\ V$, $V_{ILIM\_SEL} = 0\ V$		165	220	µA
		$V_{CTL1} = V_{CTL2} = V_{CTL3} = V_{IN}$, $V_{ILIM\_SEL} = 0\ V$		175	230	
		$V_{CTL1} = V_{CTL2} = V_{IN}$, $V_{CTL3} = 0\ V$, $V_{ILIM\_SEL} = V_{IN}$		185	240	
		$V_{CTL1} = V_{CTL2} = V_{IN}$, $V_{CTL3} = VIN$, $V_{ILIM\_SEL} = V_{IN}$		195	250	
		$V_{CTL1} = 0\ V$, $V_{CTL2} = V_{CTL3} = V_{IN}$		215	270	

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature. Thermal effects must be taken into account separately.
(2) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted: –40 ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN} ≤ 5.5 V, V_{EN} = V_{IN}, V_{ILIM_SEL} = V_{IN}, V_{CTL1} = V_{CTL2} = V_{CTL3} = V_{IN}. $R_{\overline{FAULT}}$ = $R_{\overline{STATUS}}$ = 10 kΩ, R_{ILIM_HI} = 20 kΩ, R_{ILIM_LO} = 80.6 kΩ. Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UNDERVOLTAGE LOCKOUT						
V_{UVLO}	IN rising UVLO threshold voltage		3.9	4.1	4.3	V
	Hysteresis(3)			100		mV
$\overline{FAULT}$						
	Output low voltage	$I_{\overline{FAULT}}$ = 1 mA			100	mV
	Off-state leakage	$V_{\overline{FAULT}}$ = 5.5 V			1	µA
	Over current $\overline{FAULT}$ rising and falling deglitch		5	8.2	12	ms
$\overline{STATUS}$						
	Output low voltage	$I_{\overline{STATUS}}$ = 1 mA			100	mV
	Off-state leakage	$V_{\overline{STATUS}}$ = 5.5 V			1	µA
THERMAL SHUTDOWN						
	Thermal shutdown threshold		155			°C
	Thermal shutdown threshold in current-limit		135			
	Hysteresis(3)			20		

(3) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

ELECTRICAL CHARACTERISTICS, HIGH-BANDWIDTH SWITCH

Unless otherwise noted: –40 ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN} ≤ 5.5 V, V_{EN} = V_{IN}, V_{ILIM_SEL} = V_{IN}, V_{CTL1} = V_{CTL2} = V_{CTL3} = V_{IN}. $R_{\overline{FAULT}}$ = $R_{\overline{STATUS}}$ = 10 kΩ, R_{ILIM_HI} = 20 kΩ, R_{ILIM_LO} = 80.6 kΩ, Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH-BANDWIDTH ANALOG SWITCH						
	DP/DM switch on resistance	V_{DP/DM_OUT} = 0 V, I_{DP/DM_IN} = 30 mA		2	4	Ω
		V_{DP/DM_OUT} = 2.4 V, I_{DP/DM_IN} = –15 mA		3	6	
	Switch resistance mismatch between DP/DM channels	V_{DP/DM_OUT} = 0 V, I_{DP/DM_IN} = 30 mA		0.05	0.15	Ω
		V_{DP/DM_OUT} = 2.4 V, I_{DP/DM_IN} = –15 mA		0.05	0.15	
	DP/DM switch off-state capacitance(1)	V_{EN} = 0 V, V_{DP/DM_IN} = 0.3 V, V_{ac} = 0.6 V_{pk-pk}, f = 1 MHz		3		pF
	DP/DM switch on-state capacitance(2)	V_{DP/DM_IN} = 0.3 V, V_{ac} = 0.6 V_{pk-pk}, f = 1 MHz		5.4		pF
O_{IRR}	Off-state isolation(3)	V_{EN} = 0 V, f = 250 MHz		33		dB
X_{TALK}	On-state cross channel isolation(3)	f = 250 MHz		52		dB
	Off-state leakage current	V_{EN} = 0 V, V_{DP/DM_IN} = 3.6 V, V_{DP/DM_OUT} = 0 V, measure I_{DP/DM_OUT}		0.1	1.5	µA
BW	Bandwidth (–3 dB)(3)	R_L = 50 Ω		2.6		GHz
t_{pd}	Propagation delay(3)			0.25		ns
t_{SK}	Skew between opposite transitions of the same port (t_{PHL} – t_{PLH})			0.1		ns

(1) The resistance in series with the parasitic capacitance to GND is typically 250 Ω.
(2) The resistance in series with the parasitic capacitance to GND is typically 150 Ω
(3) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

ELECTRICAL CHARACTERISTICS, CHARGING CONTROLLER

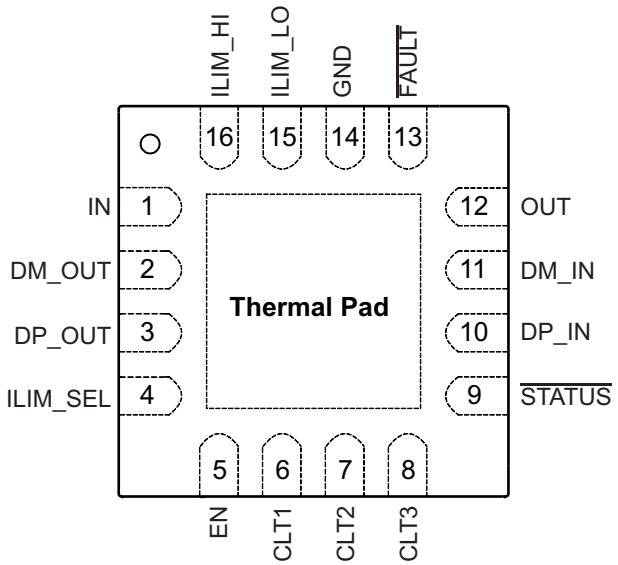
Unless otherwise noted: $-40 \le T_J \le 125°C$, $4.5\ V \le V_{IN} \le 5.5\ V$, $V_{EN} = V_{IN}$, $V_{ILIM\_SEL} = V_{IN}$, $V_{CTL1} = 0\ V$, $V_{CTL2} = V_{CTL3} = V_{IN}$. $R_{\overline{FAULT}} = R_{\overline{STATUS}} = 10\ k\Omega$, $R_{ILIM\_HI} = 20\ k\Omega$, $R_{ILIM\_LO} = 80.6\ k\Omega$, Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SHORTED MODE (BC1.2 DCP)		**VCTL1 = VIN, VCTL2 = VCTL3 = 0 V**				
	DP_IN/DM_IN shorting resistance			125	200	Ω
1.2 V Mode						
	DP_IN/DM_IN output voltage		1.19	1.25	1.31	V
	DP_IN/DM_IN output impedance		60	75	94	kΩ
DIVIDER1 MODE						
	DP_IN Divider1 output voltage		1.9	2	2.1	V
	DM_IN Divider1 output voltage		2.57	2.7	2.84	V
	DP_IN output impedance		8	10.5	12.5	kΩ
	DM_IN output impedance		8	10.5	12.5	kΩ
DIVIDER2 MODE		**IOUT = 1 A**				
	DP_IN Divider2 output voltage		2.57	2.7	2.84	V
	DM_IN Divider2 output voltage		1.9	2	2.1	V
	DP_IN output impedance		8	10.5	12.5	kΩ
	DM_IN output impedance		8	10.5	12.5	kΩ
CHARGING DOWNSTREAM PORT		**VCTL1 = VCTL2 = VCTL3 = VIN**				
V_{DM_SRC}	DM_IN CDP output voltage	$V_{DP\_IN} = 0.6\ V$, $-250\ \mu A < I_{DM\_IN} < 0\ \mu A$	0.5	0.6	0.7	V
V_{DAT_REF}	DP_IN rising lower window threshold for V_{DM_SRC} activation		0.25		0.4	V
	Hysteresis (1)			50		mV
V_{LGC_SRC}	DP_IN rising upper window threshold for V_{DM_SRC} de-activation		0.8		1	V
	Hysteresis (1)			100		mV
I_{DP_SINK}	DP_IN sink current	$V_{DP\_IN} = 0.6\ V$	40	70	100	µA
LOAD DETECT – NONPOWER WAKE		**VCTL1 = VCTL2 = VCTL3 = VIN**				
I_{LD}	IOUT rising load detect current threshold		635	700	765	mA
	Hysteresis (1)			50		mA
t_{LD_SET}	Load detect set time		140	200	275	ms
	Load detect reset time		1.9	3	4.2	s
LOAD DETECT – POWER WAKE		**VCTL1 = VCTL2 = 0 V, VCTL3 = VIN**				
I_{OS_PW}	Power wake short circuit current limit		32	55	78	mA
	I_{OUT} falling power wake reset current detection threshold		23	45	67	mA
	Reset current hysteresis (1)			5		mA
	Power wake reset time		10.7	15	20.6	s

(1) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

DEVICE INFORMATION

TPS2546-Q1 RTE PACKAGE
(Top View)

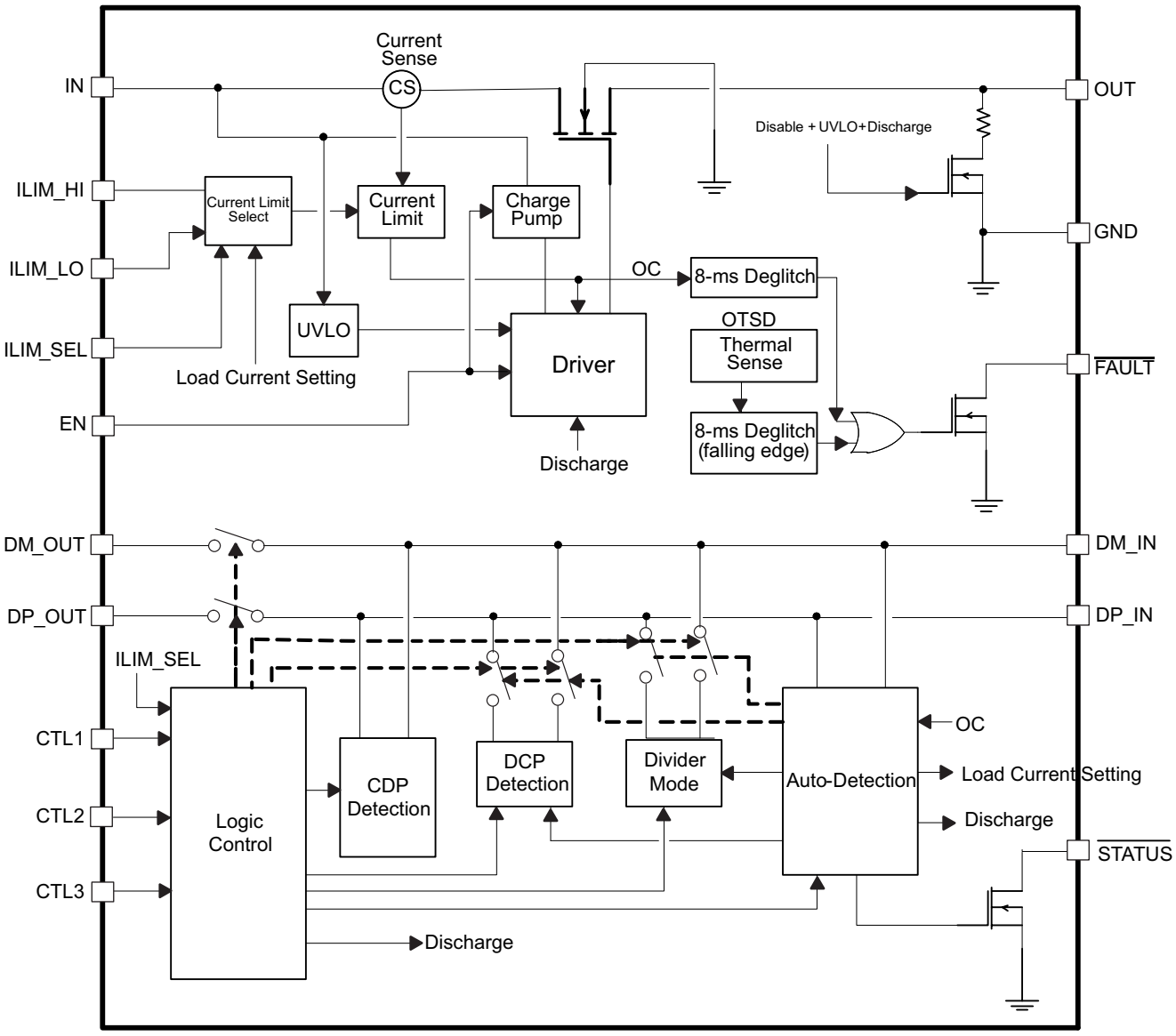


PIN FUNCTIONS

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
CTL1	6	I	The CTL pins are logic-level inputs used to control the charging mode and the signal switches (see Table 3). These pins tie directly to IN or GND without a pullup or pulldown resistor.
CTL2	7	I	
CTL3	8	I	
DM_IN	11	I/O	D– data line to downstream connector
DM_OUT	2	I/O	D– data line to USB host controller
DP_IN	10	I/O	D+ data line to downstream connector
DP_OUT	3	I/O	D+ data line to USB host controller
EN	5	I	EN is the logic-level input for turning on and off the power switch and the signal switches. Logic low turns off the signal and power switches and holds OUT in discharge. EN ties directly to IN or GND without a pullup or pulldown resistor.
$\overline{\text{FAULT}}$	13	O	This pin is the active-low open-drain output and is asserted during overtemperature or current-limit conditions.
GND	14	P	Ground connection
ILIM_HI	16	I	This pin is an external resistor connection used to set the high current-limit threshold.
ILIM_LO	15	I	This pin is an external resistor connection used to set the low current-limit threshold and the load detection current threshold. A resistor to ILIM_LO is optional; see Current-Limit Settings.
ILIM_SEL	4	I	This pin is the logic-level input signal used to control the charging mode, current limit threshold, and load detection (see Table 3). ILIM_SEL ties directly to IN or GND without a pullup or pulldown resistor.
IN	1	P	IN is the input voltage and supply voltage. Connect this pin to a 0.1-µF or greater ceramic capacitor from IN to GND and as close to the device as possible.
OUT	12	P	Power-switch output
PowerPAD™	–	–	The PowerPAD is internally connected to GND and is used to heat-sink the device to the circuit board traces. Connect the PowerPAD to the GND plane.
$\overline{\text{STATUS}}$	9	O	This pin is the active-low open-drain output and is asserted in load detection conditions.

(1) G = Ground, I = Input, O = Output, P = Power

TPS2546-Q1 FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

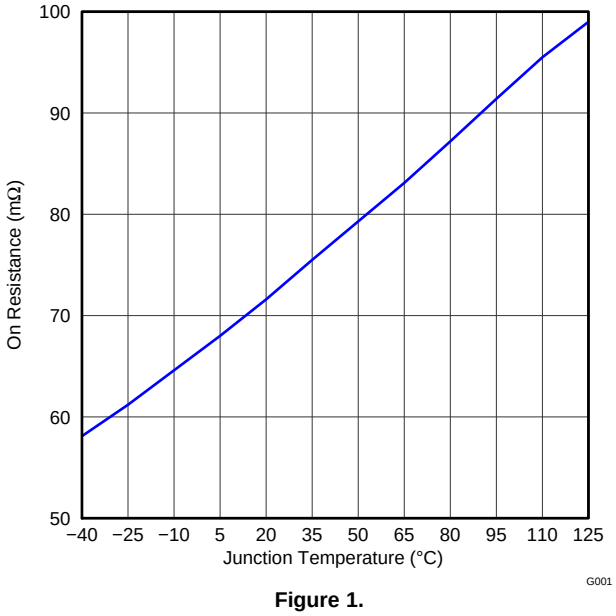


Figure 1.

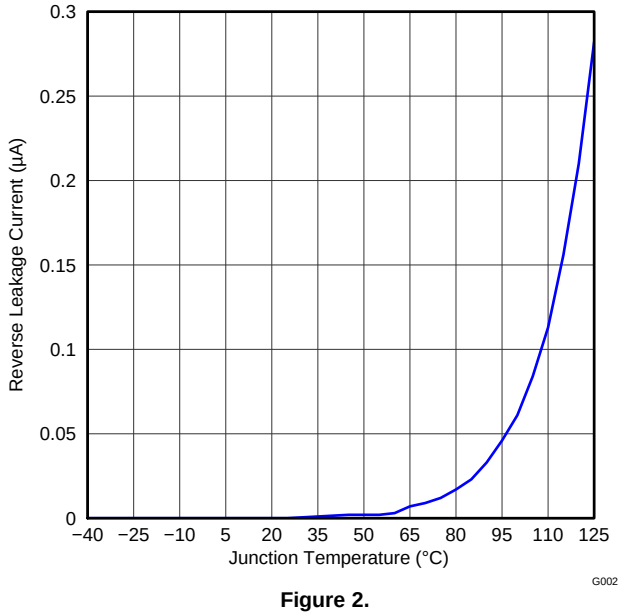


Figure 2.

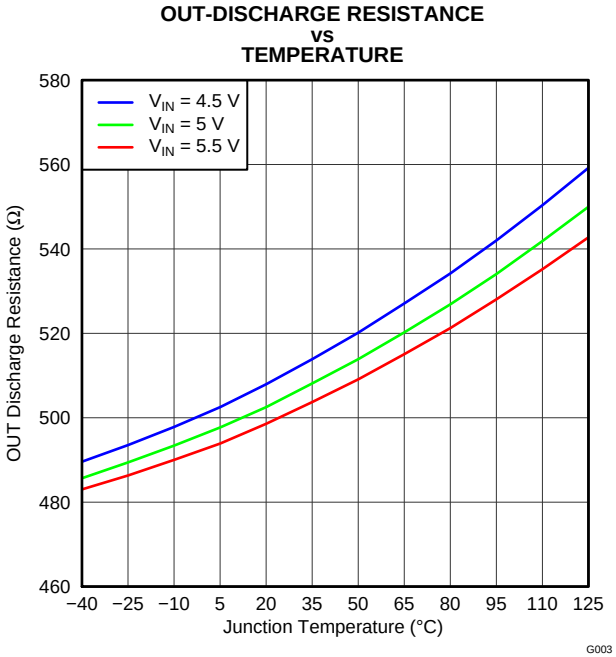


Figure 3.

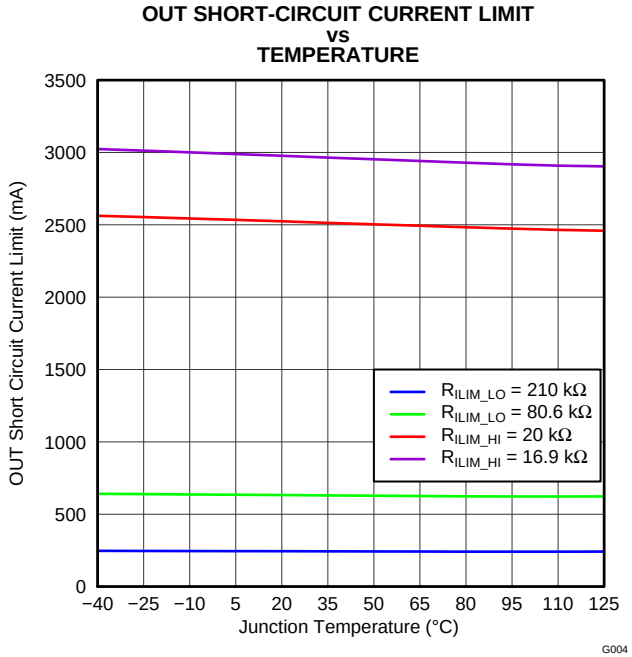


Figure 4.

TYPICAL CHARACTERISTICS (continued)

DISABLED-IN SUPPLY CURRENT vs TEMPERATURE

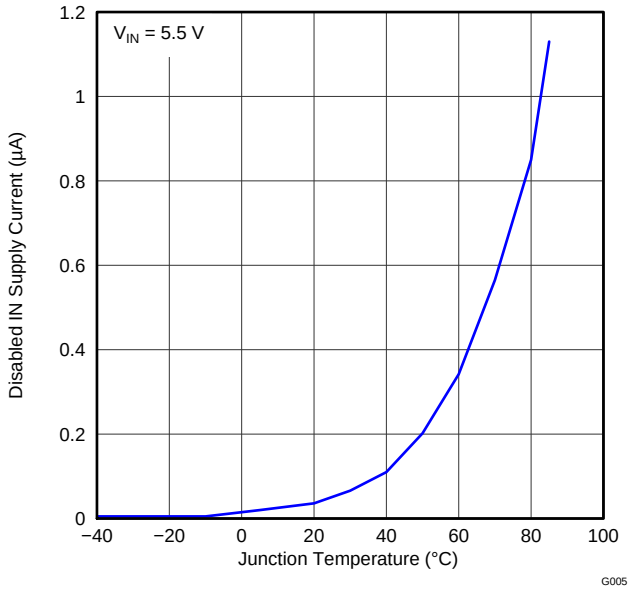


Figure 5.

ENABLED-IN SUPPLY CURRENT — SDP vs TEMPERATURE

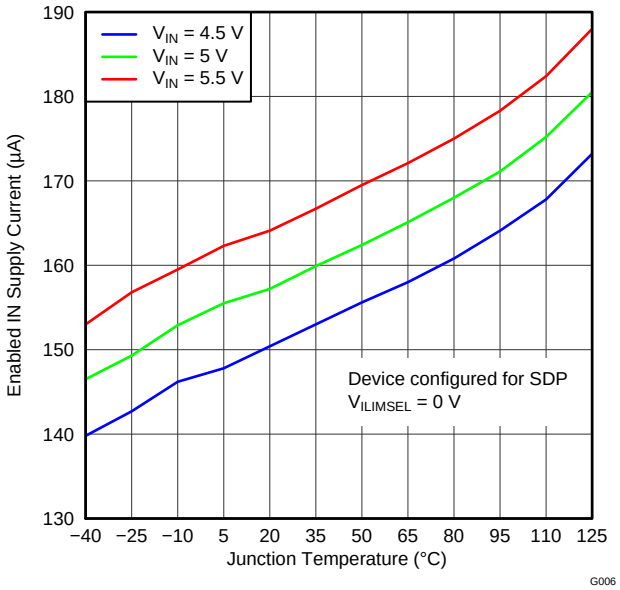


Figure 6.

ENABLED-IN SUPPLY CURRENT — CDP vs TEMPERATURE

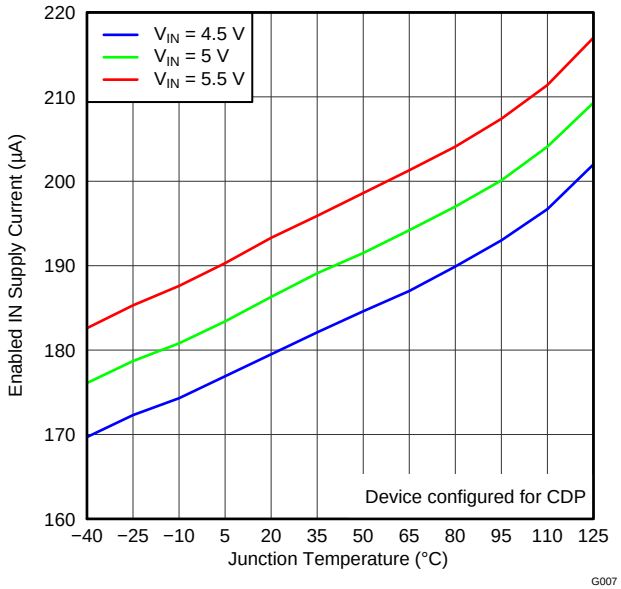


Figure 7.

ENABLED-IN SUPPLY CURRENT — DCP AUTO vs TEMPERATURE

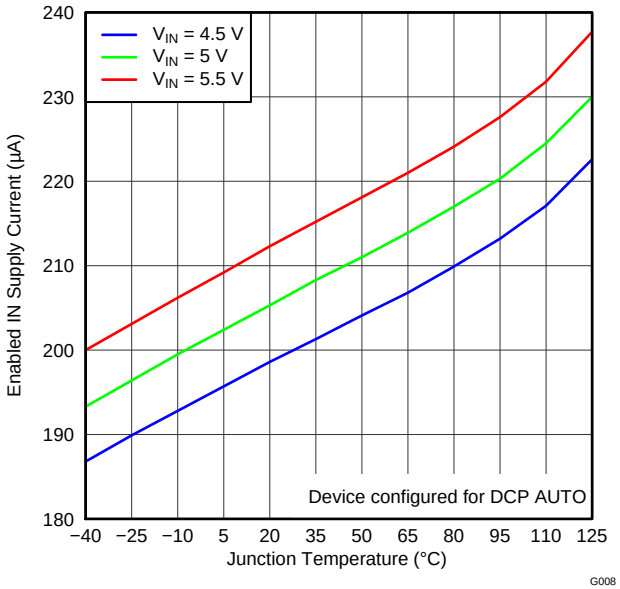


Figure 8.

TYPICAL CHARACTERISTICS (continued)

STATUS AND FAULT OUTPUT LOW VOLTAGE vs SINKING CURRENT

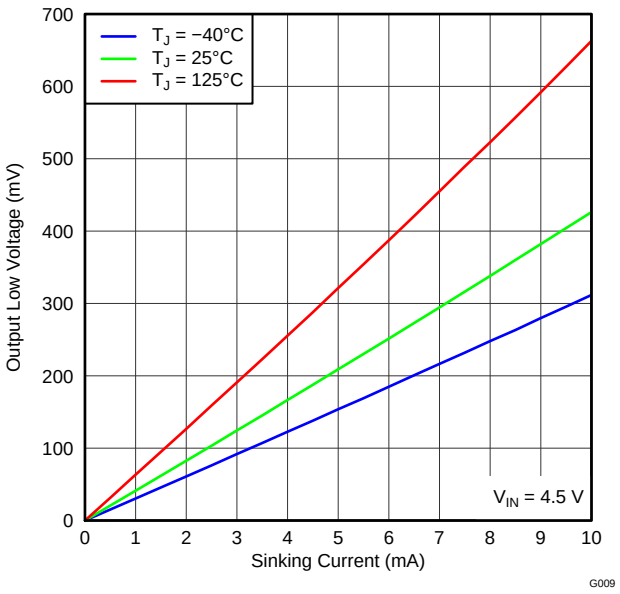


Figure 9.

DATA TRANSMISSION CHARACTERISTICS vs FREQUENCY

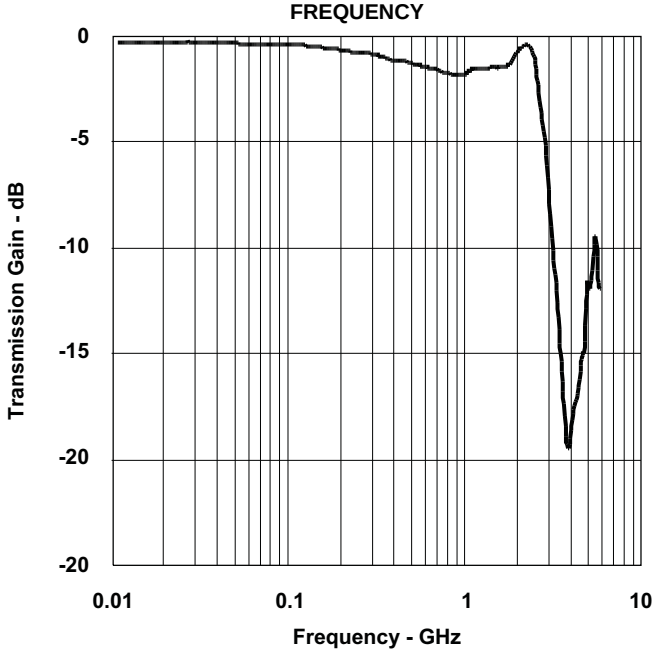


Figure 10.

OFF-STATE DATA-SWITCH ISOLATION vs FREQUENCY

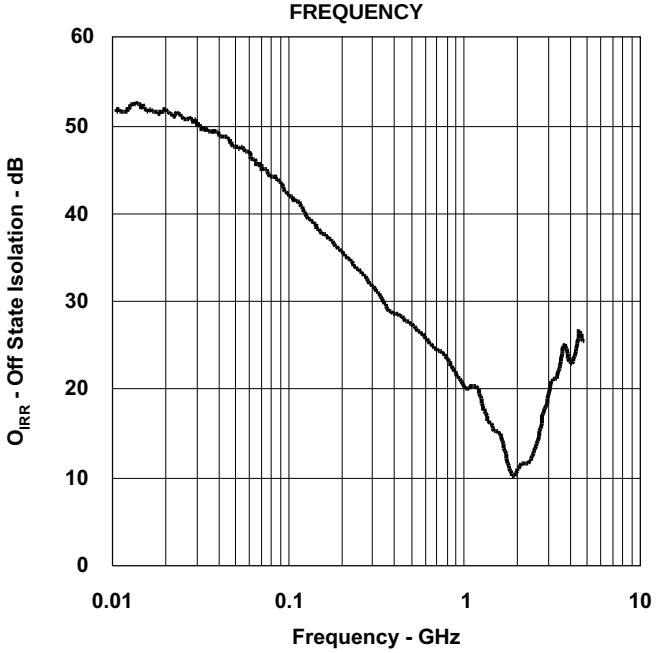


Figure 11.

ON-STATE CROSS-CHANNEL ISOLATION vs FREQUENCY

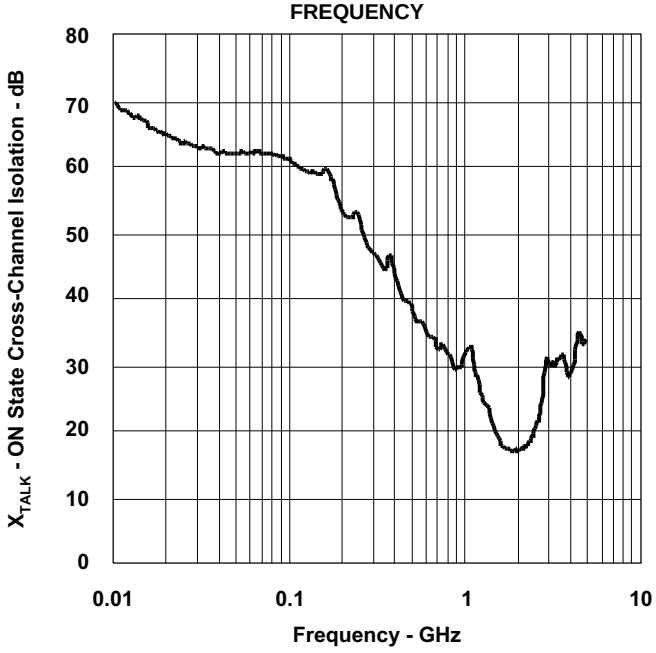


Figure 12.

TYPICAL CHARACTERISTICS (continued)

EYE DIAGRAM USING USB-COMPLIANCE TEST PATTERN (with no switch)

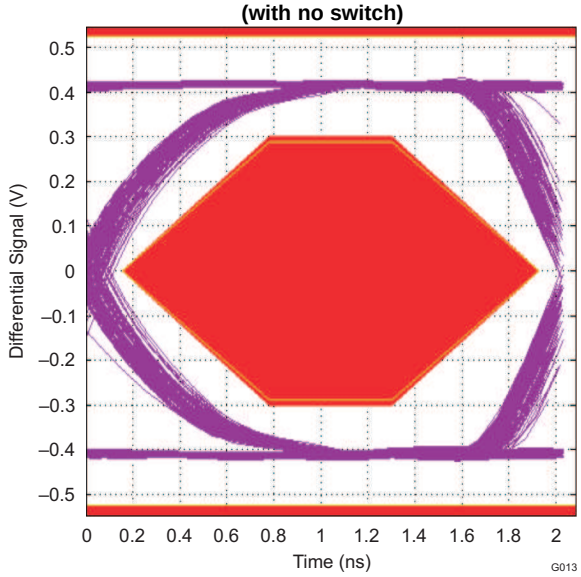


Figure 13.

EYE DIAGRAM USING USB-COMPLIANCE TEST PATTERN (with data switch)

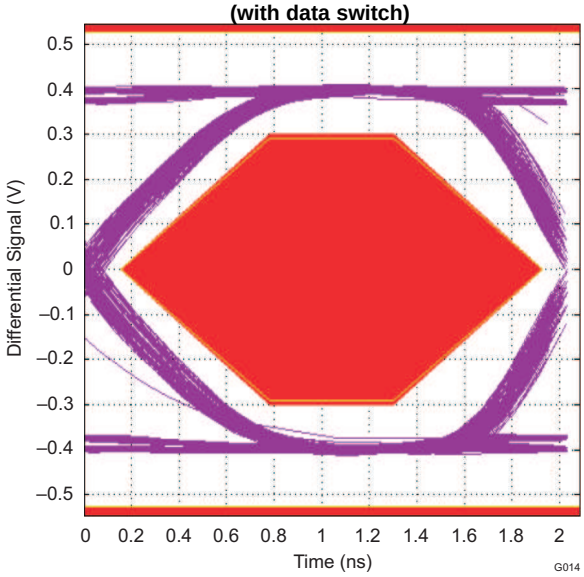


Figure 14.

I_{OUT} RISING LOAD-DETECT THRESHOLD AND OUT SHORT-CIRCUIT CURRENT LIMIT vs TEMPERATURE

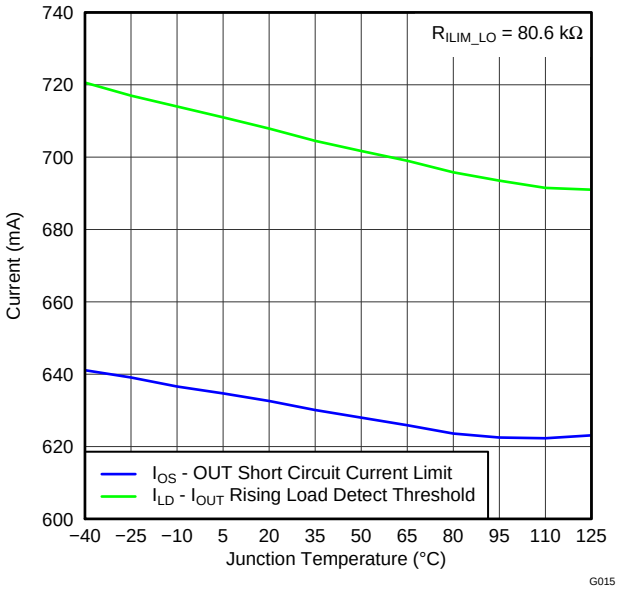


Figure 15.

LOAD DETECT SET-TIME vs TEMPERATURE

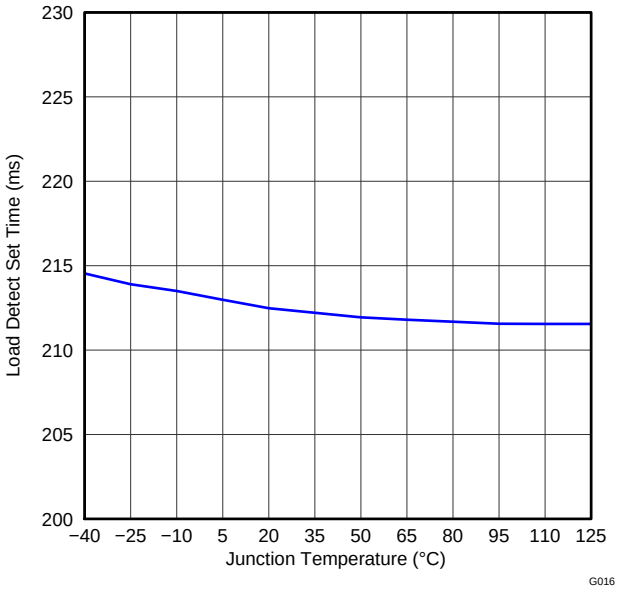


Figure 16.

TYPICAL CHARACTERISTICS (continued)

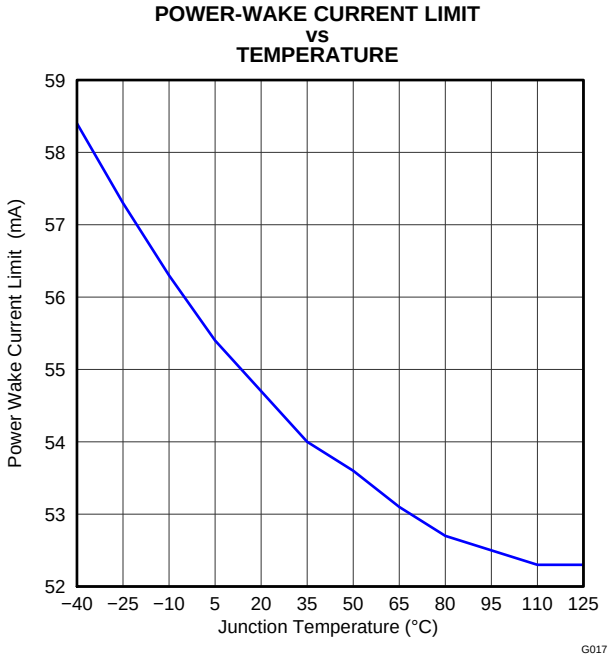


Figure 17.

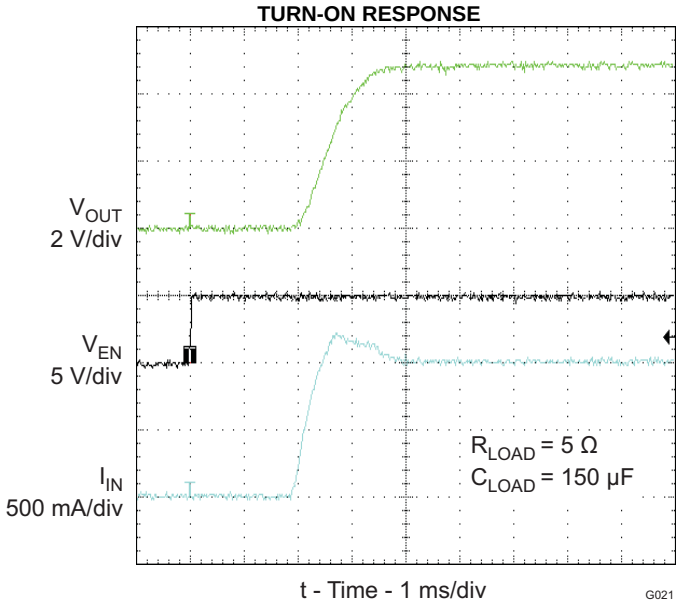


Figure 18.

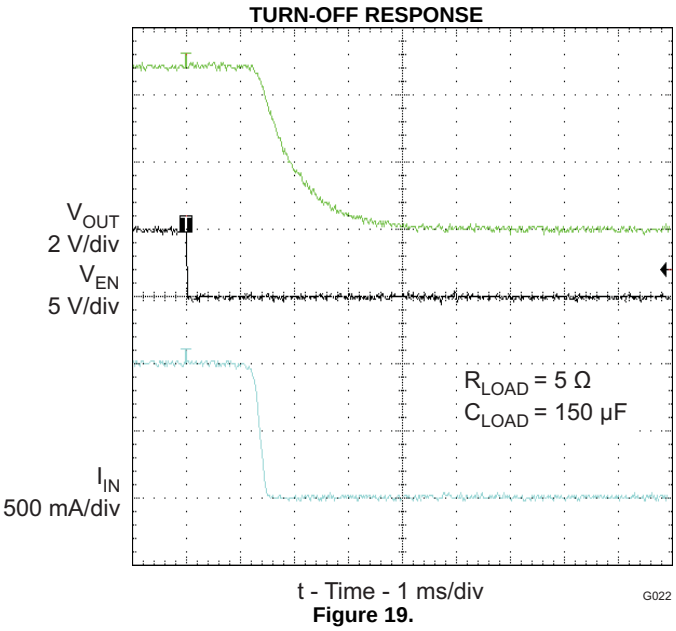


Figure 19.

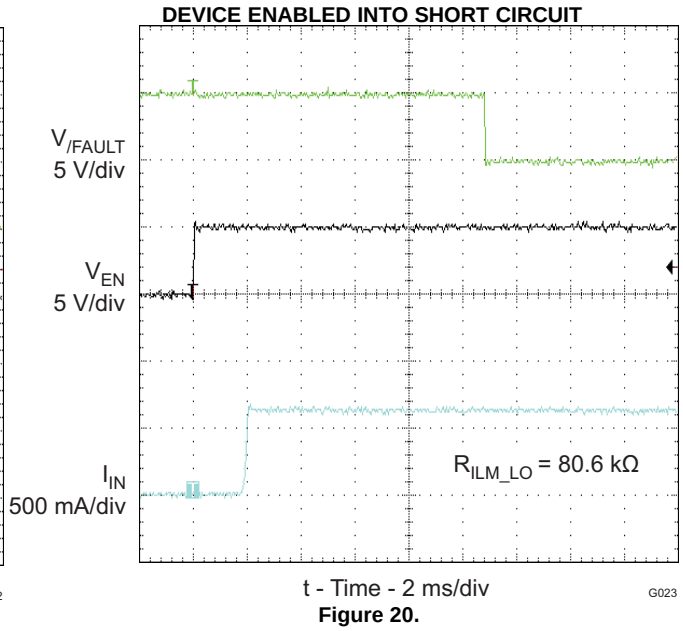


Figure 20.

TYPICAL CHARACTERISTICS (continued)

DEVICE ENABLED INTO SHORT CIRCUIT — THERMAL CYCLING

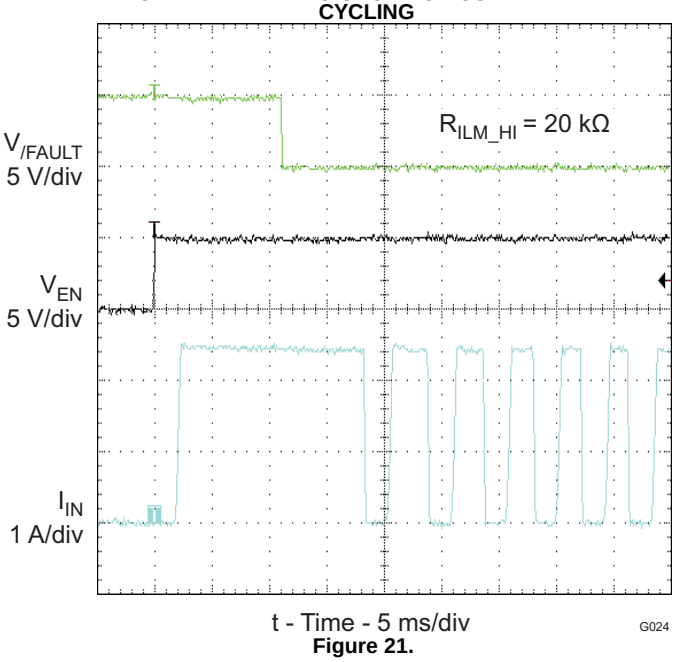


Figure 21.

SHORT CIRCUIT TO FULL LOAD RECOVERY

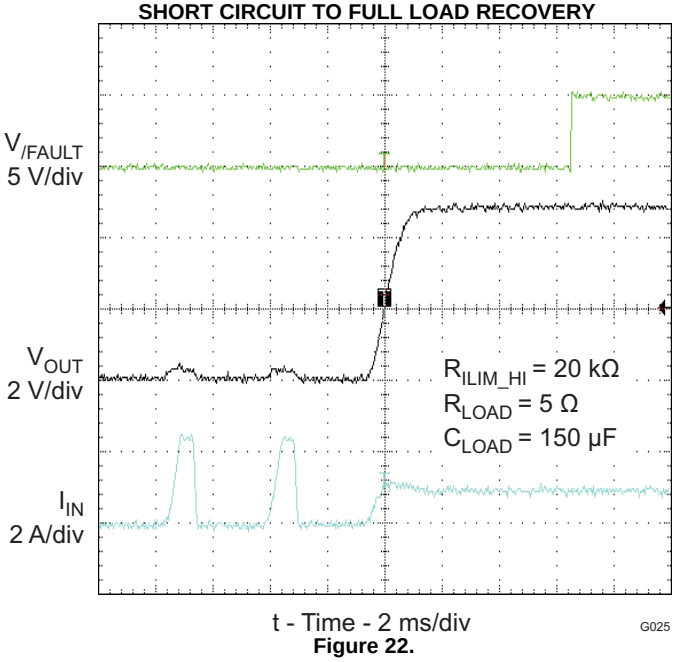


Figure 22.

PARAMETER MEASUREMENT DESCRIPTION

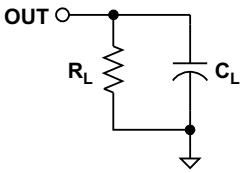


Figure 23. OUT Rise and Fall Test Load

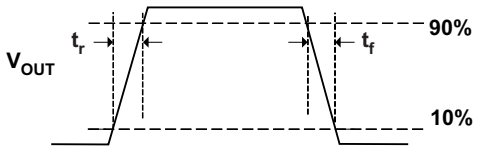


Figure 24. Power-On and Power-Off Timing

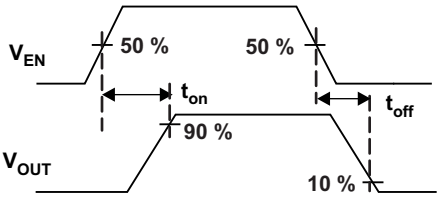


Figure 25. Enable Timing, Active-High Enable

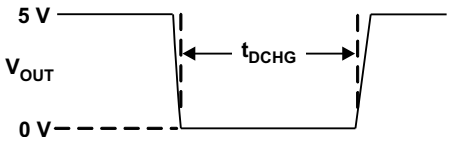


Figure 26. OUT-Discharge During Mode Change

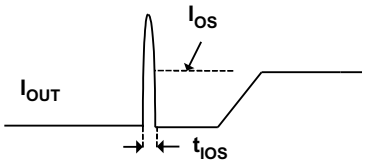


Figure 27. Output Short-Circuit Parameters

DETAILED DESCRIPTION

Overview

The following overview references various industry standards. TI recommends to consult the most up-to-date standards to ensure the most recent and accurate information. Rechargeable portable equipment requires an external power source to charge batteries. USB ports are a convenient location for charging because of an available 5-V power source. Universally accepted standards are required to ensure host and client-side devices operate together in a system to ensure power-management requirements are met. Traditionally, host ports following the USB-2.0 specification must provide at least 500 mA to downstream client-side devices. Because multiple USB devices can be attached to a single USB port through a bus-powered hub, the client-side device sets the power allotment from the host to ensure the total current draw does not exceed 500 mA. In general, each USB device is granted 100 mA and can request more current in 100-mA unit steps up to 500 mA. The host grants or denies additional current based on the available current. A USB-3.0 host port not only provides higher data rate than a USB-2.0 port but also raises the unit load from 100 mA to 150 mA. Providing a minimum current of 900 mA to downstream client-side devices is required.

Additionally, the success of USB has made the micro-USB and mini-USB connectors a popular choice for wall-adapter cables. A micro-USB or mini-USB allows a portable device to charge from both a wall adapter and USB port with only one connector. As USB charging has gained popularity, the 500-mA minimum defined by USB 2.0, or 900 mA for USB 3.0, has become insufficient for many handset and personal media players, which require a higher charging rate. Wall adapters provide much more current than 500 or 900 mA. Several new standards have been introduced defining protocol handshaking methods that allow host and client devices to acknowledge and draw additional current beyond the 500-mA and 900-mA minimum defined by USB 2.0 and USB 3.0, respectively, while still using a single micro-USB or mini-USB input connector.

The TPS2546-Q1 device supports four of the most-common USB-charging schemes found in popular hand-held media and cellular devices.

- USB Battery Charging Specification BC1.2
- Chinese Telecommunications Industry Standard YD/T 1591-2009
- Divider mode
- 1.2 V Mode

The YD/T 1591-2009 standard is a subset of the BC1.2 specification and is supported by a majority of devices that implement USB changing. Divider and 1.2-V charging schemes are supported in devices from specific and popular device makers.

The BC1.2 specification includes three different port types:

- Standard downstream port (SDP)
- Charging downstream port (CDP)
- Dedicated charging port (DCP)

BC1.2 defines a charging port as a downstream-facing USB port that provides power for charging portable equipment. Under this definition, CDP and DCP are defined as charging ports.

Table 1 lists the differences between these port types.

Table 1. Operating Modes

PORT TYPE	SUPPORT USB 2.0 COMMUNICATION	MAXIMUM ALLOWABLE CURRENT DRAW BY PORTABLE DEVICE (A)
SDP (USB 2.0)	Yes	0.5
SDP (USB 3.0)	Yes	0.9
CDP	Yes	1.5
DCP	No	1.5

Standard Downstream Port (SDP) — USB 2.0 and USB 3.0

An SDP is a traditional USB port that follows USB 2.0 and USB 3.0 protocol. An SDP supplies a minimum of 500 and 900-mA per port. USB 2.0 and USB 3.0 communications is supported, and the host controller must be active to allow charging. The TPS2546-Q1 device supports SDP mode in system-power state S0 when the system is completely powered ON and fully operational. For more details on the control pin (CTL1–CTL3) settings used to program this state, see Table 3.

Charging Downstream Port (CDP)

A CDP is a USB port that follows USB BC1.2 and supplies a minimum of 1.5 A per port. A CDP provides power and meets the USB-2.0 requirements for device enumeration. USB-2.0 communication is supported, and the host controller must be active to allow charging. The difference between CDP and SDP is the host-charge handshaking logic that identifies this port as a CDP. A CDP is identifiable by a compliant BC1.2 client device and allows for additional current draw by the client device.

The CDP hand-shaking process occurs in two steps. During step one the portable equipment outputs a nominal 0.6-V output on the D+ line and reads the voltage input on the D– line. The portable device detects the connection to an SDP if the voltage is less than the nominal data detect voltage of 0.3 V. The portable device detects the connection to a CDP if the D– voltage is greater than the nominal data detect voltage of 0.3 V and optionally less than 0.8 V.

The second step is necessary for portable equipment to determine if the equipment is connected to a CDP or a DCP. The portable device outputs a nominal 0.6-V output on the D– line and reads the voltage input on the D+ line. The portable device concludes the equipment is connected to a CDP if the data line being read remains less than the nominal data detect voltage of 0.3 V. The portable device concludes it is connected to a DCP if the data line being read is greater than the nominal data detect voltage of 0.3 V.

The TPS2546-Q1 device supports CDP mode in system-power state S0 when the system is completely powered ON and fully operational. For more details on control pin (CTL1-CTL3) settings used to program this state see Table 3.

Dedicated Charging Port (DCP)

A DCP only provides power and does not support data connection to an upstream port. As shown in the following sections, a DCP is identified by the electrical characteristics of the data lines. The TPS2546-Q1 device emulates DCP in two charging states: DCP Forced and DCP Auto (see Figure 32). In DCP-Forced state the device supports one of the two DCP charging schemes, either Divider1 or Shorted. In the DCP-Auto state, the device charge-detection state machine is activated to selectively implement charging schemes involved with the Shorted, Divider1, Divider2, and 1.2 V Mode. The Shorted DCP mode complies with BC1.2 and Chinese Telecommunications Industry Standard YD/T 1591-2009, while the Divider1, Divider2, and 1.2 V Mode are employed to charge devices that do not comply with the BC1.2 DCP standard.

DCP BC1.2 and YD/T 1591-2009

Both standards define that the D+ and D– data lines must be shorted together with a maximum series impedance of 200 Ω, as shown in Figure 28.

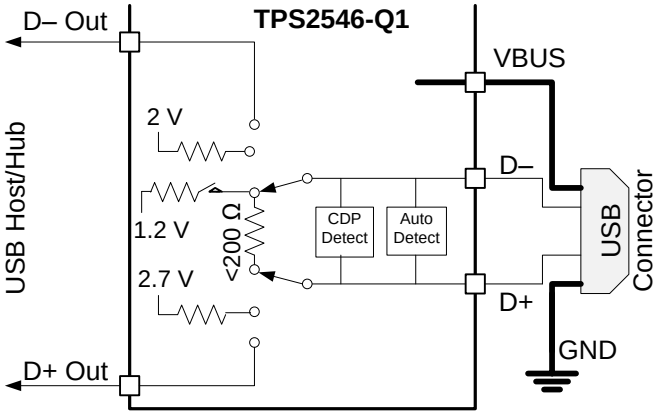


Figure 28. DCP Supporting BC1.2 and YD/T 1591-2009

DCP Divider-Charging Scheme

The device supports two divider charging schemes, Divider1 and Divider2, as shown in Figure 29 and Figure 30, respectively. In the Divider1 charging scheme the device applies 2 V and 2.7 V to D+ and D– data lines, respectively, which is reversed in Divider2 mode.

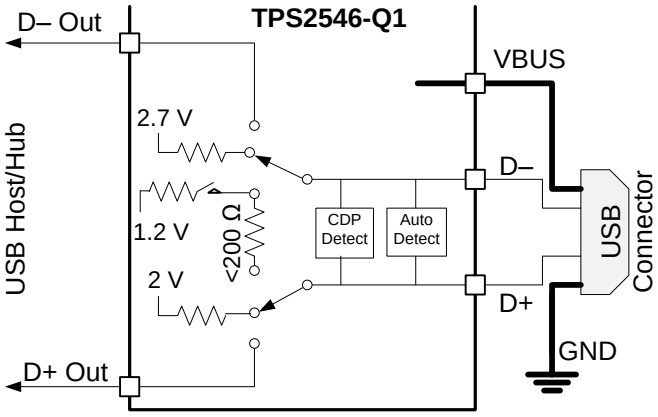


Figure 29. DCP Divider1 Charging Scheme

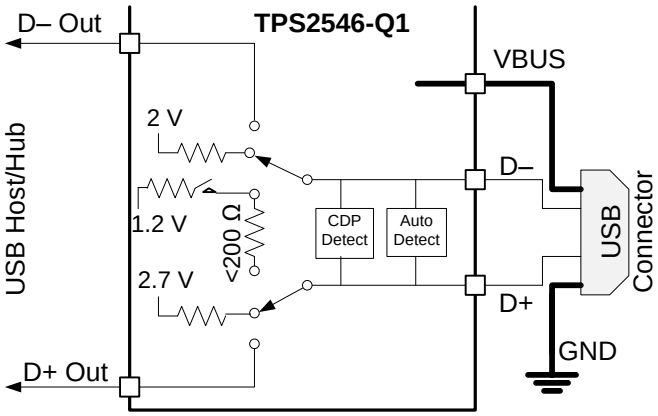


Figure 30. DCP Divider2 Charging Scheme

DCP 1.2 V Charging Scheme

The DCP 1.2 V charging scheme is used by some hand-held devices to enable fast charging at 2 A. The TPS2546-Q1 device supports this scheme in DCP-Auto state before the device enters BC1.2 Shorted state. To simulate this charging scheme, the D+ and D– lines are shorted and pulled up to 1.2 V for a fixed duration. Then the device moves to DCP Shorted mode as defined in the BC1.2 specification and as shown in Figure 31

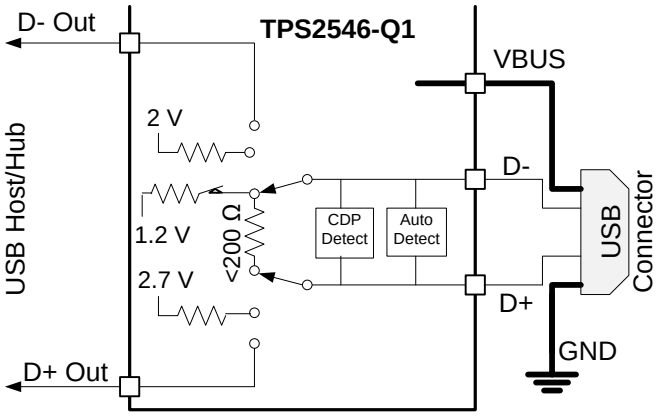


Figure 31. DCP 1.2-V Charging Scheme

DCP Auto Mode

As previously discussed, the TPS2546-Q1 device integrates an auto-detect state machine that supports all the DCP charging schemes. The auto-detect state machine starts in the Divider1 scheme, however, if a BC1.2 or YD/T 1591-2009 compliant device is attached, the TPS2546-Q1 responds by discharging OUT, turning the power switch back on and operating in 1.2 V Mode briefly before entering BC1.2 DCP mode. Then the auto-detect state machine stays in that mode until the device releases the data line, in which case the auto-detect state machine goes back to the Divider1 scheme. When a Divider1-compliant device is attached, the TPS2546-Q1 device stays in the Divider1 state.

Also, the TPS2546-Q1 device automatically switches between the Divider1 and Divider2 schemes based on the charging current drawn by the connected device. Initially, the device sets the data lines to the Divider1 scheme. If a charging current of greater than 750 mA is measured by the TPS2546-Q1 device, the auto-detect state machine switches to the Divider2 scheme. After switching to the Divider2 scheme, the auto-detect state machine tests the peripheral device to ensure that the device continues to charge at a high current. If the peripheral device continues to charge, then the auto-detect state machine stays in Divider2 scheme, otherwise the auto-detect state machine reverts to the Divider1 scheme.

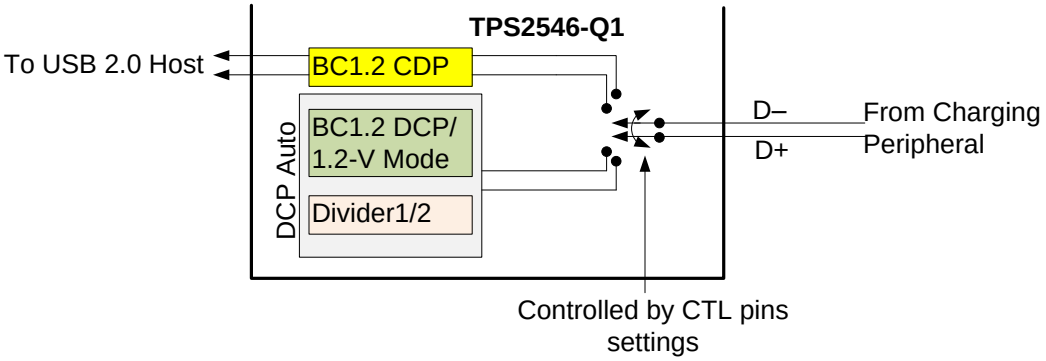


Figure 32. DCP Auto Mode

DCP Forced Shorted and DCP Forced Divider1

In this mode the device is permanently set to one of the DCP schemes (BC1.2, YD/T 1591-2009, or Divider1) as commanded by the control pin setting per Table 3.

High-Bandwidth Data Line Switch

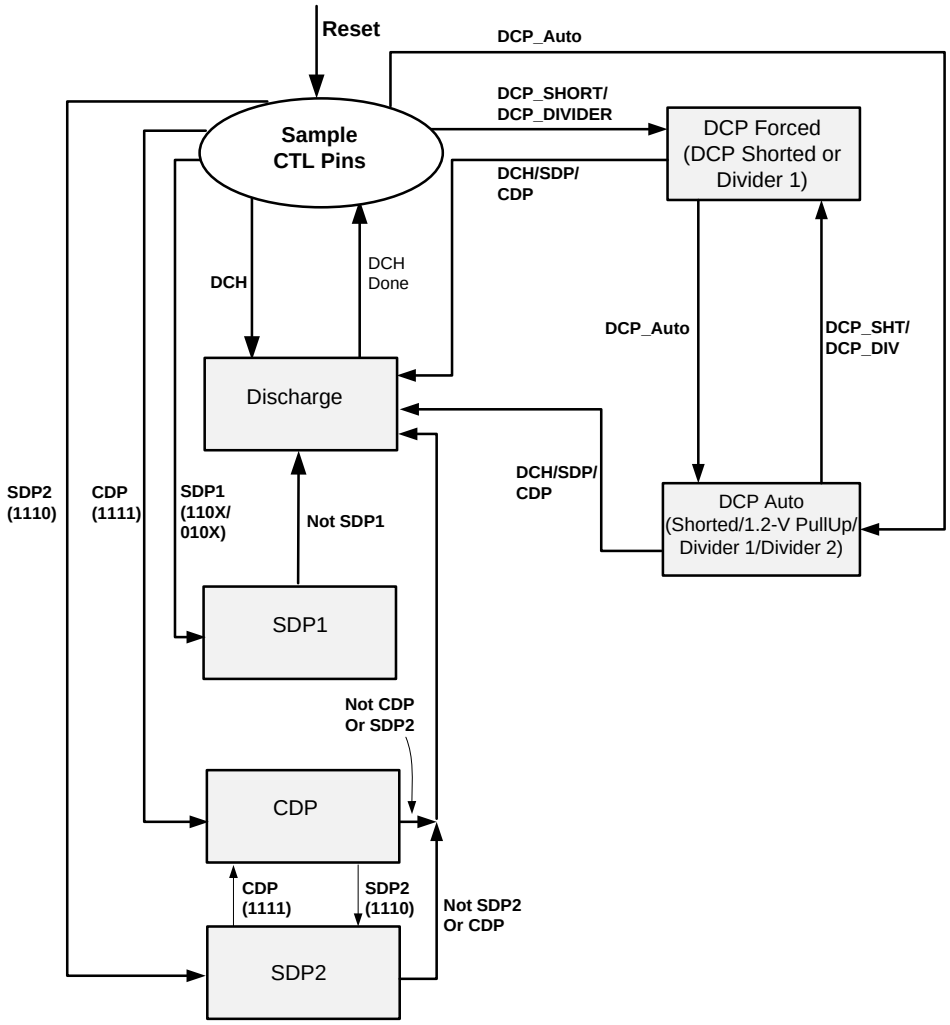
The TPS2546-Q1 device passes the D+ and D– data lines through the device to enable monitoring and handshaking while supporting the charging operation. A wide bandwidth signal switch allows data to pass through the device without corrupting signal integrity. The data line switches are turned on in any of the CDP or SDP operating modes. The EN input must be at logic high for the data line switches to be enabled.

NOTE

1. While in CDP mode, the data switches are ON, even during CDP handshaking.
2. The data line switches are OFF if EN or all CTL pins are held low, or if in DCP mode. The switches are not automatically turned off if the power switch (IN to OUT) is in current-limit.
3. The data switches are only for USB-2.0 differential pair. In the case of a USB-3.0 host, the super-speed differential pairs must be routed directly to the USB connector without passing through the TPS2546-Q1 device.
4. Data switches are OFF during OUT (VBUS) discharge.

Device Operation

Figure 33 shows the simplified device state diagram. Power-on-reset (POR) holds the device in the initial state while the output is held in discharge mode. Any POR event causes the device to renter the initial state. After POR clears, the device goes to the next state depending on the CTL lines as shown in Figure 33.



NOTE: All shaded boxes are device charging modes.
Table 2 lists the CTL settings corresponding to flow line conditions.

Figure 33. TPS2546-Q1 Charging States

Table 2. Device Control Pins

Flow Line Condition	CTL1	CTL2	CTL3	ILIM_SEL
DCH (Discharge)	0	0	0	X
CDP	1	1	1	1
SDP2 (No discharge to or from CDP)	1	1	1	0
SDP1 (Discharge to and from any charging state including CDP)	1	1	0	X
	0	1	0	X
DCP_SHORTED	1	0	0	X
DCP / DIVIDER	1	0	1	X
DCP_Auto	0	1	1	X
	0	0	1	X

Output Discharge

To allow a charging port to renegotiate current with a portable device, the TPS2546-Q1 device uses the OUT discharge function. The device proceeds by turning off the power switch while discharging OUT. The device then turns on the power switch again to reassert the OUT voltage. This discharge function is automatically applied, as shown in Figure 33. There are two discharge times, t_{DCHG_L} and t_{DCHG_S}. t_{DCHG_L} is from SDP1/SDP2/CDP to DCP_Auto, and t_{DCHG_S} is from DCP_Auto to SDP1/SDP2/CDP.

Wake-On-USB Feature (Mouse and Keyboard Wake Feature)

USB-2.0 Background Information

The data lines of the TPS2546-Q1 device interface with USB-2.0 devices. USB 2.0 defines three types of devices according to data rate. The following lists outline the three devices and the characteristics relevant to TPS2546-Q1 wake-on-USB operation.

Low-speed USB devices:

- 1.5 Mb/s
- Examples include wired mice and keyboards
- Does not include devices that require battery charging
- All signaling performed at 2-V and 0.8-V high and low logic levels
- D– goes high to signal connect and when placed into suspend
- D– goes high when not transmitting data packets

Full-speed USB devices:

- 12 Mb/s
- Examples include wireless mice and keyboards, legacy phones, and music players
- Includes some legacy devices that require battery charging
- All signaling performed at 2-V and 0.8-V high and low logic levels
- D+ goes high to signal connect and when placed into suspend
- D+ goes high when not transmitting data packets

High-speed USB devices:

- 480 Mb/s
- Examples include tablets, phones, and music players
- Includes many devices that require battery charging
- Connect and suspend signaling performed at 2-V and 0.8-V high and low logic levels
- Data packet signaling performed at logic levels below 0.8 V
- D+ goes high to signal connect and when placed into suspend (same as a full-speed device)
- D+ and D– go low when not transmitting data packets

Wake-On-USB

Wake-on-USB is the ability of a wake-configured USB device to wake a computer system from the S3 sleep-state of the device back to the S0 working state. Wake-on-USB requires the data lines to connect to the system USB host before the system is placed into S3 sleep state. Wake-on-USB also requires that the lines remain continuously connected until they are used to wake the system.

The TPS2546-Q1 device supports low-speed and high-speed human-interface-device (HID, such as mouse or keyboard) wake functions. There are two scenarios under which the TPS2546-Q1 device supports wake-on-mouse. The following list shows the specific CTL pin changes that the TPS2546-Q1 device overrides. The information is presented as CTL1, CTL2, and CTL3. The ILIM_SEL pin plays no role.

1. 111 (CDP/SDP2) to 011 (DCP-Auto)
2. 010 (SDP1) to 011 (DCP-Auto)

The 110 (SDP1)-to-011 (DCP-Auto) transition is not supported because the transition involves changes to two CTL pins. Depending on which CTL pin changes first, the device detects either a temporary 111 or 010 command. The 010 command is safe but the 111 command causes an OUT discharge as the TPS2546-Q1 device instead proceeds to the 111 state.

USB Slow-Speed and Full-Speed Device Recognition

The TPS2546-Q1 device can detect low-speed (LS) or full-speed (FS) device attachment when it is in SDP or CDP mode. According to USB specification when no device is attached, the D+ and D– lines are near ground level. When a low-speed compliant device is attached to the charging port of the TPS2546-Q1 device, the D– line is pulled high in the idle state (mouse or keyboard is not activated). However, when an FS device is attached the opposite occurs (D+ is pulled high and D– remains at ground level).

The TPS2546-Q1 device monitors both D+ and D– lines while the CTL-pin settings are in CDP or SDP mode to detect LS-HID or FS-HID device attachment. To support HID sleep wake, the TPS2546-Q1 device must first determine that it is attached to an LS or FS device when the system is in S0 power state. The TPS2546-Q1 device detects an LS or FS device as previously described. While the support of an LS-HID wake is straight forward, supporting FS-HID requires making a distinction between an FS and a high-speed (HS) device. This distinction is important because a HS device always begins as an FS device (by a 1.5-kΩ pullup resistor on D+). The negotiation for high speed then makes the distinction whereby the 1.5-kΩ pullup resistor is removed.

The TPS2546-Q1 device handles the distinction between an FS and HS device at connect by memorizing if the D+ line goes low after connect. A HS device after connect always undergoes negotiation for HS which requires the 1.5-kΩ resistor pullup on D+ to be removed. To memorize an FS device, the TPS2546-Q1 requires the peripheral device to remain connected for at least 60 seconds while the system is in S0 mode before placing the peripheral device in sleep or S3 mode.

This requirement does not apply for an LS device.

NOTE

If the system enters sleep mode earlier than the 60-second window, an FS device may not be recognized and therefore could fail to wake the system from S3.

No CTL-Pin Timing Requirement After Wake Event and Transition from S3 to S0

Unlike the TPS2543 device, there is no CTL-pin timing requirement for the TPS2546-Q1 device when the wake-configured USB device wakes the system from S3 back to S0. The TPS2543 device requires the CTL pins to transition from the DCP-Auto setting back to the SDP or CDP setting within 64 ms of the attached USB device signaling a wake event (such as a mouse click or keyboard key press). This timing condition is not a feature of the TPS2546-Q1 device.

Device Truth Table (TT)

The device truth table (TT) lists all valid bias combinations for the three control pins (CTL1 through CTL3), the ILIM_SEL pin, and the corresponding charging mode of each pin. The TT purposely does not match charging modes of the TPS2546-Q1 device with global power states (S0-S5) as the device is neutral to system power states. The TPS2546-Q1 device monitors the CTL inputs and transitions to whichever charging state it is commanded to go to (except when a LS-HID or FS-HID device is detected). For example, if sleep charging is desired when the system is in a standby or hibernate state, then the user must set the CTL pins of the TPS2546-Q1 device to correspond to the DCP_Auto charging mode per Table 3. However, when the system reenters operation mode, then the user must set control pins to correspond to SDP or CDP mode and so on.

Table 3. Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	MODE	CURRENT LIMIT SETTING	STATUS OUTPUT (Active low)	COMMENT
0	0	0	0	Discharge	N/A	OFF	OUT held low
0	0	0	1	Discharge	N/A	OFF	
0	0	1	0	DCP_Auto	ILIM_HI	OFF	Data lines disconnected
0	0	1	1	DCP_Auto	I_{OS_PW} and ILIM_HI(1)	DCP load present(2)	Data lines disconnected and Load Detect function active
0	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
0	1	0	1	SDP1	ILIM_HI	OFF	
0	1	1	0	DCP_Auto	ILIM_HI	OFF	Data lines disconnected
0	1	1	1	DCP_Auto	ILIM_HI	DCP load present(3)	Data lines disconnected and Load Detect function active
1	0	0	0	DCP_Shorted	ILIM_LO	OFF	Device forced to stay in DCP BC1.2 charging mode
1	0	0	1	DCP_Shorted	ILIM_HI	OFF	
1	0	1	0	DCP / Divider1	ILIM_LO	OFF	Device forced to stay in DCP Divider1 charging mode
1	0	1	1	DCP / Divider1	ILIM_HI	OFF	
1	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
1	1	0	1	SDP1	ILIM_HI	OFF	
1	1	1	0	SDP2(4)	ILIM_LO	OFF	
1	1	1	1	CDP(4)	ILIM_HI	CDP load present(5)	Data lines connected and Load detect active

(1) The TPS2546-Q1 current-limit (I_{OS}) automatically switches between I_{OS_PW} and the value set by ILIM_HI according to the *Load Detection – Power Wake* functionality.
(2) The DCP load present is governed by the *Load Detection – Power Wake* limits.
(3) The DCP load present is governed by the *Load Detection – Non-Power Wake* limits.
(4) OUT does not discharge when changing between 1111 and 1110.
(5) The CDP load present is governed by the *Load Detection – Non-Power Wake* limits and BC1.2 primary detection.

Use Table 4 as an aid to program the TPS2546-Q1 device according to the system states. Programming of the TPS2546-Q1 device is not restricted to the following settings.

Table 4. Control-Pin Settings Matched to System-Power States

SYSTEM GLOBAL POWER STATE	TPS2546-Q1 CHARGING MODE	CTL1	CTL2	CTL3	ILIM_SEL	CURRENT-LIMIT SETTING
S0	SDP1	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP2, no discharge to and from CDP	1	1	1	0	ILIM_LO
S0	CDP, load detection with ILIM_LO + 60-mA thresholds or if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S4 or S5	Auto mode, load detection with power-wake thresholds	0	0	1	1	ILIM_HI
S3, S4, or S5	Auto mode, no load detection	0	0	1	0	ILIM_HI
S3	Auto mode, keyboard and mouse wake up, load detection with ILIM_LO + 60-mA thresholds	0	1	1	1	ILIM_HI
S3	Auto mode, keyboard and mouse wake up, no load detection	0	1	1	0	ILIM_HI
S3	SDP1, keyboard and mouse wake up	0	1	0	1 or 0	ILIM_HI / ILIM_LO

Load Detect

The TPS2546-Q1 device offers system designers a unique power-management strategy not available from similar industry devices. The device suports two power-management schemes through the STATUS pin:

1. Power Wake (PW)
2. Port-Power Management (PPM)

Either feature is implemented in a system depending on the power savings goals for the system. In general, the PW feature is used mainly in mobile systems, like a notebook, where saving battery power when the system is in deep sleep (S4 or S5) state is imperative. The PPM feature is implemented when multiple charging ports are supported in the same system and the system power-rating cannot support high-current charging on multiple ports simultaneously.

Power Wake

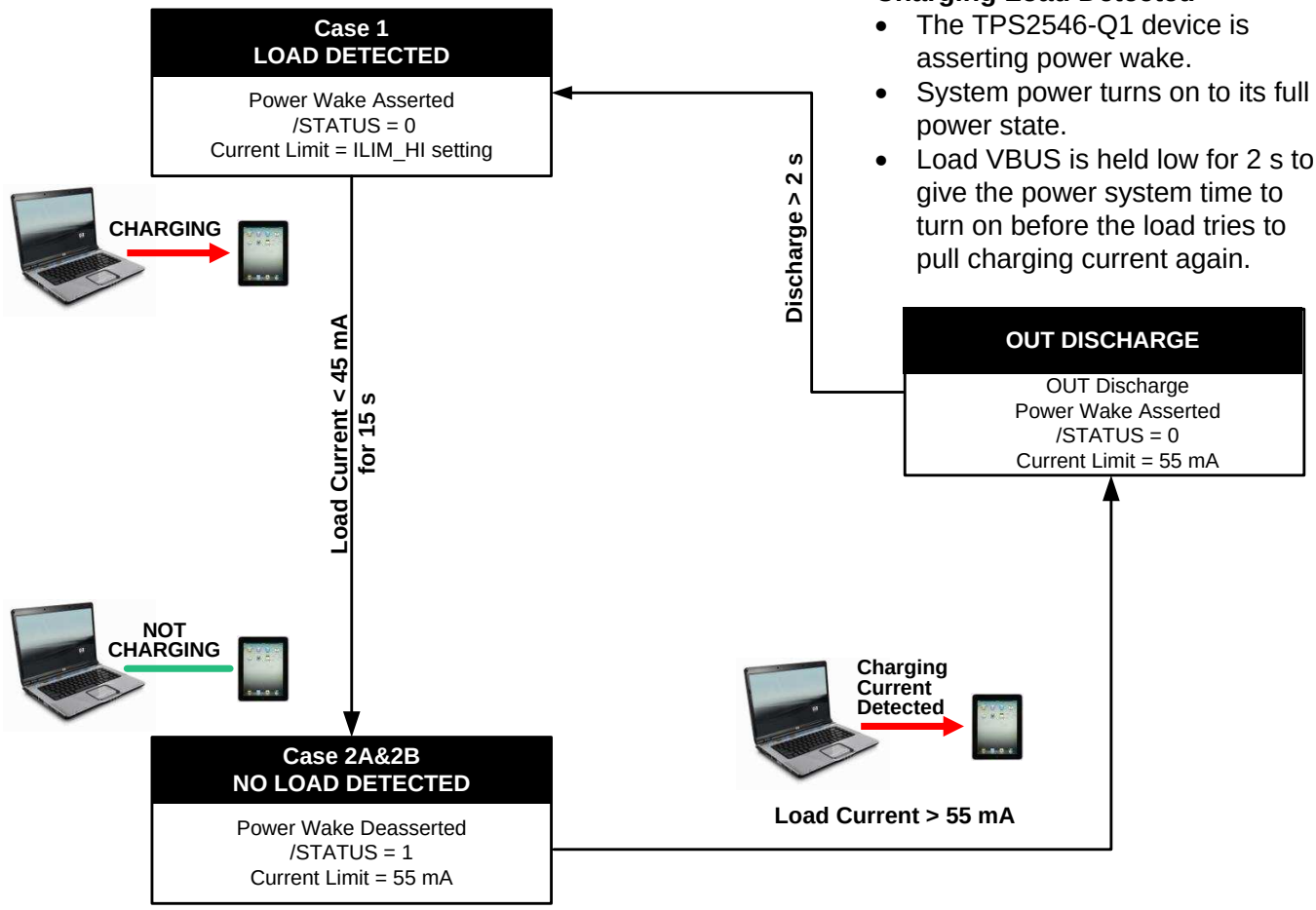
The goal of the PW feature is to save the system power when the system is in S4 or S5 state. In S4 or S5 state, the system is in deep sleep and typically runs off of the battery. In this state, every milliwatt saved translates to battery-life extension. In this state, the TPS2546-Q1 device monitors the charging current at the OUT pin. This state also provides a mechanism through the STATUS pin to switch out the high-power DC-DC controller and switch in a low-power LDO when the charging current requirement is less than 45 mA (typical) (for example: when no peripheral device is connected at the charging port or when a device has attained a full battery charge and draws less than 45 mA). See Figure 34 for the power-wake flow chart and description.

Load being Charged

- The TPS2546-Q1 device is asserting power wake.
- System power is at its full capability.
- Load can charge at high current.
- The TPS2546-Q1 device monitors port to detect when charging load is done charging or removed.

Charging Load Detected

- The TPS2546-Q1 device is asserting power wake.
- System power turns on to its full power state.
- Load VBUS is held low for 2 s to give the power system time to turn on before the load tries to pull charging current again.



Charging Load Not Detected.

- The TPS2546-Q1 device is not asserting power wake. System power is in a low power state to save energy.
- The TPS2546-Q1 device monitors port to detect when charging load is attached and tries to charge.

Figure 34. Power-Wake Flow chart

Implementing Power Wake in Notebook System

See Figure 35, Figure 36, and Figure 37 for the implementation of power wake in notebook platforms with the TPS2546-Q1 device. The power-wake function is used to select between a high-power DC-DC converter and low-power LDO (100 mA) based on charging requirements. System power-saving is achieved when the device is under no charging conditions (the connected device is fully charged or no device is connected), the DC-DC converter is turned off (to save power because the converter is less efficient in a low-power operating region), and the low-power LDO supplies standby power to the charging port.

Power wake is activated in S4 or S5 mode (0011 setting, see Table 3). The TPS2546-Q1 charges a connected device as shown in Figure 35. The $\overline{\text{STATUS}}$ pin is pulled low (Case 1) which switches-out the LDO and switches-in the DC-DC converter to handle high-current charging.

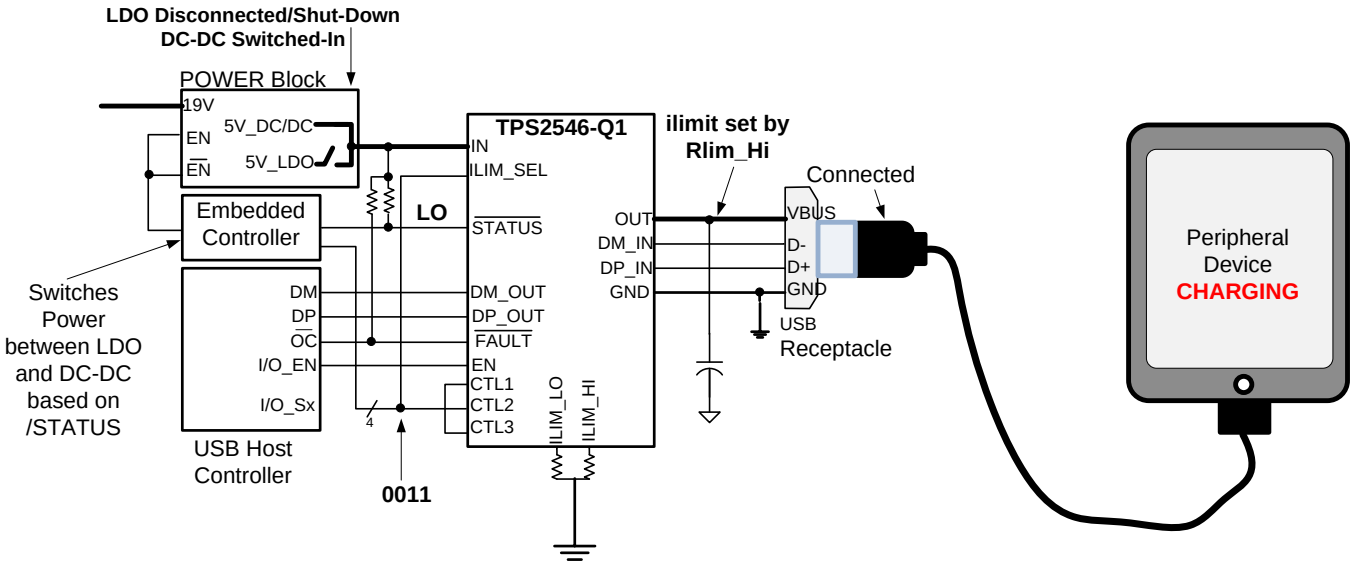


Figure 35. Case 1: System in S4 or S5, Device Charging

As shown in Case 2A and Case 2B (Figure 36 and Figure 37, respectively), when the connected device is fully charged or disconnects from the charging port, the charging current falls. If the charging current falls to less than 45 mA and stays below this threshold for more than 15 seconds, the TPS2546-Q1 device automatically sets a 55-mA internal current-limit and the $\overline{\text{STATUS}}$ pin is pulled high (see Figure 36 and Figure 37). As a result, the DC-DC converter turns off and the LDO turns on. The 55-mA current-limit prevents the output voltage of the low-power LDO from collapsing in case there is a spike in the current draw because of device attachment or other activity such as a display-panel LED turning on in a connected device.

When a device is attached and draws less than 55 mA of charging current, the TPS2546-Q1 reaches the internal current-limit (see the power-wake flow chart, Figure 34). When the device reaches the internal current-limit, device pulls $\overline{\text{STATUS}}$ low, turns on the DC-DC converter, and turns off the LDO. The TPS2546-Q1 device discharges OUT for more than 2 seconds (typical) to allow the main power supply to turn on. After the discharge of OUT, the device turns on again with the current-limit set by ILIM_HI (Case 1).

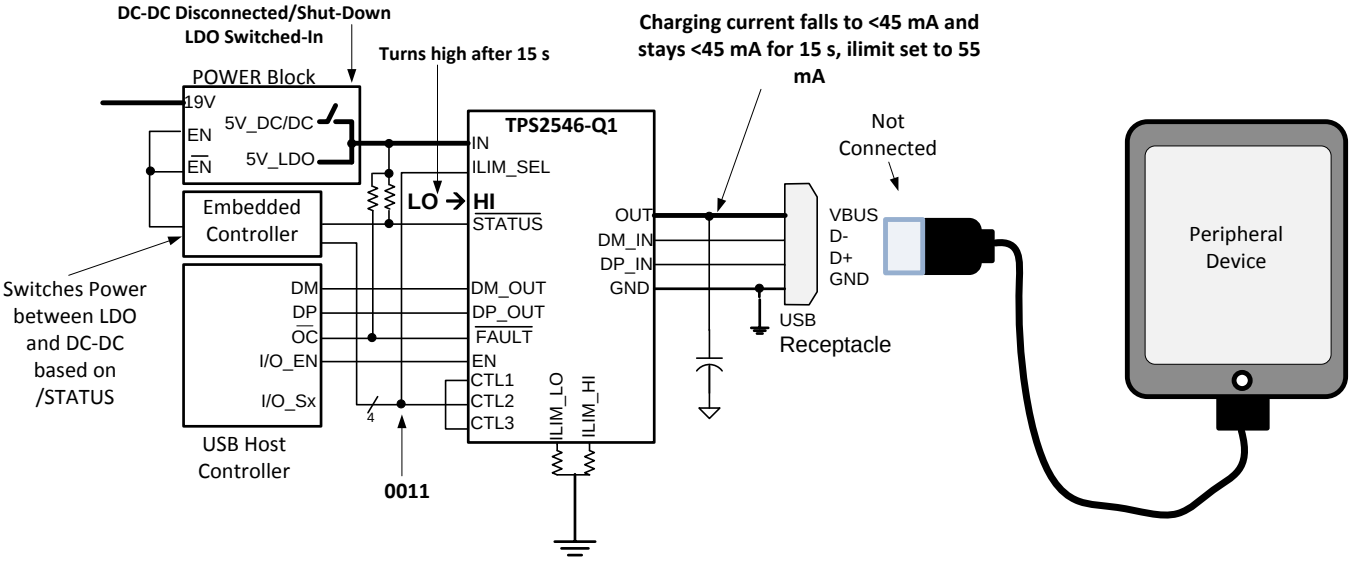


Figure 36. Case 2A: System in S4 or S5, No Device Attached

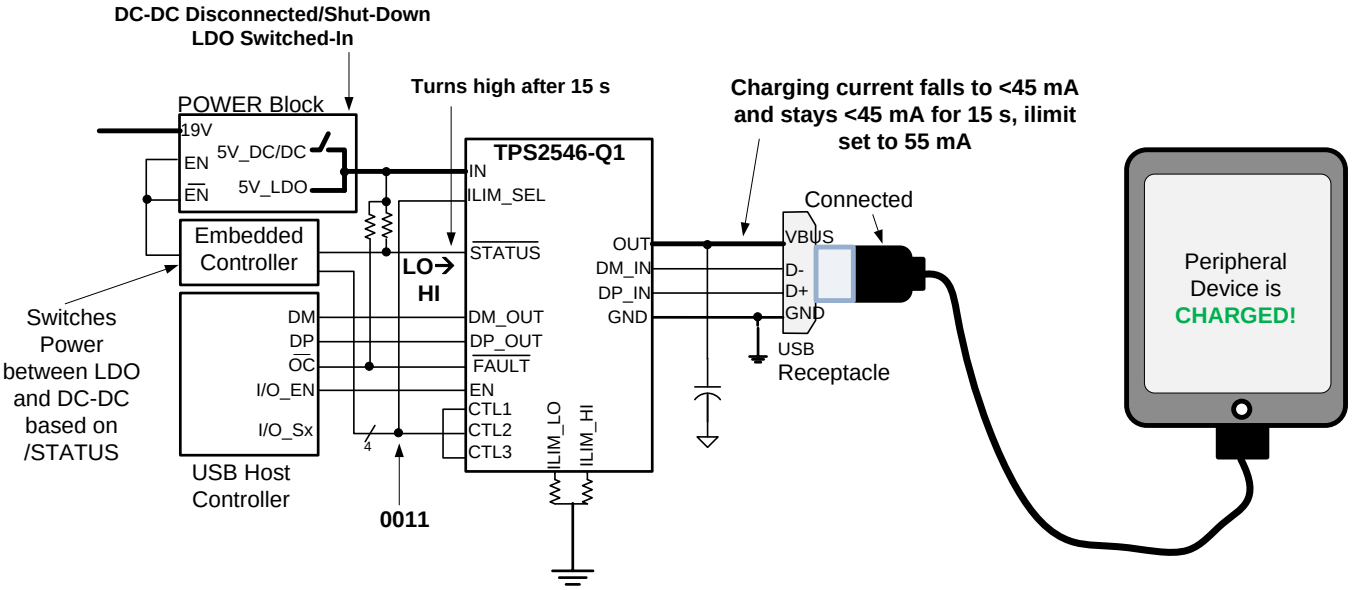


Figure 37. Case 2B: System in S4 or S5, Attached Device Fully Charged

Port Power Management

PPM is the intelligent and dynamic allocation of power. PPM is for systems that have multiple charging ports but cannot power them all simultaneously. The goals of this feature include the following:

1. Enhance the user experience by removing the need of the user to search for a charging port.
2. Design the power supply only for a reasonable charging load.

All ports are initially allowed to broadcast high-current charging. The charging current-limit is based on the setting of the ILIM_HI resistor connection. The system monitors $\overline{\text{STATUS}}$ to see when high current loads are present. Once the allowed number of ports assert $\overline{\text{STATUS}}$, the remaining ports are toggled to a noncharging port. Noncharging ports are SDP ports with a current-limit based on ILIM_LO. The TPS2546-Q1 device allows for a system to toggle between charging and noncharging ports either with or without an OUT discharge.

Benefits of PPM

The benefits of PPM include the following:

- Delivers better user experience
- Prevents overloading of system power supply
- Allows for dynamic power limits based on system state
- Allows every port to potentially be a high-power charging port
- Allows for smaller power-supply capacity because loading is controlled

PPM Details

All ports (CDP or DCP) are allowed to broadcast high-current charging. The current-limit is based on ILIM_HI. The system monitors the $\overline{\text{STATUS}}$ pin to see when high current loads are present. Once the allowed number of ports assert $\overline{\text{STATUS}}$, the remaining ports are toggled to an SDP noncharging port. The SDP current-limit is based on the ILIM_LO setting. The SDP ports are automatically toggled back to CDP or DCP mode when a charging port deasserts $\overline{\text{STATUS}}$.

Based on the CTL settings, a provision exists for a port to toggle between charging and noncharging ports either with or without a VBUS discharge (for example, when a port is in SDP2 mode (1110) and the ILIM_SEL pin toggles to 1 because of another port releasing high current requirements). The SDP2 port automatically reverts to CDP mode (1111) without a discharge event, which is desirable if this port was connected to a media device which synced data from the SDP2 port. A discharge event interrupts the syncing activity on the port and confuses the user.

The $\overline{\text{STATUS}}$ trip-point is based on the programmable ILIM_LO current-limit set point. The port is using the ILIM_HI current-limit; $\overline{\text{STATUS}}$ is *not* a current-limit. Because ILIM_LO defines the current-limit for an SDP port, use the ILIM_LO value to define a high current load. $\overline{\text{STATUS}}$ asserts in CDP and DCP when the load current is above ILIM_LO for 200 ms (typical). $\overline{\text{STATUS}}$ also asserts in CDP when an attached device completes a BC1.2 primary detection. $\overline{\text{STATUS}}$ deasserts in CDP and DCP when the load current is below ILIM_LO 10 mA for 3 seconds (typical).

Implementing PPM in a System with Two Charging Ports

Figure 38 shows the implementation of the two charging ports, each with a TPS2546-Q1 device. In this example, the 5-V power supply for the two charging ports is rated at less than 3 A or less than 15 W maximum. Both devices have R_{LIM} chosen to correspond to the low (0.9 A) and high (1.5 A) current-limit setting for the port. In this implementation the system can support only one of the two ports at 1.5-A charging current while the other port is set to SDP mode and I_{LIMIT} corresponds to 0.9 A.

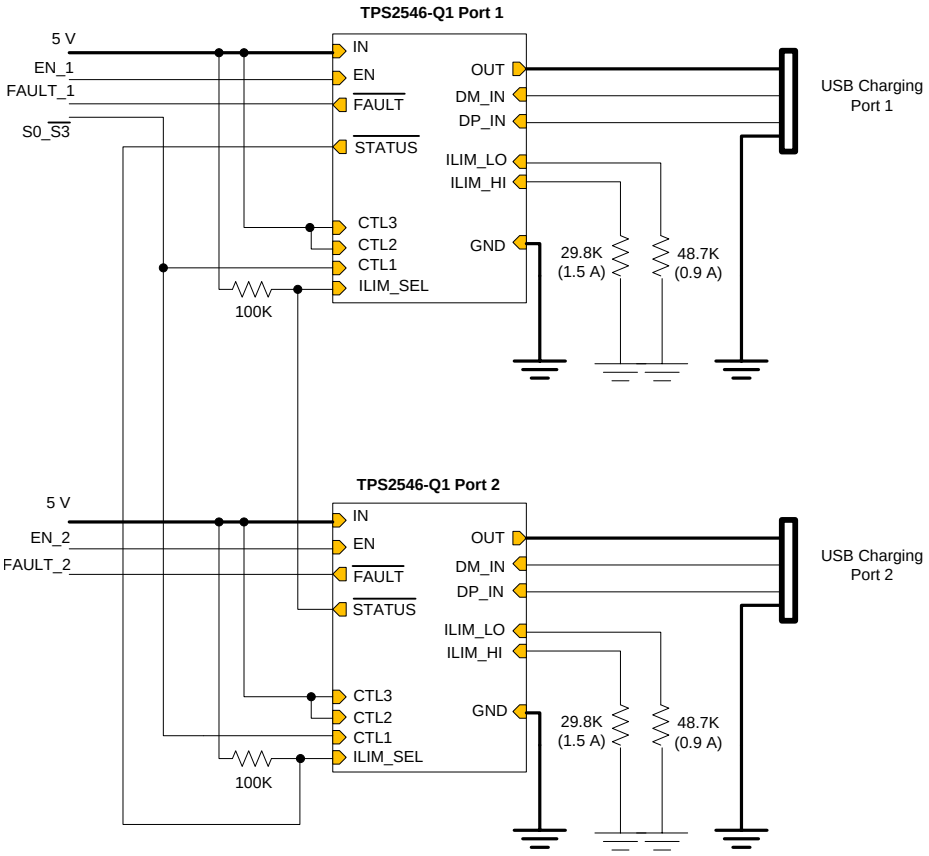


Figure 38. Implementing Port-Power Management in a System Supporting Two Charging Ports

CDP and SDP Auto Switch

The TPS2546-Q1 device is equipped with a CDP and SDP auto-switch feature to support some popular phones in the market. These popular phones do not comply to the BC1.2 specification because they fail to establish a data connection in CDP mode. These phones use primary detection (used to distinguish between an SDP and different types of charging ports) to only identify ports as SDP (data, no charge) or DCP (no data, no charge). These phones do not recognize CDP (data, charge) ports. When connected to a CDP port, these phones classify the port as a DCP and only charge the battery. Because the charging ports are configured as CDP when the computer is in S0, users do not receive the expected data connection (see Figure 39).

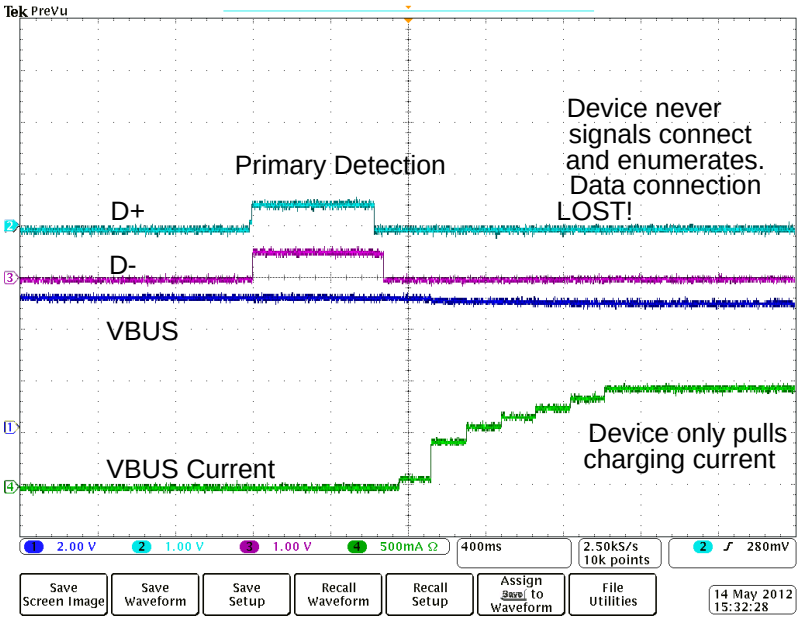


Figure 39. CDP and SDP Auto

To remedy this problem, the TPS2546-Q1 device employs a CDP and SDP auto-switch scheme to ensure these BC1.2 noncompliant phones establish data connection using the following steps.

1. The TPS2546-Q1 device determines when a noncompliant phone has wrongly classified a CDP port as a DCP port and has not made a data connection.
2. The TPS2546-Q1 device automatically completes an OUT (VBUS) discharge and reconfigures the port as an SDP.
3. When reconfigured as an SDP, the phone detects a connection to an SDP and establishes a data connection.
4. The TPS2546-Q1 device then switches automatically back to a CDP without doing an OUT (VBUS) discharge.
5. The phone continues to operate like it is connected to an SDP because OUT (VBUS) was not interrupted.

The port is now ready in CDP if a new device is attached.

Overcurrent Protection

When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur. In the first condition, the output is shorted before the device enables or before V_{IN} is applied. The TPS2546-Q1 device senses the short and immediately switches into a constant-current output. In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents flow for 1 to 2 µs (typical) before the current-limit circuit reacts. The device operates in constant-current mode after the current-limit circuit has responded. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting. The device remains off until the junction temperature cools to approximately 20°C and then restarts. The device continues to cycle on and off until the overcurrent condition is removed.

Current-Limit Settings

The TPS2546-Q1 device has two independent current-limit settings that are programmed externally with a resistor. The ILIM_HI setting is programmed with R_{ILIM_HI} connected between ILIM_HI and GND. The ILIM_LO setting is programmed with R_{ILIM_LO} connected between ILIM_LO and GND. See Table 3 for scenarios when each current-limit is used. Both settings have the same relation between the current-limit and the programming resistor.

R_{ILIM_LO} is optional and the ILIM_LO pin can be disconnected if the following conditions are met:

1. ILIM_SEL is always set high.
2. Load Detection — Port-Power Management is not used

Equation 1 programs the typical current-limit.

$$I_{OS\_typ}(mA) = \frac{50500}{(R_{ILIM\_XX}(k\Omega) + 0.1)} \quad (1)$$

R_{ILIM_XX} corresponds to either R_{ILIM_HI} or R_{ILIM_LO} as appropriate.

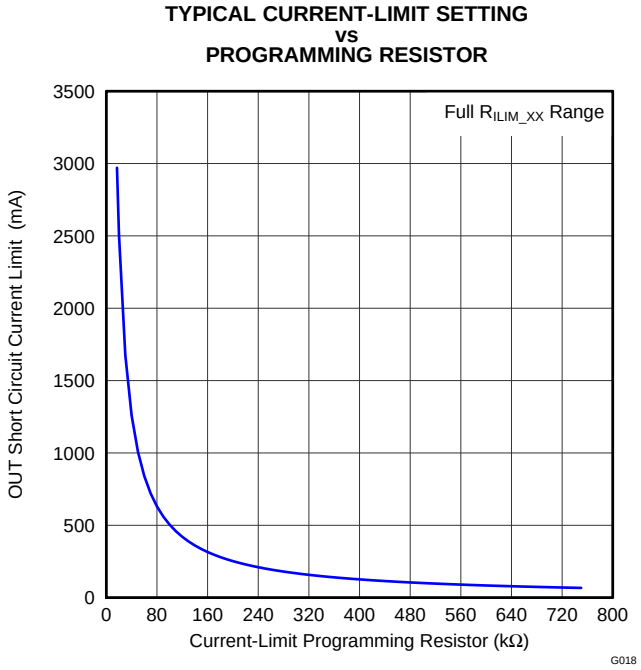


Figure 40.

Many applications require that the current-limit meet specific tolerance limits. When designing to these tolerance limits, both the tolerance of the TPS2546-Q1 current-limit and the tolerance of the external programming resistor must be taken into account. The following equations approximate the TPS2546-Q1 minimum and maximum current-limits to within a few milliamperes and are appropriate for design purposes. The equations do not constitute part of TI's published device specifications for purposes of TI's product warranty. These equations assume an ideal — no variation — external programming resistor. To take resistor tolerance into account, first determine the minimum and maximum resistor values based on the tolerance specifications and use these values in the equations. Because of the inverse relation between the current-limit and the programming resistor, use the maximum resistor value in the I_{OS_min} equation and the minimum resistor value in the I_{OS_max} equation.

$$I_{OS\_min}(mA) = \frac{45661}{(R_{ILIM\_XX}(k\Omega) + 0.1)^{0.98422}} - 30 \quad (2)$$

$$I_{OS\_max}(mA) = \frac{55639}{(R_{ILIM\_XX}(k\Omega) + 0.1)^{1.0143}} + 30 \quad (3)$$

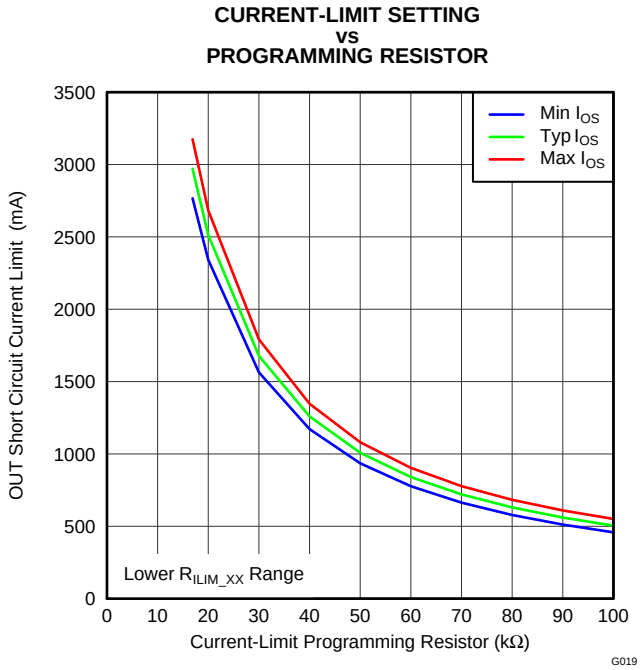


Figure 41.

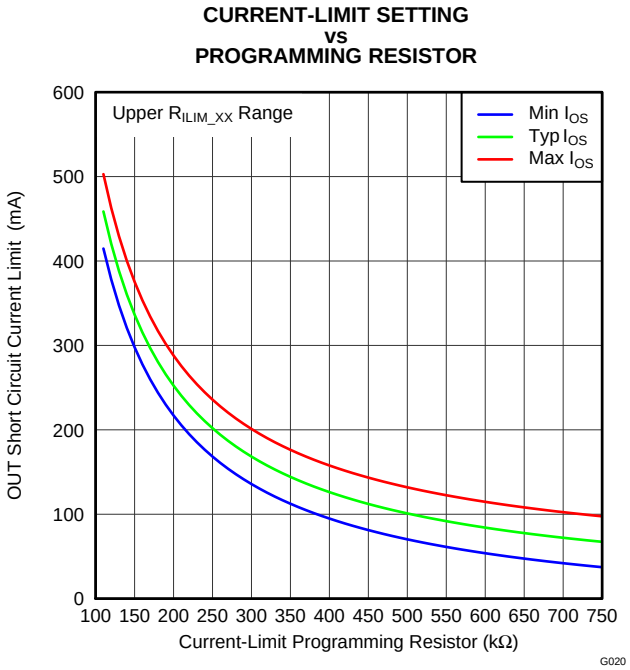


Figure 42.

The traces routing the R_{ILIM_XX} resistors must be a sufficiently low resistance as to not affect the current-limit accuracy. The ground connection for the R_{ILIM_XX} resistors is also very important. The resistors must reference back to the GND pin of the TPS2546-Q1 device. Follow normal board layout practices to ensure that current flow from other parts of the board does not impact the ground potential between the resistors and the GND pin of the TPS2546-Q1 device.

FAULT Response

The $\overline{\text{FAULT}}$ open-drain output is asserted (active low) during an overtemperature or current-limit condition. The output remains asserted until the fault condition is removed. The TPS2546-Q1 device is designed to eliminate false $\overline{\text{FAULT}}$ reporting by using an internal deglitch circuit for current-limit conditions without the need for external circuitry. This elimination ensures that $\overline{\text{FAULT}}$ is not accidentally asserted because of normal operation such as starting into a heavy capacitive load. Overtemperature conditions are not deglitched and assert the $\overline{\text{FAULT}}$ signal immediately.

Undervoltage Lockout

The undervoltage-lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold for ULVO. Built-in hysteresis prevents unwanted oscillations on the output due to input voltage drop from large current surges.

Thermal Sense

Two independent thermal-sensing circuits protect the TPS2546-Q1 device if the temperature exceeds recommended operating conditions. These circuits monitor the operating temperature of the power-distribution switch and disable operation. The device operates in constant-current mode during an overcurrent condition, which increases the voltage drop across power switch. The power dissipation in the package is proportional to the voltage drop across the power switch, so the junction temperature rises during an overcurrent condition. The first thermal sensor turns off the power switch when the die temperature exceeds 135°C and the device is in current limit. The second thermal sensor turns off the power switch when the die temperature exceeds 155°C regardless of whether the power switch is in current limit. Hysteresis is built into both thermal sensors, and the switch turns on after the device has cooled by approximately 20°C. The switch continues to cycle off and then on until the fault is removed. The open-drain false-reporting output, $\overline{\text{FAULT}}$, is asserted (active low) during an overtemperature shutdown condition.

REVISION HISTORY

Changes from Original (October 2013) to Revision A **Page**

- Deleted *Qualified for Automotive Applications* and Temperature Grade 1 text from *FEATURES* list 1
- Changed D+ and D– to D+/D– in *FEATURES* list 1
- Changed load detection bullet in *FEATURES* list 1
- Deleted USB-compatible bullet from *FEATURES* list 1
- Deleted *Integrated* from MOSFET bullet in *FEATURES* list 1
- Changed document status from *Product Preview* to *Production Data* 1
- Changed DISCHARGE specification in the ELECTRICAL CHARACTERISTICS section by splitting T_{DCHG} into long and short time, and removing test condition for R_{DCHG} 3
- Deleted max value for DP/DM switch off-state capacitance parameter in the *ELECTRICAL CHARACTERISTICS, HIGH-BANDWIDTH SWITCH* table 4
- Deleted max value for DP/DM switch on-state capacitance parameter in the *ELECTRICAL CHARACTERISTICS, HIGH-BANDWIDTH SWITCH* table 4
- Deleted max value for t_{SK} in the *ELECTRICAL CHARACTERISTICS, HIGH-BANDWIDTH SWITCH* table 4
- Deleted *TPS2543 Only* from block diagram 7
- Deleted discharge time of 2 seconds from the *TPS2546-Q1 Charging States* image in the *Device Operation* section 20
- Changed flow line condition names for DCP_SHORT and DCP_DIVIDER in the *Device Control Pins* table to match those listed in the *Truth Table* 20
- Added t_{DCHG_L} and t_{DCHG_S} text to the *Output Discharge* section 21

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2546QRTERQ1	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2546Q	Samples
TPS2546QRTETQ1	PREVIEW	WQFN	RTE	16	250	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS2546-Q1 :

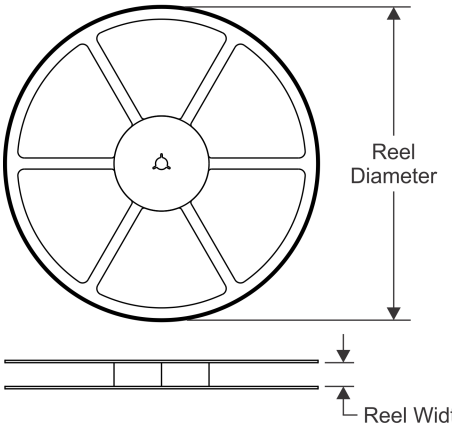
- Catalog: TPS2546

NOTE: Qualified Version Definitions:

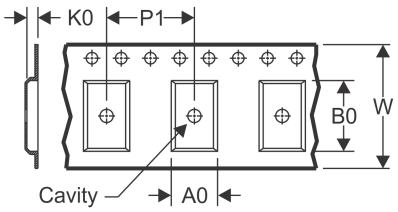
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

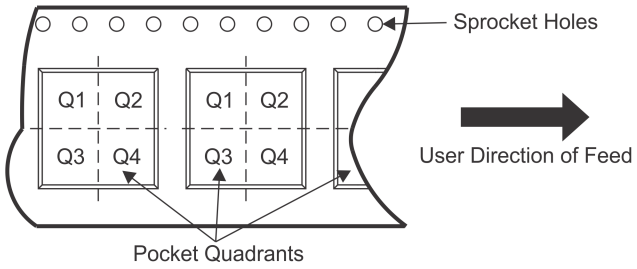


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

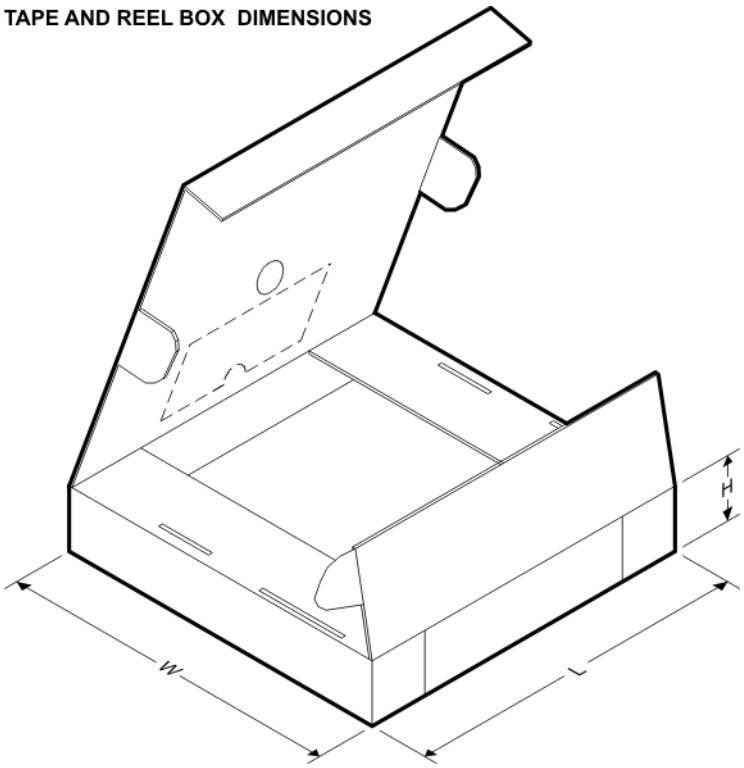
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2546QRTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

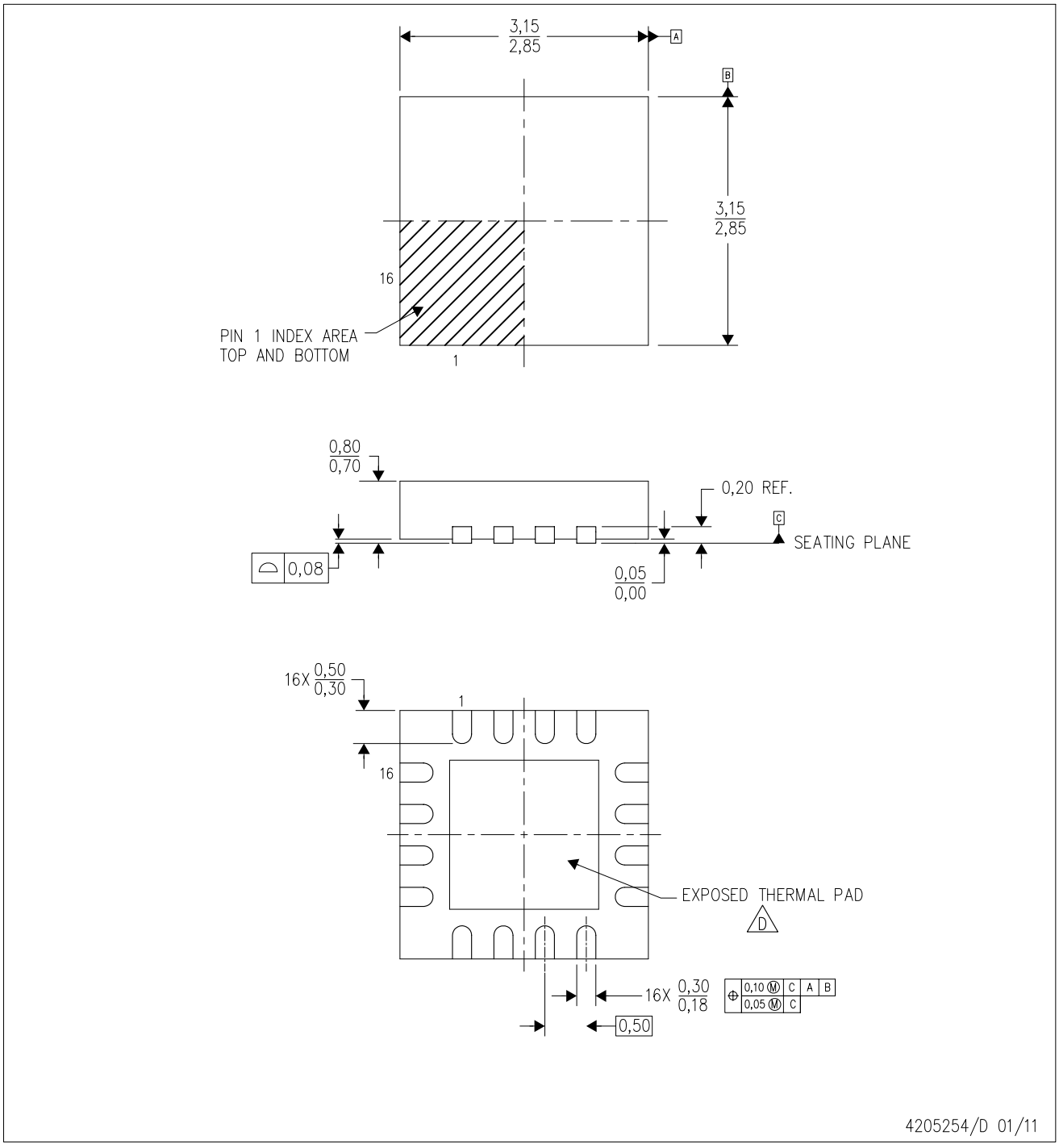
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2546QRTERQ1	WQFN	RTE	16	3000	367.0	367.0	35.0

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

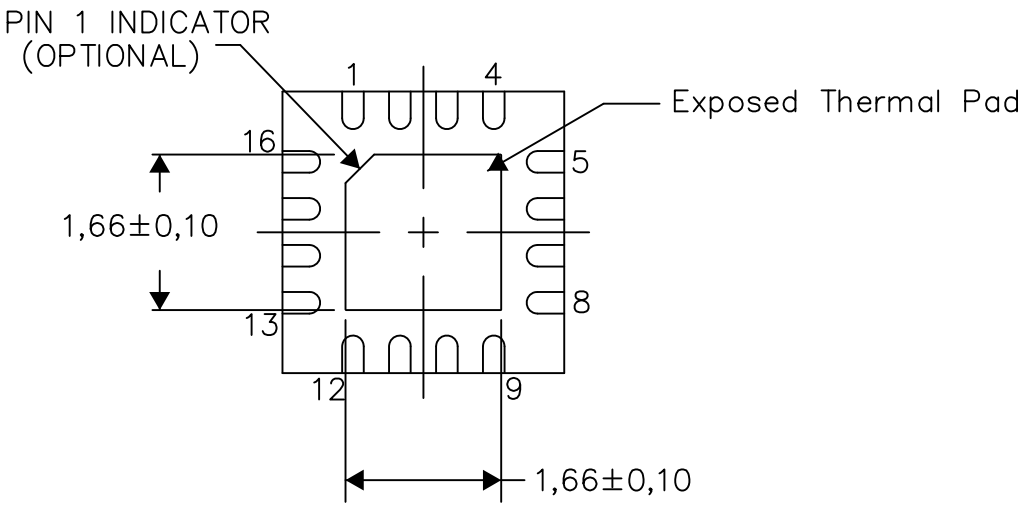
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206446–8/R 10/14

NOTE: A. All linear dimensions are in millimeters

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