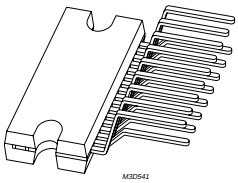

TDA8944AJ

2 x 7 W BTL audio amplifier with DC gain control

Rev. 01 — 01 March 2002 **Product data**

1. General description

The TDA8944AJ is a dual-channel audio power amplifier with DC gain control. It has an output power of 2 × 7 W at an 8 Ω load and a 12 V supply. The circuit contains two Bridge-Tied Load (BTL) amplifiers with an all-NPN output stage and standby/mute logic. The overall gain can be adjusted from +30 dB down to −50 dB using a DC control voltage. This feature can be used for volume control or a preset gain.
The TDA8944AJ comes in a 17-pin DIL-bent-SIL (DBS) power package and is pin compatible with the TDA8944J.

2. Features

- Gain/volume adjustment via a DC control pin
- Soft clipping
- Operating at a low supply voltage
- Standby and mute mode
- No on/off switching plops
- Low standby current
- High supply voltage ripple rejection
- Outputs short-circuit protected to ground, supply and across the load
- Thermally protected
- Printed-circuit board compatible with TDA8946AJ and TDA8580J.

3. Applications

- Mains fed applications (e.g. TV sound)
- PC audio
- Portable audio.

4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	12	18	V
I_q	quiescent supply current	V_{CC} = 12 V; R_L = ∞	-	40	50	mA
I_{stb}	standby supply current		-	-	10	µA
P_o	output power	THD = 10%; R_L = 8 Ω; V_{CC} = 12 V	6	7	-	W
THD	total harmonic distortion	P_o = 1 W	-	0.07	0.5	%

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Table 1: Quick reference data...*continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_{v(max)}$	maximum voltage gain		29	30	31	dB
$G_{v(cr)}$	voltage gain control range		-	80	-	dB
SVRR	supply voltage ripple rejection		-	55	-	dB

5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
TDA8944AJ	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

6. Block diagram

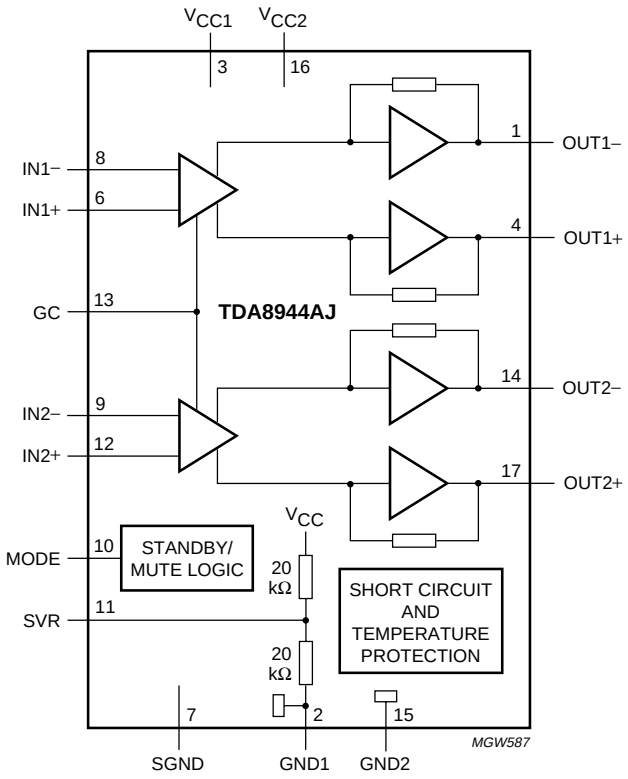


Fig 1. Block diagram.

7. Pinning information

7.1 Pinning

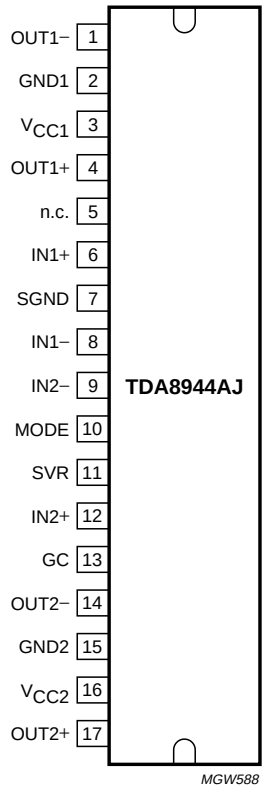


Fig 2. Pin configuration.

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
OUT1–	1	negative loudspeaker terminal 1
GND1	2	ground channel 1
V_{CC1}	3	supply voltage channel 1
OUT1+	4	positive loudspeaker terminal 1
n.c.	5	not connected
IN1+	6	positive input 1
SGND	7	signal ground
IN1–	8	negative input 1
IN2–	9	negative input 2
MODE	10	mode selection input (standby, mute, operating)
SVR	11	half supply voltage decoupling (ripple rejection)
IN2+	12	positive input 2

Table 3: Pin description *...continued*

Symbol	Pin	Description
GC	13	DC gain control
OUT2–	14	negative loudspeaker terminal 2
GND2	15	ground channel 2
V_{CC2}	16	supply voltage channel 2
OUT2+	17	positive loudspeaker terminal 2

8. Functional description

The TDA8944AJ is a stereo BTL audio power amplifier capable of delivering 2 × 7 W output power to an 8 Ω load at THD = 10%, using a 12 V power supply and an external heatsink. The gain of both amplifiers can be adjusted through a DC control voltage (pin GC). This feature can be used for volume control or a preset gain.

With the three-level MODE input the device can be switched from ‘standby’ to ‘mute’ and to ‘operating’ mode.

The TDA8944AJ outputs are protected by an internal thermal shutdown protection mechanism and a short-circuit protection.

8.1 Input configuration

The TDA8944AJ inputs can be driven symmetrical (floating) as well as asymmetrical. In the asymmetrical mode one input pin is connected via a capacitor to the signal source and the other input is connected to the signal ground. This signal ground should be as close as possible to the SVR (electrolytic) capacitor ground. Note that the DC level of the input pins is half of the supply voltage V_{CC}, so coupling capacitors for both pins are necessary.

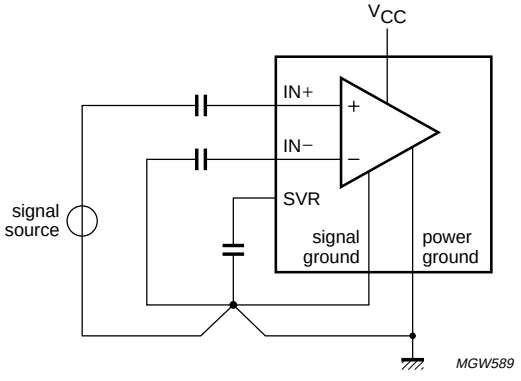


Fig 3. Asymmetrical input configuration.

The input cut-off frequency is:

$$f_{i(cut-off)} = \frac{1}{2\pi(0.5 \times R_i \times C_i)} \quad (1)$$

For R_i = 32 kΩ and C_i = 220 nF:

$$f_{i(cut-off)} = \frac{1}{2\pi(0.5 \times 32 \times 10^3 \times 220 \times 10^{-9})} = 45.2 \text{ Hz} \quad (2)$$

As shown in Equation 2, large capacitors values for the inputs are not necessary; so the switch-on delay during charging of the input capacitors can be minimized. This results in a good low frequency response and good switch-on behaviour.

Remark: To prevent high frequency oscillations do not leave the inputs open, connect a capacitor of 4.7 nF across the input pins close to the device (see Figure 15).

8.2 Power amplifier

The power amplifier is a Bridge-Tied Load (BTL) amplifier with an all-NPN output stage, capable of delivering a peak output current of 2 A.

The BTL principle offers the following advantages:

- Lower peak value of the supply current
- The ripple frequency on the supply voltage is twice the signal frequency
- No expensive DC-blocking capacitor
- Good low frequency performance.

8.2.1 Output power measurement

The output power as a function of the supply voltage is measured on the output pins at THD = 10%; see Figure 10. The maximum output power is limited by the supply voltage of 12 V and the maximum available output current: 2 A repetitive peak current.

8.2.2 Headroom

Typical CD music requires at least 12 dB (factor 15.85) dynamic headroom - compared to the average power output - for transferring the loudest parts without distortion. At V_{CC} = 12 V, R_L = 8 Ω and P_o = 4 W at THD = 0.2% (see Figure 8), the Average Listening Level (ALL) - music power - without any distortion yields:

$$P_{o(ALL)} = \frac{4 \text{ W}}{15.85} = 252.4 \text{ mW} \quad (3)$$

The power dissipation can be derived from Figure 12 on page 11 for 0 dB respectively 12 dB headroom.

Table 4: Power rating as function of headroom

Headroom	Power output (THD = 0.2%)	Power dissipation
0 dB	P_o = 4 W	P = 7.8 W
12 dB	$P_{o(ALL)}$ = 252.4 mW	P = 4.0 W

For the average listening level a power dissipation of 4 W can be used for a heatsink calculation.

8.3 Mode selection

The TDA8944AJ has three functional modes, which can be selected by applying the proper DC voltage to pin MODE.

Standby — In this mode the current consumption is very low and the outputs are floating. The device is in standby mode when $V_{MODE} > (V_{CC} - 0.5\ V)$, or when the MODE pin is left floating.

Mute — In this mode the amplifier is DC-biased but not operational (no audio output). This allows the input coupling capacitors to be charged to avoid pop-noise. The device is in mute mode when $3.5\ V < V_{MODE} < (V_{CC} - 1.5\ V)$.

Operating — In this mode the amplifier is operating normally. The operating mode is activated at $V_{MODE} < 1.0\ V$.

8.3.1 Switch-on and switch-off

To avoid audible plops during supply voltage switch-on or switch-off, the device is set to standby mode before the supply voltage is applied (switch-on) or removed (switch-off).

The switch-on and switch-off time can be influenced by an RC-circuit on the MODE pin. Rapid on/off switching of the device or the rapid switching of the MODE pin may cause ‘click-and pop-noise’. This can be prevented by proper timing of the RC-circuit on the MODE pin.

8.4 DC gain control

The gain of both amplifiers can be adjusted (logarithmic) by applying an external DC voltage source on pin GC (see Figure 6). The DC voltage source range is 0.5 to 4.0 V. This feature can be used for volume control or a preset gain.

The maximum voltage gain is set at +30 dB and the control range is more than 80 dB, so the minimal gain is less than –50 dB. When pin GC is not connected, the gain is set at +24 dB.

8.5 Supply Voltage Ripple Rejection (SVRR)

The SVRR is measured with an electrolytic capacitor of 10 µF on pin SVR at a bandwidth of 10 Hz to 80 kHz. Figure 14 illustrates the SVRR as function of the frequency. A larger capacitor value on the SVR pin improves the ripple rejection behavior at the lower frequencies.

8.6 Built-in protection circuits

The TDA8944AJ contains two types of protection circuits, i.e. short-circuit and thermal shutdown.

8.6.1 Short-circuit protection

Short-circuit to ground or supply line — This is detected by a so-called 'missing current' detection circuit which measures the current in the positive supply line and the current in the ground line. A difference between both currents larger than 0.8 A, switches the power stage to the standby mode; high impedance of the outputs and very low supply current.

Short-circuit across the load — This is detected by an absolute-current measurement. An absolute-current larger than 2 A, switches the power stage to standby mode; high impedance of the outputs and a very low supply current.

8.6.2 Thermal shutdown protection

The junction temperature is measured by a temperature sensor; at a junction temperature of approximately 150 °C this detection circuit switches the power stage to the standby mode; high impedance of the outputs and very low supply current.

9. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	no signal	–0.3	+25	V
		operating	–0.3	+18	V
V_I	input voltage		–0.3	V_{CC} + 0.3	V
I_{ORM}	repetitive peak output current		-	2	A
T_{stg}	storage temperature	non-operating	–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
P_{tot}	total power dissipation		-	18	W
$V_{CC(sc)}$	supply voltage to guarantee short-circuit protection		-	15	V

10. Thermal characteristics

Table 6: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	both channels driven	4.5	K/W

11. Static characteristics

Table 7: Static characteristics

V_{CC} = 12 V; T_{amb} = 25 °C; R_L = 8 Ω; V_{MODE} = 0 V; V_i = 0 V; measured in test circuit Figure 15; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage	operating		4.5	12	18	V
I_q	quiescent supply current	R_L = ∞	[1]	-	40	50	mA
I_{stb}	standby supply current	V_{MODE} = V_{CC}		-	-	10	µA
V_O	DC output voltage		[2]	-	6	-	V
ΔV_{OUT}	differential output voltage offset		[3]	-	-	170	mV
V_{MODE}	mode selection input voltage	operating mode		0	-	1.0	V
		mute mode		3.5	-	V_{CC} – 1.5	V
		standby mode		V_{CC} – 0.5	-	V_{CC}	V
I_{MODE}	mode selection input current	0 < V_{MODE} < V_{CC}		-	-	20	µA
V_{GC}	gain control voltage (pin GC)	pin GC not connected		-	2.75	-	V
I_{GC}	current into pin GC	V_{GC} = 0 V		-	600	-	µA

[1] With a load connected at the outputs the quiescent current will increase, the maximum of this increase being equal to the differential output voltage offset (ΔV_{OUT}) divided by the load resistance (R_L).

[2] The DC output voltage with respect to ground is approximately 0.5V_{CC}.

[3] $\Delta V_{OUT} = |V_{OUT+} - V_{OUT-}|$.

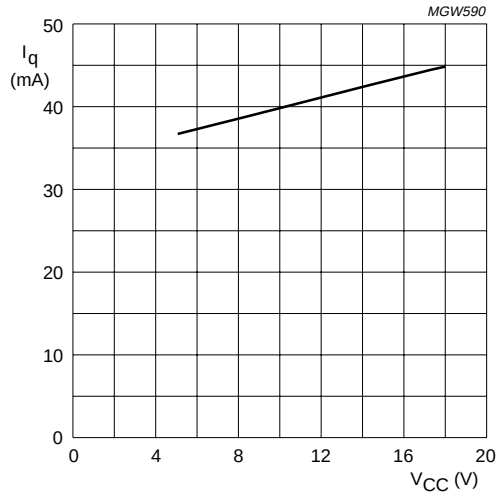
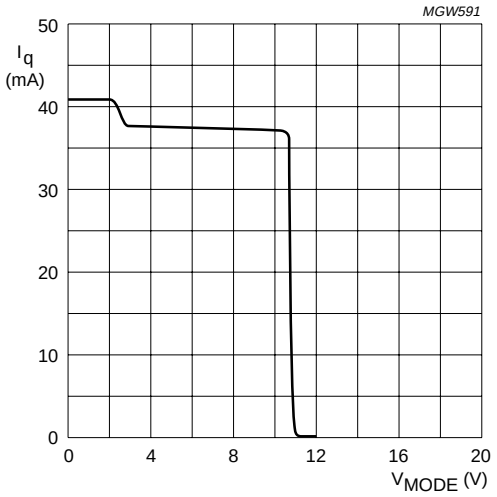


Fig 4. Quiescent current as function of supply voltage.



V_{CC} = 12 V

Fig 5. Quiescent current as function of mode voltage.

12. Dynamic characteristics

Table 8: Dynamic characteristics

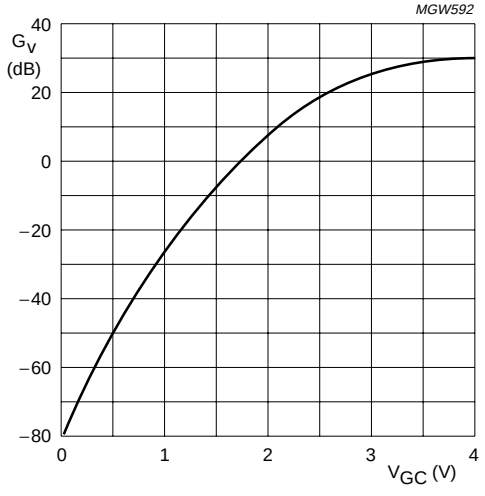
V_{CC} = 12 V; T_{amb} = 25 °C; R_L = 8 Ω; f = 1 kHz; V_{MODE} = 0 V; G_v = 30 dB; V_{GC} = 4.0 V; measured in test circuit Figure 15; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_o	output power	THD = 10%		6	7	-	W
		THD = 0.5%		-	5	-	W
THD	total harmonic distortion	P_o = 1 W		-	0.07	0.5	%
$G_{v(max)}$	maximum voltage gain			29	30	31	dB
$G_{v(cr)}$	gain control range	0.5 < V_{GC} < 4.0 V		-	80	-	dB
$V_{i(rms)}$	input voltage (RMS value)	G_v = 0 dB; THD <1%		1.0	-	-	V
$Z_{i(dif)}$	differential input impedance			50	65	-	kΩ
$V_{n(o)}$	noise output voltage	V_{GC} = 4.0 V	[1]	-	120	150	μV
		V_{GC} = 1.0 V	[1]	-	30	-	μV
SVRR	supply voltage ripple rejection	f_{ripple} = 1 kHz	[2]	-	55	-	dB
		f_{ripple} = 100 Hz to 20 kHz	[2]	-	55	-	dB
$V_{o(mute)}$	output voltage	mute mode	[3]	-	30	50	μV
α_{cs}	channel separation	R_{source} = 0 Ω		50	75	-	dB
$\lvert\Delta G_v\rvert$	channel unbalance	G_v = 0 dB; V_{GC} = 1.8 V		-	-	1	dB

[1] The noise output voltage is measured at the output in a frequency range from 20 Hz to 20 kHz (unweighted), with a source impedance R_{source} = 0 Ω at the input.

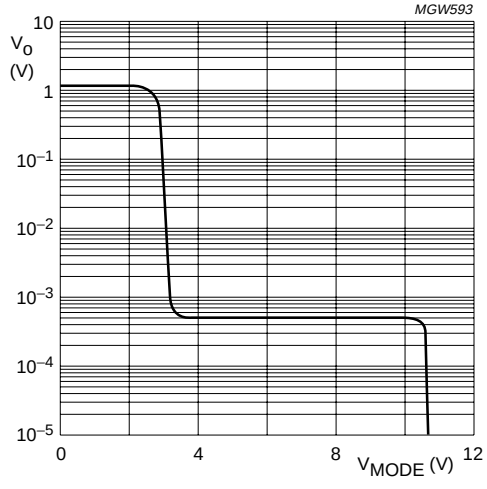
[2] Supply voltage ripple rejection is measured at the output, with a source impedance R_{source} = 0 Ω at the input. The ripple voltage is a sine wave with a frequency f_{ripple} and an amplitude of 700 mV (RMS), which is applied to the positive supply rail.

[3] Output voltage in mute mode is measured with V_{GC} = 0 V and an input voltage of 1 V (RMS) in a bandwidth of 20 kHz, thus including noise.



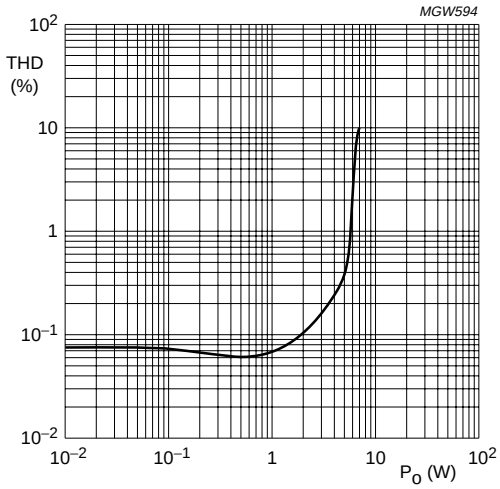
V_{CC} = 12 V

Fig 6. Voltage gain as function of control voltage.



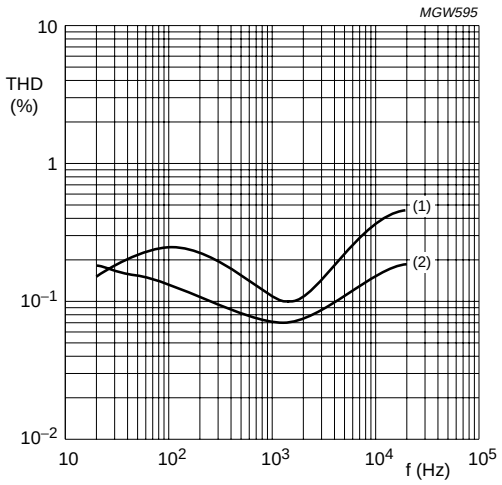
V_i = 30 mV; V_{CC} = 12 V

Fig 7. Output voltage as function of mode voltage.



V_{CC} = 12 V

Fig 8. Total harmonic distortion as function of output power.

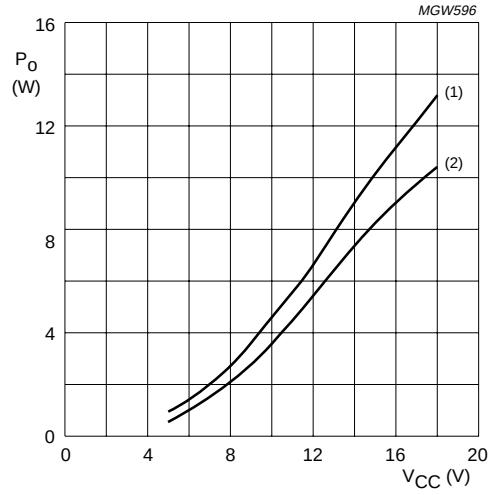


V_{CC} = 12 V; no bandpass filter applied

(1) P_o = 0.1 W

(2) P_o = 1 W

Fig 9. Total harmonic distortion as function of frequency.

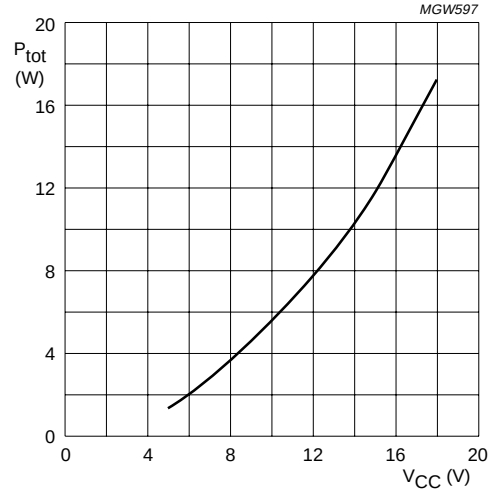


R_L = 8 Ω

(1) THD = 10%

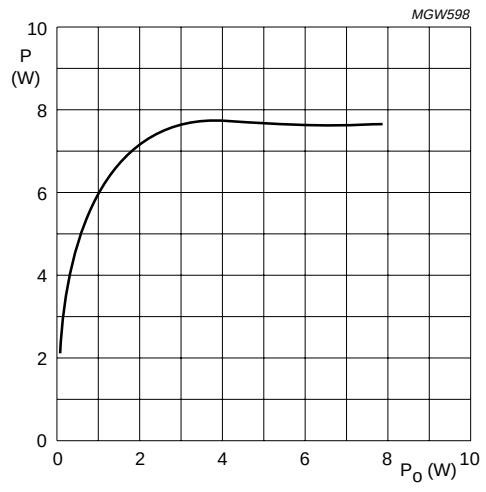
(2) THD = 1%

Fig 10. Output power as function of supply voltage.



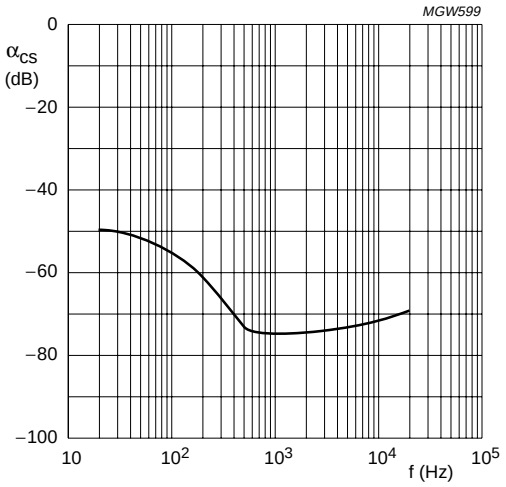
R_L = 8 Ω

Fig 11. Total power dissipation (worst-case) as function of supply voltage.



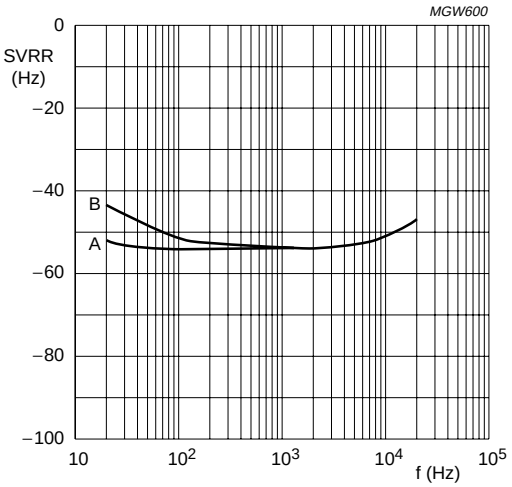
V_{CC} = 12 V; R_L = 8 Ω

Fig 12. Power dissipation as function of output power.



V_{CC} = 12 V; no bandpass filter applied

Fig 13. Channel separation as function of frequency.



V_{CC} = 12 V; R_{source} = 0 Ω; V_{ripple} = 707 mV (RMS); a bandpass filter of 10 Hz to 80 kHz has been applied.

Curve A: inputs short-circuited

Curve B: inputs short-circuited and connected to ground.

Fig 14. Supply voltage ripple rejection as function of frequency.

13. Internal circuitry

Table 9: Internal circuitry

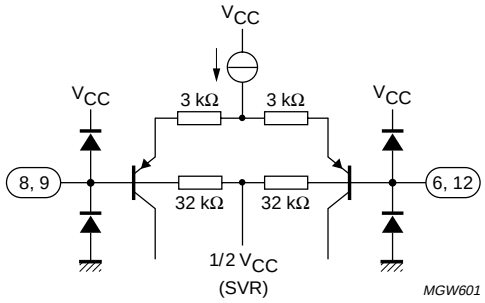
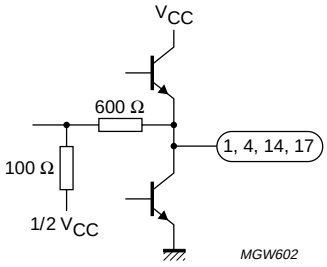
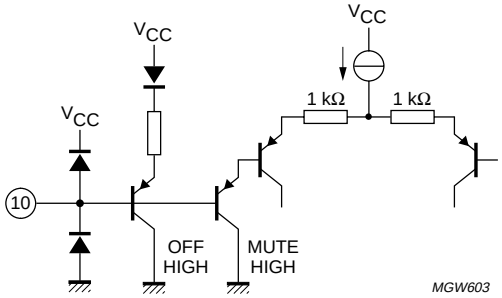
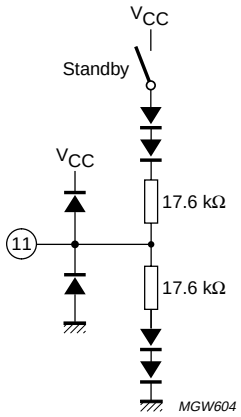
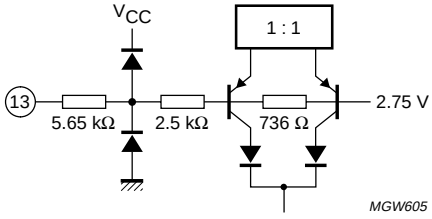
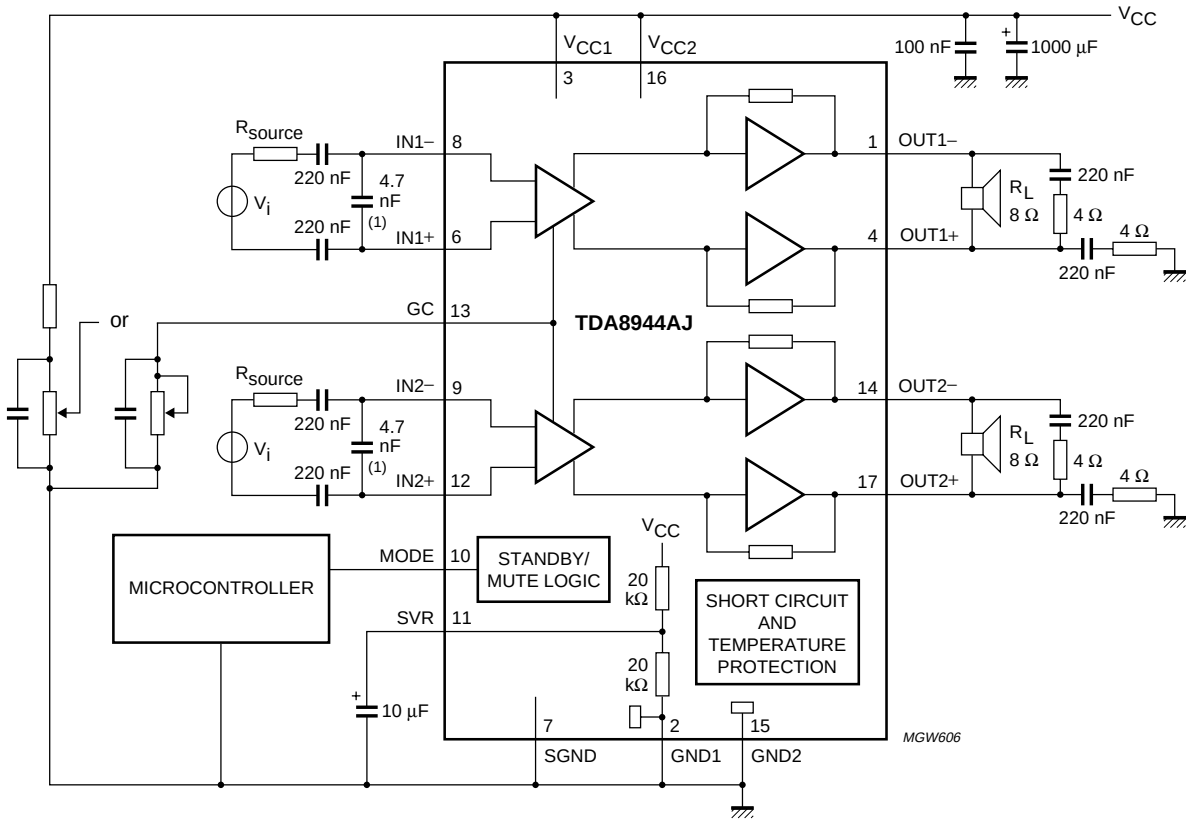
Pin	Symbol	Equivalent circuit
6 and 8	IN1+ and IN1–	
12 and 9	IN2+ and IN2–	
1 and 4	OUT1– and OUT1+	
14 and 17	OUT2– and OUT2+	
10	MODE	

Table 9: Internal circuitry *…continued*

Pin	Symbol	Equivalent circuit
11	SVR	
13	GC	

14. Application information



(1) To prevent high frequency oscillations do not leave the inputs open, connect a capacitor of 4.7 nF across the input pins close to the device.

Fig 15. Application diagram.

14.1 Printed-circuit board

14.1.1 Layout and grounding

For a high system performance level certain grounding techniques are essential. The input reference grounds have to be tied with their respective source grounds and must have separate tracks from the power ground tracks; this will prevent the large (output) signal currents from interfering with the small AC input signals. The small-signal ground tracks should be physically located as far as possible from the power ground tracks. Supply and output tracks should be as wide as possible for delivering maximum output power.

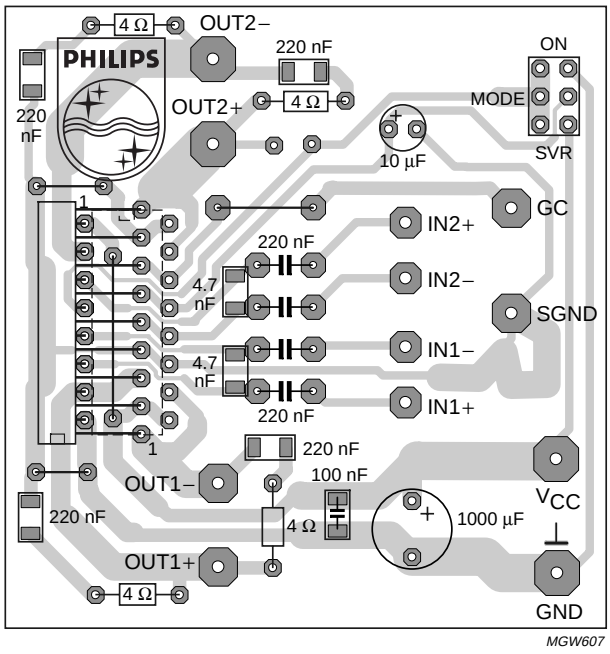


Fig 16. Printed-circuit board layout (single-sided); components view.

14.1.2 Power supply decoupling

Proper supply bypassing is critical for low-noise performance and high supply voltage ripple rejection. The respective capacitor location should be as close as possible to the device and grounded to the power ground. Proper power supply decoupling also prevents oscillations.

For suppressing higher frequency transients (spikes) on the supply line a capacitor with low ESR - typical 100 nF - has to be placed as close as possible to the device. For suppressing lower frequency noise and ripple signals, a large electrolytic capacitor - e.g. 1000 µF or greater - must be placed close to the device.

The bypass capacitor on the SVR pin reduces the noise and ripple on the midrail voltage. For good THD and noise performance a low ESR capacitor is recommended.

14.2 Thermal behaviour and heatsink calculation

The measured maximum thermal resistance of the IC package, $R_{th(j\text{-}mb)}$ is 4.5 K/W. A calculation for the heatsink can be made, with the following parameters:

T_{amb} = 50 °C

V_{CC} = 12 V and R_L = 8 Ω

$T_{j(max)}$ = 150 °C

$R_{th(tot)}$ is the total thermal resistance between the junction and the ambient including the heatsink. In the heatsink calculations the value of $R_{th(mb\text{-}h)}$ is ignored.

At V_{CC} = 12 V and R_L = 8 Ω the measured worst-case sine-wave dissipation is 8 W; see Figure 12. For $T_{j(max)}$ = 150 °C the temperature rise - caused by the power dissipation - is: 150 − 50 = 100 °C.

$P \times R_{th(tot)} = 100$ °C

$R_{th(tot)} = 100/8 = 12.5$ K/W

$R_{th(h-a)} = R_{th(tot)} - R_{th(j-mb)} = 12.5 - 4.5 = 8.0$ K/W.

The calculation above is for an application at worst-case (stereo) sine-wave output signals. In practice music signals will be applied, which decreases the maximum power dissipation to approximately half of the sine-wave power dissipation (see Section 8.2.2). This allows for the use of a smaller heatsink:

$P \times R_{th(tot)} = 100$ °C

$R_{th(tot)} = 100/(0.5 \times 8) = 25$ K/W

$R_{th(h-a)} = R_{th(tot)} - R_{th(j-mb)} = 25 - 4.5 = 20.5$ K/W.

To increase the lifetime of the IC, $T_{j(max)}$ should be reduced to 125 °C. This requires a heatsink of approximately 14 K/W for music signals.

15. Test information

15.1 Quality information

The *"General Quality Specification for Integrated Circuits, SNW-FQ-611D"* is applicable (ordering code 9397 750 05459).

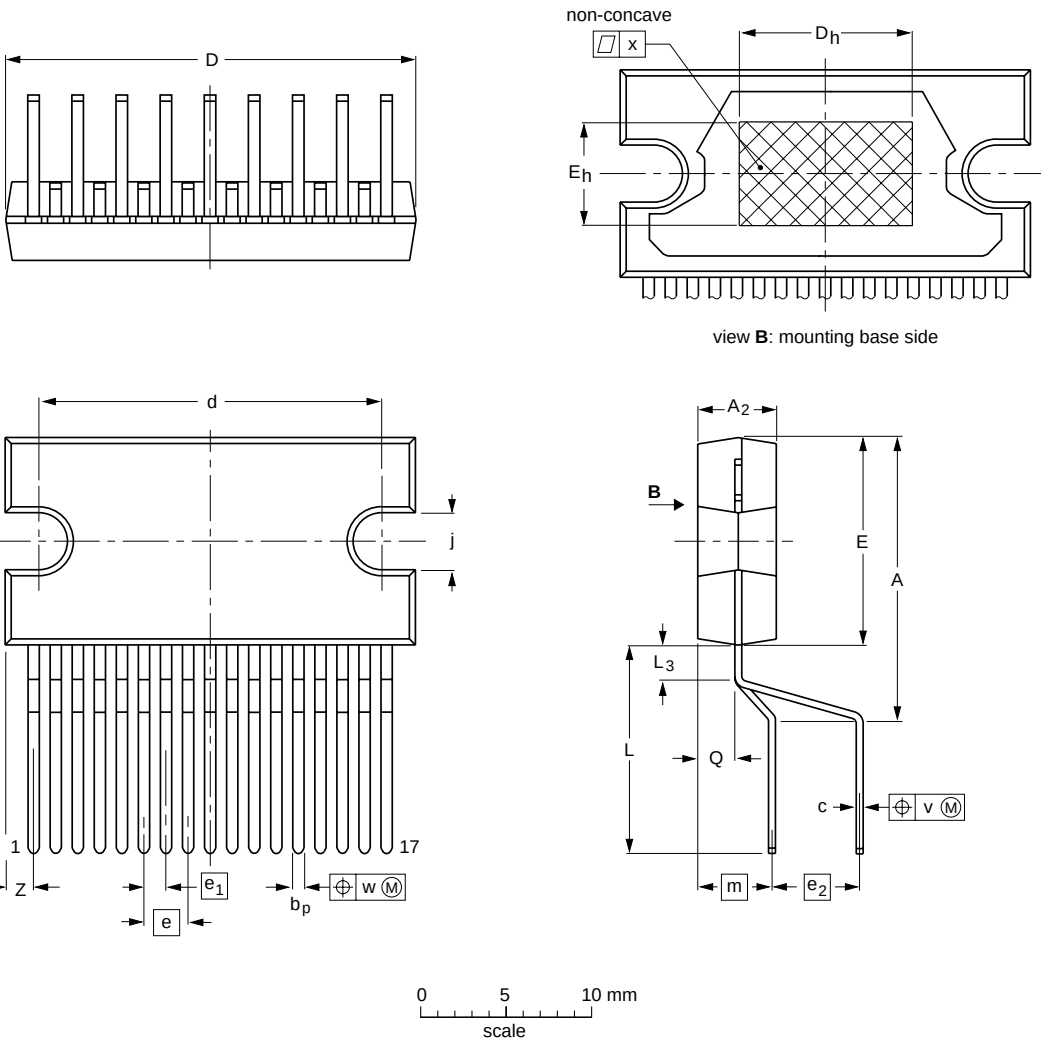
15.1.1 Test conditions

T_{amb} = 25 °C; V_{CC} = 12 V; f = 1 kHz; R_L = 8 Ω; audio pass band 22 Hz to 22 kHz; unless otherwise specified.

Remark: In the graphs as function of frequency no bandpass filter was applied; see Figure 9 and 13.

16. Package outline

DBS17P: plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm) **SOT243-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.4	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.4	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT243-1						~~97-12-16~~ 99-12-17

Fig 17. DBS17P package outline.

17. Soldering

17.1 Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

17.2 Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

17.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

17.4 Package related soldering information

Table 10: Suitability of through-hole mount IC packages for dipping and wave soldering methods

Package	Soldering method	
	Dipping	Wave
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable[1]

[1] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

18. Revision history

Table 11: Revision history

Rev	Date	CPCN	Description
01	20020301	-	Product data (9397 750 09433)

19. Data sheet status

Data sheet status[1]	Product status[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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