



STGE50NC60WD

N-channel 50A - 600V - ISOTOP
Ultra fast switching PowerMESH™ IGBT

Features

Type	V _{CES}	V _{CE(sat)} (Max) @25°C	I _C @100°C
STGE50NC60WD	600V	2.5V	50A

- High current capability
- High frequency operation
- Low C_{RES}/C_{IES} ratio (no cross-conduction susceptibility)
- Very soft ultra fast recovery antiparallel diode

Description

Using the latest high voltage technology based on a patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, the PowerMESH™ IGBTs, with outstanding performances. The suffix "W" identifies a family optimized for very high frequency applications.

Applications

- Very high frequency inverters
- HF, SMPS and PFC in both hard switching and resonant topologies
- UPS
- Motor drivers
- Welding

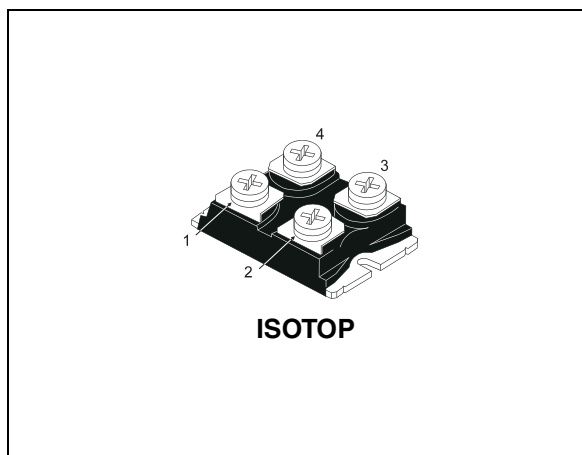


Figure 1. Internal schematic diagram

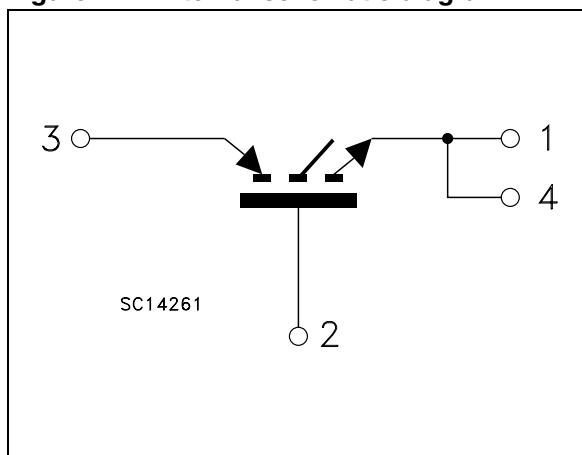


Table 1. Device summary

Order code	Marking	Package	Packaging
STGE50NC60WD	GE50NC60WD	ISOTOP	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage ($s_{GS} = 0$)	600	V
$I_C^{(1)}$	Collector current (continuous) at $T_C = 25^\circ\text{C}$	100	A
$I_C^{(1)}$	Collector current (continuous) at $T_C = 100^\circ\text{C}$	50	A
$I_{CL}^{(2)}$	Collector current (pulsed)	250	A
V_{GE}	Gate-emitter voltage	± 20	V
I_F	Diode RMS forward current at $T_C = 25^\circ\text{C}$	30	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	260	W
T_{stg}	Storage temperature	-55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature		

1. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{JMAX} - T_C}{R_{THJ-C} \times V_{CESAT(MAX)}(T_C, I_C)}$$

2. Pulse width limited by T_{Jmax}

Table 3. Thermal resistance

Symbol	Parameter	Min	Typ	Max	Unit
$R_{thj-case}$	Thermal resistance junction-case (IGBT)	--	--	0.48	$^\circ\text{C/W}$
$R_{thj-case}$	Thermal resistance junction-case (diode)	--	--	1.5	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-amb	--	--	50	$^\circ\text{C/W}$

2 Electrical characteristics

($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	$I_C = 1\text{ mA}$, $V_{GE} = 0$	600			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE} = 15\text{ V}$, $I_C = 40\text{ A}$ $V_{GE} = 15\text{ V}$, $I_C = 40\text{ A}$, $T_C = 125\text{ }^{\circ}\text{C}$		2.1 1.9	2.6	V V
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}$, $I_C = 250\text{ }\mu\text{A}$	3.75		5.75	V
I_{CES}	Collector cut-off current ($V_{GE} = 0$)	$V_{CE} = \text{Max rating}$, $T_C = 25\text{ }^{\circ}\text{C}$ $V_{CE} = \text{Max rating}$, $T_C = 125\text{ }^{\circ}\text{C}$			500 5	μA mA
I_{GES}	Gate-emitter leakage current ($V_{CE} = 0$)	$V_{GE} = \pm 20\text{ V}$, $V_{CE} = 0$			± 100	nA
g_{fs}	Forward transconductance	$V_{CE} = 15\text{ V}$, $I_C = 40\text{ A}$		25		S

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies}	Input capacitance	$V_{CE} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GE} = 0$		4700		pF
C_{oes}	Output capacitance			410		pF
C_{res}	Reverse transfer capacitance			90		pF
Q_g	Total gate charge	$V_{CE} = 390\text{ V}$, $I_C = 40\text{ A}$, $V_{GE} = 15\text{ V}$, Figure 17		195		nC
Q_{ge}	Gate-emitter charge			32		nC
Q_{gc}	Gate-collector charge			82		nC

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 390V, I_C = 40A$		52		ns
t_r	Current rise time	$R_G = 3.3\Omega, V_{GE} = 15V,$		17		ns
$(di/dt)_{on}$	Turn-on current slope	<i>Figure 16, Figure 18</i>		2400		A/ μs
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 390V, I_C = 40A$		50		ns
t_r	Current rise time	$R_G = 3.3\Omega, V_{GE} = 15V,$		19		ns
$(di/dt)_{on}$	Turn-on current slope	$T_j = 125^\circ C$ <i>Figure 16, Figure 18</i>		2020		A/ μs
$t_{r(Voff)}$	Off voltage rise time	$V_{CC} = 390V, I_C = 40A$		31		ns
$t_{d(Voff)}$	Turn-off delay time	$R_G = 3.3\Omega, V_{GE} = 15V,$		240		ns
t_f	Current fall time	<i>Figure 16, Figure 18</i>		35		ns
$t_{r(Voff)}$	Off voltage rise time	$V_{CC} = 390V, I_C = 40A$		59		ns
$t_{d(Voff)}$	Turn-off delay time	$R_G = 3.3\Omega, V_{GE} = 15V,$		280		ns
t_f	Current fall time	$T_j = 125^\circ C$ <i>Figure 16, Figure 18</i>		63		ns

Table 7. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$E_{on}^{(1)}$	Turn-on switching losses	$V_{CC} = 390V, I_C = 40A$		365	470	μJ
$E_{off}^{(2)}$	Turn-off switching losses	$R_G = 3.3\Omega, V_{GE} = 15V,$		560	790	μJ
E_{ts}	Total switching losses	<i>Figure 18</i>		925	1260	μJ
$E_{on}^{(1)}$	Turn-on switching losses	$V_{CC} = 390V, I_C = 40A$		635		μJ
$E_{off}^{(2)}$	Turn-off switching losses	$R_G = 3.3\Omega, V_{GE} = 15V,$		910		μJ
E_{ts}	Total switching losses	$T_j = 125^\circ C$ <i>Figure 18</i>		1545		μJ

1. E_{on} is the turn-on losses when a typical diode is used in the test circuit in *Figure 18*. If the IGBT is offered in a package with a co-pak diode, the co-pak diode is used as external diode. IGBTs & Diode are at the same temperature ($25^\circ C$ and $125^\circ C$)
2. Turn-off losses include also the tail of the collector current

Table 8. Collector-emitter diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_f	Forward on-voltage	$I_f = 15\text{A}$		1.5	2.9	V
		$I_f = 15\text{A}, T_j = 125^\circ\text{C}$		1.2		V
		$I_f = 40\text{A}, T_j = 125^\circ\text{C}$		1.35		V
t_{rr}	Reverse recovery time	$I_f = 40\text{A}, V_R = 50\text{V},$ $T_j = 25^\circ\text{C}, di/dt = 100\text{ A}/\mu\text{s}$ Figure 19		55		ns
Q_{rr}	Reverse recovery charge			100		nC
I_{rrm}	Reverse recovery current			3.6		A
t_{rr}	Reverse recovery time	$I_f = 40\text{A}, V_R = 50\text{V},$ $T_j = 125^\circ\text{C}, di/dt = 100\text{A}/\mu\text{s}$ Figure 19		164		ns
Q_{rr}	Reverse recovery charge			525		nC
I_{rrm}	Reverse recovery current			6.4		A

2.1 Electrical characteristics (curves)

Figure 2. Output characteristics

Figure 3. Transfer characteristics

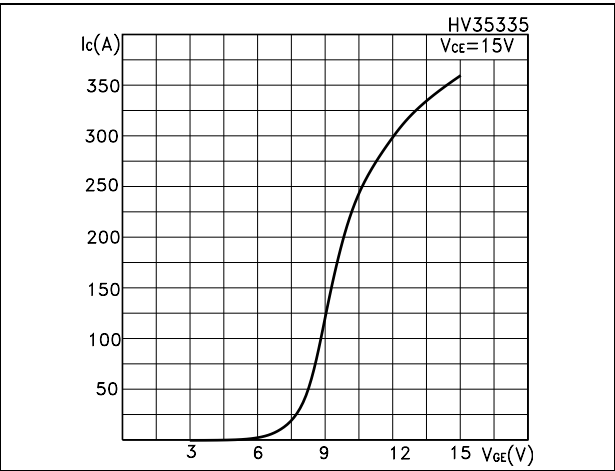
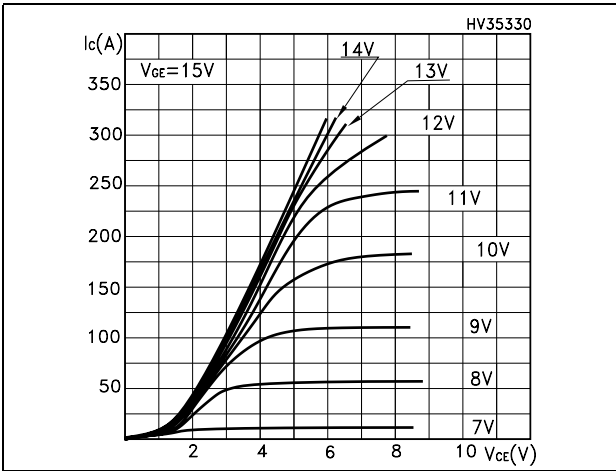


Figure 4. Transconductance

Figure 5. Collector-emitter on voltage vs temperature

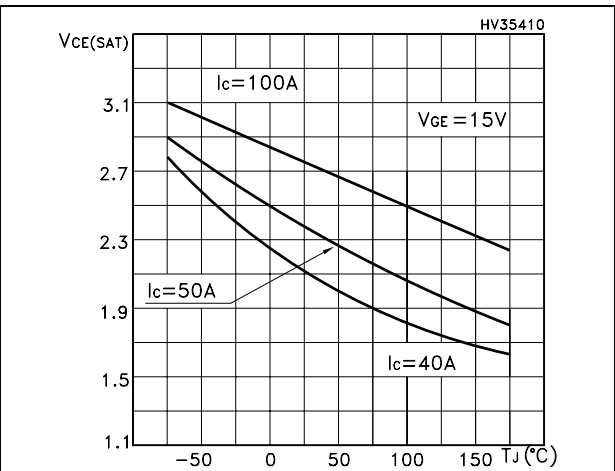
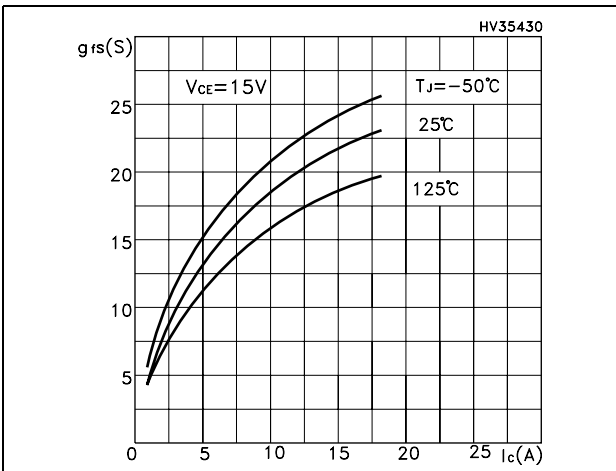


Figure 6. Gate charge vs gate-source voltage

Figure 7. Capacitance variations

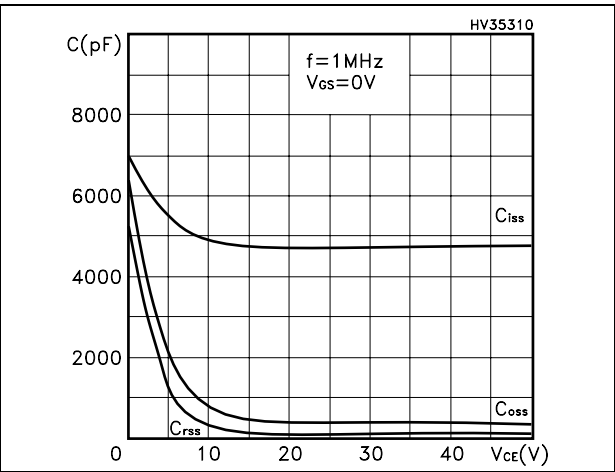
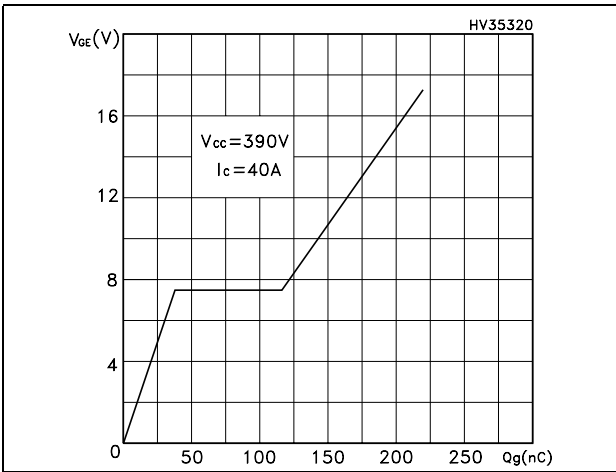


Figure 8. Normalized gate threshold voltage vs temperature

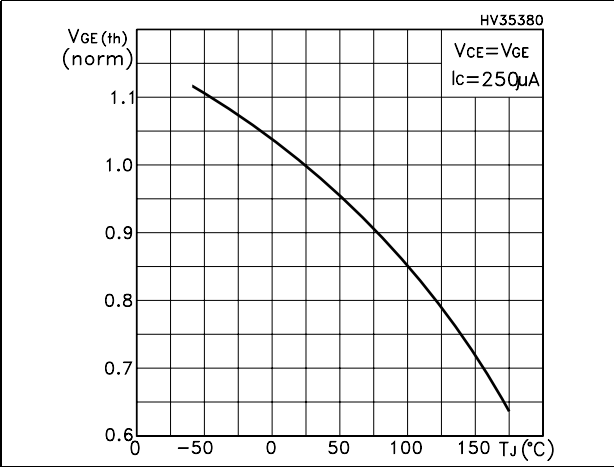


Figure 9. Collector-emitter on voltage vs collector current

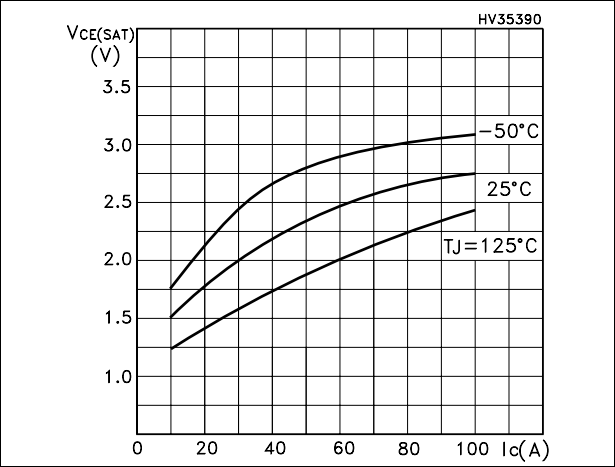


Figure 10. Normalized breakdown voltage vs temperature

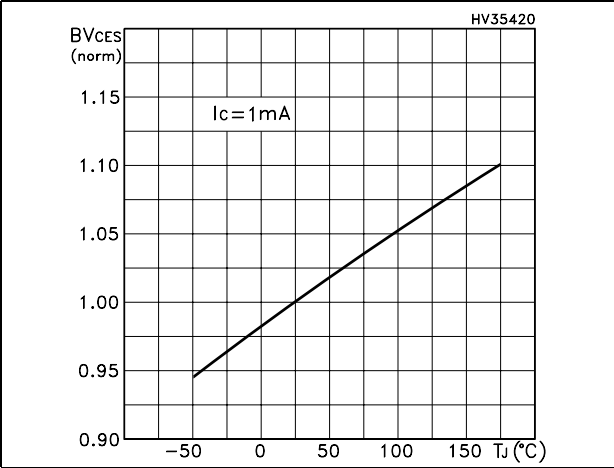


Figure 11. Switching losses vs temperature

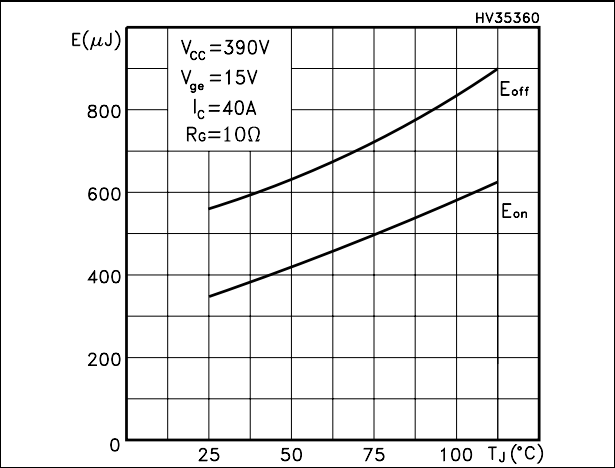


Figure 12. Switching losses vs gate resistance

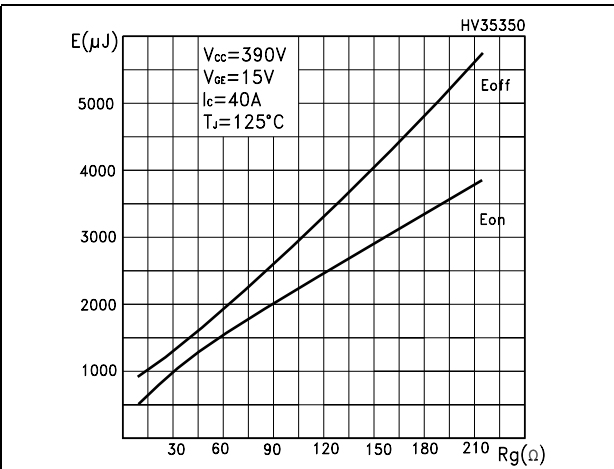


Figure 13. Switching losses vs collector current

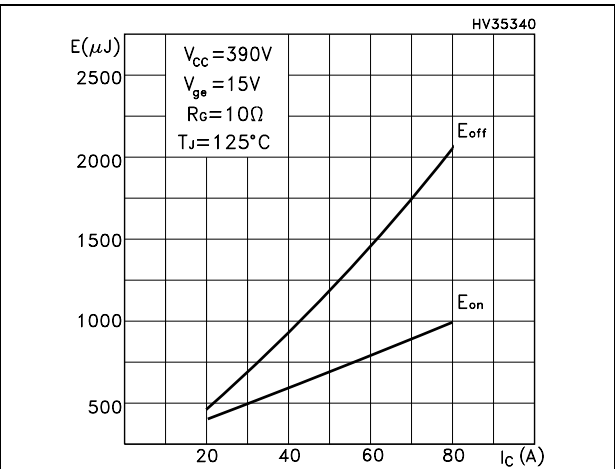


Figure 14. Turn-off SOA

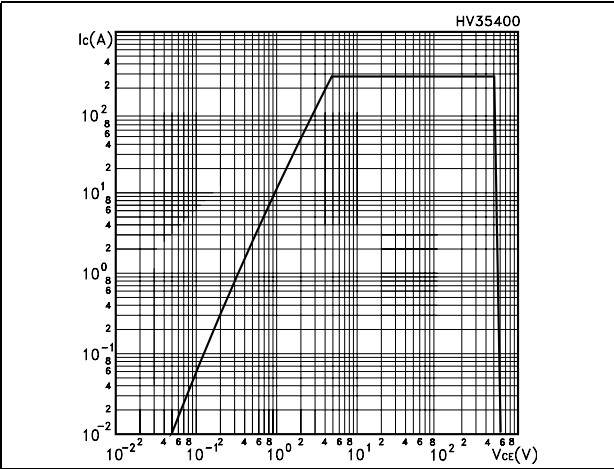
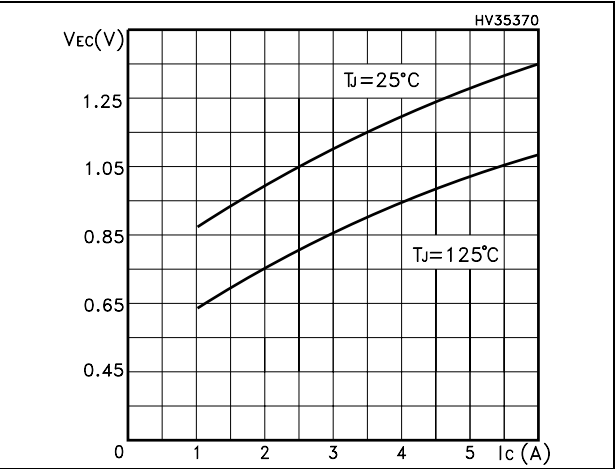


Figure 15. Emitter-collector diode characteristics



3 Test circuit

Figure 16. Test circuit for inductive load switching

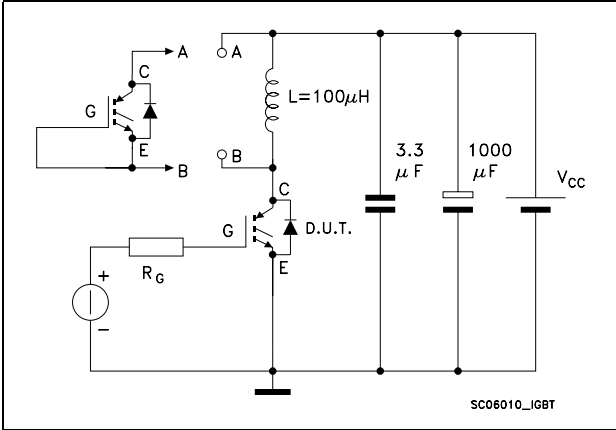


Figure 17. Gate charge test circuit

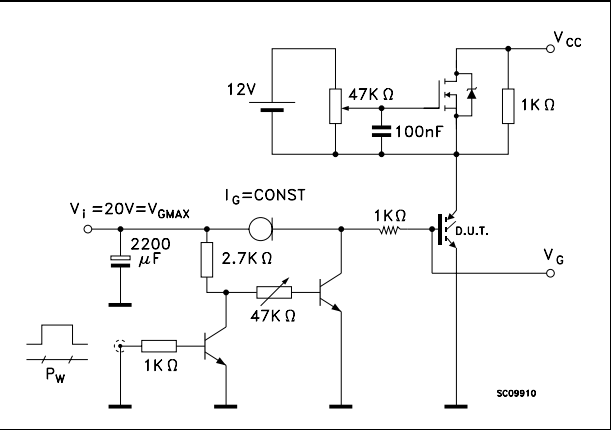


Figure 18. Switching waveform

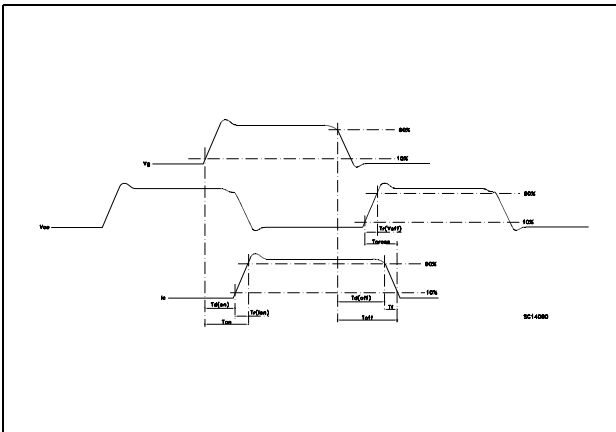
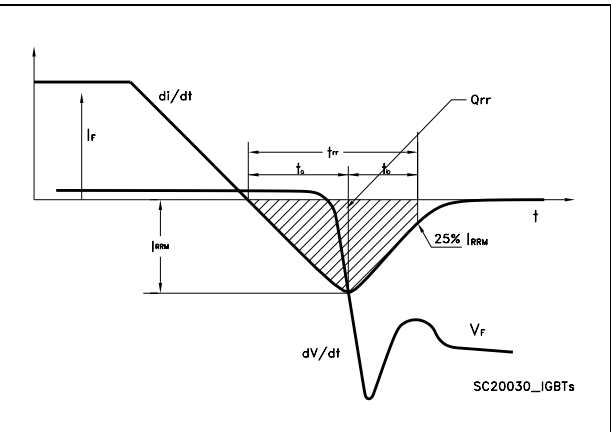


Figure 19. Diode recovery time waveform

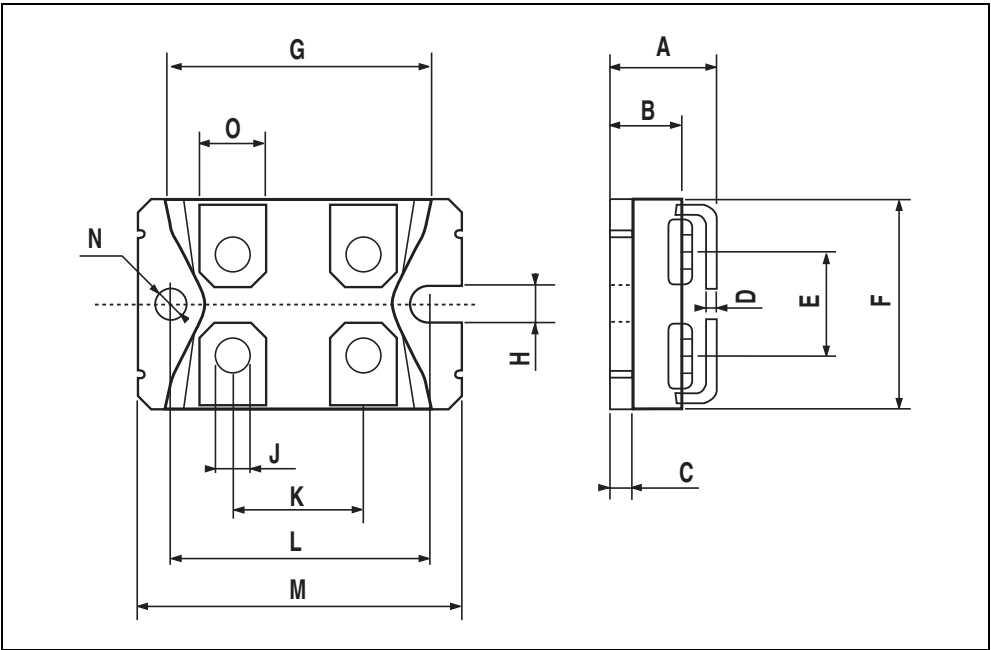


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

ISOTOP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	11.8		12.2	0.466		0.480
B	8.9		9.1	0.350		0.358
C	1.95		2.05	0.076		0.080
D	0.75		0.85	0.029		0.033
E	12.6		12.8	0.496		0.503
F	25.15		25.5	0.990		1.003
G	31.5		31.7	1.240		1.248
H	4			0.157		
J	4.1		4.3	0.161		0.169
K	14.9		15.1	0.586		0.594
L	30.1		30.3	1.185		1.193
M	37.8		38.2	1.488		1.503
N	4			0.157		
O	7.8		8.2	0.307		0.322



5 Revision History

Table 9. Revision history

Date	Revision	Changes
07-May-2006	1	First release
24-Jul-2007	2	New Figure 1: Internal schematic diagram

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