CY7C4122KV13/CY7C4142KV13

144-Mbit QDR™-IV XP SRAM

Features

- 144-Mbit density (8 M × 18, 4 M × 36)
- Total Random Transaction Rate[1] of 2132 MT/s
- Maximum operating frequency of 1066 MHz
- Read latency of 8.0 clock cycles and write latency of 5.0 clock cycles
- Eight-bank architecture enables one access per bank per cycle
- Two-word burst on all accesses
- Dual independent bidirectional data ports
  - Double data rate (DDR) data ports
  - Supports concurrent read/write transactions on both ports
- Single address port used to control both data ports
  - DDR address signaling
- Single data rate (SDR) control signaling
- High-speed transceiver logic (HSTL) and stub series terminated logic (SSTL) compatible signaling (JESD8-16A compliant)
  - I/O V_{DDQ} = 1.2 V ± 50 mV or 1.25 V ± 50 mV
- Pseudo open drain (POD) signaling (JESD8-24 compliant)
  - I/O V_{DDQ} = 1.1 V ± 50 mV or 1.2 V ± 50 mV
- Core voltage
  - V_{DD} = 1.3 V ± 40 mV
- On-die termination (ODT)
  - Programmable for clock, address/command, and data inputs
- Internal self-calibration of output impedance through ZQ pin
- Bus inversion to reduce switching noise and power
  - Programmable on/off for address and data
- Address bus parity error protection
- Training sequence for per-bit deskew
- On-chip error correction code (ECC) to reduce soft error rate (SER)
- JTAG 1149.1 test access port (JESD8-26 compliant)
  - 1.3 V LVCMOS signaling
- Available in 361-ball FCBGA Pb-free package (21 × 21 mm)

Configurations

CY7C4122KV13 – 8 M × 18

CY7C4142KV13 – 4 M × 36

Functional Description

The QDR-IV XP (Xtreme Performance) SRAM is a high-performance memory device optimized to maximize the number of random transactions per second by the use of two independent bidirectional data ports.

These ports are equipped with DDR interfaces and designated as port A and port B respectively. Accesses to these two data ports are concurrent and independent of each other. Access to each port is through a common address bus running at DDR. The control signals are running at SDR and determine if a read or write should be performed.

There are three types of differential clocks:

- (CK, CK#) for address and command clocking
- (DKA, DKA#, DKB, DKB#) for data input clocking
- (QKA, QKA#, QKB, QKB#) for data output clocking

Addresses for port A are latched on the rising edge of the input clock (CK), and addresses for port B are latched on the falling edge of the input clock (CK).

This QDR-IV XP SRAM is internally partitioned into eight internal banks. Each bank can be accessed once for every clock cycle, enabling the SRAM to operate at high frequencies.

The QDR-IV XP SRAM device is offered in a two-word burst option and is available in × 18 and × 36 bus width configurations.

For an ×18 bus-width configuration, there are 22 address bits, and for an ×36 bus width configuration, there are 21 address bits respectively.

An on-chip ECC circuitry detects and corrects all single-bit memory errors including those induced by soft error events, such as cosmic rays and alpha particles. The resulting SER of these devices is expected to be less than 0.01 FITs/Mb, a four-order-of-magnitude improvement over previous generation SRAMs.

For a complete list of related resources, click here.

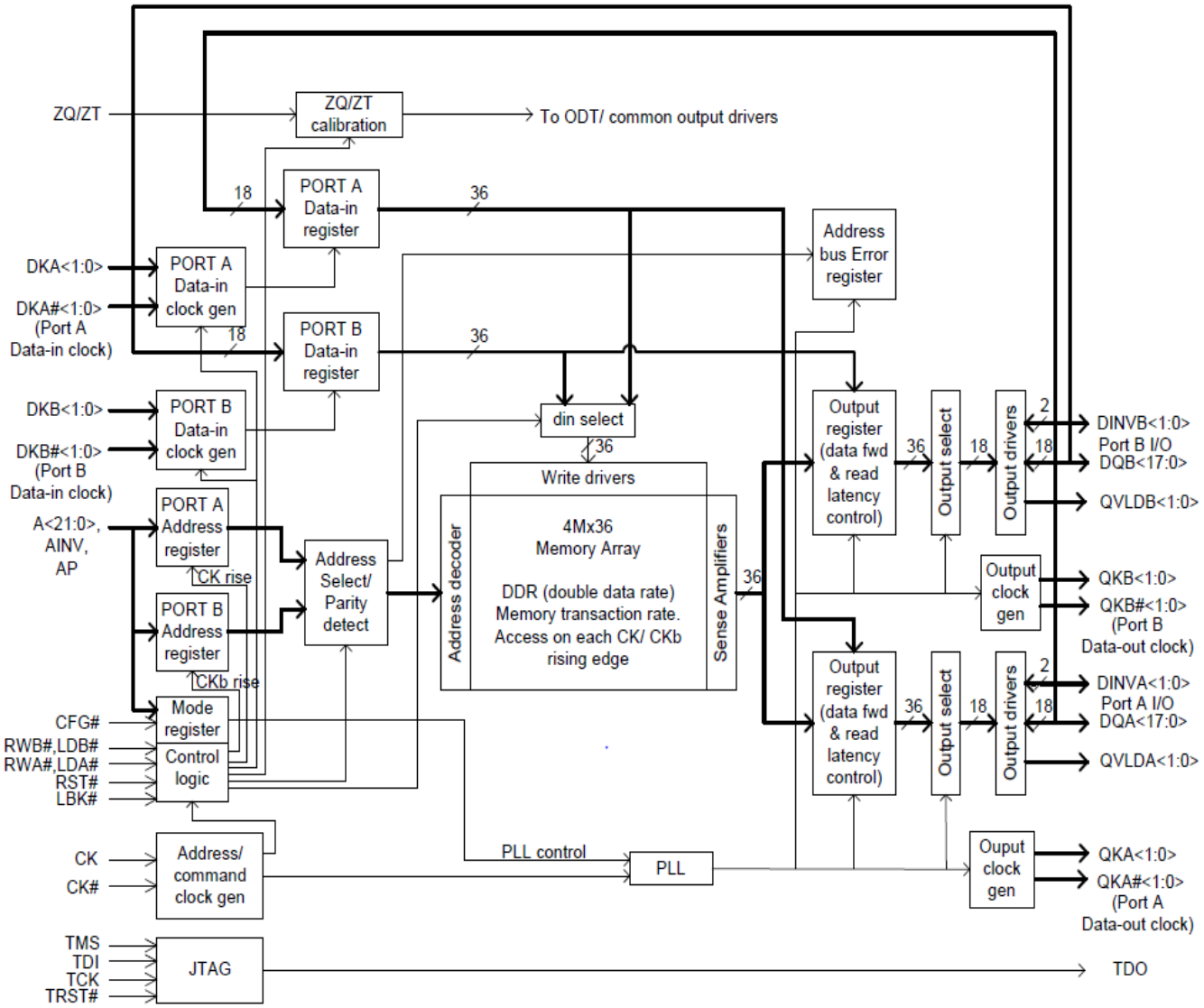
Selection Guide

Description		QDR-IV 2132 (MT/s)	QDR-IV 1866 (MT/s)	Unit
Maximum operating frequency		1066	933	MHz
Maximum operating current	×18	4100	3400	mA
	×36	4500	4000	

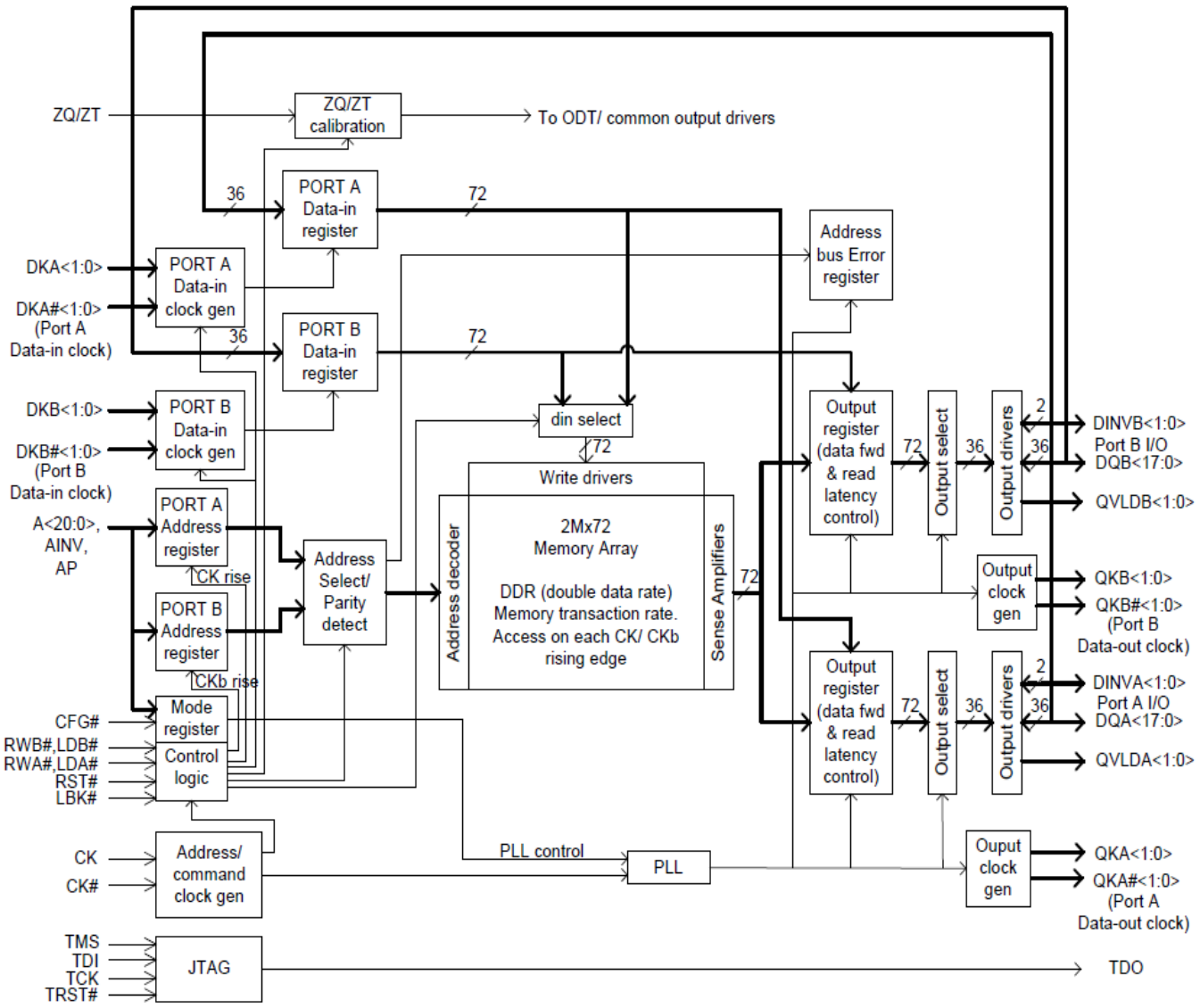
Note

1. RTR (Random Transaction Rate) is defined as the number of fully random memory accesses (reads or writes) that can be performed on the memory. RTR is measured in million transactions per second.

Logic Block Diagram – CY7C4122KV13



Logic Block Diagram – CY7C4142KV13



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Pin Configurations

Figure 1. 361-ball FCBGA pinout

CY7C4122KV13 (8 M × 18)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	VSS	VDDQ	VSS	DQA 5	VDDQ	DQA 7	VSS	DQA 8	VSS	LBK0#	VSS	DQA 17	VSS	DQA 16	VDDQ	DQA 14	VSS	VDDQ	VSS
B	VDD	DNU	VDDQ	VSS	DNU	VDDQ	DQA 1	VDDQ	VDD	LBK1#	VDD	VDDQ	DQA 10	VDDQ	DNU	VSS	VDDQ	DNU	VDD
C	VSS	VDDQ	QvId A0	QKA0	VSS	DQA 2	VDDQ	DQA 0	VSS	VDDQ	VSS	DQA 9	VDDQ	DQA 11	VSS	QKA1	QvId A1	VDDQ	VSS
D	VDD	VSS	QKA0#	VDDQ	DQA 3	VSS	DQA 4	DINV A0	VDD	CFG#	VDD	DINV A1	DQA 13	VSS	DQA 12	VDDQ	QKA1#	VSS	VDD
E	VSS	DNU	VDDQ	VREF	VSS	VDDQ	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDDQ	VSS	VREF	VDDQ	DNU	VSS
F	VDDQ	VSS	DKA0#	DKA0	DQA 6	VSS	VDDQ	A13	VDD	A0	VDD	A14	VDDQ	VSS	DQA 15	DKA1	DKA1#	VSS	VDDQ
G	VSS	DNU	VSS	DNU	VDDQ	VDD	A3	VSS	A21 144M	A1	A22 288M	VSS	A4	VDD	VDDQ	DNU	VSS	DNU	VSS
H	VDD	VSS	DNU	VSS	DNU	VSS	VSS	LDA#	VDDQ	RWA#	VDDQ	LDB#	VSS	VSS	DNU	VSS	DNU	VSS	VDD
J	VSS	DNU	VDDQ	DNU	VSS	VDD	A5	VSS	A19 36M	CK	A20 72M	VSS	A6	VDD	VSS	DNU	VDDQ	DNU	VSS
K	TDI	TRST#	TCK	VSS	VDD	VSS	VDD	VREF	VDDQ	CK#	VDDQ	VREF	VDD	VSS	VDD	VSS	TMS	RST#	TDO
L	VSS	DNU	VDDQ	DNU	VSS	VDD	A7	VDD	A17	RWB#	A18 18M	VDD	A8	VDD	VSS	DNU	VDDQ	DNU	VSS
M	VDD	VSS	DNU	VSS	DNU	VSS	VSS	A11	VDDQ	AINV	VDDQ	A12	VSS	VSS	DNU	VSS	DNU	VSS	VDD
N	VSS	DNU	VSS	DNU	VDDQ	VDD	A9	VSS	A23 576M	A2	A24 1152M	VSS	A10	VDD	VDDQ	DNU	VSS	DNU	VSS
P	VDDQ	VSS	DKB0#	DKB0	DQB 6	VSS	VDDQ	A15	VDD	AP	VDD	A16	VDDQ	VSS	DQB 15	DKB1	DKB1#	VSS	VDDQ
R	VSS	DNU	VDDQ	VREF	VSS	VDDQ	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDDQ	VSS	VREF	VDDQ	DNU	VSS
T	VDD	VSS	QKB0#	VDDQ	DQB 3	VSS	DQB 4	DINV B0	VDD	DNU	VDD	DINV B1	DQB 13	VSS	DQB 12	VDDQ	QKB1#	VSS	VDD
U	VSS	VDDQ	QvId B0	QKB0	VSS	DQB 2	VDDQ	DQB 0	VSS	VDDQ	VSS	DQB 9	VDDQ	DQB 11	VSS	QKB1	QvId B1	VDDQ	VSS
V	VDD	DNU	VDDQ	VSS	DNU	VDDQ	DQB 1	VDDQ	VDD	PE#	VDD	VDDQ	DQB 10	VDDQ	DNU	VSS	VDDQ	DNU	VDD
W	VSS	VDDQ	VSS	DQB 5	VDDQ	DQB 7	VSS	DQB 8	VSS	ZQ/ZT	VSS	DQB 17	VSS	DQB 16	VDDQ	DQB 14	VSS	VDDQ	VSS

Pin Configurations (continued)

Figure 2. 361-ball FCBGA pinout

CY7C4142KV13 (4 M × 36)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	VSS	VDDQ	VSS	DQA 5	VDDQ	DQA 7	VSS	DQA 8	VSS	LBK0#	VSS	DQA 26	VSS	DQA 25	VDDQ	DQA 23	VSS	VDDQ	VSS
B	VDD	DQA 13	VDDQ	VSS	DQA 17	VDDQ	DQA 1	VDDQ	VDD	LBK1#	VDD	VDDQ	DQA 19	VDDQ	DQA 35	VSS	VDDQ	DQA 31	VDD
C	VSS	VDDQ	QvId A0	QKA0	VSS	DQA 2	VDDQ	DQA 0	VSS	VDDQ	VSS	DQA 18	VDDQ	DQA 20	VSS	QKA1	QvId A1	VDDQ	VSS
D	VDD	VSS	QKA0#	VDDQ	DQA 3	VSS	DQA 4	DINV A0	VDD	CFG#	VDD	DINV A1	DQA 22	VSS	DQA 21	VDDQ	QKA1#	VSS	VDD
E	VSS	DQA 14	VDDQ	VREF	VSS	VDDQ	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDDQ	VSS	VREF	VDDQ	DQA 32	VSS
F	VDDQ	VSS	DKA0#	DKA0	DQA 6	VSS	VDDQ	A13	VDD	A0	VDD	A14	VDDQ	VSS	DQA 24	DKA1	DKA1#	VSS	VDDQ
G	VSS	DQA 15	VSS	DQA 16	VDDQ	VDD	A3	VSS	A21 288M	A1	A22 576M	VSS	A4	VDD	VDDQ	DQA 34	VSS	DQA 33	VSS
H	VDD	VSS	DQA 9	VSS	DQA 10	VSS	VSS	LDA#	VDDQ	RWA#	VDDQ	LDB#	VSS	VSS	DQA 28	VSS	DQA 27	VSS	VDD
J	VSS	DQA 11	VDDQ	DQA 12	VSS	VDD	A5	VSS	A19 72M	CK	A20 144M	VSS	A6	VDD	VSS	DQA 30	VDDQ	DQA 29	VSS
K	TDI	TRST#	TCK	VSS	VDD	VSS	VDD	VREF	VDDQ	CK#	VDDQ	VREF	VDD	VSS	VDD	VSS	TMS	RST#	TDO
L	VSS	DQB 11	VDDQ	DQB 12	VSS	VDD	A7	VDD	A17	RWB#	A18 36M	VDD	A8	VDD	VSS	DQB 30	VDDQ	DQB 29	VSS
M	VDD	VSS	DQB 9	VSS	DQB 10	VSS	VSS	A11	VDDQ	AINV	VDDQ	A12	VSS	VSS	DQB 28	VSS	DQB 27	VSS	VDD
N	VSS	DQB 15	VSS	DQB 16	VDDQ	VDD	A9	VSS	A23 1152M	A2	A24 2304M	VSS	A10	VDD	VDDQ	DQB 34	VSS	DQB 33	VSS
P	VDDQ	VSS	DKB0#	DKB0	DQB 6	VSS	VDDQ	A15	VDD	AP	VDD	A16	VDDQ	VSS	DQB 24	DKB1	DKB1#	VSS	VDDQ
R	VSS	DQB 14	VDDQ	VREF	VSS	VDDQ	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDDQ	VSS	VREF	VDDQ	DQB 32	VSS
T	VDD	VSS	QKB0#	VDDQ	DQB 3	VSS	DQB 4	DINV B0	VDD	DNU	VDD	DINV B1	DQB 22	VSS	DQB 21	VDDQ	QKB1#	VSS	VDD
U	VSS	VDDQ	QvId B0	QKB0	VSS	DQB 2	VDDQ	DQB 0	VSS	VDDQ	VSS	DQB 18	VDDQ	DQB 20	VSS	QKB1	QvId B1	VDDQ	VSS
V	VDD	DQB 13	VDDQ	VSS	DQB 17	VDDQ	DQB 1	VDDQ	VDD	PE#	VDD	VDDQ	DQB 19	VDDQ	DQB 35	VSS	VDDQ	DQB 31	VDD
W	VSS	VDDQ	VSS	DQB 5	VDDQ	DQB 7	VSS	DQB 8	VSS	ZQ/ZT	VSS	DQB 26	VSS	DQB 25	VDDQ	DQB 23	VSS	VDDQ	VSS

Pin Definitions

Pin Name	I/Os	Pin Description
CK, CK#	Input Clock	**Address/Command Input Clock**. CK and CK# are differential clock inputs. All control and address input signals are sampled on both the rising and falling edges of CK. The rising edge of CK samples the control and address inputs for port A, while the falling edge of CK samples the control and address inputs for port B. CK# is 180 degrees out of phase with CK.

A[x:0]	Input	**Address Inputs**. Sampled on the rising edge of both CK and CK# clocks during active read and write operations. These address inputs are used for read and write operations on both ports. The lower three address pins (A0, A1, and A2) select the bank that will be accessed. These address inputs are also known as bank address pins.
		For (×36) data width - Address inputs A[20:0] are used and A[24:21] are reserved.
		For (×18) data width - Address inputs A[21:0] are used and A[24:22] are reserved.
		The reserved address inputs are No Connects and may be tied high, tied low, or left floating.

AP	Input	**Address Parity Input**. Used to provide even parity across the address pins.
		For (×36) data width - AP covers address inputs A[20:0]
		For (×18) data width - AP covers address inputs A[21:0]

PE#	Output	**Address Parity Error Flag**. Asserted LOW when address parity error is detected. Once asserted, PE# will remain LOW until cleared by a Configuration Register command.

AINV	Input	**Address Inversion Pin for Address and Address Parity Inputs**.
		For (×36) data width - AINV covers address inputs A[20:0] and the address parity input (AP).
		For (×18) data width - AINV covers address inputs A[21:0] and the address parity input (AP).

DKA[1:0], DKA#[1:0], DKB[1:0], DKB#[1:0]	Input	**Data Input Clock**. DKA[0] / DKA#[0] controls the DQA[17:0] inputs for ×36 configuration and DQA[8:0] inputs for ×18 configuration respectively DKA[1] / DKA#[1] controls the DQA[35:18] inputs for ×36 configuration and DQA[17:9] inputs for ×18 configuration respectively DKB[0] / DKB#[0] controls the DQB[17:0] inputs for ×36 configuration and DQB[8:0] inputs for ×18 configuration respectively DKB[1] / DKB#[1] controls the DQB[35:18] inputs for ×36 configuration and DQB[17:9] inputs for ×18 configuration respectively
QKA[1:0], QKA#[1:0], QKB[1:0], QKB#[1:0]	Output	**Data Output Clock**. QKA[0] / QKA#[0] controls the DQA[17:0] outputs for ×36 configuration and DQA[8:0] outputs for ×18 configuration respectively QKA[1] / QKA#[1] controls the DQA[35:18] outputs for ×36 configuration and DQA[17:9] outputs for ×18 configuration respectively QKB[0] / QKB#[0] controls the DQB[17:0] outputs for ×36 configuration and DQB[8:0] outputs for ×18 configuration respectively QKB[1] / QKB#[1] controls the DQB[35:18] outputs for ×36 configuration and DQB[17:9] outputs for ×18 configuration respectively

DQA[x:0], DQB[x:0]	Input/Output	**Data Input/Output**.Bidirectional data bus.
		For (×36) data width – $DQA_{[35:0]}$; $DQB_{[35:0]}$
		For (×18) data width – $DQA_{[17:0]}$; $DQB_{[17:0]}$

DINVA[1:0], DINVB[1:0]	Input/Output	**Data Inversion Pin for DQ Data Bus**. DINVA[0] covers DQA[17:0] for ×36 configuration and DQA[8:0] for ×18 configuration respectively DINVA[1] covers DQA[35:18] for ×36 configuration and DQA[17:9] for ×18 configuration respectively DINVB[0] covers DQB[17:0] for ×36 configuration and DQB[8:0] for ×18 configuration respectively DINVB[1] covers DQB[35:18] for ×36 configuration and DQB[17:9] for ×18 configuration respectively
LDA#, LDB#	Input	**Synchronous Load Input**. LDA# is sampled on the rising edge of the CK clock, while LDB# is sampled on the falling edge of CK clock. LDA# enables commands for data port A and LDB# enables commands for data port B. LDx# enables the commands when LDx# is LOW and disables the commands when LDx# is HIGH. When the command is disabled, new commands are ignored, but internal operations continue.

Pin Definitions (continued)

Pin Name	I/Os	Pin Description
RWA#, RWB#	Input	**Synchronous Read/Write Input**. RWA# input is sampled on the rising edge of the CK clock, while RWB# is sampled on the falling edge of the CK clock. The RWA# input is used in conjunction with the LDA# input to select a Read or Write Operation. Similarly, the RWB# input is used in conjunction with the LDB# input to select a read or write operation.
QVLDA[1:0], QVLDB[1:0]	Output	**Output Data Valid Indicator**. The QVLD pin indicates valid output data. QVLD is edge-aligned with QKx and QKx#.
ZQ/ZT	Input	**Output Impedance Matching Input**. This input is used to tune the device outputs to the system data bus impedance.
CFG#	Input	**Configuration bit**. This pin is used to configure different mode registers.
RST#	Input	**Active Low Asynchronous RST**. This pin is active when RST# is LOW and inactive when RST# is HIGH. The RST# pin has an internal pull-down resistor.
LBK0#, LBK1#	Input	**Loopback mode for control and address/command/clock deskewing**.
TMS	Input	**Test Mode Select Input pin for JTAG**. This pin may be left unconnected if the JTAG function is not used in the circuit.
TDI	Input	**Test Data Input pin for JTAG**. This pin may be left unconnected if the JTAG function is not used in the circuit.
TCK	Input	**Test Clock Input pin for JTAG**. This pin must be tied to VSS if the JTAG function is not used in the circuit.
TDO	Output	**Test Data Output pin for JTAG**. This pin may be left unconnected if the JTAG function is not used in the circuit.
TRST#	Input	**Test Reset Input pin for JTAG**. This pin must be tied to VDD if the JTAG function is not used in the system. TRST# input is applicable only in JTAG mode.
DNU	N/A	**Do Not Use**. Do not use pins.
VREF	Reference	**Reference Voltage Input**. Static input used to set the reference level for inputs, outputs, and AC measurement points.
VDD	Power	**Power Supply Inputs to the Core of the Device**.
VDDQ	Power	**Power Supply Inputs for the Outputs of the Device**.
VSS	Ground	**Ground for the Device**.

Functional Overview

The QDR-IV XP SRAM is a two-word burst synchronous SRAM equipped with dual independent bidirectional data ports. The following sections describe the device operation.

Clocking

There are three groups of clock signals: CK/CK#, DKx/DKx#, and QKx/QKx#, where x can be A or B, referring to the respective ports.

The CK/CK# clock is associated with the address and control pins: A[24:0], LDA#, LDB#, RWA#, RWB#. The CK/CK# transitions are centered with respect to the address and control signal transitions.

The DKx/DKx# clocks are associated with write data. The DKx/DKx# clocks are used as source-centered clocks for the DDR DQx and DINVx pins, when acting as inputs for the write data.

The QKx/QKx# clocks are associated with read data. The QKx/QKx# clocks are used as source-synchronous clocks for the double data rate DQx and DINVx pins, when acting as outputs for the read data.

Command Cycles

The QDR-IV XP SRAM read and write commands are driven by the control inputs (LDA#, LDB#, RWA#, and RWB#) and the Address Bus.

The port A control inputs (LDA# and RWA#) are sampled at the **rising** edge of the input clock. The port B control inputs (LDB# and RWB#) are sampled at the **falling** edge of the input clock.

For port A:

When LDA# = 0 and RWA# = 1, a read operation is initiated.

When LDA# = 0 and RWA# = 0, a write operation is initiated.

The address is sampled on the **rising** edge of the input clock.

For port B:

When LDB# = 0 and RWB# = 1, a read operation is initiated.

When LDB# = 0 and RWB# = 0, a write operation is initiated.

The address is sampled on the **falling** edge of the input clock.

Read and Write Data Cycles

Read data is supplied to the DQA pins exactly eight clock cycles from the **rising** edge of the CK signal corresponding to the cycle where the read command was initiated. QVLDA is asserted one-half clock cycle prior to the first data word driven on the bus. It is deasserted one-half cycle prior to the last data word driven on the bus. Data outputs are tristated in the clock following the last data word.

Read data is supplied to the DQB pins exactly eight clock cycles from the **falling** edge of the CK signal corresponding to the cycle that the read command was initiated. QVLDB is asserted one-half clock cycle prior to the first data word driven on the bus. It is deasserted one-half cycle prior to the last data word driven on the bus. Data outputs are tristated in the clock following the last data word.

Write data is supplied to the DQA pins exactly five clock cycles from the **rising** edge of the CK signal corresponding to the cycle that the write command was initiated.

Write data is supplied to the DQB pins exactly five clock cycles from the **falling** edge of the CK signal corresponding to the cycle that the write command was initiated.

Banking Operation

The QDR-IV XP SRAM is designed with eight internal banks. The lower three address pins (A0, A1, and A2) select the bank that will be accessed. These address inputs are also known as bank address pins.

Bank Access Rules

1. On the **rising** edge of the input clock, **any bank address** may be accessed. This is the address associated with port A.
2. On the **falling** edge of the input clock, **any other bank address** may be accessed. This is the address associated with port B.
3. If port A did **not** issue a command on the **rising** edge of the input clock, then port B may access **any bank address** on the **falling** edge of the input clock.
4. From the **rising edge** of the input clock cycle to the **next rising edge** of the input clock, there is **no address restriction**. Port A may access any bank at any time.

To clarify, the banking restriction only applies in a single clock cycle. Since the port A address is sampled on the rising edge of the input clock, there are no restrictions with port A access. Because the port B address is sampled on the falling edge of the input clock, port B has the restriction that it must use a different bank than port A.

Banking Violations

1. Accesses for port A cannot cause a banking violation, only accesses to port B can.
2. If port B tries to access the same bank as port A, then the **port B access** to the memory array is **ignored**. The port A access will still occur normally.
3. If the requested cycle on port B was a write, then there will be no external indication that a banking violation occurred.
4. If the requested cycle on port B was a read, then there will be no QVLDB signal generated. Outputs will remain tristated.

Address and Data Bus Inversion

To reduce simultaneous switching noise and I/O current, QDR-IV XP SRAM provides the ability to invert all address and data pins.

The AINV pin indicates whether the address bus, A[24:0], and the address parity bit, AP, is inverted. The address bus and parity bit are considered one group. The function of the AINV is controlled by the memory controller. However, the following rules should be used in the system design:

- For a ×36 configuration part, 21 address pins plus 1 parity bit are used for 22 signals in the address group.If the number of 0's in the address group is $\geq$11, AINV is set to 1 by the controller. As a result, no more than 11 pins may switch in the same direction during each bit time.

- For a ×18 data width part, 22 address pins plus 1 parity bit are used for 23 signals in the address group. If the number of 0's in the address group is ≥12, AINV is set to 1 by the controller. As a result, no more than 12 pins may switch in the same direction during each bit time.

The DINVA and DINVB pins indicate whether the corresponding DQA and DQB pins are inverted.

- For a ×36 data width part, the data bus for each port is split into groups of 18 pins. Each 18-pin data group is guaranteed to be driving less than or equal to 10 pins low on any given cycle.If the number of 0's in the data group is ≥10, DINV is set to 1. As a result, no more than 10 pins may switch in the same direction during each bit time.
- For a ×18 data width part, the data bus for each port is split into groups of 9 pins. Each 9-pin data group is guaranteed to be driving less than or equal to five pins low on any given cycle. If the number of 0's in the data group is ≥5, DINV is set to 1. As a result, no more than five pins may switch in the same direction during each bit time.

AINV, DINVA[1:0], DINVB[1:0] are all active high. When set to 1, the corresponding bus is inverted. If the data inversion feature is programmed to be OFF, then the DINVA/DINVB output bits will always be driven to 0.

These functions are programmable through the configuration registers and can be enabled or disabled for the address bus and the data bus independently.

During configuration register read and write cycles, the address inversion input is ignored and the data inversion output is always driven to 0 when the register read data is driven on the data bus. Specifically, the register read data is driven on DQA[7:0] and the DINVA[0] bit is driven to 0. All other DQA/DQB data bits and DINVA/DINVB bits are tristated. In addition, the address parity input (AP) is ignored.

Address Parity

The QDR-IV XP SRAM provides an address parity feature to provide integrity on the address bus. Two pins are provided to support this function: AP and PE#.

The AP pin is used to provide an even parity across the address pins. The value of AP is set so that the total number of 1's (including the AP bit) is even. The AP pin is a DDR input.

Internally, when an address parity error is detected, the access to the memory array is ignored if it was a write cycle. A read access continues normally even if an address parity error is detected.

Externally, the PE# pin is used to indicate that an address parity error has occurred. This pin is Active Low and is set to 0 within RL cycles after the address parity error is detected. It remains asserted until the error is cleared through the configuration registers.

The address parity function is optional and can be enabled or disabled in the configuration registers.

During configuration register read and write cycles, the address parity input is ignored. Parity is not checked during these cycles.

Note The memory controller should generate address parity based on the address bus first. Address inversion is done later on the address bus and address parity bit.

Port Enable

The QDR-IV XP SRAM has two independent bidirectional data ports. However, some system designers may either choose to use only one port, or use one port as read-only and one port as write-only.

If a port is used in a unidirectional mode, disable the data clocks (DKx/DKx# or QKx/QKx#) to reduce EMI effects in the system. In addition, disable the corresponding control input (RWx#).

Port B may be programmed to be entirely disabled. If port B is not used, then the following must happen:

- The data clocks (DKB/DKB# and QKB/QKB#) and the control inputs (LDB# and RWB#) must be disabled.
- All data bus signals must be tri-stated. This includes DQB, DINVB, and QVLDB.
- All input signals related to port B can be left floating or tied to either 1 or 0 without any adverse effects on the port A operation.
- When port B is not used, all output signals related to port B are inactive.

A configuration register option is provided to specify if one of the ports is not used or is operating in a unidirectional mode.

On-Die Termination (ODT) Operation

When enabled, the ODT circuits for the chip will be enabled during all NOP and write cycles. The ODT is temporarily disabled only during read cycles because the read data is driven out.

Specifically, ODT is disabled one-half clock cycle before the first beat of the read data is driven on the data bus and remains disabled during the entire read operation. ODT is enabled again one-half clock cycle after the last beat of read data is driven on the data bus.

JTAG Operation

The JTAG interface uses five signals: TRST#, TCK, TMS, TDI, and TDO. For normal JTAG operation, the use of TRST# is **not** optional for this device.

While in the JTAG mode, the following conditions are true:

- ODT for all pins is disabled.

If the JTAG function is not used in the system, then the TRST# pin must be tied to VDD and the TCK input must be driven low or tied to VSS. TMS, TDI, and TDO may be left floating.

Power-Up and Reset

The QDR-IV XP SRAM has specific power-up and reset requirements to guarantee reliable operation.

Power-Up Sequence

- Apply V_{DD} before V_{DDQ}.
- Apply V_{DDQ} before V_{REF} or at the same time as V_{REF}.

Reset Sequence

Refer to the Reset timing diagram (Figure 16 on page 41).

1. As the power comes up, all inputs may be in an undefined state, except RST# and TRST#, which must be LOW during t_{PWR}.
2. The first signal that should be driven to the device is the input clock (CK/CK#), which may be unstable for the duration of t_{PWR}.
3. After the input clock has stabilized, all the control inputs should be driven to a valid value as follows:
   a. RST# = 0
   b. CFG# = 1
   c. LBK0# = 1
   d. LBK1# = 1
   e. LDA# = 1
   f. LDB# = 1
4. Reset should remain asserted, while all other control inputs deasserted, for a minimum time of 200 µs (t_{RSS}).
5. At the rising edge of reset, the address bits A[13:0] are sampled to load in the ODT values and Port Enable values. After reset, internal operations in the device may start. This may include operations, such as PLL initialization and resetting internal registers.
6. However, all external control signals must remain deasserted for a minimum time of 400000 clocks (t_{RSH}). During this time all other signals (data and address busses) should be driven to a valid level. All inputs to the device should be driven to a valid level.
7. After this, the device is in normal operating mode and ready to respond to control inputs.

Typically, after a reset sequence, the system starts to perform a training sequence involving the steps outlined in the following section.

However, RST# may be asserted at any time by the system and the system may wish to initiate normal read/write operations after a reset sequence, without going through another training sequence. The chip should be able to accept normal read/write operations immediately following t_{RSH} after the deassertion of RST#.

PLL Reset Operation

The configuration registers contain a bit to reset the PLL. Operating the QDR-IV XP SRAM device without the PLL enabled is not supported—timing characteristics are not guaranteed when the PLL is disabled. However, this bit is intended to allow the system to reset the PLL locking circuitry.

Resetting the PLL is accomplished by first programming the PLL Reset bit to 1 to disable the PLL, and then programming the bit to 0 to enable the PLL. After these steps, the PLL will relock to the input clock. A wait time of tPLL is required.

Operation Modes

The QDR-IV XP SRAM has three unique modes of operation:

1. Configuration
2. Loopback
3. Memory Access

These modes are defined by the level of the control signals CFG#, LBK0#, LBK1#, LDA#, LDB#.

It is intended that these operations are mutually exclusive. In other words, one operation mode cannot be performed simultaneously with another operation mode.

There is no priority given for inadvertently asserting the control signals at the wrong time. The internal chip behavior is not defined for improper control signal assertion. The system must strictly adhere to proper mode transitions, as defined in the following sections, for proper device operation.

Configuration

A Configuration operation mode is entered when the CFG# signal is asserted. Memory Access or Loopback operations should not be performed for a minimum of 32 clocks prior to entering this mode.

While in this mode, the control signals LDB#, LBK0#, and LBK1# must not be asserted. However, LDA# is used to perform the actual Register Read and Write operations.

Memory Access or Loopback operations should not be performed for a minimum of 32 clocks after exiting this mode.

Loopback

A Loopback operation mode is entered when the LBK0# and/or LBK1# signals are asserted. Memory Access or Configuration operations should not be performed for a minimum of 32 clocks prior to entering this mode.

Just after entering this mode, an additional 32 clocks are required before the part is ready to accept toggling valid inputs for training.

While in this mode, LDA# and LDB# may be toggled for training.

Memory Access or Configuration operations should not be performed for a minimum of 32 clocks after exiting this mode.

Data inversion is not used during the Loopback mode. Even if the configuration register has this feature enabled, it is temporarily ignored during the Loopback mode.

Memory Access

If the control signals CFG#, LBK0#, and LBK1# are not asserted, then the device is in the Memory Access mode. This mode is the normal operating mode of the device.

While in this mode, a memory access cycle is performed when the LDA# and/or LDB# signals are asserted. The control signals CFG#, LBK0#, and LBK1# must not be asserted when performing a memory access cycle.

A memory access should not be performed for a minimum of 32 clocks prior to leaving this mode.

Deskew Training Sequence

The QDR-IV XP SRAM provides support that allows a memory controller to deskew signals for a high-speed operation. The memory controller provides the deskew function if deskew is desired. During the deskew operation, the QDR-IV XP SRAM operates in the Loopback mode.

Refer to the Loopback Timing Diagram (Figure 15 on page 40).

Deskew is achieved in three steps:

1. Control/address deskew
2. Read data deskew
3. Write data deskew

Control/Address Deskew

Assert LBK0# to 0 and/or LBK1# to 0.

The following 39 signals are looped back:

- DKA0, DKA0#, DKA1, DKA1#
- DKB0, DKB0#, DKB1, DKB1#
- LDA#, RWA#, LDB#, RWB#
- A[24:0], AINV, AP

The clock inputs DKA0, DKA0#, DKA1#, DKB0, DKB0#, DKB1, and DKB1# are free-running clock inputs and should be continuously running during the training sequence. In addition, a wait time of tPLL is needed.

Refer to Table 1 on page 14 for the loopback signal mapping.

For each pin that is looped back, the input pin is sampled on both the rising and falling edges using the input clock (CK/CK#).

The value output on the rising edge of the output clock (QKA/QKA#) will be the value that was sampled on the rising edge of the input clock.

The value output on the falling edge of the output clock (QKA/QKA#) will be the **inverted** value that was sampled on the falling edge of the input clock.

The delay from the input pins to the DQA outputs is t_{LBL}, which is 16 clocks.

Read Data Deskew

At this time, the address, control, and data input clocks are already deskewed.

Read data deskew requires a training pattern to be written into the memory using data held at constant values.

Complex data patterns, such as the following, may be written into the memory using the non-deskewed DQA and/or DQB signals and the write training enable bit.

Write training enable set to 1:
During Write Data Cycles:
The First Data Beat (First Data Burst) is sampled from the data bus.
The Second Data Beat (Second Data Burst) is the **inverted** sample from the same data bus.

Write training enable set to 0:
During Write Data Cycles:
Both First and Second Data Beats are sampled from the data bus, which is the normal operation.

The Write Training Enable bit has no effect on the read data cycles.

After the data pattern is written into the memory, standard read commands permit the system to deskew with respect to the QK/QK# data output clocks the following signals:

DQA, DINVA, QVLDA, DQB, DINVB, QVLDB

Write Data Deskew

Write data deskew is performed using write commands to the memory followed by read commands.

The deskewed read data path is used to determine whether or not the write data was received correctly by the device.

This permits the system to deskew with respect to the DK/DK# input data clocks the following signals:

DQA, DINVA, DQB, DINVB

I/O Signaling Standards

Several I/O signaling standards are supported by the QDR-IV, which are programmable by the user. They are:

- 1.2 V and 1.25 V HSTL/SSTL
- 1.1 V and 1.2 V POD

The I/O Signaling Standard is programmed on the rising edge of reset by sampling the address bus inputs. Once programmed, the value cannot be changed. Only the rising edge of another reset can change the value.

All address, control, and data I/O signals — with the exception of six pins (listed as LVCMOS in the LVCMOS Signaling section) — will program to comply with HSTL/SSTL or POD.

HSTL/SSTL Signaling

HSTL/SSTL is supported at the V_{DDQ} voltages of 1.2 V and 1.25 V nominal.

The ODT termination values can be set to:

- 40, 60, or 120 ohms with a 220-ohm reference resistor
- 50 or 100 ohms with a 180-ohm reference resistor.

The drive strength can be programmed to:

- 40 or 60 ohms with a 220-ohm reference resistor
- 50 ohms with a 180-ohm reference resistor

A reference resistor of 180 ohms or 220 ohms is supported with HSTL/SSTL signaling.

POD Signaling

POD is supported at V_{DDQ} voltages of 1.1 V and 1.2 V nominal.

The ODT termination values can be set to:

- 50 or 100 ohms with a 180-ohm reference resistor
- 60 or 120 ohms with a 220-ohm reference resistor

The drive strength can be programmed to:

- 50 ohms with a 180-ohm reference resistor
- 40 or 60 ohms with a 220-ohm reference resistor

A reference resistor of 180 ohms or 220 ohms is supported with POD signaling.

LVCMOS Signaling

Six I/O signals are permanently set to use LVCMOS signaling at a voltage of 1.3-V nominal. These signals are referenced to the core voltage supply, V_{DD}. They are:

RST#, TRST#, TCK, TMS, TDI, and TDO

All the five JTAG signals as well as the main reset input are 1.3-V LVCMOS.

In addition, ODT is disabled at all times on these LVCMOS signals.

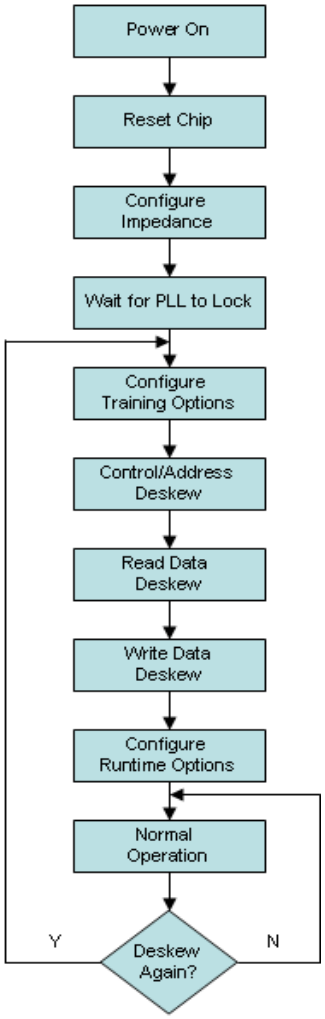
Initialization

The QDR-IV XP SRAM must be initialized before it can operate in the normal functional mode. Initialization uses four special pins:

- RST# pin to reset the device
- CFG# pin to program the configuration registers
- LBK0# and LBK1# pins for the loopback function

The following flowchart illustrates the initialization procedure:

Figure 3. Flowchart illustrating initialization procedure



Power on

Apply power to the chip as described in the power-up sequence in Power-Up Sequence.

Reset Chip

Apply reset to the QDR-IV XP SRAM as described in Reset Sequence.

Configure the Impedance

Assert Config (CFG# = 0) and program the impedance control register.

Wait for the PLL to Lock

Since the input impedance is updated, allow the PLL time (t_{PLL}) to lock to the input clock.

Configure Training Options

At this time, the address and data inversion options need to be programmed. In addition, the write training function needs to be enabled.

Assert Config (CFG# = 0) and program:

- Write Training (Turn On)
- Address Inversion Enable
- Data Inversion Enable

Control/Address Deskew

Control and address deskew can now be performed by the memory controller.

Read Data Deskew

After control and address deskew, the read data path is deskewed as previously described in Deskew Training Sequence.

Write Data Deskew

Write data path is deskewed following the read data path deskew.

Configure Runtime Options

After the training is complete, disable the write training function. Finally, enable the address parity option at this time.

Assert Config (CFG# = 0) and program:

- Write Training (Turn off)
- Parity Enable

Normal Operation

If the system detects a need to deskew again, the process must start again from the Configure Training Options step.The following table defines the loopback mapping:

Table 1. Loopback Signal Mapping

Input Pin LBK0# = 0 LBK1# = 0	Input Pin LBK0# = 0 LBK1# = 1	Input Pin LBK0# = 1 LBK1# = 0	Output Pin
A0	A13	DKA0	DQA0
A1	A14	DKA0#	DQA1
A2	A15	DKA1	DQA2
A3	A16	DKA1#	DQA3
A4	A17	LDA#	DQA4
A5	A18	RWA#	DQA5
A6	A19	DKB0	DQA6
A7	A20	DKB0#	DQA7
A8	A21	DKB1	DQA8
A9	A22	DKB1#	DQA9
A10	A23	LDB#	DQA10
A11	A24	RWB#	DQA11
A12	AINV	AP	DQA12

Configuration Registers

The QDR-IV XP SRAM contains internal registers that are programmed by the system using a special configuration cycle. These registers are used to enable and control several options, as described this section. All registers are 8-bits wide. The write operation is performed using only the address pins to define the register address and register write data. For a read operation, the register read data is provided on the data port A output pins. Refer to Figure 14 on page 39 for programming details.

During the rising edge of RST#, the address pins A[13:0] are sampled. The value sampled becomes the reset value of certain bits in the registers defined in Table 2 on page 15. This is used to set termination, impedance, and port configuration values immediately upon reset. These values can be overwritten later through a register write operation.

When a parity error occurs, the complete address of the ***first*** error is recorded in registers 4, 5, 6, and 7 along with the port A/B error bit. The port A/B error bit will indicate from which port the address parity error came — 0 for port A and 1 for port B. This information will remain latched until cleared by writing a 1 to the address parity error clear bit in register 3.

Two counters are used to indicate if multiple address parity errors occurred. The Port A error count is a running count of the number of parity errors on port A addresses, and similarly the port B error count is a running count of the number of parity errors on port B addresses. They will each independently count to a maximum value of 3 and then stop counting. These counters are free-running and they are both reset by writing a 1 to the address parity error clear bit in register 3.

Configuration Registers Description

Table 2. Configuration Register Table

Register Address	Description
0	Termination Control Register
1	Impedance Control Register
2	Option Control Register
3	Function Control Register
4	Address Parity Status Register 0
5	Address Parity Status Register 1
6	Address Parity Status Register 2
7	Address Parity Status Register 3

Configuration Register Definitions

Table 3. Address 0: Termination Control Register (Read/Write)

Function	ODT Global Enable	ODT/ZQ Auto Update	Address / Command Input Group IU[2]	Address / Command Input Group IU[1]	Address / Command Input Group IU[0]	Clock Input Group KU[2]	Clock Input Group KU[1]	Clock Input Group KU[0]
Bit Location	7	6	5	4	3	2	1	0
Reset Value	A7	A6	A5	A4	A3	A2	A1	A0
Note: ODT/ZQ Auto Update needs to be turned on if ODT/ZQ configuration is changed								

Table 4. Address 1: Impedance Control Register (Read/Write)

Function	Pull-Down Group PD[1]	Pull-Down Group PD[0]	Pull-Up Group PU[1]	Pull-Up Group PU[0]	Unused	Data Input Group QU[2]	Data Input Group QU[1]	Data Input Group QU[0]
Bit Location	7	6	5	4	3	2	1	0
Reset Value	1	0	1	0	0	A10	A9	A8

Table 5. Address 2: Option Control Register (Read/Write Bits 7-3) (Read-Only Bits 2-0) [2]

Function	Write Train Enable	Data Inv Enable	Address Inv Enable	Address Parity Enable	PLL Reset	I/O Type	Port Enable[1]	Port Enable[0]
Bit Location	7	6	5	4	3	2	1	0
Reset Value	0	0	0	0	0	A13	A12	A11

Table 6. Address 3: Function Control Register (Write Only)

Function	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Address Parity Error Clear
Bit Location	7	6	5	4	3	2	1	0
Reset Value	0	0	0	0	0	0	0	0

Note
2. The Bits 2-0 are read only and can be changed only on the rising edge of reset

Table 7. Address 4: Address Parity Status Register 0 (Read Only)

Function	Port B Error Count (1:0)	Port A Error Count (1:0)	Port A/B Error	AINV Bit	Unused	Unused
Bit Location	7:6	5:4	3	2	1	0
Reset Value	00	00	0	0	0	0

Table 8. Address 5: Address Parity Status Register 1 (Read Only)

Function	Address (23:16)
Bit Location	7:0
Reset Value	00000000
Note: Unused address locations will be read as 0	

Table 9. Address 6: Address Parity Status Register 2 (Read Only)

Function	Address (15:8)
Bit Location	7:0
Reset Value	00000000

Table 10. Address 7: Address Parity Status Register 3 (Read Only)

Function	Address (7:0)
Bit Location	7:0
Reset Value	00000000

I/OType and Port Enable Bit Definitions

Table 11. I/O Type Bit Definition specified in Address 2: Option Control Register

I/O Type	Function
0	HSTL / SSTL
1	POD

Table 12. Port Enable Bit Definition specified in Address 2: Option Control Register

Port Enable [1:0]		Function	Port B Mode	Port A Mode	Port B Clocks and Controls	Port A Clocks and Controls
0	0	Fixed Port Mode	Write Only	Read Only	DKB - On QKB - Off LDB# - On RWB# - Off	DKA - Off QKA - On LDA# - On RWA# - Off
0	1	Only Port A Enable	Disabled	Enabled	DKB - Off QKB - Off LDB# - Off RWB# - Off	DKA - On QKA - On LDA# - On RWA# - On
1	0	Not supported	Disabled	Disabled	DKB - Off QKB - Off LDB# - Off RWB# - Off	DKA - Off QKA - Off LDA# - Off RWA# - Off
1	1	Both Ports Enabled	Enabled	Enabled	DKB - On QKB - On LDB# - On RWB# - On	DKA - On QKA - On LDA# - On RWA# - On

ODT Termination Bit Definitions

Table 13. Clock Input Group Bit Definition specified in Address 0: Termination Control Register

ODT Global Enable	KU[2:0]			Divisor Value	Termination Value HSTL/SSTL Mode		Termination Value POD Mode	
					ZT 180 ohm	ZT 220 ohm	ZT 180 ohm	ZT 220 ohm
0	X	X	X	–	OFF	OFF	OFF	OFF
1	0	0	0	–	OFF	OFF	OFF	OFF
1	0	0	1	8.33%	Not supported	Not supported	Not supported	Not supported
1	0	1	0	12.50%	Not supported	Not supported	Not supported	Not supported
1	0	1	1	16.67%	Not supported	40 ohm	Not supported	Not supported
1	1	0	0	25%	50 ohm	60 ohm	50 ohm	60 ohm
1	1	0	1	50%	100 ohm	120 ohm	100 ohm	120 ohm
1	1	1	0	–	Not supported	Not supported	Not supported	Not supported
1	1	1	1	–	Not supported	Not supported	Not supported	Not supported
Note: Termination values are accurate to +/- 15% ZQ tolerance is 1%								

Table 14. Address/Command Input Group Bit Definition specified in Address 0: Termination Control Register

ODT Global Enable	IU[2:0]			Divisor Value	Termination Value HSTL/ SSTL Mode		Termination Value POD Mode	
					ZT 180 ohm	ZT 220 ohm	ZT 180 ohm	ZT 220 ohm
0	X	X	X	–	OFF	OFF	OFF	OFF
1	0	0	0	–	OFF	OFF	OFF	OFF
1	0	0	1	8.33%	Not supported	Not supported	Not supported	Not supported
1	0	1	0	12.50%	Not supported	Not supported	Not supported	Not supported
1	0	1	1	16.67%	Not supported	40 ohm	Not supported	Not supported
1	1	0	0	25%	50 ohm	60 ohm	50 ohm	60 ohm
1	1	0	1	50%	100 ohm	120 ohm	100 ohm	120 ohm
1	1	1	0	–	Not supported	Not supported	Not supported	Not supported
1	1	1	1	–	Not supported	Not supported	Not supported	Not supported
Note: Termination values are accurate to +/- 15% ZQ tolerance is 1%								

Table 15. Data Input Group Bit Definition specified in Address 1: Impedance Control Register

ODT Global Enable	QU[2:0]			Divisor Value	Termination Value HSTL/ SSTL Mode		Termination Value POD Mode	
					ZT 180 ohm	ZT 220 ohm	ZT 180 ohm	ZT 220 ohm
0	X	X	X	–	OFF	OFF	OFF	OFF
1	0	0	0	–	OFF	OFF	OFF	OFF
1	0	0	1	8.33%	Not supported	Not supported	Not supported	Not supported
1	0	1	0	12.50%	Not supported	Not supported	Not supported	Not supported
1	0	1	1	16.67%	Not supported	40 ohm	Not supported	Not supported
1	1	0	0	25%	50 ohm	60 ohm	50 ohm	60 ohm
1	1	0	1	50%	100 ohm	120 ohm	100 ohm	120 ohm
1	1	1	0	–	Not supported	Not supported	Not supported	Not supported
1	1	1	1	–	Not supported	Not supported	Not supported	Not supported
Note: Termination values are accurate to +/- 15% ZQ tolerance is 1%								

Drive Strength Bit Definitions

Table 16. Pull-Up Driver Bit Definition specified in Address 1: Impedance Control Register

PU[1:0]		Divisor Value	Impedance Value HSTL/ SSTL Mode		Impedance Value POD Mode	
			ZT 180 ohm	ZT 220 ohm	ZT 180 ohm	ZT 220 ohm
0	0	14.17%	Not supported	Not supported	Not supported	Not supported
0	1	16.67%	Not supported	40 ohm	Not supported	40 ohm
1	0	25%	50 ohm	60 ohm	50 ohm	60 ohm
1	1	–	Not supported	Not supported	Not supported	Not supported
Note: Termination values are accurate to +/- 15% ZQ tolerance is 1%						

Table 17. Pull-Down Driver Bit Definition specified in Address 1: Impedance Control Register

PD[1:0]		Divisor Value	Impedance Value HSTL/ SSTL Mode		Impedance Value POD Mode	
			ZT 180 ohm	ZT 220 ohm	ZT 180 ohm	ZT 220 ohm
0	0	14.17%	Not supported	Not supported	Not supported	Not supported
0	1	16.67%	Not supported	40 ohm	Not supported	40 ohm
1	0	25%	50 ohm	60 ohm	50 ohm	60 ohm
1	1	–	Not supported	Not supported	Not supported	Not supported
Note: Termination values are accurate to +/- 15% ZQ tolerance is 1%						

IEEE 1149.1 Serial Boundary Scan (JTAG)

QDR-IV XP SRAMs incorporate a serial boundary scan test access port (TAP) in the FCBGA package. This part is fully compliant with IEEE Standard #1149.1-2001. In the JTAG mode, the ODT feature for all pins is disabled.

If the JTAG function is not used in the circuit, then TCK inputs must be driven low or tied to VSS. TRST#, TMS, TDI, and TDO may be left floating. An internal pull-up resistor is implemented on the TRST#, TMS, and TDI inputs to ensure that these inputs are HIGH during t_{PWR}.

Test Access Port

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see TAP Controller State Diagram on page 22. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any register.

Test Data-Out (TDO)

The TDO output pin is used to serially clock data out from the registers. The output is active, depending upon the current state of the TAP state machine (see Instruction Codes on page 26). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Test Reset (TRST#)

The TRST# input pin is used to reset the TAP controller.

Alternatively, a reset may be performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK.

This reset does not affect the operation of the SRAM and can be performed while the SRAM is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a high Z state.

TAP Registers

Registers are connected between the TDI and TDO pins to scan the data in and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins, as shown in TAP Controller Block Diagram on page 23. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a RST state, as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This enables shifting of data through the SRAM with minimal delay. The bypass register is set LOW (VSS) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all of the input and output pins on the SRAM. Several No Connect (NC) pins are also included in the scan register to reserve pins for higher density devices.

The boundary scan register is loaded with the contents of the RAM input and output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the input and output ring.

Boundary Scan Order on page 27 shows the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in Identification Register Definitions on page 26.

TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in Instruction Codes on page 26. Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in this section in detail.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction after it is shifted in, the TAP controller must be moved into the Update-IR state.

IDCODE

The IDCODE instruction loads a vendor-specific, 32-bit code into the instruction register. It also places the instruction register between the TDI and TDO pins and shifts the IDCODE out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register at power-up or whenever the TAP controller is supplied a Test-Logic-RST state.

SAMPLE Z

The SAMPLE Z instruction connects the boundary scan register between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a High Z state until the next command is supplied during the Update IR state. Both Port A and Port B are enabled once this command has been executed.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the input and output pins is captured in the boundary scan register.

Remember that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that an input or output undergoes a transition during the Capture-DR state. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and $\overline{CK}$ captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD places an initial data pattern at the latched parallel outputs of the boundary scan register cells before the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required, that is, while the data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST

The EXTEST instruction drives the preloaded data out through the system output pins. This instruction also connects the boundary scan register for serial access between the TDI and TDO in the Shift-DR controller state. Both Port A and Port B are enabled after this command is executed.

EXTEST OUTPUT BUS TRISTATE

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tristate mode.

The boundary scan register has output enable control bits located at Bit #49 and Bit #50. Bit# 49 enables the output pins for DQB and Bit#50 enables DQA and PE# pins.

When these scan cells, called the "extest output bus tristate," are latched into the preload register during the Update-DR state in the TAP controller, they directly control the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a High Z condition.

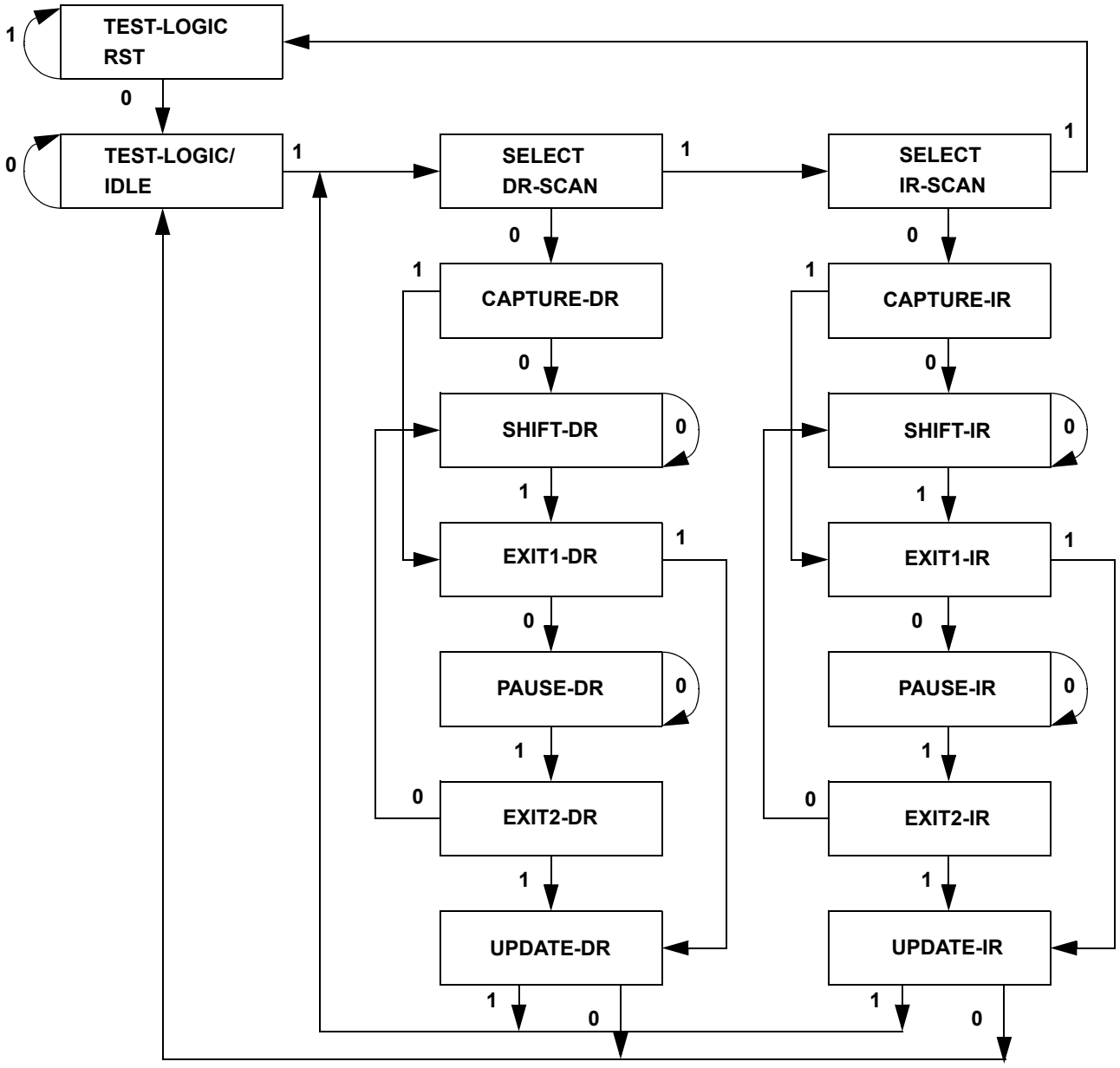
These bits can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the Shift-DR state. During Update-DR, the value loaded into that shift-register cell latches into the preload register. When the EXTEST instruction is entered, these bits directly controls the output Q-bus pins. Note that these bits are pre-set LOW to disable the output when the device is powered up, and also when the TAP controller is in the Test-Logic-RST state.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram

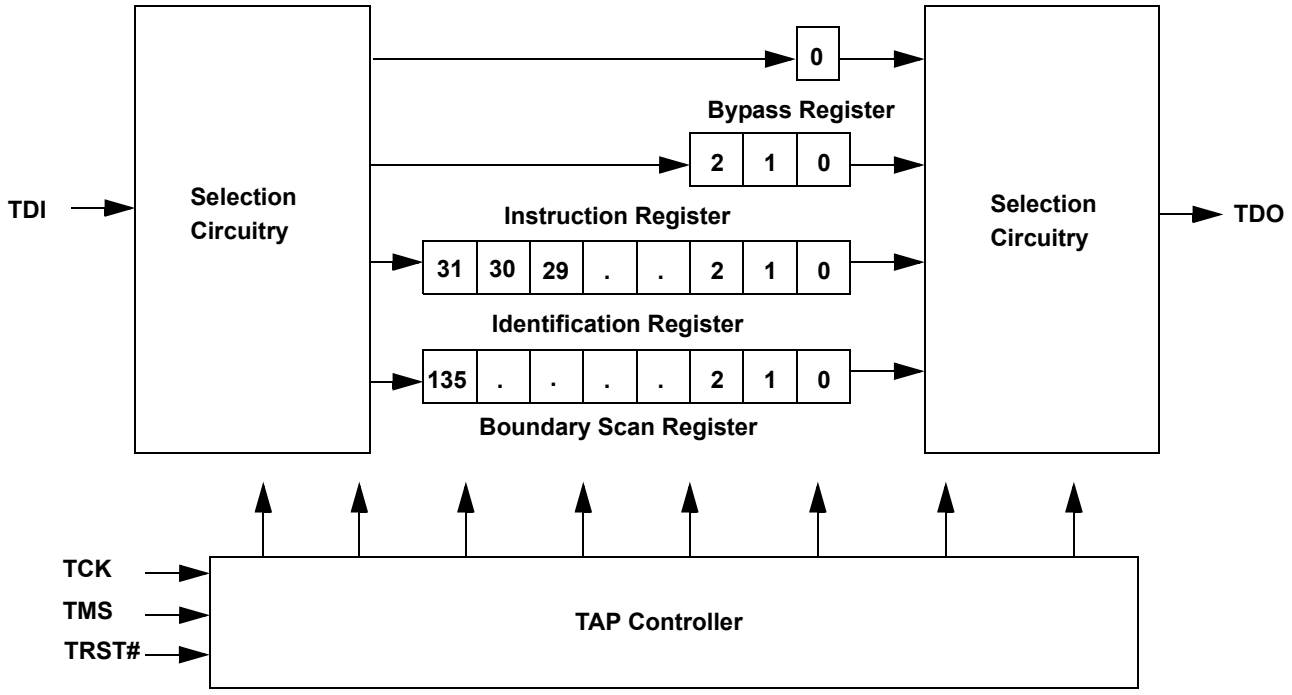
Figure 4. TAP Controller State Diagram [3]



Note
3. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

TAP Controller Block Diagram

Figure 5. TAP Controller Block Diagram



TAP Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}	LVCMOS high-level output voltage	I_{OH} = 100 µA	V_{DD} × 0.8	–	V
V_{OL}	LVCMOS low-level output voltage	I_{OL} = 100 µA	–	V_{DD} × 0.2	V
V_{IH}	LVCMOS high-level input voltage (DC)		V_{DD} × 0.7	V_{DD} + 0.2	V
V_{IL}	LVCMOS low-level input voltage (DC)		–0.2	V_{DD} × 0.3	V
I_X	LVCMOS input leakage current		–	10	µA
I_{OZ}	LVCMOS output leakage current		–	10	µA

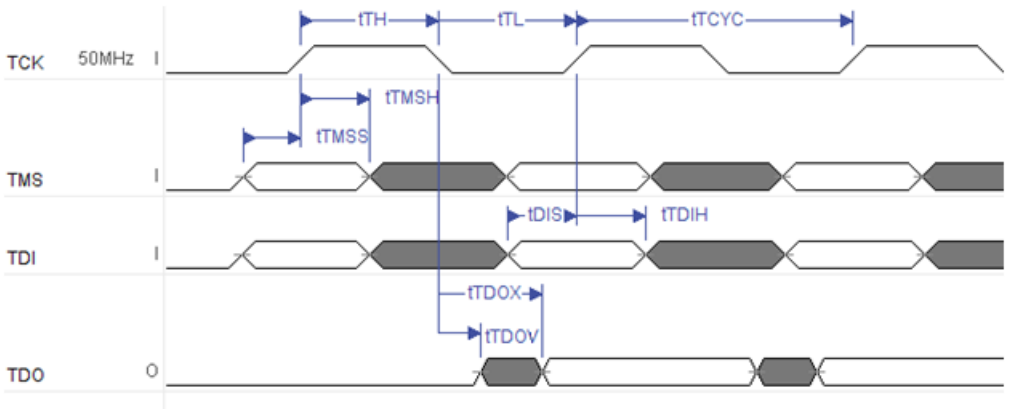
TAP AC Switching Characteristics

Over the Operating Range

Parameter	Description	Min	Max	Unit
t_{TCYC}	TCK clock cycle time	50	–	ns
t_{TF}	TCK clock frequency	–	20	MHz
t_{TH}	TCK clock HIGH	20	–	ns
t_{TL}	TCK clock LOW	20	–	ns
Setup Times				
t_{TMSS}	TMS setup to TCK clock rise	5	–	ns
t_{TDIS}	TDI setup to TCK clock rise	5	–	ns
t_{CS}	Capture setup to TCK rise	5	–	ns
Hold Times				
t_{TMSH}	TMS hold after TCK clock rise	5	–	ns
t_{TDIH}	TDI hold after clock rise	5	–	ns
t_{CH}	Capture hold after clock rise	5	–	ns
Output Times				
t_{TDOV}	TCK clock LOW to TDO valid	–	10	ns
t_{TDOX}	TCK clock LOW to TDO invalid	0	–	ns
Note: t_{CS} and t_{CH} refer to setup and hold time requirements of latching data from the boundary scan register.				

TAP Timing Diagram

Figure 6. TAP Timing Diagram



Identification Register Definitions

Instruction Field	Value		Description
	CY7C4122KV13	CY7C4142KV13	
Revision Number (31:29)	000	000	Version number.
Cypress Device ID (28:12)	11011010101010011	11011010101100011	Defines the type of SRAM.
Cypress JEDEC ID (11:1)	00000110100	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence (0)	1	1	Indicates the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	136

Instruction Codes

Instruction	Code	Description
EXTEST	000	Captures the input and output ring contents.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the input and output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the input and output contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

Boundary Scan Order

Bit	Bump	CY7C4142KV13 ×36 Device	CY7C4122KV13 ×18 Device
0	12A	DQA<26>	DQA<17>
1	13B	DQA<19>	DQA<10>
2	14A	DQA<25>	DQA<16>
3	15B	DQA<35>	NC
4	16A	DQA<23>	DQA<14>
5	18B	DQA<31>	NC
6	17C	QVLDA<1>	QVLDA<1>
7	16C	QKA<1>	QKA<1>
8	14C	DQA<20>	DQA<11>
9	12C	DQA<18>	DQA<9>
10	12D	DINVA<1>	DINVA<1>
11	13D	DQA<22>	DQA<13>
12	15D	DQA<21>	DQA<12>
13	17D	QKA#<1>	QKA#<1>
14	18E	DQA<32>	NC
15	15F	DQA<24>	DQA<15>
16	16F	DKA<1>	DKA<1>
17	17F	DKA#<1>	DKA#<1>
18	18G	DQA<33>	NC
19	16G	DQA<34>	NC
20	17H	DQA<27>	NC
21	15H	DQA<28>	NC
22	16J	DQA<30>	NC
23	18J	DQA<29>	NC
24	18K	RST#	RST#
25	18L	DQB<29>	NC
26	16L	DQB<30>	NC
27	15M	DQB<28>	NC
28	17M	DQB<27>	NC
29	18N	DQB<33>	NC
30	16N	DQB<34>	NC
31	15P	DQB<24>	DQB<15>
32	16P	DKB<1>	DKB<1>
33	17P	DKB#<1>	DKB#<1>
34	18R	DQB<32>	NC
35	17T	QKB#<1>	QKB#<1>
36	15T	DQB<21>	DQB<12>
37	13T	DQB<22>	DQB<13>
38	12T	DINVB<1>	DINVB<1>
39	12U	DQB<18>	DQB<9>
40	14U	DQB<20>	DQB<11>
41	16U	QKB<1>	QKB<1>
42	17U	QVLDB<1>	QVLDB<1>
43	18V	DQB<31>	NC
44	15V	DQB<35>	NC
45	13V	DQB<19>	DQB<10>
46	12W	DQB<26>	DQB<17>

Boundary Scan Order (continued)

Bit	Bump	CY7C4142KV13 ×36 Device	CY7C4122KV13 ×18 Device
47	14W	DQB<25>	DQB<16>
48	16W	DQB<23>	DQB<14>
49		Internal_DQB	Internal_DQB
50		Internal_DQA	Internal_DQA
51	10V	PE#	PE#
52	8P	A<15>	A<15>
53	7N	A<9>	A<9>
54	9N	NC/1152M	NC/576M
55	10P	AP	AP
56	10N	A<2>	A<2>
57	11N	NC/2304M	NC/1152M
58	12P	A<16>	A<16>
59	13N	A<10>	A<10>
60	13L	A<8>	A<8>
61	12M	A<12>	A<12>
62	11L	A<18>	A<18>
63	10L	RWB#	RWB#
64	10M	AINV	AINV
65	9L	A<17>	A<17>
66	8M	A<11>	A<11>
67	7L	A<7>	A<7>
68	7J	A<5>	A<5>
69	9J	A<19>	A<19>
70	10K	CK#	CK#
71	10J	CK	CK
72	11J	A<20>	A<20>
73	13J	A<6>	A<6>
74	12H	LDB#	LDB#
75	10H	RWA#	RWA#
76	8H	LDA#	LDA#
77	7G	A<3>	A<3>
78	9G	NC/288M	A<21>
79	10G	A<1>	A<1>
80	11G	NC/576M	NC/288M
81	13G	A<4>	A<4>
82	12F	A<14>	A<14>
83	10F	A<0>	A<0>
84	8F	A<13>	A<13>
85	10D	CFG#	CFG#
86	10B	LBK#<1>	LBK#<1>
87	10A	LBK#<0>	LBK#<0>
88	8A	DQA<8>	DQA<8>
89	7B	DQA<1>	DQA<1>
90	6A	DQA<7>	DQA<7>
91	5B	DQA<17>	NC
92	4A	DQA<5>	DQA<5>
93	2B	DQA<13>	NC
94	3C	QVLDA<0>	QVLDA<0>
95	4C	QKA<0>	QKA<0>

Boundary Scan Order (continued)

Bit	Bump	CY7C4142KV13 ×36 Device	CY7C4122KV13 ×18 Device
96	6C	DQA<2>	DQA<2>
97	8C	DQA<0>	DQA<0>
98	8D	DINVA<0>	DINVA<0>
99	7D	DQA<4>	DQA<4>
100	5D	DQA<3>	DQA<3>
101	3D	QKA#<0>	QKA#<0>
102	2E	DQA<14>	NC
103	3F	DKA#<0>	DKA#<0>
104	4F	DKA<0>	DKA<0>
105	5F	DQA<6>	DQA<6>
106	4G	DQA<16>	NC
107	2G	DQA<15>	NC
108	3H	DQA<9>	NC
109	5H	DQA<10>	NC
110	4J	DQA<12>	NC
111	2J	DQA<11>	NC
112	2L	DQB<11>	NC
113	4L	DQB<12>	NC
114	5M	DQB<10>	NC
115	3M	DQB<9>	NC
116	2N	DQB<15>	NC
117	4N	DQB<16>	NC
118	5P	DQB<6>	DQB<6>
119	4P	DKB<0>	DKB<0>
120	3P	DKB#<0>	DKB#<0>
121	2R	DQB<14>	NC
122	3T	QKB#<0>	QKB#<0>
123	5T	DQB<3>	DQB<3>
124	7T	DQB<4>	DQB<4>
125	8T	DINVB<0>	DINVB<0>
126	8U	DQB<0>	DQB<0>
127	6U	DQB<2>	DQB<2>
128	4U	QKB<0>	QKB<0>
129	3U	QVLDB<0>	QVLDB<0>
130	2V	DQB<13>	NC
131	5V	DQB<17>	NC
132	7V	DQB<1>	DQB<1>
133	8W	DQB<8>	DQB<8>
134	6W	DQB<7>	DQB<7>
135	4W	DQB<5>	DQB<5>

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Maximum junction temperature ..... 125 °C

Supply voltage on V_{DD} relative to GND .....–0.3 V to +1.35 V

Supply voltage on V_{DDQ} relative to GND .....–0.3 V to +1.35 V

DC input voltage .....–0.3 V to +1.35 V

Current into outputs (low) ..... 20 ma

Static discharge voltage (MIL-STD-883, M. 3015) ..... > 2001V

Latch up current .....> 200 mA

Operating Range

Table 18. Operating Range

Range	Case Temperature (T_C)	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	1.3 V ± 40 mV	1.1 V ± 50 mV
			1.2 V ± 50 mV

Neutron Soft Error Immunity

Table 19. Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU	Logical single-bit upsets	25 °C	0	0.01	FIT/Mb
LMBU	Logical multi-bit upsets	25 °C	0	0.01	FIT/Mb
SEL	Single event latch-up	85 °C	0	0.1	FIT/Dev

** No LMBU or SEL events occurred during testing*; this column represents a statistical χ^2, 95% confidence limit calculation. For more details refer to Application Note, Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates – AN54908.

Electrical Characteristics

Over the Operating Range

Parameter	Description	Min	Typ	Max	Unit
POD Signaling Mode					
V_{DD}[4]	Core supply voltage (1.3 V ± 40 mV)	1.26	1.3	1.34	V
V_{DDQ} [4]	POD I/O supply voltage (1.1 V ± 50 mV)	1.05	1.1	1.15	V
	POD I/O supply voltage (1.2 V ± 50 mV)	1.15	1.2	1.25	V
V_{REF} [4, 5]	POD reference voltage	V_{DDQ} × 0.69	V_{DDQ} × 0.7	V_{DDQ} × 0.71	V
$V_{OL(DC)}$ [4]	POD low-level output voltage (DC)	–	–	0.5	V
$V_{IH(DC)}$ [4, 6]	POD high-level input voltage (DC)	V_{REF} + 0.08	–	V_{DDQ} + 0.15	V
$V_{IL(DC)}$ [4, 6]	POD low level input voltage	–0.15	–	V_{REF} – 0.08	V
$V_{IH(AC)}$ [4, 7]	POD high-level input voltage (DC)	V_{REF} + 0.15	–	–	V
$V_{IL(AC)}$ [4, 7]	POD low-level input voltage	–	–	V_{REF} – 0.15	V
$V_{MP(DC)}$	POD differential input mid-point voltage; Pin and Pin#	V_{REF} – 0.08	–	V_{REF} + 0.08	V
$V_{ID(DC)}$	POD differential input differential voltage (DC); Pin and Pin#	0.16	–	–	V
$V_{ID(AC)}$	POD differential input differential voltage (AC); Pin and Pin#	0.30	–	–	V
V_{IN}	POD single-ended input voltage; Pin and Pin#	0.27	–	V_{DDQ} + 0.15	V
V_{INS}	POD single-ended input voltage slew rate; Pin and Pin#	3	–	–	V/ns
$V_{IX(AC)}$	POD differential input crossing point voltage (AC); Pin and Pin#	V_{REF} – 0.08	–	V_{REF} + 0.08	V

Notes
4. All voltages referenced to VSS (GND).
5. Peak to Peak AC noise on V_{REF} must not exceed +/–2% V_{DDQ}(DC).
6. V_{IH}/V_{IL}(DC) are specified with ODT disabled.
7. V_{IH}/V_{IL}(AC) is a test condition specified to guarantee at which the receiver must meet its timing specifications with ODT enabled.

Electrical Characteristics (continued)

Over the Operating Range

Parameter	Description	Min	Typ	Max	Unit
I_X [8]	POD input leakage current	–	–	200	µA
I_{OZ} [8]	POD output leakage current	–	–	200	µA
I_{DD} [9, 10]	V_{DD} operating supply (1066 MHz, ×18)	–	2800	4100	mA
	V_{DD} operating supply (1066 MHz, ×36)	–	3920	4500	mA
	V_{DD} operating supply (933 MHz, ×18)	–	2520	3400	mA
	V_{DD} operating supply (933 MHz, ×36)	–	3520	4000	mA
HSTL/SSTL Signaling Mode					
V_{DD} [11]	Core supply voltage (1.3 V ±40 mV)	1.26	1.3	1.34	V
V_{DDQ} [11]	I/O supply voltage (1.2 V ±50 mV)	1.15	1.2	1.25	V
	I/O supply voltage (1.25 V ±50 mV)	1.2	1.25	1.3	V
$V_{REF(DC)}$ [11, 12]	HSTL/SSTL reference voltage (DC)	V_{DDQ} × 0.48	V_{DDQ} × 0.5	V_{DDQ} × 0.52	V
$V_{REF(AC)}$ [11, 12]	HSTL/SSTL reference voltage (AC)	V_{DDQ} × 0.47	V_{DDQ} × 0.5	V_{DDQ} × 0.53	V
$V_{IH(DC)}$ [11, 13]	HSTL/SSTL high-level input voltage (DC)	V_{REF} + 0.08	–	V_{DDQ} + 0.15	V
$V_{IL(DC)}$ [11, 13]	HSTL/SSTL low-level input voltage (DC)	–0.15	–	V_{REF} – 0.08	V
$V_{IH(AC)}$ [11, 14]	HSTL/SSTL high-level input voltage (AC)	V_{REF} + 0.15	–	V_{DDQ} + 0.24	V
$V_{IL(AC)}$ [11, 14]	HSTL/SSTL low-level input voltage (AC)	–0.24	–	V_{REF} – 0.15	V
$V_{OH(DC)}$ [11]	HSTL/SSTL high-level output voltage (DC) – I_{OH} = –0.25 × V_{DDQ}/R_{OH}	V_{DDQ} × 0.712	V_{DDQ} × 0.75	–	V
$V_{OL(DC)}$ [11]	HSTL/SSTL low-level output voltage (DC) – I_{OL} = 0.25 × V_{DDQ}/R_{OL}	–	V_{DDQ} × 0.25	V_{DDQ} × 0.288	V
V_{IX}	HSTL/SSTL input voltage cross-point	–	V_{DDQ} × 0.5	–	V
$V_{DIF(AC)}$	HSTL/SSTL AC input differential voltage	0.30	–	V_{DDQ} + 0.48	V
$V_{DIF(DC)}$	HSTL/SSTL DC input differential voltage	0.16	–	V_{DDQ} + 0.30	V
$V_{DIF(CM)}$	HSTL/SSTL DC common mode input	V_{DDQ} × 0.4	V_{DDQ} × 0.5	V_{DDQ} × 0.6	V
V_{OX}	HSTL/SSTL output voltage cross-point	–	V_{DDQ} × 0.5	–	V
$V_{OUT(AC)}$	HSTL/SSTL AC output voltage	–0.24	–	V_{DDQ} + 0.24	V
$V_{OUT(DC)}$	HSTL/SSTL DC output voltage	–0.15	–	V_{DDQ} + 0.15	V
I_X [8]	HSTL/SSTL input leakage current	–	–	200	µA
I_{OZ} [8]	HSTL/SSTL output leakage current	–	–	200	µA
I_{DD} [9, 10]	V_{DD} operating supply (1066 MHz, ×18)	–	2800	4100	mA
	V_{DD} operating supply (1066 MHz, ×36)	–	3920	4500	mA
	V_{DD} operating supply (933 MHz, ×-18)	–	2520	3400	mA
	V_{DD} operating supply (933 MHz, ×-36)	–	3520	4000	mA

Notes
8. Output driver into High Z with ODT disabled.
9. The operation current is calculated with 50% read cycle and 50% write cycle.
10. Typical operation current specifications are tested at 1.3V V_{DD}.
11. All voltages referenced to VSS (GND).
12. Peak to Peak AC noise on V_{REF} must not exceed +/–2% V_{DDQ}(DC).
13. V_{IH}/V_{IL}(DC) are specified with ODT disabled.
14. V_{IH}/V_{IL}(AC) is a test condition specified to guarantee at which the receiver must meet its timing specifications with ODT enabled.

Capacitance

Table 20. Capacitance

Parameter [15]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 1.3 V, V_{DDQ} = 1.25 V	4	pF
C_O	Output capacitance		4	pF

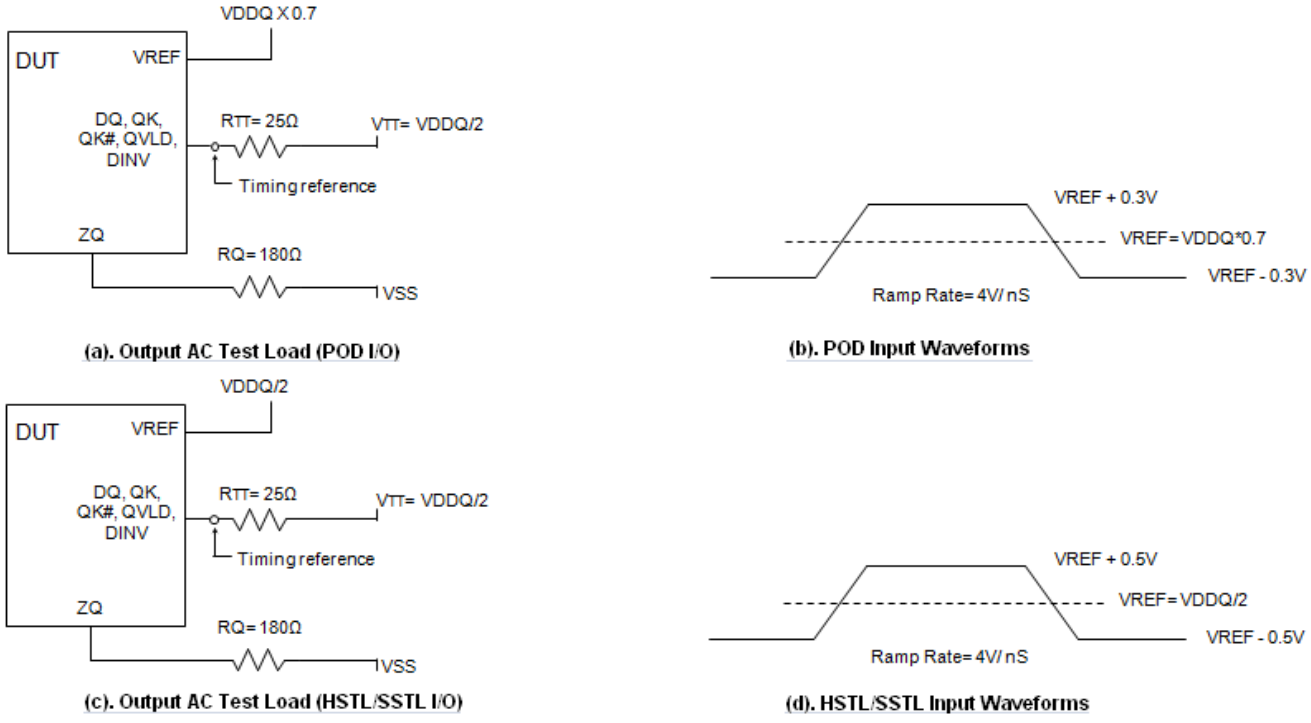
Thermal Resistance

Table 21. Thermal Resistance

Parameter [15]	Description	Test Conditions		361-ball FCBGA Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	With Still Air (0 m/s)	12.00	°C/W
			With Air Flow (1 m/s)	10.57	°C/W
			With Air Flow (3 m/s)	9.09	°C/W
Θ_{JB}	Thermal resistance (junction to board)			3.03	°C/W
Θ_{JC}	Thermal resistance (junction to case)			0.029	°C/W

AC Test Load and Waveform

Figure 7. AC Test Load and Waveform



Note
15. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics

Over the Operating Range [16, 17, 18, 19, 20, 21, 22, 23]

Cypress Parameter	Description	1066 MHz		933 MHz		Unit
		Min	Max	Min	Max	
t_{CK}	CK, DKx, QKx clock period	0.938	1.875	1.071	2.143	ns
t_{CKL}	CK, DKx LOW time	0.45*	–	0.45*	–	t_{CK}
t_{CKH}	CK, DKx HIGH time	0.45*	–	0.45*	–	t_{CK}
t_{JIT}(per)	Clock period jitter	–0.055	0.055	–0.060	0.060	ns
t_{JIT}(cc)	Cycle-to-cycle jitter	–	0.110	–	0.120	ns
t_{AS}	A to CK setup	0.125	–	0.135	–	ns
t_{AH}	CK to A hold	0.125	–	0.135	–	ns
t_{ASH}	CK to A setup-hold window	0.170	–	0.180	–	ns
t_{CS}	LDx#, RWx# to CK setup	0.150	–	0.180	–	ns
t_{CH}	CK to LDx#, RWx# hold	0.150	–	0.180	–	ns
t_{CSH}	CK to LDx#, RWx# setup-hold window	0.170	–	0.180	–	ns
t_{CKDK}	CK to DKx skew	–0.15	0.15	–0.172	0.172	ns
t_{IS}	DQx, DINVx to DKx setup	0.125	–	0.135	–	ns
t_{IH}	DKx to DQx, DINVx hold	0.125	–	0.135	–	ns
t_{ISH0}	DKx[0] to DQx[17:0], DINVx[0] (× 36) or DKx[0] to DQx[8:0], DINVx[0] (× 18) setup-hold window	0.150	–	0.180	–	ns
t_{ISH1}	DKx[1] to DQx[35:18], DINVx[1] (× 36) or DKx[1] to DQx[17:9], DINVx[1] (× 18) setup-hold window	0.150	–	0.180	–	ns
t_{Rise} (se)	Single-ended output signal rise time 20%-80%	2	6	2	6	V/ns
t_{Fall} (se)	Single-ended output signal fall time 20%-80%	2	6	2	6	V/ns
t_{Rise} (diff)	Differential output signal rise time 20%-80%	3	10	3	10	V/ns
t_{Fall} (diff)	Differential output signal fall time 20%-80%	3	10	3	10	V/ns
t_{QKL}	QKx LOW time	0.45*	–	0.45*	–	t_{CK}
t_{QKH}	QKx HIGH time	0.45*	–	0.45*	–	t_{CK}
t_{CKQK}	CK to QKx skew	–0.225	0.225	–0.257	0.257	ns
t_{QKQ0}	QKx[0] to DQx[17:0], DINVx[0] (× 36) or QKx[0] to DQx[8:0], DINVx[0] (× 18)	–	0.075	–	0.085	ns
t_{QH0}	QKx[0] to DQx[17:0], DINVx[0] (× 36) or QKx[0] to DQx[8:0], DINVx[0] (× 18)	0.40*	–	0.40*	–	t_{CK}
t_{QKQ1}	QKx[1] to DQx[35:18], DINVx[1] (× 36) or QKx[1] to DQx[17:9], DINVx[1] (× 18)	–	0.075	–	0.085	ns
t_{QH1}	QKx[1] to DQx[35:18], DINVx[1] (× 36) or QKx[1] to DQx[17:9], DINVx[1] (× 18)	0.40*	–	0.40*	–	t_{CK}

Notes
16. x refers to Port A and Port B. For example, DQx refers to DQA and DQB.
17. Input hold timing assumes rising edge slew rate of 4 V/ns measured from V_{IL}/V_{IH} (DC) to V_{REF}.
18. Input setup timing assumes falling edge slew rate of 4 V/ns measured from V_{REF} to V_{IL}/V_{IH} (AC).
19. All output timing assumes the load shown in Figure 7 on page 32.
20. Setup/hold window, t_{ASH}, t_{CSH}, t_{ISH} are used for pin to pin timing budgeting and cannot be directly applied without performing de-skew training.
21. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
22. Frequency drift is not allowed.
23. t_{QKL}, t_{QKH}, t_{QKQ}, t_{QKQX}, t_{ASH}, t_{CSH} and t_{ISH} are guaranteed by design.

Switching Characteristics (continued)

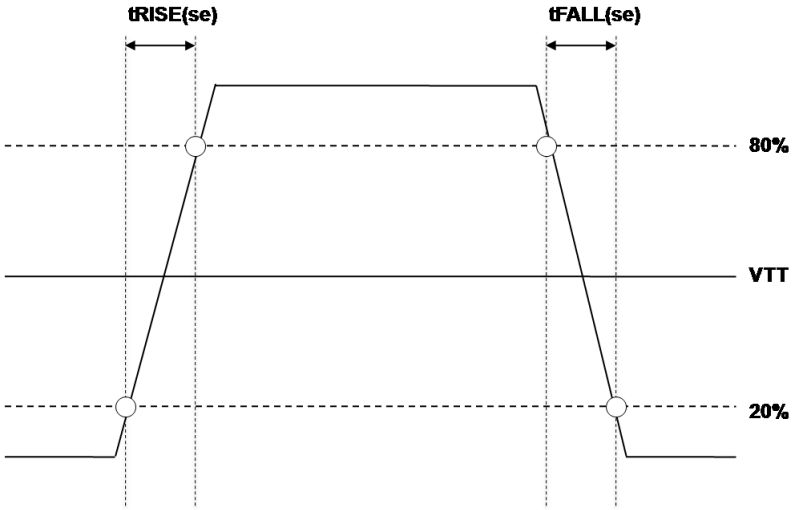
Over the Operating Range [16, 17, 18, 19, 20, 21, 22, 23]

Cypress Parameter	Description	1066 MHz		933 MHz		Unit
		Min	Max	Min	Max	
t_{QKQV0}	QKx[0] to QVLDx	–	0.112	–	0.128	ns
t_{QVH0}	QKx[0] to QVLDx	0.85*	–	0.85*	–	t_{CK}
t_{QKQV1}	QKx[1] to QVLDx	–	0.112	–	0.128	ns
t_{QVH1}	QKx[1] to QVLDx	0.85*	–	0.85*	–	t_{CK}
t_{PWR}	V_{DD} (Typical) to the first access	200	–	200	–	ms
t_{RSS}	RST# pulse width	200	–	200	–	µs
t_{RSH}	RST# deasserted to first active command	400000*	–	400000*	–	t_{CK}
t_{RDS}	A to RST# setup	500*	–	500*	–	t_{CK}
t_{RDH}	A to RST# hold	500*	–	500*	–	t_{CK}
t_{TSS}	TRST# pulse width	200	–	200	–	µs
t_{TSH}	TRST# deasserted to first JTAG command	200	–	200	–	µs
t_{PLL}	Time for PLL to stabilize after being reset	–	100	–	100	µs
t_{LBL}	Loopback latency	16*	16*	16*	16*	t_{CK}
t_{CD}	Loopback output delay	–	5	–	5	ns
t_{CFGS}	Active mode to Configuration mode	32*	–	32*	–	t_{CK}
t_{CFGH}	Configuration mode to Active mode Register Access without ODT or PLL programming updates	32*	–	32*	–	t_{CK}
t_{CFGH}	Configuration mode to Active mode Register Access with ODT programming updates	4096*	–	4096*	–	t_{CK}
t_{CFGH}	Configuration mode to Active mode Register Access with PLL programming updates	100	–	100	–	µs
t_{CFGD}	Configuration command to Configuration command	80*	–	80*	–	t_{CK}
t_{CLDS}	CFG# assertion to LDA# assertion	32*	–	32*	–	t_{CK}
t_{CLDH}	LDA# deassertion to CFG# deassertion	32*	–	32*	–	t_{CK}
t_{CLDW}	LDA# pulse width for Configuration command	16*	–	16*	–	t_{CK}
t_{CRDL}	LDA# assertion to Read Data Latency	–	32*	–	32*	t_{CK}
t_{CRDH}	CFG# deassertion to Read Data Hold	0*	32*	0*	32*	t_{CK}
t_{DQVLD}	DQAx to QVLDA<0> in Configuration mode	–2	2	–2	2	t_{CK}

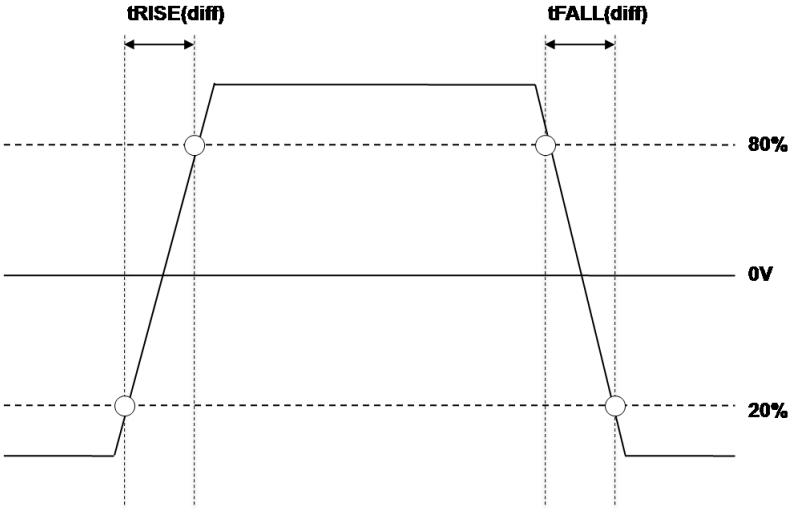
Switching Waveforms

Figure 8. Rise and Fall Time Definitions for Output Signals

Nominal Rise-Fall Time Definition for Single-Ended Output Signals



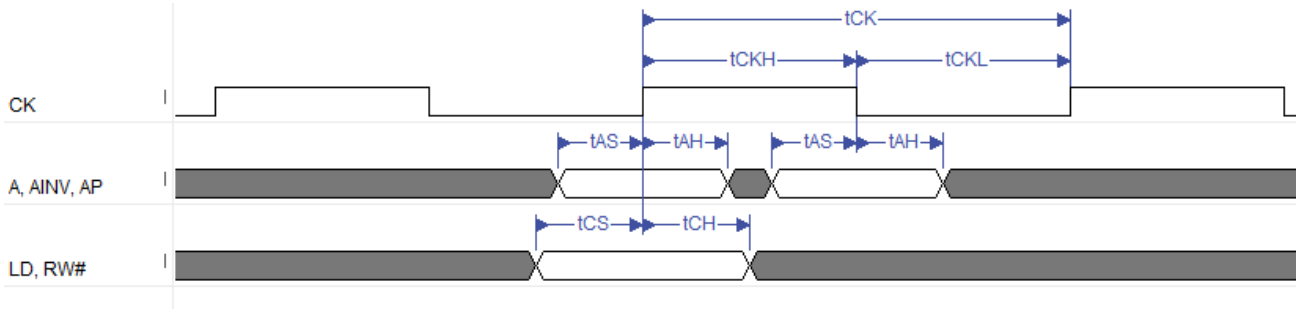
Nominal Rise-Fall Time Definition for Differential Output Signals



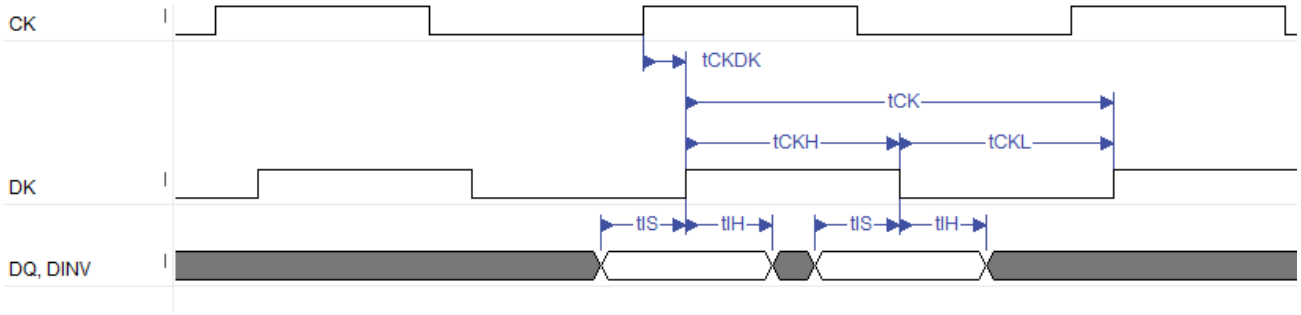
Switching Waveforms (continued)

Figure 9. Input and Output Timing Waveforms

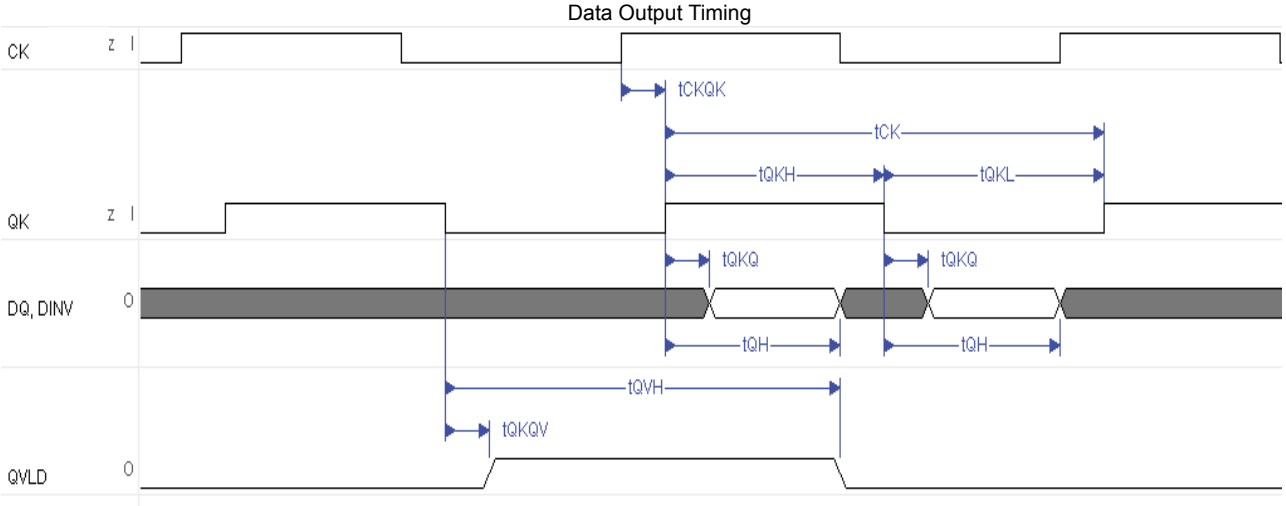
Address and Command Input Timing



Data Input Timing



Data Output Timing



Switching Waveforms (continued)

Figure 10. Waveforms for 8.0 Cycle Read Latency (Read to Write Timing Waveform)

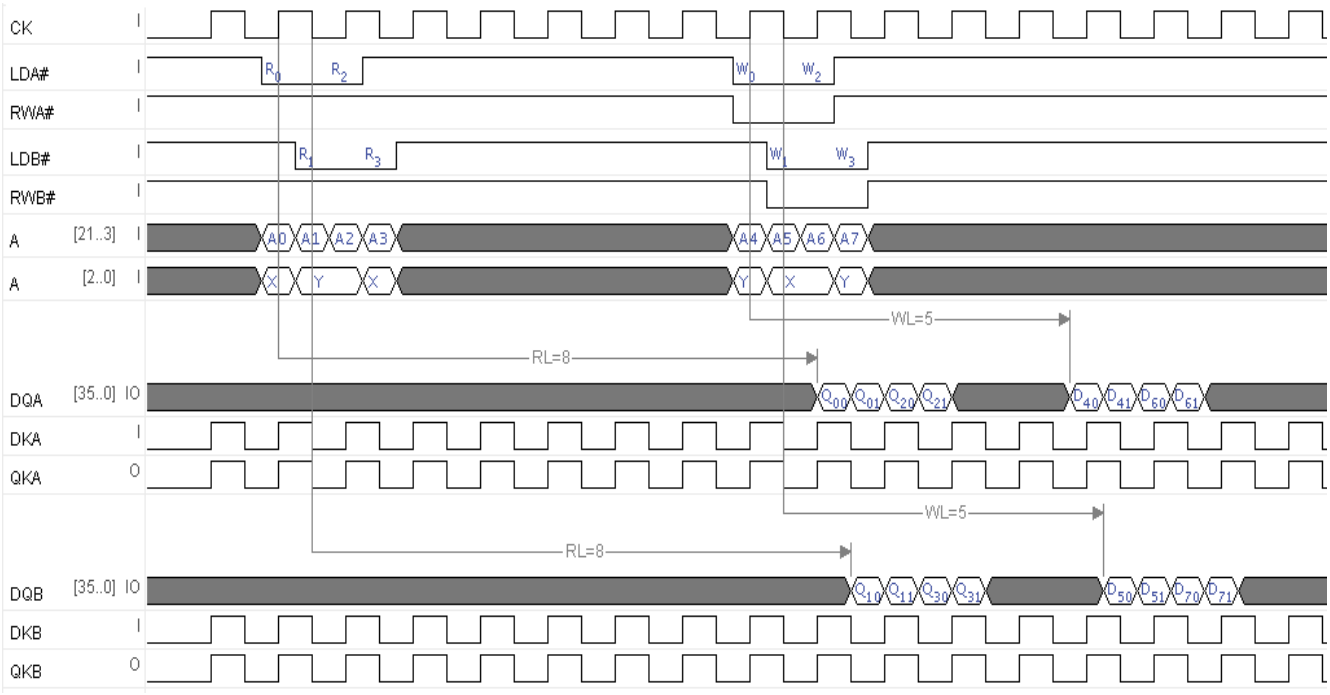
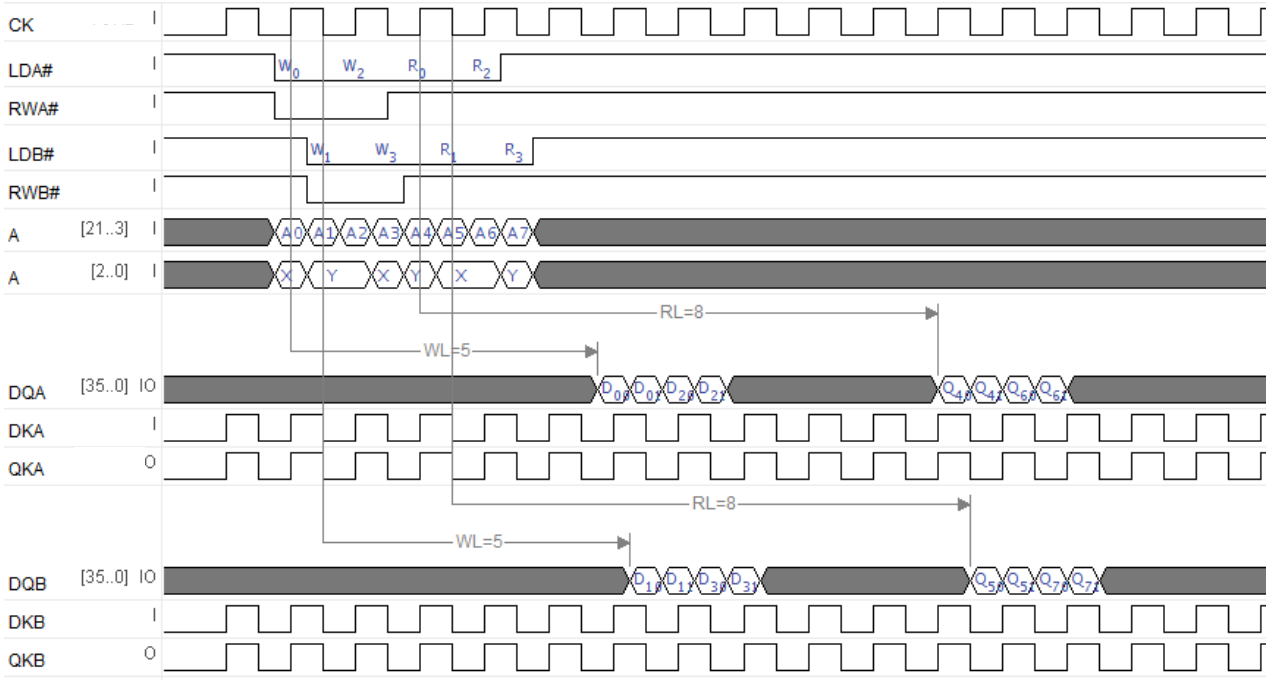


Figure 11. Waveforms for 8.0 Cycle Read Latency (Write to Read Timing Waveform)



Switching Waveforms (continued)

Figure 12. Configuration Write Timing Waveform

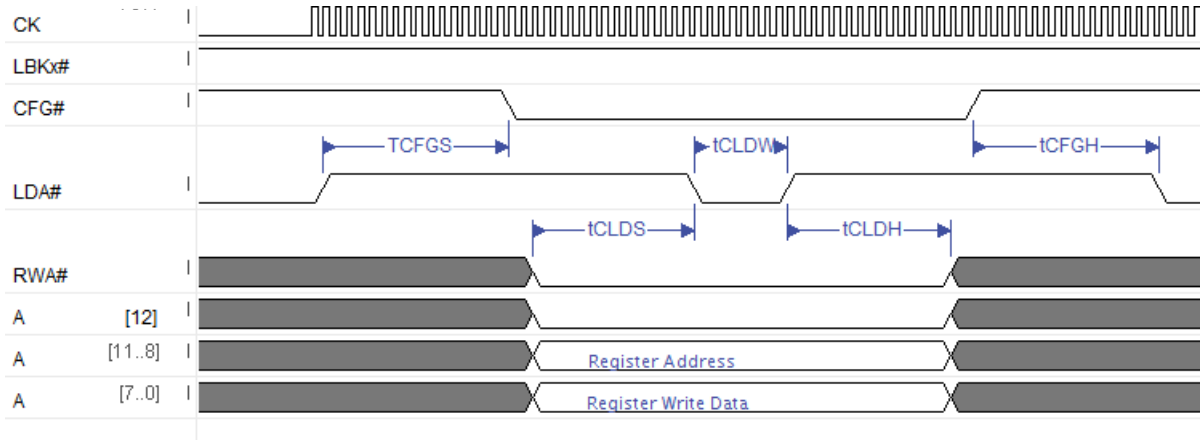
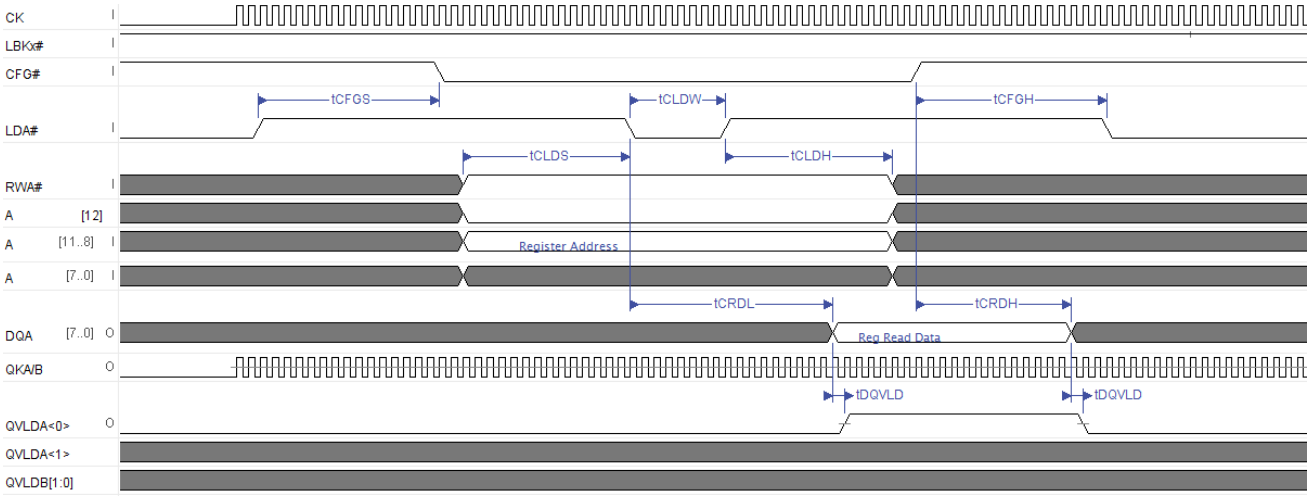


Figure 13. Configuration Read Timing Waveform

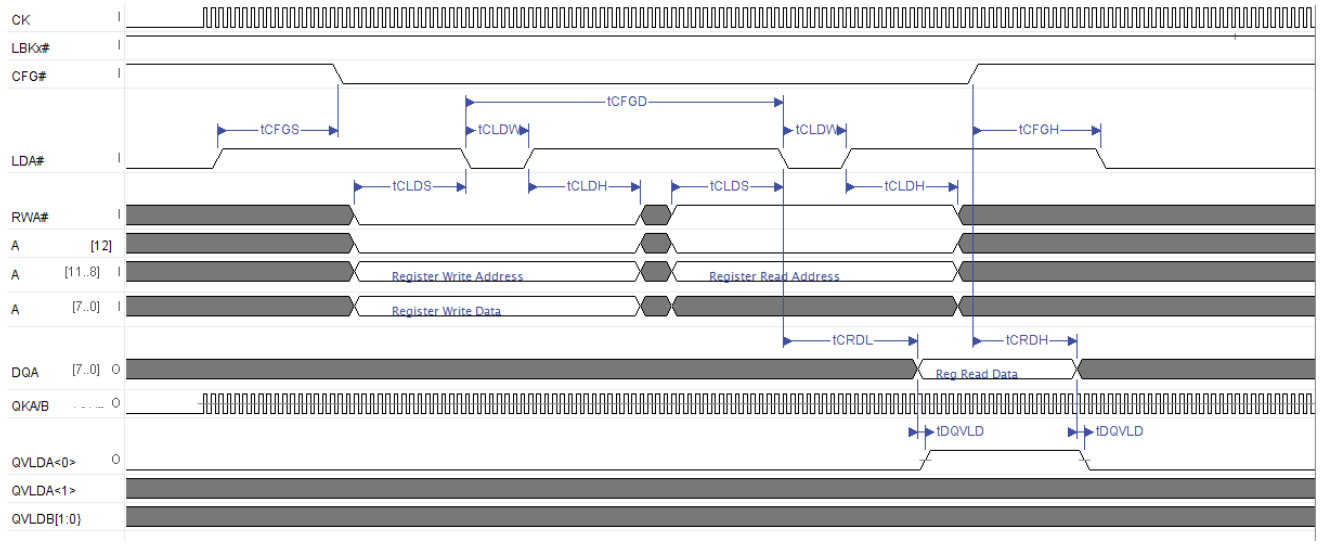


Note: DQA[x:8] and DQB data bus is a don't care in Configuration Mode

Switching Waveforms (continued)

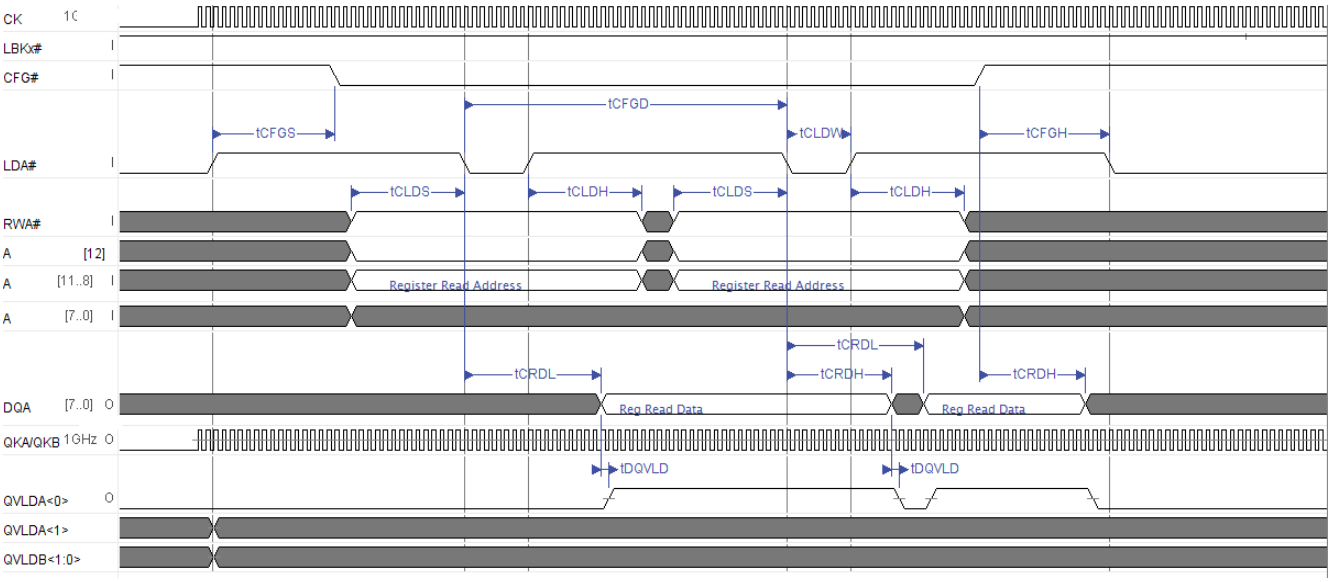
Figure 14. Configuration Write and Read Timing Waveform

(a) Configuration Multiple Cycle - Write followed by Read Operation



Note: DQA[x:8] and DQB data bus is a don't care in Configuration Mode

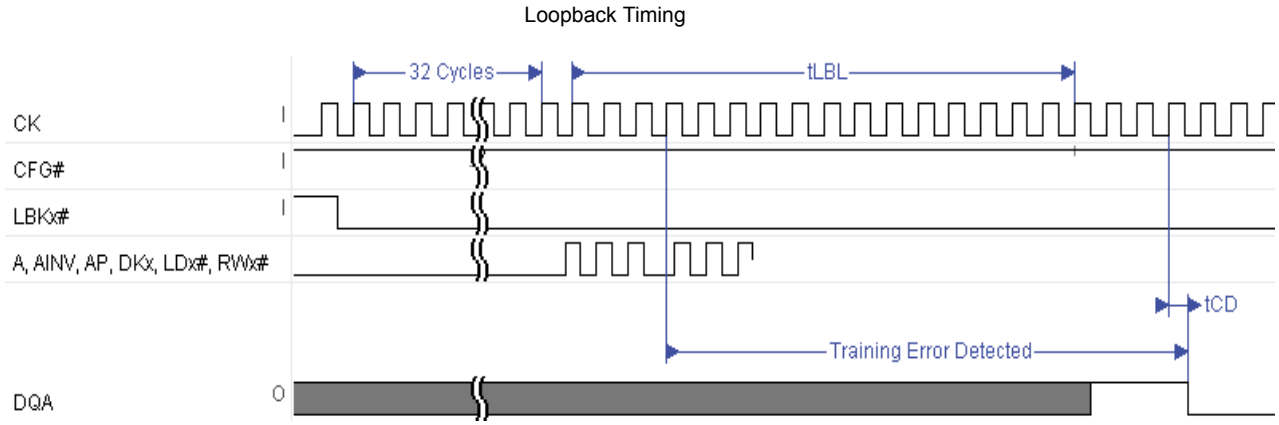
(b) Configuration Multiple Cycle - Back to Back Read Operation



Note: DQA[x:8] and DQB data bus is a don't care in Configuration Mode

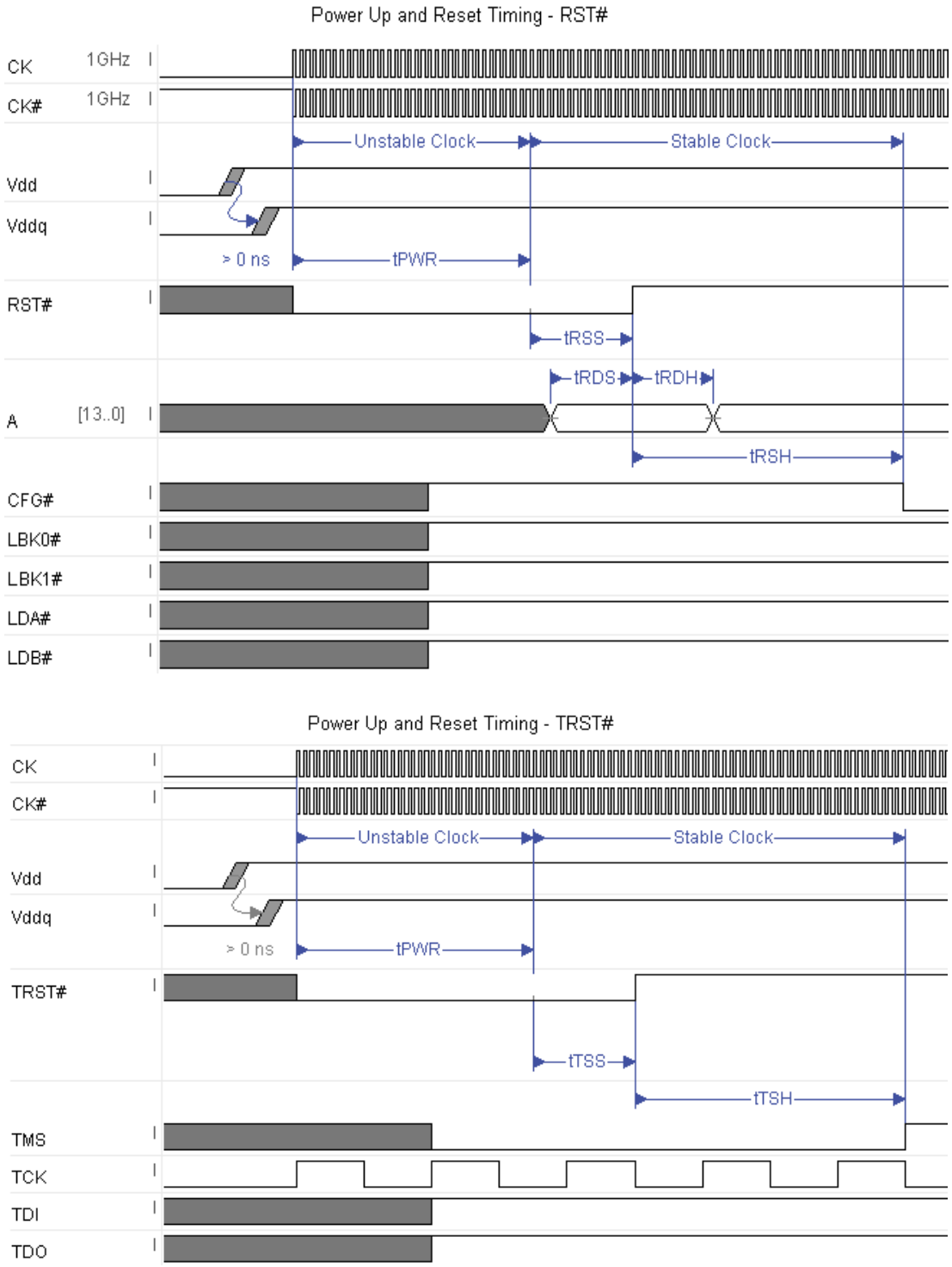
Switching Waveforms (continued)

Figure 15. Loopback TIming



Switching Waveforms (continued)

Figure 16. Reset TImings



Ordering Information

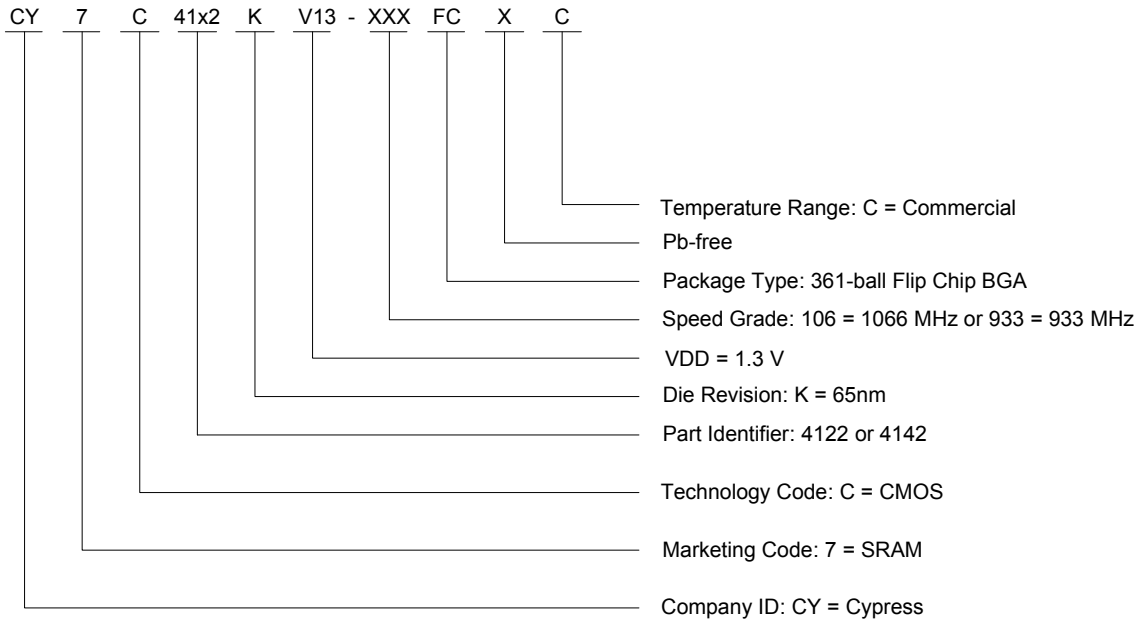
The following table Table 22 contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at http://www.cypress.com/go/datasheet/offices.

Table 22. Ordering Information

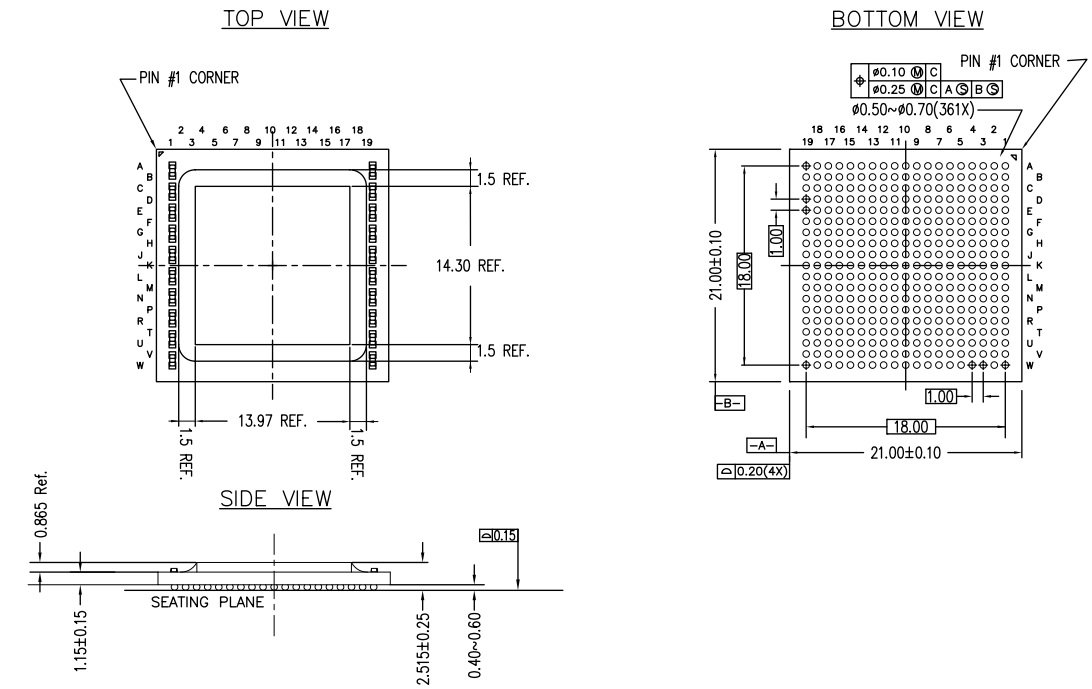
Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
1066	CY7C4122KV13-106FCXC	001-70319	361-ball FCBGA (21 × 21 × 2.515 mm) Pb-free	Commercial
	CY7C4142KV13-106FCXC			
933	CY7C4122KV13-933FCXC	001-70319	361-ball FCBGA (21 × 21 × 2.515 mm) Pb-free	Commercial
	CY7C4142KV13-933FCXC			

Ordering Code Definitions



Package Diagram

Figure 17. 361-ball FCBGA (21 × 21 × 2.515 mm) FR0AA Package Outline, 001-70319



NOTES:

ALL DIMENSIONS ARE IN MILLIMETERS
SOLDER BALL DIAMETER: 0.63
SOLDER PAD TYPE: SOLDER MASK DEFINED (SMD)
PACKAGE CODE: FR0AA

001-70319 *D

Acronyms

Table 23. Acronyms used in this document

Acronym	Description
DDR	Double Data Rate
RTR	Random Transaction Rate
EIA	Electronic Industries Alliance
EMI	Electromagnetic Interference
FCBGA	Flip-Chip Ball Grid Array
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
JTAG	Joint Test Action Group
LMBU	Logical Multiple Bit Upset
LSB	Least Significant Bit
LSBU	Logical Single Bit Upset
MSB	Most Significant Bit
ODT	On-Die Termination
PLL	Phase Locked Loop
QDR	Quad Data Rate
SDR	Single Data Rate
SEL	Single Event Latch-up
SER	Soft Error Rate
SRAM	Static Random Access Memory
TAP	Test Access Port
TCK	Test Clock
TDI	Test Data-In
TDO	Test Data-Out
TMS	Test Mode Select

Document Conventions

Units of Measure

Table 24. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Errata

This section describes the errata for the 144-Mb QDR-IV SRAMs. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Part Numbers Affected

Part Number	Device Characteristics
CY7C4122KV13 / CY7C4142KV13	144-Mbit QDR-IV XP SRAM

QDR-IV Qualification Status

Product Status: In Production

QDR-IV Errata Summary

The following table defines the errata applicability to available QDR-IV family devices.

Items	Part Number	Silicon Revision	Fix Status
1. On-Die Termination (ODT) auto update failure.	CY7C4122KV13 CY7C4142KV13	Revision *C (before DC1444) [24]	Fixed in revision *D silicon (from DC1445)
2. Failure occurs during the No Operation (NOP) followed by the read operation.			

Note
24. DCXXYY: “DC = Date Code”, “XX = Year 20XX”, “YY = Week YY”.

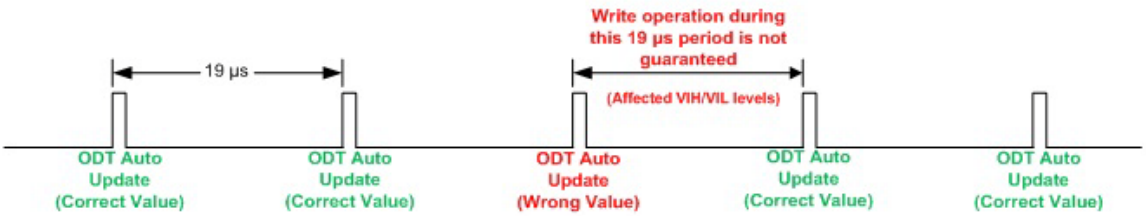
1. On-Die Termination (ODT) auto update failure.

QDR-IV SRAMs support ODT for address, control, clock and data pins. The ODT feature calibrates and updates the termination resistance value every 19 µs if the 'ODT/ZQ Auto Update' configuration register is set to logic HIGH.

■ Problem Definition

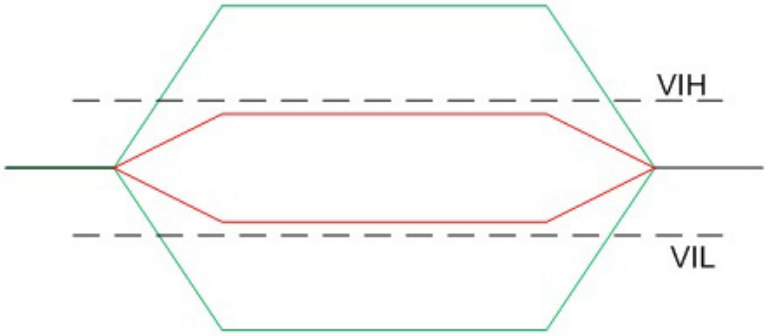
The ODT auto update functionality does not always update the correct ODT value, which can result in the wrong input impedance value and thereby affecting the input VIL/VIH levels (refer to the following figure).

Figure 18. ODT Auto Update Timing



In the case of a correct ODT value update, the QDR-IV gets the input signal with correct VIH/VIL level (signal in green) while in the other case, the input signal attenuates (signal in red) because of the wrong ODT value update and QDR-IV might not recognize the accurate input signal.

Figure 19. Input Signal Representation during ODT update



■ Parameters Affected

The electrical characteristics parameters related to input signal voltage levels are affected.

Parameter	Description
$VIH_{(DC)}$	POD/HSTL/SSTL high-level input voltage
$VIL_{(DC)}$	POD/HSTL/SSTL low level input voltage
$VIH_{(AC)}$	POD/HSTL/SSTL high-level input voltage
$VIL_{(AC)}$	POD/HSTL/SSTL low-level input voltage
$VID_{(DC)}$	POD differential input differential voltage (DC)
$VID_{(AC)}$	POD differential input differential voltage (AC)
VIN	POD single-ended input voltage
$VDIF_{(AC)}$	HSTL/SSTL AC input differential voltage
$VDIF_{(DC)}$	HSTL/SSTL DC input differential voltage
$VDIF_{(CM)}$	HSTL/SSTL DC common mode input

■ **Trigger Condition**

Configuring ODT/ZQ Auto Update configuration register to logic HIGH.

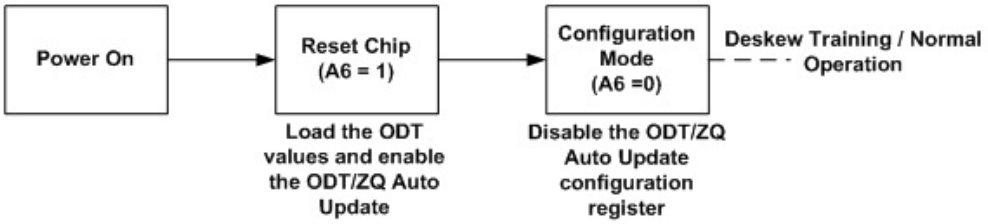
■ **Scope of Impact**

Causes write and read operation failure.

■ **Workaround**

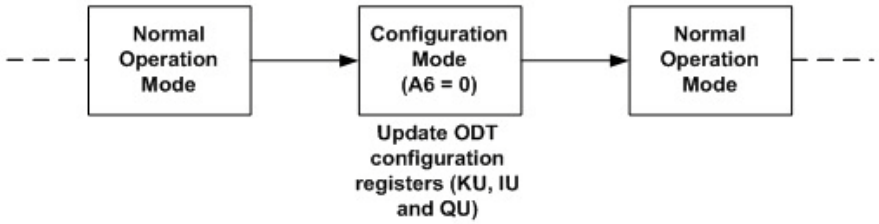
Configure the ODT values for the respective input pins and enable the ODT/ZQ Auto Update configuration register (Logic HIGH) during the power-up by providing the data through A[13:0] at the rising edge of the reset. During this operation, address bit A6 updates the ODT/ZQ Auto Update configuration register bit. Then disable the ODT/ZQ Auto Update configuration register (logic LOW) during the configuration step (refer to the following figure). As a result, the ODT auto update will be disabled during the normal QDR-IV SRAM operation, but the correct termination value will be set.

Figure 20. Workaround (Memory Configuration)



However, the ODT value might vary because of the temperature or voltage variations. In this case as shown in the following figure, perform the manual ODT update by entering in to the configuration mode and update all the ODT configuration registers (KU, IU and QU). The manual ODT update can be scheduled when memory is not being accessed.

Figure 21. Workaround (Manual ODT Configuration)



■ **Fix Status**

The fix for the above issue has been identified and the new silicon available in January, 2015 will not have this defect.

2. Failure occurs during the No Operation (NOP) followed by the read operation.

■ **Problem Definition**

QDR-IV SRAM read operations intermittently fail with a No Operation (NOP) followed by a read operation. The following figure explains about port A operation (at rising edge) and the same explanation can be applied to port B (at falling edge).

Figure 22. Write – NOP – Read Condition

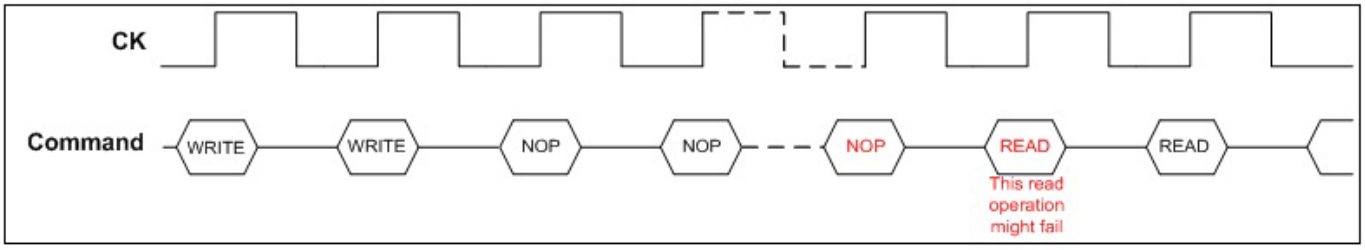
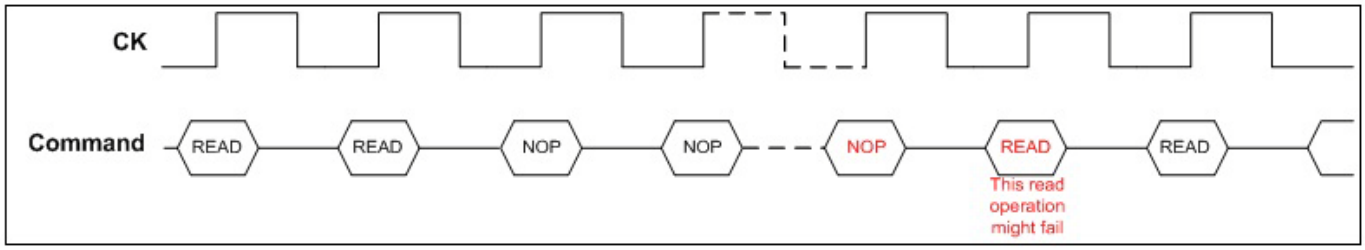


Figure 23. Read – NOP – Read Condition



■ **Parameters Affected**

Functional failures.

■ **Trigger Condition(s)**

No Operation (NOP) followed by the read operation sometimes resulting in a read failure.

■ **Scope of Impact**

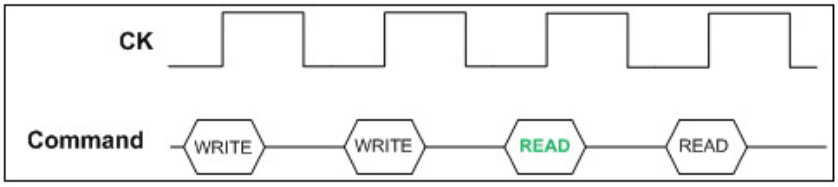
Causes read operation failure on output data bits.

■ **Workaround**

There are three identified workarounds to avoid NOP before the read operation.

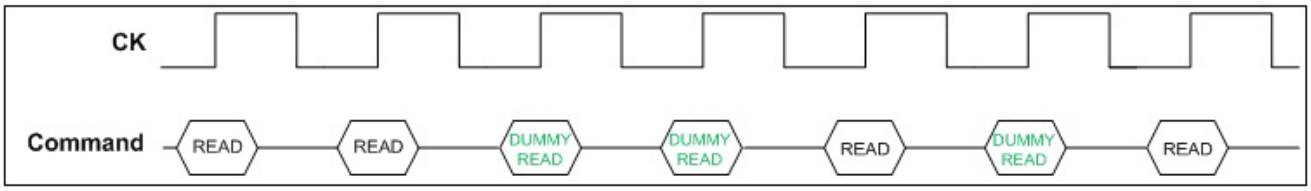
a. In the case of write operation – NOP – read operation sequence if possible, ignore the NOP between the write and read operation and perform a write operation followed by the read operation to avoid the NOP prior to the read operation.

Figure 24. Write – Read Condition



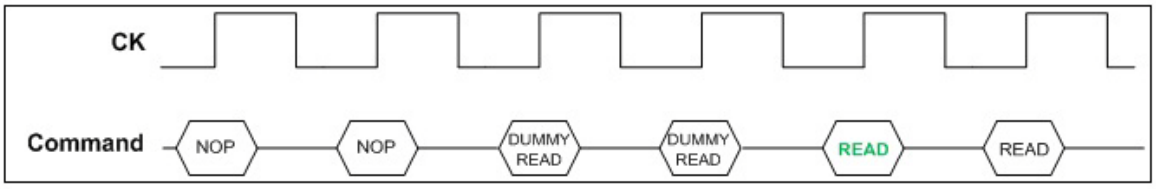
b. Insert the dummy reads between the real read operations to avoid the NOP between the read operations. For an example, if the functionality needs one or two NOP cycles between the read operations then insert the dummy reads accordingly instead of NOP cycles as shown in the figure below.

Figure 25. Read – Dummy Read – Read Condition



c. In the case of NOP followed by the read operation, perform two dummy reads and only consider the data from the third read access (Ignore the data from the first two read accesses)

Figure 26. NOP – Dummy Read – Read Condition



■ **Fix Status**

The fix for the above issue has been identified and the new silicon available in January, 2015 will not have this defect.

Document History Page

Document Title: CY7C4122KV13/CY7C4142KV13, 144-Mbit QDR™-IV XP SRAM Document Number: 001-68255				
Rev.	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
*J	4283232	03/25/2014	PRIT	Post to web.
*K	4410859	06/17/2014	PRIT	Updated AC Test Load and Waveform: Updated Figure 7 (Changed value of RQ resistor from 200 Ω to 180 Ω). Updated Switching Characteristics: Added t_{ASH}, t_{CSH}, t_{ISH} parameters and their details. Updated Note 20 and 23. Completing Sunset Review.
*L	4502995	09/15/2014	PRIT	Updated Switching Characteristics: Updated Note 23. Updated Package Diagram: spec 001-70319 – Changed revision from *C to *D.
*M	4573944	11/19/2014	PRIT	Updated Functional Description: Added “For a complete list of related resources, click here.” at the end. Added Errata.

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