

## FGMD12SR6020\*A

## Data Sheet

3-14.4Vdc Input, 20A, 0.45-5.5Vdc Output

The Digital **Tomodachi** Series of non-isolated dc-dc converters deliver exceptional electrical and thermal performance in DOSA based footprints for Point-of-Load converters. Operating from a 3.0Vdc-14.4Vdc input, these are the converters of choice for Intermediate Bus Architecture (IBA) and Distributed Power Architecture applications that require high efficiency, tight regulation, and high reliability in elevated temperature environments with low airflow. The PMBus interface supports a range of commands to both control and monitor the module. The module also includes the Tunable Loop™ feature that allows the user to optimize the dynamic response of the converter to match the load with reduced amount of output capacitance leading to savings on cost and PWB area.

The **FGMD12SR6020\*A** converter of the **Tomodachi** Series delivers 20A of output current at a tightly regulated programmable and PMBus control output voltage of 0.45Vdc to 5.5Vdc. The thermal performance of the **FGMD12SR6020\*A** is best-in-class: Little derating is needed up to 85°C, under natural convection.

### Applications

- Intermediate Bus Architecture
- Telecommunications
- Data/Voice processing
- Distributed Power Architecture
- Computing (Servers, Workstations)
- Test Equipments



### Features

- Compliant to RoHS EU Directive 2002/95/EC
- Delivers up to 20A (110W)
- High efficiency, no heatsink required
- Negative and Positive ON/OFF logic
- DOSA based
- Small size: 20.32 x 11.43 x 8.5mm (0.8 in x 0.45 in x 0.335 in)
- Tape & reel packaging
- Programmable output voltage from 0.6V to 5.5V via external resistor. Digitally adjustable down to 0.45Vdc
- Digital interface through the PMBus™ # protocol
- Tunable Loop™ to optimize dynamic output voltage response
- Flexible output voltage sequencing EZ-SEQUENCE
- Power Good signal
- Fixed switching frequency with capability of external synchronization
- Auto-reset output over-current protection
- Remote ON/OFF
- Ability to sink and source current
- No minimum load required
- Start up into pre-biased output
- UL\* 60950-1 2<sup>nd</sup> Ed. Recognized, CSA† C22.2 No. 60950-1-07 Certified, and VDE‡ (EN60950-1 2<sup>nd</sup> Ed.) (Pending)
- ISO\*\* 9001 and ISO 14001 certified manufacturing facilities

\* UL is a registered trademark of Underwriters Laboratories, Inc.

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**Absolute Maximum Ratings**

Stresses in excess of the absolute maximum ratings may lead to degradation in performance and reliability of the converter and may result in permanent damage.

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
<b>ABSOLUTE MAXIMUM RATINGS<sup>1</sup></b>					
Input Voltage	Continuous	-0.3		15	Vdc
SEQ, SYNC, Vs+				7	Vdc
CLK, DATA, SMBALERT				3.6	Vdc
Operating Temperature	Ambient temperature	-40		85	°C
Storage Temperature		-55		125	°C
Output Voltage		0.45		5.5	Vdc

**Electrical Specifications**

All specifications apply over specified input voltage, output load, and temperature range, unless otherwise noted.

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
<b>INPUT CHARACTERISTICS</b>					
Operating Input Voltage Range		3.0		14.4	Vdc
Maximum Input Current	Vin=3V to 14V, Io-max			19	Adc
Input Stand-by Current	Vin=12V, module disabled		16.4		mA
Input No Load Current	Vout=5.0V		134		mA
	Vout=0.6V		69		mA
Inrush Transient, I <sup>2</sup> t				1	A <sup>2</sup> s
Input Reflected-Ripple Current	Peak-to-peak (5Hz to 20MHz, 1uH source impedance; Vin=0 to 14V, Io-max)		50		mAp-p
Input Ripple Rejection (120Hz)			-64		dB

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### Electrical Specifications (Continued)

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
<b>OUTPUT CHARACTERISTICS</b>					
Output Voltage Set Point	With 0.1% tolerance for external resistor used to set output voltage	-1.0		+1.0	%Vout
Output Voltage Range	(Over all operating input voltage, resistive load and temperature conditions until end of life)	-3.0		+3.0	%Vout
Adjustment Range (selected by an external resistor)	Some output voltages may not be possible depending on the input voltage – see feature description section	0.6		5.5	Vdc
PMBus Adjustable Output Voltage Range		-25		+25	%Vout
PMBus Output Voltage Adjustment Step Size			0.4		%Vout
Remote Sense Range				0.5	Vdc
Output Regulation (for $V_o \geq 2.5Vdc$ )	Line ( $V_{in}$ = min to max)			0.4	% Vout
	Load ( $I_o$ = min to max)			10	mV
Output Regulation (for $V_o < 2.5Vdc$ )	Line ( $V_{in}$ = min to max)			5	mV
	Load ( $I_o$ = min to max)			10	mV
Output Ripple and Noise	$V_{in}=12V$ , $I_o$ = min to max, $C_o$ = 0.1uF+22uF ceramic capacitors				
Peak to Peak	5MHz to 20MHz bandwidth		50	100	mVp-p
RMS	5MHz to 20MHz bandwidth		20	38	mVrms
External Load Capacitance <sup>1</sup>	Plus full load (resistive)				%
Without the Tunable Loop	$ESR \geq 1m\Omega$	2x47		4x47	uF
With the Tunable Loop	$ESR \geq 0.15m\Omega$	2x47		1,000	uF
	$ESR \geq 10m\Omega$	2x47		10,000	uF
Output Current Range	(in either sink or source mode)	0		20	Adc
Output Current Limit Inception (Hiccup mode)	Current limit does not operate in sink mode		130		% $I_o$ -max
Output Short-Circuit Current	$V_o \leq 250mV$ , Hiccup mode		1.4		Arms
Efficiency					
$V_{in} = 12Vdc$ , $T_a = 25^\circ C$ , $I_o = max$	$V_{out}=5.0Vdc$		95.2		%
	$V_{out}=3.3Vdc$		93.8		%
	$V_{out}=2.5Vdc$		92.6		%
	$V_{out}=1.8Vdc$		90.4		%
	$V_{out}=1.2Vdc$		87.1		%
	$V_{out}=0.6Vdc$		79.2		%

<sup>1</sup> External capacitors may require using the new Tunable Loop™ feature to ensure that the module is stable as well as getting the best transient response. See the Tunable Loop™ section for details.

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## Electrical Specifications (Continued)

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
Switching Frequency			500		kHz
Frequency Synchronization					
Synchronization Frequency Range		425		600	kHz
High Level Input Voltage		2.0			V
Low Level Input Voltage				0.4	V
Input Current, SYNC				100	nA
Minimum Pulse Width, SYNC		100			nS
Maximum SYNC rise time		100			nS

## General Specifications

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
Calculated MTBF	$I_o = 0.8 * I_{o-max}$ , $T_a = 40^{\circ}\text{C}$ Telecordia Issue 2 Method 1 Case 3		15,455,614		Hours
Weight			4.45(0.16)		g (oz.)

## Feature Specifications

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
ON/OFF Signal Interface	$V_{in} = \text{min to max}$ , open collector or equivalent, Signal reference to GND				
Positive Logic					
Logic High (Module ON)					
Input High Current				1	mA
Input High Voltage		2.0		$V_{in-max}$	V
Logic Low (Module OFF)					
Input Low Current				1	mA
Input Low Voltage		-0.2		0.6	V
Negative Logic	On/Off pin is open collector/drain logic input with external pull-up resistor; signal reference to GND				
Logic High (Module OFF)					
Input High Current				1	mA
Input High Voltage		2		$V_{in-max}$	V
Logic Low (Module ON)					
Input Low Current				10	uA
Input Low Voltage		-0.2		0.6	V

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### Feature Specifications

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
Turn-On Delay Time	Vin = Vin-nom, Io = Io-max, Vo to within $\pm 1\%$ of steady state				
Case 1: On/Off input is enabled and then input power is applied	delay from instant at which Vin = Vin-min until Vo = 10% of Vo-set		1.2		ms
Case 2: Input power is applied for at least one second and then the On/Off input is enabled	delay from instant at which Von/Off is enabled until Vo = 10% of Vo-set		800		us
Output voltage Rise time	time for Vo to rise from 10% of Vo-set to 90% of Vo-set		2.7		ms
Output voltage overshoot with or without maximum external capacitance	Ta = 25°C, Vin = Vin-min to Vin-max, Io = Io-min to Io-max			3.0	%Vout
Over Temperature Protection	(See Thermal Considerations section)		120		°C
PMBus Over Temperature Warning Threshold *			130		°C
Tracking Accuracy	Vin-min to Vom-max, Io-min to Io-max, VSEQ < Vo				
Power-Up: 2V/ms				100	mV
Power-Down: 2V/ms				100	mV
Input Under Voltage Lockout					
Turn-on Threshold				3.25	Vdc
Turn-off Threshold		2.6			Vdc
Hysteresis			0.25		Vdc
PMBus Adjustable Input Under Voltage Lockout Thresholds		2.5		14	Vdc
Resolution of Adjustable Input Under Voltage Threshold				500	mV
PGOOD (Power Good)					
Signal Interface Open Drain, Vsupply $\leq$ 5VDC					
Overvoltage threshold for PGOOD ON			108		%Vout
Overvoltage threshold for PGOOD OFF			105		%Vout
Undervoltage threshold for PGOOD ON			92		%Vout
Undervoltage threshold for PGOOD OFF			90		%Vout
Pulldown resistance of PGOOD pin				50	$\Omega$
Sink current capability into PGOOD pin				5	mA

\* Over temperature Warning – Warning may not activate before alarm and unit may shutdown before warning

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## Digital Interface Specifications

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
<b>PMBus Signal Interface Characteristics</b>					
Input High Voltage (CLK, DATA)		2.1		3.6	V
Input Low Voltage (CLK, DATA)				0.8	V
Input high level current (CLK, DATA)		-10		10	uA
Input low level current (CLK, DATA)		-10		10	uA
Output Low Voltage (CLK, DATA, SMBALERT#)	I <sub>OUT</sub> =2mA			0.4	V
Output high level open drain leakage current (DATA, SMBALERT#)	V <sub>OUT</sub> =3.6V	0		10	uA
Pin capacitance			0.7		pF
PMBus Operating frequency range	Slave Mode	10		400	kHz
Data hold time	Receive Mode	0			nS
	Transmit Mode	300			nS
Data setup time		250			nS
<b>Measurement System Characteristics</b>					
Read delay time		153	192	231	us
Output current measurement range		0		26	A
Output current measurement resolution		62.5			mA
Output current measurement gain accuracy (at 25°C)				±5	%
Output current measurement offset				0.1	A
V <sub>out</sub> measurement range		0		5.5	V
V <sub>out</sub> measurement resolution			15.625		mV
V <sub>out</sub> measurement accuracy		-15		5	%
V <sub>out</sub> measurement offset		-3		3	%
V <sub>in</sub> measurement range		0		14.4	V
V <sub>in</sub> measurement resolution			32.5		mV
V <sub>in</sub> measurement accuracy		-15		5	%
V <sub>in</sub> measurement offset		-5.5	-2	1.4	%

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### Design Considerations

#### Input Filtering

The **FGMD12SR6020\*A** converter should be connected to a low ac-impedance source. A highly inductive source can affect the stability of the module. An input capacitance must be placed directly adjacent to the input pin of the module, to minimize input ripple voltage and ensure module stability.

To minimize input voltage ripple, ceramic capacitors are recommended at the input of the module. Fig-1 shows the input ripple voltage for various output voltages at 20A of load current with 2x22uF or 3x22uF ceramic capacitors and an input of 12V.

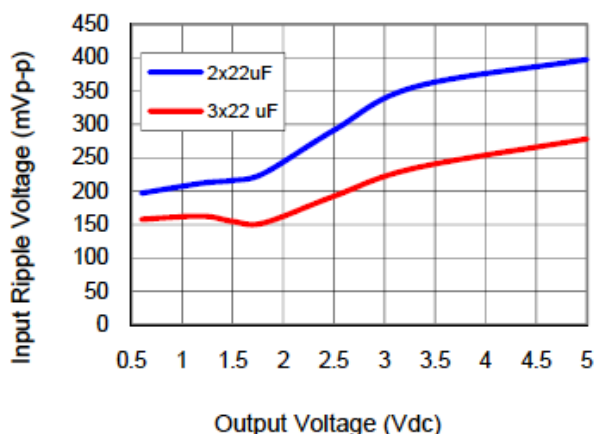


Fig-1: Input ripple voltage for various output voltages with 2x22uF or 3x22uF ceramic capacitors at the input (20A load). Input voltage is 12V.

#### Output Filtering

The **FGMD12SR6020\*A** is designed for low output ripple voltage and will meet the maximum output ripple specification with 0.1uF ceramic and 2x47uF ceramic capacitors at the output of the module. However, additional output filtering may be required by the system designer for a number of reasons. First, there may be a need to further reduce the output ripple and noise of the module. Second, the dynamic response characteristics may need to be customized to a particular load step change.

To reduce the output ripple and improve the dynamic response to a step load change, additional capacitance at the output can be used. Low ESR polymer and ceramic capacitors are recommended to

improve the dynamic response of the module. Fig-2 provides output ripple information for different external capacitance values at various Vo and a full load current of 20A. For stable operation of the module, limit the capacitance to less than the maximum output capacitance as specified in the electrical specification table. Optimal performance of the module can be achieved by using the Tunable Loop™ feature described later in this data sheet.

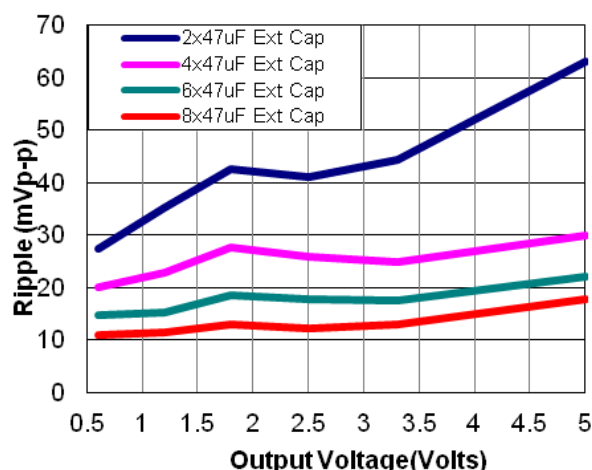


Fig-2: Output ripple voltage for various output voltages with external 2x47uF, 4x47uF, 6x47uF or 8x47uF ceramic capacitors at the output (20A load). Input voltage is 12V.

#### Safety Consideration

For safety agency approval the power module must be installed in compliance with the spacing and separation requirements of the end-use safety agency standards, i.e., UL 60950-1 2nd, CSA C22.2 No. 60950-1-07, DIN EN 60950-1:2006 + A11 (VDE0805 Teil 1 + A11):2009-11; EN 60950-1:2006 + A11:2009-03.

For the converter output to be considered meeting the requirements of safety extra-low voltage (SELV), the input must meet SELV requirements. The power module has extra-low voltage (ELV) outputs when all inputs are ELV.

The FGMD12SR6020\*A series were tested using an external Littelfuse 456 series fast-acting fuse rated at 30A, 100 Vdc in the ungrounded input.



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### Analog Feature Descriptions

#### Remote On/Off

The module can be turned ON and OFF either by using the ON/OFF pin (Analog interface) or through the PMBus interface (Digital). The module can be configured in a number of ways through the PMBus interface to react to the two ON/OFF inputs:

- Module ON/OFF can be controlled only through the analog interface (digital interface ON/OFF commands are ignored)
- Module ON/OFF can be controlled only through the PMBus interface (analog interface is ignored)
- Module ON/OFF can be controlled by either the analog or digital interface

The default state of the module (as shipped from the factory) is to be controlled by the analog interface only. If the digital interface is to be enabled, or the module is to be controlled only through the digital interface, this change must be made through the PMBus. These changes can be made and written to non-volatile memory on the module so that it is remembered for subsequent use.

#### Analog ON/OFF

The **FGMD12SR6020\*A** power modules feature an On/Off pin for remote On/Off operation. Two On/Off logic options are available. In the Positive Logic On/Off option, (device code suffix "P" - see Ordering Information), the module turns ON during a logic High on the On/Off pin and turns OFF during a logic Low. With the Negative Logic On/Off option, (device code suffix "N" - see Ordering Information), the module turns OFF during logic High and ON during logic Low. The On/Off signal should be always referenced to ground. For either On/Off logic option, leaving the On/Off pin disconnected will turn the module ON when input voltage is present.

For positive logic modules, the circuit configuration for using the On/Off pin is shown in Figure 39. When the external transistor Q2 is in the OFF state, the internal transistor Q7 is turned ON, which turns Q3 OFF which keeps Q6 OFF and Q5 OFF. This allows the internal PWM #Enable signal to be pulled up by the internal 3.3V, thus turning the module ON. When transistor Q2 is turned ON, the On/Off pin is pulled low, which turns Q7 OFF which turns Q3, Q6 and Q5 ON and the internal PWM #Enable signal is pulled low and the module is OFF. A suggested value for  $R_{pullup}$  is 20k $\Omega$ .

For negative logic On/Off modules, the circuit configuration is shown in Fig. 40. The On/Off pin should be pulled high with an external pull-up resistor

(suggested value for the 3V to 14V input range is 20k $\Omega$ ). When transistor Q2 is in the OFF state, the On/Off pin is pulled high, transistor Q3 is turned ON. This turns Q6 ON, followed by Q5 turning ON which pulls the internal ENABLE low and the module is OFF. To turn the module ON, Q2 is turned ON pulling the On/Off pin low, turning transistor Q3 OFF, which keeps Q6 and Q5 OFF resulting in the PWM Enable pin going high.

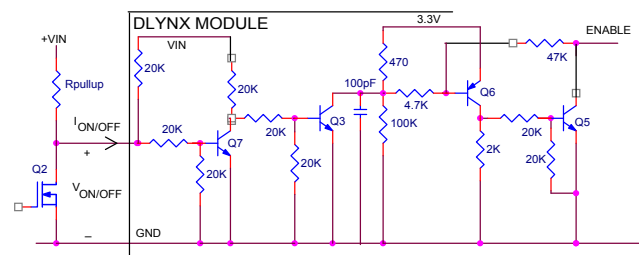


Fig-3: Circuit configuration for using positive On/Off logic.

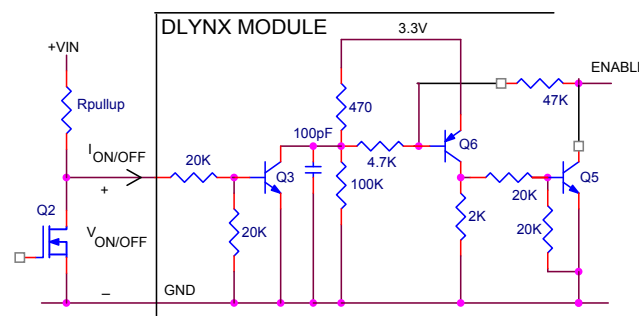


Fig-4: Circuit configuration for using negative On/Off logic.

#### Digital ON/OFF

Please see the Digital Feature Descriptions section.

#### Monotonic Start-up and Shut-down

The module has monotonic start-up and shutdown behavior for any combination of rated input voltage, output current and operating temperature range.

#### Startup into Pre-biased Output



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The module can start into a prebiased output as long as the prebias voltage is 0.5V less than the set output voltage.

### Analog Output Voltage Programming

The output voltage of the module is programmable to any voltage from 0.6dc to 5.5Vdc by connecting a resistor between the Trim and SIG\_GND pins of the module. Certain restrictions apply on the output voltage set point depending on the input voltage. These are shown in the Output Voltage vs. Input Voltage Set Point Area plot in Fig-5. The Upper Limit curve shows that for output voltages lower than 1V, the input voltage must be lower than the maximum of 14.4V. The Lower Limit curve shows that for output voltages higher than 0.6V, the input voltage needs to be larger than the minimum of 3V.

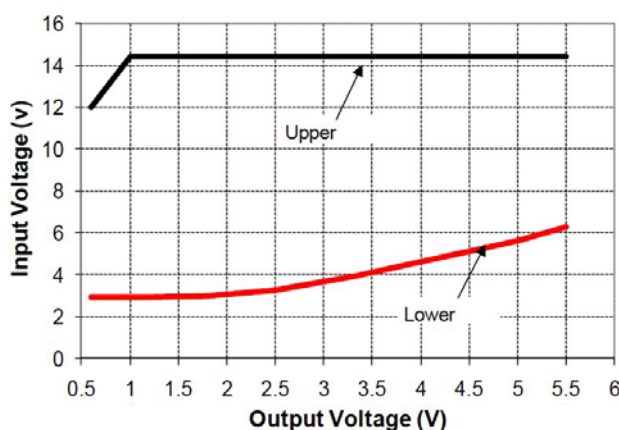
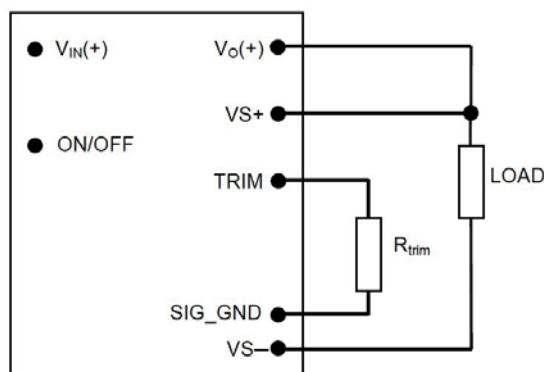


Fig-5: Output Voltage vs. Input Voltage Set Point Area plot showing limits where the output voltage can be set for different input voltages.



**Caution** – Do not connect SIG\_GND to GND elsewhere in the layout.

Fig-6: Output Voltage vs. Input Voltage Set Point Area plot showing limits where the output voltage can be set for different input voltages.

Without an external resistor between Trim and SIG\_GND pins, the output of the module will be 0.6Vdc. To calculate the value of the trim resistor,  $R_{trim}$  for a desired output voltage, should be as per the following equation:

$$R_{TRIM} = \frac{12}{(V_{O-REQ} - 0.6)} [k\Omega]$$

$R_{trim}$  is the external resistor in kohm  
 $V_{o-req}$  is the desired output voltage

Note that the tolerance of a trim resistor will affect the tolerance of the output voltage. Standard 1% or 0.5% resistors may suffice for most applications; however, a tighter tolerance can be obtained by using two resistors in series instead of one standard value resistor.

Table 1 lists calculated values of  $R_{TRIM}$  for common output voltages. For each value of  $R_{TRIM}$ , Table 1 also shows the closest available standard resistor value.

Table 1: Trim Resistor Value	
$V_{O-REG}$ [V]	$R_{TRIM}$ [k $\Omega$ ]
0.6	Open
0.9	40
1.0	30
1.2	20
1.5	13.33
1.8	10
2.5	6.316
3.3	4.444
5.0	2.727

### Digital Output Voltage Adjustment

Please see the Digital Feature Descriptions section.

### Remote Sense

The power module has a Remote Sense feature to minimize the effects of distribution losses by regulating the voltage at the SENSE pins. The voltage between the SENSE pin and VOUT pin should not exceed 0.5V

### Analog Voltage Margining

Output voltage margining can be implemented in the module by connecting a resistor,  $R_{margin-up}$ , from

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the Trim pin to the ground pin for margining-up the output voltage and by connecting a resistor, Rmargin-down, from the Trim pin to output pin for margining-down. Fig-7 shows the circuit configuration for output voltage margining. The POL Programming Tool, available at [www.fdk.com](http://www.fdk.com) under the Downloads section, also calculates the values of Rmargin-up and Rmargin-down for a specific output voltage and % margin. Please consult your local FDK FAE for additional details.

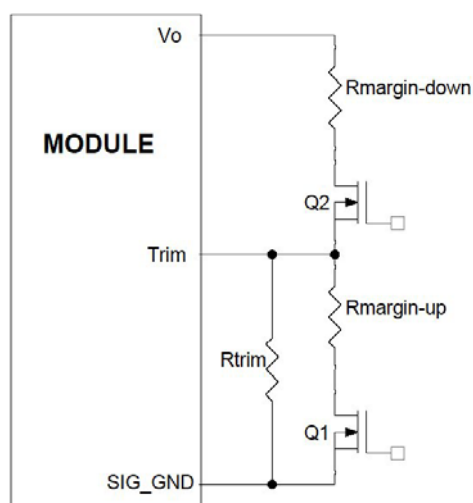


Fig-7: Circuit Configuration for margining Output Voltage.

### Digital Output Voltage Margining

Please see the Digital Feature Descriptions section.

### Output Voltage Sequencing

The power module includes a sequencing feature, EZSEQUENCE that enables users to implement various types of output voltage sequencing in their applications. This is accomplished via an additional sequencing pin. When not using the sequencing feature, leave it unconnected.

The voltage applied to the SEQ pin should be scaled down by the same ratio as used to scale the output voltage down to the reference voltage of the module. This is accomplished by an external resistive divider connected across the sequencing voltage before it is fed to the SEQ pin as shown in Fig-8. In addition, a small capacitor (suggested value 100pF) should be connected across the lower resistor R1.

For all **Tomodachi** modules, the minimum recommended delay between the ON/OFF signal and the sequencing signal is 10ms to ensure that the

module output is ramped up according to the sequencing signal. This ensures that the module soft-start routine is completed before the sequencing signal is allowed to ramp up.

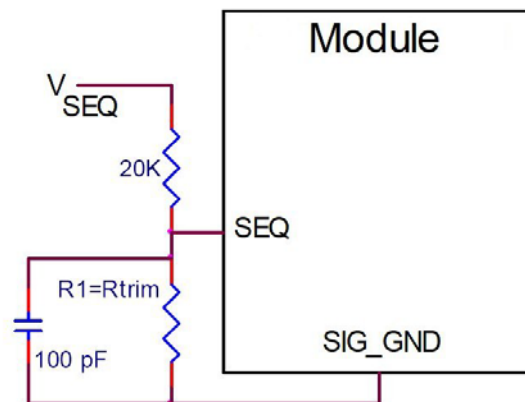


Fig-8: Circuit showing connection of the sequencing signal to the SEQ pin.

When the scaled down sequencing voltage is applied to the SEQ pin, the output voltage tracks this voltage until the output reaches the set-point voltage. The final value of the sequencing voltage must be set higher than the set-point voltage of the module. The output voltage follows the sequencing voltage on a one-to-one basis. By connecting multiple modules together, multiple modules can track their output voltages to the voltage applied on the SEQ pin.

To initiate simultaneous shutdown of the modules, the SEQ pin voltage is lowered in a controlled manner. The output voltage of the modules tracks the voltages below their set-point voltages on a one-to-one basis. A valid input voltage must be maintained until the tracking and output voltages reach ground potential.

Note that in all digital **Tomodachi** series of modules, the PMBus Output Undervoltage Fault will be tripped when sequencing is employed. This will be detected using the STATUS\_WORD and STATUS\_VOUT PMBus commands. In addition, the SMBALERT# signal will be asserted low as occurs for all faults and warnings. To avoid the module shutting down due to the Output Undervoltage Fault, the module must be set to continue operation without interruption as the response to this fault (see the description of the PMBus command VOUT\_UV\_FAULT\_RESPONSE for additional information).

### Over-Current Protection

To provide protection in a fault (output overload) condition, the unit is equipped with internal

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current-limiting circuitry and can endure current limiting continuously. At the point of current-limit inception, the unit enters hiccup mode. The unit operates normally once the output current is brought back into its specified range.

### Digital Adjustable Overcurrent Warning

Please see the Digital Feature Descriptions section.

### Over-Temperature Protection

To provide protection in a fault condition, the unit is equipped with a thermal shutdown circuit. The unit will shut down if the over-temperature threshold of 120°C (typ) is exceeded at the thermal reference point Tref. Once the unit goes into thermal shutdown it will then wait to cool before attempting to restart.

### Digital Temperature Status via PMBus

Please see the Digital Feature Descriptions section.

### Digitally Adjustable Output Over and Under Voltage Protection

Please see the Digital Feature Descriptions section.

### Input Under-Voltage Lockout (UVLO)

At input voltages below the input under-voltage lockout limit, the module operation is disabled. The module will begin to operate at an input voltage above the under-voltage lockout turn-on threshold.

### Digitally Adjustable Input Undervoltage Lockout

Please see the Digital Feature Descriptions section.

### Digitally Adjustable Power Good Thresholds

Please see the Digital Feature Descriptions section.

### Synchronization

The module switching frequency can be synchronized to a signal with an external frequency within a specified range. Synchronization can be done by using the external signal applied to the SYNC pin of the module as shown in Fig-1, with the converter being synchronized by the rising edge of the external signal. The Electrical Specifications table

specifies the requirements of the external SYNC signal. If the SYNC pin is not used, the module should free run at the default switching frequency. **If synchronization is not being used, connect the SYNC pin to GND.**

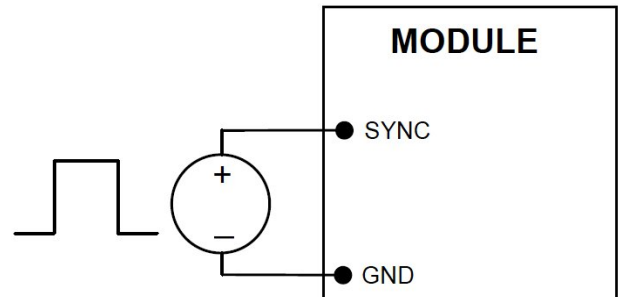


Fig-9: External source connections to synchronize switching frequency of the module.

### Measuring Output Current, Output Voltage and Input Voltage

Please see the Digital Feature Descriptions section.

### Dual Layout

Identical dimensions and pin layout of Analog and Digital **Tomodachi** modules permit migration from one to the other without needing to change the layout. In both cases the trim resistor is connected between trim and signal ground. The output of the analog module cannot be trimmed down to 0.45V

### Power Good

The module provides a Power Good (PGOOD) signal that is implemented with an open-drain output to indicate that the output voltage is within the regulation limits of the power module. The PGOOD signal will be de-asserted to a low state if any condition such as overtemperature, overcurrent or loss of regulation occurs that would result in the output voltage going  $\pm 10\%$  outside the setpoint value. The PGOOD terminal can be connected through a pullup resistor (suggested value 100K $\Omega$ ) to a source of 5VDC or lower.

### Tunable Loop™

The module has a feature that optimizes transient response of the module called Tunable Loop™

External capacitors are usually added to the output of the module for two reasons: to reduce output ripple and noise (see Fig-2) and to reduce output voltage

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deviations from the steady-state value in the presence of dynamic load current changes. Adding external capacitance however affects the voltage control loop of the module, typically causing the loop to slow down with sluggish response. Larger values of external capacitance could also cause the module to become unstable.

The Tunable Loop™ allows the user to externally adjust the voltage control loop to match the filter network connected to the output of the module. The Tunable Loop™ is implemented by connecting a series R-C between the SENSE and TRIM pins of the module, as shown in Fig-11. This R-C allows the user to externally adjust the voltage loop feedback compensation of the module.

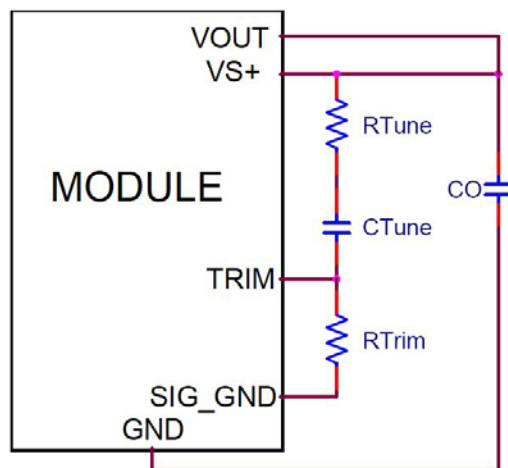


Fig-11: Circuit diagram showing connection of  $R_{TUNE}$  and  $C_{TUNE}$  to tune the control loop of the module.

Recommended values of  $R_{TUNE}$  and  $C_{TUNE}$  for different output capacitor combinations are given in Tables 2 and 3. Table 2 shows the recommended values of  $R_{TUNE}$  and  $C_{TUNE}$  for different values of ceramic output capacitors up to 1000uF that might be needed for an application to meet output ripple and noise requirements. Selecting  $R_{TUNE}$  and  $C_{TUNE}$  according to Table 2 will ensure stable operation of the module. In applications with tight output voltage limits in the presence of dynamic current loading, additional output capacitance will be required. Table 3 lists recommended values of  $R_{TUNE}$  and  $C_{TUNE}$  in order to meet 2% output voltage deviation limits for some common output voltages in the presence of a 10A to 20A step change (50% of full load), with an input voltage of 12V.

Please contact your FDK technical representative to obtain more details of this feature as well as for guidelines on how to select the right value of external

R-C to tune the module for best transient performance and stable operation for other output capacitance values or input voltages other than 12V.

**Table 2: General recommended value of  $R_{TUNE}$  and  $C_{TUNE}$  for  $V_{in}=12V$  and various external ceramic capacitor combinations.**

Co	2x47uF	4x47uF	6x47uF	10x47uF	20x47uF
$R_{TUNE}$	330	330	270	220	180
$C_{TUNE}$	47pF	560pF	1200pF	2200pF	4700pF

**Table 3: Recommended values of  $R_{TUNE}$  and  $C_{TUNE}$  to obtain transient deviation of 2% of  $V_{out}$  for a 10A step load with  $V_{in}=12V$ .**

Vo	5V	3.3V	2.5V	1.8V	1.2V	0.6V
Co	8x47uF	5x47uF + 330uF Polymer	2x47uF + 2x330uF Polymer	2x47uF + 3x330uF Polymer	1x47uF + 5x330uF Polymer	1x47uF + 11x330uF Polymer
$R_{TUNE}$	220	220	220	220	180	180
$C_{TUNE}$	1500pF	2200pF	3300pF	5600pF	10nF	47nF
$\Delta V$	100mV	64mV	49mV	36mV	24mV	12mV

Note: The capacitors used in the Tunable Loop table are 47uF/3m ESR ceramic and 330uF/12m ESR polymer capacitors.



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### Digital Feature Description

#### PMBus Interface Capability

The 20A Digital **Tomodachi** power modules have a PMBus interface that supports both communication and control. The PMBus Power Management Protocol Specification can be obtained from [www.pmbus.org](http://www.pmbus.org). The modules support a subset of version 1.1 of the specification (see Table 6 for a list of the specific commands supported). Most module parameters can be programmed using PMBus and stored as defaults for later use.

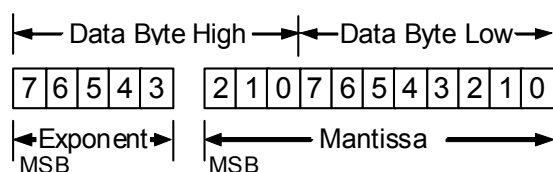
All communication over the module PMBus interface must support the Packet Error Checking (PEC) scheme. The PMBus master must generate the correct PEC byte for all transactions, and check the PEC byte returned by the module.

The module also supports the SMBALERT response protocol whereby the module can alert the bus master if it wants to talk. For more information on the SMBus alert response protocol, see the System Management Bus (SMBus) specification.

The module has non-volatile memory that is used to store configuration settings. Not all settings programmed into the device are automatically saved into this non-volatile memory, only those specifically identified as capable of being stored can be saved (see Table 6 for which command parameters can be saved to non-volatile storage).

#### PMBus Data Format

For commands that set thresholds, voltages or report such quantities, the module supports the "Linear" data format among the three data formats supported by PMBus. The Linear Data Format is a two byte value with an 11-bit, two's complement mantissa and a 5-bit, two's complement exponent. The format of the two data bytes is shown below:



The value of the number is then given by  

$$\text{Value} = \text{Mantissa} \times 2^{\text{Exponent}}$$

#### PMBus Addressing

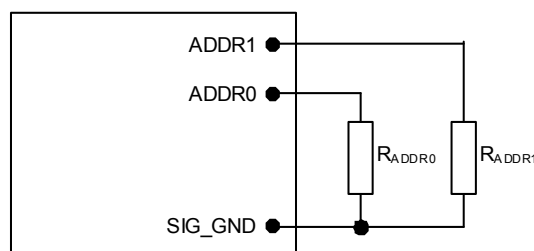
The power module can be addressed through the PMBus using a device address. The module has 64

possible addresses (0 to 63 in decimal) which can be set using resistors connected from the ADDR0 and ADDR1 pins to SIG\_GND. Note that some of these addresses (0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 40, 44, 45, 55 in decimal) are reserved according to the SMBus specifications and may not be useable. The address is set in the form of two octal (0 to 7) digits, with each pin setting one digit. The ADDR1 pin sets the high order digit and ADDR0 sets the low order digit. The resistor values suggested for each digit are shown in Table 4 (1% tolerance resistors are recommended). Note that if either address resistor value is outside the range specified in Table 4, the module will respond to address 127.

**Table 4:**

Digit	Resistor Value [kΩ]
0	10
1	15.4
2	23.7
3	36.5
4	54.9
5	84.5
6	130
7	200

The user must know which I<sup>2</sup>C addresses are reserved in a system for special functions and set the address of the module to avoid interfering with other system operations. Both 100kHz and 400kHz bus speeds are supported by the module. Connection for the PMBus interface should follow the High Power DC specifications given in section 3.1.3 in the SMBus specification V2.0 for the 400kHz bus speed or the Low Power DC specifications in section 3.1.2. The complete SMBus specification is available from the SMBus web site, [smbus.org](http://smbus.org).



**Fig-12:** Circuit showing connection of resistors used to set the PMBus address of the module.

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### PMBus Enabled On/Off

The module can also be turned on and off via the PMBus interface. The OPERATION command is used to actually turn the module on and off via the PMBus, while the ON\_OFF\_CONFIG command configures the combination of analog ON/OFF pin input and PMBus commands needed to turn the module on and off. Bit [7] in the OPERATION command data byte enables the module, with the following functions:

- 0 : Output is disabled
- 1 : Output is enabled

This module uses the lower five bits of the ON\_OFF\_CONFIG data byte to set various ON/OFF options as follows:

Bit Position	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r
Function	PU	CMD	CPR	POL	CPA
Default Value	1	0	1	1	1

**PU:** Sets the default to either operate any time input power is present or for the ON/OFF to be controlled by the analog ON/OFF input and the PMBus OPERATION command. This bit is used together with the CP, CMD and ON bits to determine startup.

Bit Value	Action
0	Module powers up any time power is present regardless of state of the analog ON/OFF pin
1	Module does not power up until commanded by the analog ON/OFF pin and the OPERATION command as programmed in bits [2:0] of the ON_OFF_CONFIG register.

**CMD:** The CMD bit controls how the device responds to the OPERATION command.

Bit Value	Action
0	Module ignores the ON bit in the OPERATION command
1	Module responds to the ON bit in the OPERATION command

**CPR:** Sets the response of the analog ON/OFF pin. This bit is used together with the CMD, PU and ON bits to determine startup.

Bit Value	Action
0	Module ignores the analog ON/OFF pin, i.e. ON/OFF is only controlled through the PMBUS via the OPERATION command
1	Module requires the analog ON/OFF pin to be asserted to start the unit

### PMBus Adjustable Soft Start Rise Time

The soft start rise time can be adjusted in the module via PMBus. When setting this parameter, make sure that the charging current for output capacitors can be delivered by the module in addition to any load current to avoid nuisance tripping of the overcurrent protection circuitry during startup. The TON\_RISE command sets the rise time in ms, and allows choosing soft start times between 600us and 9ms, with possible values listed in Table 5. Note that the exponent is fixed at -4 (decimal) and the upper two bits of the mantissa are also fixed at 0.

Table 5		
Rise Time	Exponent	Mantissa
600us	11100	00000001010
900us	11100	00000001110
1.2ms	11100	00000010011
1.8ms	11100	00000011101
2.7ms	11100	00000101011
4.2ms	11100	00001000011
6.0ms	11100	00001100000
9.0ms	11100	00010010000

### Output Voltage Adjustment Using the PMBus

The VOUT\_SCALE\_LOOP parameter is important for a number of PMBus commands related to output voltage trimming, margining, over/under voltage protection and the PGOOD thresholds. The output voltage of the module is set as the combination of the voltage divider formed by RTrim and a 20kΩ upper divider resistor inside the module, and the internal reference voltage of the module. The reference voltage  $V_{REF}$  is nominally set at 600mV, and the output regulation voltage is then given by

$$V_{OUT} = \left[ \frac{20000 + RTrim}{RTrim} \right] \times V_{REF}$$

Hence the module output voltage is dependent on the value of RTrim which is connected external to the module. The information on the output voltage divider ratio is conveyed to the module through the VOUT\_SCALE\_LOOP parameter which is calculated as follows:

$$VOUT\_SCALE\_LOOP = \frac{RTrim}{20000 + RTrim}$$

The VOUT\_SCALE\_LOOP parameter is specified using the "Linear" format and two bytes. The upper five bits [7:3] of the high byte are used to set the exponent which is fixed at -9 (decimal). The remaining three bits of the high byte [2:0] and the



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eight bits of the lower byte are used for the mantissa. The default value of the mantissa is 00100000000 corresponding to 256 (decimal), corresponding to a divider ratio of 0.5. The maximum value of the mantissa is 512 corresponding to a divider ratio of 1. Note that the resolution of the VOUT\_SCALE\_LOOP command is 0.2%.

When PMBus commands are used to trim or margin the output voltage, the value of  $V_{REF}$  is what is changed inside the module, which in turn changes the regulated output voltage of the module.

The nominal output voltage of the module can be adjusted with a minimum step size of 0.4% over a  $\pm 25\%$  range from nominal using the VOUT\_TRIM command over the PMBus.

The VOUT\_TRIM command is used to apply a fixed offset voltage to the output voltage command value using the "Linear" mode with the exponent fixed at -10 (decimal). The value of the offset voltage is given by

$$V_{OUT(offset)} = VOUT\_TRIM \times 2^{-10}$$

This offset voltage is added to the voltage set through the divider ratio and nominal  $V_{REF}$  to produce the trimmed output voltage. The valid range in two's complement for this command is -4000h to 3999h. The high order two bits of the high byte must both be either 0 or 1. If a value outside of the  $\pm 25\%$  adjustment range is given with this command, the module will set its output voltage to the nominal value (as if VOUT\_TRIM had been set to 0), assert SMBALRT#, set the CML bit in STATUS\_BYTE and the invalid data bit in STATUS\_CML.

### Output Voltage Margining Using the PMBus

The module can also have its output voltage margined via PMBus commands. The command VOUT\_MARGIN\_HIGH sets the margin high voltage, while the command VOUT\_MARGIN\_LOW sets the margin low voltage. Both the VOUT\_MARGIN\_HIGH and VOUT\_MARGIN\_LOW commands use the "Linear" mode with the exponent fixed at -10 (decimal). Two bytes are used for the mantissa with the upper bit [7] of the high byte fixed at 0. The actual margined output voltage is a combination of the VOUT\_MARGIN\_HIGH or VOUT\_MARGIN\_LOW and the VOUT\_TRIM values as shown below.

$$V_{OUT(MH)} = (VOUT\_MARGIN\_HIGH + VOUT\_TRIM) \times 2^{-10}$$

$$V_{OUT(ML)} = (VOUT\_MARGIN\_LOW + VOUT\_TRIM) \times 2^{-10}$$

Note that the sum of the margin and trim voltages cannot be outside the  $\pm 25\%$  window around the nominal output voltage. The data associated with VOUT\_MARGIN\_HIGH and VOUT\_MARGIN\_LOW can be stored to non-volatile memory using the STORE\_DEFAULT\_ALL command.

The module is commanded to go to the margined high or low voltages using the OPERATION command. Bits [5:2] are used to enable margining as follows:

00XX	: Margin Off
0101	: Margin Low (Ignore Fault)
0110	: Margin Low (Act on Fault)
1001	: Margin High (Ignore Fault)
1010	: Margin High (Act on Fault)

### PMBus Adjustable Overcurrent Warning

The module can provide an overcurrent warning via the PMBus. The threshold for the overcurrent warning can be set using the parameter IOUT\_OC\_WARN\_LIMIT. This command uses the "Linear" data format with a two byte data word where the upper five bits [7:3] of the high byte represent the exponent and the remaining three bits of the high byte [2:0] and the eight bits in the low byte represent the mantissa. The exponent is fixed at -1 (decimal). The upper five bits of the mantissa are fixed at 0 while the lower six bits are programmable with a default value of 13.5 (decimal). The resolution of this warning limit is 500mA. The value of the IOUT\_OC\_WARN\_LIMIT can be stored to non-volatile memory using the STORE\_DEFAULT\_ALL command.

### Temperature Status via PMBus

The module can provide information related to temperature of the module through the STATUS\_TEMPERATURE command. The command returns information about whether the pre-set over temperature fault threshold and/or the warning threshold have been exceeded.

### PMBus Adjustable Output Over and Under Voltage Protection

The module has output over and under voltage protection capability. The PMBus command VOUT\_OV\_FAULT\_LIMIT is used to set the output over voltage threshold from four possible values: 108%, 110%, 112% or 115% of the commanded output voltage. The command VOUT\_UV\_FAULT\_LIMIT sets the threshold that causes an output under voltage fault and can also be

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selected from four possible values: 92%, 90%, 88% or 85%. The default values are 112% and 88% of commanded output voltage. Both commands use two data bytes formatted as two's complement binary integers. The "Linear" mode is used with the exponent fixed to -10 (decimal) and the effective over or under voltage trip points given by:

$$V_{OUT(OV\_REQ)} = (VOUT\_OV\_FAULT\_LIMIT) \times 2^{-10}$$

$$V_{OUT(UV\_REQ)} = (VOUT\_UV\_FAULT\_LIMIT) \times 2^{-10}$$

Values within the supported range for over and undervoltage detection thresholds will be set to the nearest fixed percentage. Note that the correct value for VOUT\_SCALE\_LOOP must be set in the module for the correct over or under voltage trip points to be calculated.

In addition to adjustable output voltage protection, the 20A Digital **Tomodachi** module can also be programmed for the response to the fault. The VOUT\_OV\_FAULT\_RESPONSE and VOUT\_UV\_FAULT\_RESPONSE commands specify the response to the fault. Both these commands use a single data byte with the possible options as shown below.

1. Continue operation without interruption (Bits [7:6] = 00, Bits [5:3] = xxx)
2. Continue for four switching cycles and then shut down if the fault is still present, followed by no restart or continuous restart (Bits [7:6] = 01, Bits [5:3] = 000 means no restart, Bits [5:3] = 111 means continuous restart)
3. Immediate shut down followed by no restart or continuous restart (Bits [7:6] = 10, Bits [5:3] = 000 means no restart, Bits [5:3] = 111 means continuous restart).
4. Module output is disabled when the fault is present and the output is enabled when the fault no longer exists (Bits [7:6] = 11, Bits [5:3] = xxx).

Note that separate response choices are possible for output over voltage or under voltage faults.

**PMBus Adjustable Input Undervoltage Lockout**

The module allows adjustment of the input under voltage lockout and hysteresis. The command VIN\_ON allows setting the input voltage turn on threshold, while the VIN\_OFF command sets the input voltage turn off threshold. For the VIN\_ON command, possible values are 2.75V, and 3V to 14V in 0.5V steps. For the VIN\_OFF command, possible values are 2.5V to 14V in 0.5V steps. If other values are entered for either command, they will be mapped to the closest of the allowed values.

Both the VIN\_ON and VIN\_OFF commands use the "Linear" format with two data bytes. The upper five bits represent the exponent (fixed at -2) and the remaining 11

bits represent the mantissa. For the mantissa, the four most significant bits are fixed at 0.

**Power Good**

The module provides a Power Good (PGOOD) signal that is implemented with an open-drain output to indicate that the output voltage is within the regulation limits of the power module. The PGOOD signal will be de-asserted to a low state if any condition such as overtemperature, overcurrent or loss of regulation occurs that would result in the output voltage going outside the specified thresholds. The PGOOD thresholds are user selectable via the PMBus (the default values are as shown in the Feature Specifications Section). Each threshold is set up symmetrically above and below the nominal value. The POWER\_GOOD\_ON command sets the output voltage level above which PGOOD is asserted (lower threshold). For example, with a 1.2V nominal output voltage, the POWER\_GOOD\_ON threshold can set the lower threshold to 1.14 or 1.1V. Doing this will automatically set the upper thresholds to 1.26 or 1.3V.

The POWER\_GOOD\_OFF command sets the level below which the PGOOD command is de-asserted. This command also sets two thresholds symmetrically placed around the nominal output voltage. Normally, the POWER\_GOOD\_ON threshold is set higher than the POWER\_GOOD\_OFF threshold.

**Both POWER\_GOOD\_ON and POWER\_GOOD\_OFF commands use the "Linear" format with the exponent fixed at -10 (decimal). The two thresholds are given by**

$$V_{OUT(PGOOD\_ON)} = (POWER\_GOOD\_ON) \times 2^{-10}$$

$$V_{OUT(PGOOD\_OFF)} = (POWER\_GOOD\_OFF) \times 2^{-10}$$

Both commands use two data bytes with bit [7] of the high byte fixed at 0, while the remaining bits are r/w and used to set the mantissa using two's complement representation. Both commands also use the VOUT\_SCALE\_LOOP parameter so it must be set correctly. The default value of POWER\_GOOD\_ON is set at 1.1035V and that of the POWER\_GOOD\_OFF is set at 1.08V. The values associated with these commands can be stored in non-volatile memory using the STORE\_DEFAULT\_ALL command.

**The PGOOD terminal can be connected through a pullup resistor (suggested value 100KΩ) to a source of 5VDC or lower.**

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**Data Sheet****Measurement of Output Current, Output Voltage and Input Voltage**

The module is capable of measuring key module parameters such as output current and voltage and input voltage and providing this information through the PMBus interface. Roughly every 200us, the module makes 16 measurements each of output current, voltage and input voltage. Average values of of these 16 measurements are then calculated and placed in the appropriate registers. The values in the registers can then be read using the PMBus interface.

**Measuring Output Current Using the PMBus**

The module measures current by using the inductor winding resistance as a current sense element. The inductor winding resistance is then the current gain factor used to scale the measured voltage into a current reading. This gain factor is the argument of the IOUT\_CAL\_GAIN command, and consists of two bytes in the linear data format. The exponent uses the upper five bits [7:3] of the high data byte in two's complement format and is fixed at -15 (decimal). The remaining 11 bits in two's complement binary format represent the mantissa. During manufacture, each module is calibrated by measuring and storing the current gain factor into non-volatile storage.

The current measurement accuracy is also improved by each module being calibrated during manufacture with the offset in the current reading. The IOUT\_CAL\_OFFSET command is used to store and read the current offset. The argument for this command consists of two bytes composed of a 5-bit exponent (fixed at -4d) and a 11-bit mantissa. This command has a resolution of 62.5mA and a range of -4000mA to +3937.5mA.

The READ\_IOUT command provides module average output current information. This command only supports positive or current sourced from the module. If the converter is sinking current a reading of 0 is provided. The READ\_IOUT command returns two bytes of data in the linear data format. The exponent uses the upper five bits [7:3] of the high data byte in two's complement format and is fixed at -4 (decimal). The remaining 11 bits in two's complement binary format represent the mantissa with the 11<sup>th</sup> bit fixed at 0 since only positive numbers are considered valid.

Note that the current reading provided by the module is not corrected for temperature. The temperature corrected current reading for module temperature  $T_{Module}$  can be estimated using the following equation

$$I_{OUT,CORR} = \frac{I_{READ\_OUT}}{1 + [(T_{IND} - 30) \times 0.00393]}$$

where  $I_{OUT,CORR}$  is the temperature corrected value of the current measurement,  $I_{READ\_OUT}$  is the module current measurement value,  $T_{IND}$  is the temperature of the inductor winding on the module. Since it may be difficult to measure  $T_{IND}$ , it may be approximated by an estimate of the module temperature.

**Measuring Output Voltage Using the PMBus**

The module can provide output voltage information using the READ\_VOUT command. The command returns two bytes of data all representing the mantissa while the exponent is fixed at -10 (decimal). During manufacture of the module, offset and gain correction values are written into the non-volatile memory of the module. The command VOUT\_CAL\_OFFSET can be used to read and/or write the offset (two bytes consisting of a 16-bit mantissa in two's complement format) while the exponent is always fixed at -10 (decimal). The allowed range for this offset correction is -125 to 124mV. The command VOUT\_CAL\_GAIN can be used to read and/or write the gain correction - two bytes consisting of a five-bit exponent (fixed at -8) and a 11-bit mantissa. The range of this correction factor is -0.125V to +0.121V, with a resolution of 0.004V. The corrected output voltage reading is then given by:

$$V_{OUT}(Final) = [V_{OUT}(Initial) \times (1 + VOUT\_CAL\_GAIN)] + VOUT\_CAL\_OFFSET$$

**Measuring Input Voltage Using the PMBus**

The module can provide output voltage information using the READ\_VIN command. The command returns two bytes of data in the linear format. The upper five bits [7:3] of the high data form the two's complement representation of the exponent which is fixed at -5 (decimal). The remaining 11 bits are used for two's complement representation of the mantissa, with the 11<sup>th</sup> bit fixed at zero since only positive numbers are valid.

During module manufacture, offset and gain correction values are written into the non-volatile memory of the module. The command VIN\_CAL\_OFFSET can be used to read and/or write the offset - two bytes consisting of a five-bit exponent (fixed at -5) and a 11-bit mantissa in two's complement format. The allowed range for this offset correction is -2 to 1.968V, and the resolution is

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32mV. The command VIN\_CAL\_GAIN can be used to read and/or write the gain correction - two bytes consisting of a five-bit exponent (fixed at -8) and a 11-bit mantissa. The range of this correction factor is -0.125V to +0.121V, with a resolution of 0.004V. The corrected output voltage reading is then given by:

$$V_{IN}(Final) = [V_{IN}(Initial) \times (1 + VIN\_CAL\_GAIN)] + VIN\_CAL\_OFFSET$$

Reading the Status of the Module using the PMBus

The module supports a number of status information commands implemented in PMBus. However, not all features are supported in these commands. A 1 in the bit position indicates the fault that is flagged.

**STATUS\_BYTE:** Returns one byte of information with a summary of the most critical device faults.

Bit Position	Flag	Default Value
7	X	0
6	OFF	0
5	VOUT Overvoltage	0
4	IOUT Overcurrent	0
3	VIN Undervoltage	0
2	Temperature	0
1	CML (Comm. Memory Fault)	0
0	None of the above	0

**STATUS\_WORD:** Returns two bytes of information with a summary of the module's fault/warning conditions.

### Low Byte

Bit Position	Flag	Default Value
7	X	0
6	OFF	0
5	VOUT Overvoltage	0
4	IOUT Overcurrent	0
3	VIN Undervoltage	0
2	Temperature	0
1	CML (Comm. Memory Fault)	0
0	None of the above	0

### High Byte

Bit Position	Flag	Default Value
7	VOUT fault or warning	0
6	IOUT fault or warning	0
5	X	0
4	X	0
3	POWER_GOOD# (is negated)	0
2	X	0
1	X	0
0	X	0

**STATUS\_VOUT:** Returns one byte of information relating to the status of the module's output voltage related faults.

Bit Position	Flag	Default Value
7	VOUT OV Fault	0
6	X	0
5	X	0
4	VOUT UV Fault	0
3	X	0
2	X	0
1	X	0
0	X	0

**STATUS\_IOUT:** Returns one byte of information relating to the status of the module's output voltage related faults.

Bit Position	Flag	Default Value
7	IOUT OC Fault	0
6	X	0
5	IOUT OC Warning	0
4	X	0
3	X	0
2	X	0
1	X	0
0	X	0

**STATUS\_TEMPERATURE:** Returns one byte of information relating to the status of the module's temperature related faults.

Bit Position	Flag	Default Value
7	OT Fault	0
6	OT Warning	0
5	X	0
4	X	0
3	X	0
2	X	0
1	X	0
0	X	0



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**STATUS\_CML:** Returns one byte of information relating to the status of the module's communication related faults.

Bit Position	Flag	Default Value
7	Invalid/Unsupported Command	0
6	Invalid/Unsupported Command	0
5	Packet Error Check Failed	0
4	X	0
3	X	0
2	X	0
1	Other Communication Fault	0
0	X	0

**MFR\_VIN\_MIN:** Returns minimum input voltage as two data bytes of information in Linear format (upper five bits are exponent – fixed at -2, and lower 11 bits are mantissa in two's complement format – fixed at 12)

**MFR\_VOUT\_MIN:** Returns minimum output voltage as two data bytes of information in Linear format (upper five bits are exponent – fixed at -10, and lower 11 bits are mantissa in two's complement format – fixed at 614)

**MFR\_SPECIFIC\_00:** Returns information related to the type of module. Bits [7:2] in the Low Byte indicate the module type (000010 corresponds to the FGMD12SR6020 module). Bits 1:0 in the High Byte are used to indicate the manufacturer ID, with 01 reserved for FDK.

**Low Byte**

Bit Position	Flag	Default Value
7:2	Module Name	000010
1:0	Reserved	10

**High Byte**

Bit Position	Flag	Default Value
7:0	Module Revision Number	None
1:0	Manufacturer ID	01

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3-14.4Vdc Input, 20A, 0.45-5.5Vdc Output

### Summary of Supported PMBus Commands

Please refer to the PMBus 1.1 specification for more details of these commands.

Table 6

Hex Code	Command	Brief Description	Non-Volatile Memory Storage																																													
01	OPERATION	<p>Turn Module on or off. Also used to margin the output voltage</p> <table><tr><th>Format</th><th colspan="8">Unsigned Binary</th></tr><tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><th>Access</th><td>r/w</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r</td><td>r</td></tr><tr><th>Function</th><td>On</td><td>X</td><td colspan="4">Margin</td><td>X</td><td>X</td></tr><tr><th>Default Value</th><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>X</td><td>X</td></tr></table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r	r/w	r/w	r/w	r/w	r	r	Function	On	X	Margin				X	X	Default Value	0	0	0	0	0	0	X	X	
Format	Unsigned Binary																																															
Bit Position	7	6	5	4	3	2	1	0																																								
Access	r/w	r	r/w	r/w	r/w	r/w	r	r																																								
Function	On	X	Margin				X	X																																								
Default Value	0	0	0	0	0	0	X	X																																								
02	ON_OFF_CONFIG	<p>Configures the ON/OFF functionality as a combination of analog ON/OFF pin and PMBus commands</p> <table><tr><th>Format</th><th colspan="8">Unsigned Binary</th></tr><tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><th>Access</th><td>r</td><td>r</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r</td></tr><tr><th>Function</th><td>X</td><td>X</td><td>X</td><td>pu</td><td>cmd</td><td>cpr</td><td>pol</td><td>cpa</td></tr><tr><th>Default Value</th><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr></table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r/w	r/w	r/w	r/w	r	Function	X	X	X	pu	cmd	cpr	pol	cpa	Default Value	0	0	0	1	0	1	1	1	YES
Format	Unsigned Binary																																															
Bit Position	7	6	5	4	3	2	1	0																																								
Access	r	r	r	r/w	r/w	r/w	r/w	r																																								
Function	X	X	X	pu	cmd	cpr	pol	cpa																																								
Default Value	0	0	0	1	0	1	1	1																																								
03	CLEAR_FAULTS	Clear any fault bits that may have been set, also releases the SMBALERT# signal if the device has been asserting it.																																														
10	WRITE_PROTECT	<p>Used to control writing to the module via PMBus. Copies the current register setting in the module whose command code matches the value in the data byte into non-volatile memory (EEPROM) on the module</p> <table><tr><th>Format</th><th colspan="8">Unsigned Binary</th></tr><tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><th>Access</th><td>r/w</td><td>r/w</td><td>r/w</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td></tr><tr><th>Function</th><td>bit7</td><td>bit6</td><td>bit5</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr><tr><th>Default Value</th><td>0</td><td>0</td><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr></table> <p>Bit5: 0 – Enables all writes as permitted in bit6 or bit7 1 – Disables all writes except the WRITE_PROTECT, OPERATION and ON_OFF_CONFIG (bit 6 and bit7 must be 0) Bit 6: 0 – Enables all writes as permitted in bit5 or bit7 1 – Disables all writes except for the WRITE_PROTECT and OPERATION commands (bit5 and bit7 must be 0) Bit7: 0 – Enables all writes as permitted in bit5 or bit6 1 – Disables all writes except for the WRITE_PROTECT command (bit5 and bit6 must be 0)</p>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	x	x	x	x	x	Function	bit7	bit6	bit5	X	X	X	X	X	Default Value	0	0	0	X	X	X	X	X	YES
Format	Unsigned Binary																																															
Bit Position	7	6	5	4	3	2	1	0																																								
Access	r/w	r/w	r/w	x	x	x	x	x																																								
Function	bit7	bit6	bit5	X	X	X	X	X																																								
Default Value	0	0	0	X	X	X	X	X																																								
11	STORE_DEFAULT_ALL	Copies all current register settings in the module into non-volatile memory (EEPROM) on the module. Takes about 50ms for the command to execute.																																														
12	RESTORE_DEFAULT_ALL	Restores all current register settings in the module from values in the module non-volatile memory (EEPROM)																																														
13	STORE_DEFAULT_CODE	<p>Copies the current register setting in the module whose command code matches the value in the data byte into non-volatile memory (EEPROM) on the module</p> <table><tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><th>Access</th><td>w</td><td>w</td><td>w</td><td>w</td><td>w</td><td>w</td><td>w</td><td>w</td></tr><tr><th>Function</th><td colspan="8">Command code</td></tr></table>	Bit Position	7	6	5	4	3	2	1	0	Access	w	w	w	w	w	w	w	w	Function	Command code																										
Bit Position	7	6	5	4	3	2	1	0																																								
Access	w	w	w	w	w	w	w	w																																								
Function	Command code																																															
14	RESTORE_DEFAULT_CODE	<p>Restores the current register setting in the module whose command code matches the value in the data byte from the value in the module non-volatile memory (EEPROM)</p> <table><tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><th>Access</th><td>w</td><td>w</td><td>w</td><td>w</td><td>w</td><td>w</td><td>w</td><td>w</td></tr><tr><th>Function</th><td colspan="8">Command code</td></tr></table>	Bit Position	7	6	5	4	3	2	1	0	Access	w	w	w	w	w	w	w	w	Function	Command code																										
Bit Position	7	6	5	4	3	2	1	0																																								
Access	w	w	w	w	w	w	w	w																																								
Function	Command code																																															
20	VOUT_MODE	<p>The module has MODE set to Linear and Exponent set to -10. These values cannot be changed</p> <table><tr><th>Bit Position</th><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><th>Access</th><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><th>Function</th><td colspan="4">Mode</td><td colspan="4">Exponent</td></tr><tr><th>Default Value</th><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr></table>	Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Mode				Exponent				Default Value	0	0	0	1	0	1	1	0										
Bit Position	7	6	5	4	3	2	1	0																																								
Access	r	r	r	r	r	r	r	r																																								
Function	Mode				Exponent																																											
Default Value	0	0	0	1	0	1	1	0																																								



**FGMD12SR6020\*A**
**Data Sheet**

3-14.4Vdc Input, 20A, 0.45-5.5Vdc Output

Table 6 (continued)

Hex Code	Command	Brief Description	Non-Volatile Memory Storage																																																																																	
22	VOUT_TRIM	<div>Apply a fixed offset voltage to the output voltage command value</div> <table><tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="8">High Byte</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="8">Low Byte</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	Format	Linear, two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	High Byte								Default Value	0	0	0	0	0	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Low Byte								Default Value	0	0	0	0	0	0	0	0	YES
Format	Linear, two's complement binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w																																																																												
Function	High Byte																																																																																			
Default Value	0	0	0	0	0	0	0	0																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w																																																																												
Function	Low Byte																																																																																			
Default Value	0	0	0	0	0	0	0	0																																																																												
25	VOUT_MARGIN_HIGH	<div>Sets the target voltage for margining the output high</div> <table><tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="8">High Byte</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="8">Low Byte</td></tr><tr><td>Default Value</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr></table>	Format	Linear, two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	High Byte								Default Value	0	0	0	0	0	1	0	1	Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Low Byte								Default Value	0	1	0	0	0	1	1	1	YES
Format	Linear, two's complement binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w																																																																												
Function	High Byte																																																																																			
Default Value	0	0	0	0	0	1	0	1																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w																																																																												
Function	Low Byte																																																																																			
Default Value	0	1	0	0	0	1	1	1																																																																												
26	VOUT_MARGIN_LOW	<div>Sets the target voltage for margining the output low</div> <table><tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="8">High Byte</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="8">Low Byte</td></tr><tr><td>Default Value</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr></table>	Format	Linear, two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	High Byte								Default Value	0	0	0	0	0	1	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Low Byte								Default Value	0	1	0	1	0	0	0	1	YES
Format	Linear, two's complement binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w																																																																												
Function	High Byte																																																																																			
Default Value	0	0	0	0	0	1	0	0																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w																																																																												
Function	Low Byte																																																																																			
Default Value	0	1	0	1	0	0	0	1																																																																												
29	VOUT_SCALE_LOOP	<div>Sets the scaling of the output voltage – equal to the feedback resistor divider ratio</div> <table><tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="4">Exponent</td><td colspan="4">Mantissa</td></tr><tr><td>Default Value</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="8">Mantissa</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	Format	Linear, two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r/w	r/w	Function	Exponent				Mantissa				Default Value	1	0	1	1	1	0	0	1	Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Mantissa								Default Value	0	0	0	0	0	0	0	0	YES
Format	Linear, two's complement binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r/w	r/w																																																																												
Function	Exponent				Mantissa																																																																															
Default Value	1	0	1	1	1	0	0	1																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w																																																																												
Function	Mantissa																																																																																			
Default Value	0	0	0	0	0	0	0	0																																																																												
35	VIN_ON	<div>Sets the value of input voltage at which the module turns on</div> <table><tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Function</td><td colspan="4">Exponent</td><td colspan="4">Mantissa</td></tr><tr><td>Default Value</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="8">Mantissa</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr></table>	Format	Linear, two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Exponent				Mantissa				Default Value	1	1	1	1	0	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Mantissa								Default Value	0	0	0	0	1	0	1	1	YES
Format	Linear, two's complement binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	Exponent				Mantissa																																																																															
Default Value	1	1	1	1	0	0	0	0																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w																																																																												
Function	Mantissa																																																																																			
Default Value	0	0	0	0	1	0	1	1																																																																												

# FGMD12SR6020\*A

## Data Sheet

3-14.4Vdc Input, 20A, 0.45-5.5Vdc Output

Table 6 (continued)

Hex Code	Command	Brief Description	Non-Volatile Memory Storage																																																																																	
36	VIN_OFF	Sets the value of input voltage at which the module turns off	YES																																																																																	
		<table><tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Function</td><td colspan="4">Exponent</td><td colspan="4">Mantissa</td></tr><tr><td>Default Value</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="8">Mantissa</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr></table>		Format	Linear, two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Exponent				Mantissa				Default Value	1	1	1	1	0	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Mantissa								Default Value	0	0	0	0	1	0	1	0
		Format		Linear, two's complement binary																																																																																
		Bit Position		7	6	5	4	3	2	1	0																																																																									
		Access		r	r	r	r	r	r	r	r																																																																									
		Function		Exponent				Mantissa																																																																												
		Default Value		1	1	1	1	0	0	0	0																																																																									
		Bit Position		7	6	5	4	3	2	1	0																																																																									
		Access		r	r/w	r/w	r/w	r/w	r/w	r/w	r/w																																																																									
Function	Mantissa																																																																																			
Default Value	0	0	0	0	1	0	1	0																																																																												
38	IOUT_CAL_GAIN	Returns the value of the gain correction term used to correct the measured output current	YES																																																																																	
		<table><tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r/w</td></tr><tr><td>Function</td><td colspan="4">Exponent</td><td colspan="4">Mantissa</td></tr><tr><td>Default Value</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>V</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="8">Mantissa</td></tr><tr><td>Default Value</td><td colspan="8">V: Variable based on factory calibration</td></tr></table>		Format	Linear, two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r/w	Function	Exponent				Mantissa				Default Value	1	0	0	0	1	0	0	V	Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Mantissa								Default Value	V: Variable based on factory calibration							
		Format		Linear, two's complement binary																																																																																
		Bit Position		7	6	5	4	3	2	1	0																																																																									
		Access		r	r	r	r	r	r	r	r/w																																																																									
		Function		Exponent				Mantissa																																																																												
		Default Value		1	0	0	0	1	0	0	V																																																																									
		Bit Position		7	6	5	4	3	2	1	0																																																																									
		Access		r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w																																																																									
Function	Mantissa																																																																																			
Default Value	V: Variable based on factory calibration																																																																																			
39	IOUT_CAL_OFFSET	Returns the value of the offset correction term used to correct the measured output current	YES																																																																																	
		<table><tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r/w</td><td>r</td><td>r</td></tr><tr><td>Function</td><td colspan="4">Exponent</td><td colspan="4">Mantissa</td></tr><tr><td>Default Value</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>V</td><td>0</td><td>0</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="8">Mantissa</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td colspan="6">V: Variable based on factory calibration</td></tr></table>		Format	Linear, two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r/w	r	r	Function	Exponent				Mantissa				Default Value	1	1	1	0	0	V	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w	Function	Mantissa								Default Value	0	0	V: Variable based on factory calibration					
		Format		Linear, two's complement binary																																																																																
		Bit Position		7	6	5	4	3	2	1	0																																																																									
		Access		r	r	r	r	r	r/w	r	r																																																																									
		Function		Exponent				Mantissa																																																																												
		Default Value		1	1	1	0	0	V	0	0																																																																									
		Bit Position		7	6	5	4	3	2	1	0																																																																									
		Access		r	r	r/w	r/w	r/w	r/w	r/w	r/w																																																																									
Function	Mantissa																																																																																			
Default Value	0	0	V: Variable based on factory calibration																																																																																	
40	VOUT_OV_FAULT_LIMIT	Sets the voltage level for an output overvoltage fault	YES																																																																																	
		<table><tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="8">High Byte</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="8">Low Byte</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr></table>		Format	Linear, two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	High Byte								Default Value	0	0	0	0	0	1	0	1	Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Low Byte								Default Value	0	0	0	0	1	0	1	0
		Format		Linear, two's complement binary																																																																																
		Bit Position		7	6	5	4	3	2	1	0																																																																									
		Access		r	r/w	r/w	r/w	r/w	r/w	r/w	r/w																																																																									
		Function		High Byte																																																																																
		Default Value		0	0	0	0	0	1	0	1																																																																									
		Bit Position		7	6	5	4	3	2	1	0																																																																									
		Access		r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w																																																																									
Function	Low Byte																																																																																			
Default Value	0	0	0	0	1	0	1	0																																																																												
41	VOUT_OV_FAULT_RESPONSE	Instructs the module on what action to take in response to a output overvoltage fault	YES																																																																																	
		<table><tr><td>Format</td><td colspan="8">Unsigned Binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Function</td><td>RSP [1]</td><td>RSP [0]</td><td>RS[2]</td><td>RS[1]</td><td>RS[0]</td><td>X</td><td>X</td><td>X</td></tr><tr><td>Default Value</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr></table>		Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r	r	r	Function	RSP [1]	RSP [0]	RS[2]	RS[1]	RS[0]	X	X	X	Default Value	1	1	1	1	1	1	0	0																																				
		Format		Unsigned Binary																																																																																
		Bit Position		7	6	5	4	3	2	1	0																																																																									
		Access		r/w	r/w	r/w	r/w	r/w	r	r	r																																																																									
Function	RSP [1]	RSP [0]	RS[2]	RS[1]	RS[0]	X	X	X																																																																												
Default Value	1	1	1	1	1	1	0	0																																																																												

**FGMD12SR6020\*A**
**Data Sheet**

3-14.4Vdc Input, 20A, 0.45-5.5Vdc Output

Table 6 (continued)

Hex Code	Command	Brief Description	Non-Volatile Memory Storage																																																																																	
44	VOUT_UV_FAULT_LIMIT	<div>Sets the voltage level for an output undervoltage fault</div> <table><tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="8">High Byte</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="8">Low Byte</td></tr><tr><td>Default Value</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr></table>	Format	Linear, two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	High Byte								Default Value	0	0	0	0	0	1	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Low Byte								Default Value	1	0	0	0	1	1	1	1	YES
Format	Linear, two's complement binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w																																																																												
Function	High Byte																																																																																			
Default Value	0	0	0	0	0	1	0	0																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w																																																																												
Function	Low Byte																																																																																			
Default Value	1	0	0	0	1	1	1	1																																																																												
45	VOUT_UV_FAULT_RESPONSE	<div>Instructs the module on what action to take in response to a output undervoltage fault</div> <table><tr><td>Format</td><td colspan="8">Unsigned Binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Function</td><td>RSP [1]</td><td>RSP [0]</td><td>RS[2]</td><td>RS[1]</td><td>RS[0]</td><td>X</td><td>X</td><td>X</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr></table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r	r	r	Function	RSP [1]	RSP [0]	RS[2]	RS[1]	RS[0]	X	X	X	Default Value	0	0	0	0	0	1	0	0	YES																																				
Format	Unsigned Binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r/w	r/w	r/w	r/w	r/w	r	r	r																																																																												
Function	RSP [1]	RSP [0]	RS[2]	RS[1]	RS[0]	X	X	X																																																																												
Default Value	0	0	0	0	0	1	0	0																																																																												
46	IOUT_OC_FAULT_LIMIT	<div>Sets the output overcurrent fault level in A (cannot be changed)</div> <table><tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Function</td><td colspan="4">Exponent</td><td colspan="4">Mantissa</td></tr><tr><td>Default Value</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Function</td><td colspan="8">Mantissa</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr></table>	Format	Linear, two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Exponent				Mantissa				Default Value									Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Mantissa								Default Value	0	0	1	1	0	1	0	0	YES
Format	Linear, two's complement binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	Exponent				Mantissa																																																																															
Default Value																																																																																				
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	Mantissa																																																																																			
Default Value	0	0	1	1	0	1	0	0																																																																												
4A	IOUT_OC_WARN_LIMIT	<div>Sets the output overcurrent warning level in A</div> <table><tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Function</td><td colspan="4">Exponent</td><td colspan="4">Mantissa</td></tr><tr><td>Default Value</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="8">Mantissa</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr></table>	Format	Linear, two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Exponent				Mantissa				Default Value	1	1	1	1	1	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w	Function	Mantissa								Default Value	0	0	1	1	0	0	1	0	YES
Format	Linear, two's complement binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	Exponent				Mantissa																																																																															
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Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w																																																																												
Function	Mantissa																																																																																			
Default Value	0	0	1	1	0	0	1	0																																																																												
5E	POWER_GOOD_ON	<div>Sets the output voltage level at which the PGOOD pin is asserted high</div> <table><tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="8">High Byte</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="8">Low Byte</td></tr><tr><td>Default Value</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr></table>	Format	Linear, two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	High Byte								Default Value	0	0	0	0	0	1	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Low Byte								Default Value	0	1	1	0	1	0	1	0	YES
Format	Linear, two's complement binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w																																																																												
Function	High Byte																																																																																			
Default Value	0	0	0	0	0	1	0	0																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w																																																																												
Function	Low Byte																																																																																			
Default Value	0	1	1	0	1	0	1	0																																																																												

**FGMD12SR6020\*A**
**Data Sheet**

3-14.4Vdc Input, 20A, 0.45-5.5Vdc Output

Table 6 (continued)

Hex Code	Command	Brief Description	Non-Volatile Memory Storage																																																																																	
5F	POWER_GOOD_OFF	<p>Sets the output voltage level at which the PGOOD pin is de-asserted low</p> <table><tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="8">High Byte</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="8">Low Byte</td></tr><tr><td>Default Value</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr></table>	Format	Linear, two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	High Byte								Default Value	0	0	0	0	0	1	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Low Byte								Default Value	0	1	0	1	0	0	1	0	YES
Format	Linear, two's complement binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w																																																																												
Function	High Byte																																																																																			
Default Value	0	0	0	0	0	1	0	0																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w																																																																												
Function	Low Byte																																																																																			
Default Value	0	1	0	1	0	0	1	0																																																																												
61	TON_RISE	<p>Sets the rise time of the output voltage during startup</p> <table><tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r/w</td></tr><tr><td>Function</td><td colspan="4">Exponent</td><td colspan="4">Mantissa</td></tr><tr><td>Default Value</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="8">Mantissa</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr></table>	Format	Linear, two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r/w	Function	Exponent				Mantissa				Default Value	1	1	1	0	0	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Mantissa								Default Value	0	0	1	0	1	0	1	0	YES
Format	Linear, two's complement binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r/w																																																																												
Function	Exponent				Mantissa																																																																															
Default Value	1	1	1	0	0	0	0	0																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w																																																																												
Function	Mantissa																																																																																			
Default Value	0	0	1	0	1	0	1	0																																																																												
78	STATUS_BYTE	<p>Returns one byte of information with a summary of the most critical module faults</p> <table><tr><td>Format</td><td colspan="8">Unsigned Binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Flag</td><td>X</td><td>OFF</td><td>VOUT_OV</td><td>IOU_OC</td><td>VIN_UV</td><td>TEMP</td><td>CML</td><td>OTHE R</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Flag	X	OFF	VOUT_OV	IOU_OC	VIN_UV	TEMP	CML	OTHE R	Default Value	0	0	0	0	0	0	0	0																																					
Format	Unsigned Binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Flag	X	OFF	VOUT_OV	IOU_OC	VIN_UV	TEMP	CML	OTHE R																																																																												
Default Value	0	0	0	0	0	0	0	0																																																																												
79	STATUS_WORD	<p>Returns two bytes of information with a summary of the module's fault/warning conditions</p> <table><tr><td>Format</td><td colspan="8">Unsigned binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Flag</td><td>VOUT</td><td>IOU_OC</td><td>X</td><td>X</td><td>PGO OD</td><td>X</td><td>X</td><td>X</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Flag</td><td>X</td><td>OFF</td><td>VOUT_OV</td><td>IOU_OC</td><td>VIN_UV</td><td>TEMP</td><td>CML</td><td>OTHE R</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	Format	Unsigned binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Flag	VOUT	IOU_OC	X	X	PGO OD	X	X	X	Default Value	0	0	0	0	0	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Flag	X	OFF	VOUT_OV	IOU_OC	VIN_UV	TEMP	CML	OTHE R	Default Value	0	0	0	0	0	0	0	0	
Format	Unsigned binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Flag	VOUT	IOU_OC	X	X	PGO OD	X	X	X																																																																												
Default Value	0	0	0	0	0	0	0	0																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Flag	X	OFF	VOUT_OV	IOU_OC	VIN_UV	TEMP	CML	OTHE R																																																																												
Default Value	0	0	0	0	0	0	0	0																																																																												
7A	STATUS_VOUT	<p>Returns one byte of information with the status of the module's output voltage related faults</p> <table><tr><td>Format</td><td colspan="8">Unsigned Binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Flag</td><td>VOUT_OV</td><td>X</td><td>X</td><td>VOUT_UV</td><td>X</td><td>X</td><td>X</td><td>X</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Flag	VOUT_OV	X	X	VOUT_UV	X	X	X	X	Default Value	0	0	0	0	0	0	0	0																																					
Format	Unsigned Binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Flag	VOUT_OV	X	X	VOUT_UV	X	X	X	X																																																																												
Default Value	0	0	0	0	0	0	0	0																																																																												
7B	STATUS_IOUT	<p>Returns one byte of information with the status of the module's output current related faults</p> <table><tr><td>Format</td><td colspan="8">Unsigned Binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Flag</td><td>IOU_OC</td><td>X</td><td>IOU_OC_WA RN</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Flag	IOU_OC	X	IOU_OC_WA RN	X	X	X	X	X	Default Value	0	0	0	0	0	0	0	0																																					
Format	Unsigned Binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Flag	IOU_OC	X	IOU_OC_WA RN	X	X	X	X	X																																																																												
Default Value	0	0	0	0	0	0	0	0																																																																												

**FGMD12SR6020\*A**
**Data Sheet**

3-14.4Vdc Input, 20A, 0.45-5.5Vdc Output

Table 6 (continued)

Hex Code	Command	Brief Description	Non-Volatile Memory Storage																																																																																	
7D	STATUS_TEMPERATURE	<div>Returns one byte of information with the status of the module's temperature related faults</div> <table><tr><td>Format</td><td colspan="8">Unsigned Binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Flag</td><td>OT_FAULT</td><td>OT_WARN</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Flag	OT_FAULT	OT_WARN	X	X	X	X	X	X	Default Value	0	0	0	0	0	0	0	0																																					
Format	Unsigned Binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Flag	OT_FAULT	OT_WARN	X	X	X	X	X	X																																																																												
Default Value	0	0	0	0	0	0	0	0																																																																												
7E	STATUS_CML	<div>Returns one byte of information with the status of the module's communication related faults</div> <table><tr><td>Format</td><td colspan="8">Unsigned Binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Flag</td><td>Invalid Command</td><td>Invalid Data</td><td>PEC Fail</td><td>X</td><td>X</td><td>X</td><td>Other Comm Fault</td><td>X</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Flag	Invalid Command	Invalid Data	PEC Fail	X	X	X	Other Comm Fault	X	Default Value	0	0	0	0	0	0	0	0																																					
Format	Unsigned Binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Flag	Invalid Command	Invalid Data	PEC Fail	X	X	X	Other Comm Fault	X																																																																												
Default Value	0	0	0	0	0	0	0	0																																																																												
88	READ_VIN	<div>Returns the value of the input voltage applied to the module</div> <table><tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Function</td><td colspan="5">Exponent</td><td colspan="3">Mantissa</td></tr><tr><td>Default Value</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Function</td><td colspan="8">Mantissa</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	Format	Linear, two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Exponent					Mantissa			Default Value	1	1	0	1	1	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Mantissa								Default Value	0	0	0	0	0	0	0	0	
Format	Linear, two's complement binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	Exponent					Mantissa																																																																														
Default Value	1	1	0	1	1	0	0	0																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	Mantissa																																																																																			
Default Value	0	0	0	0	0	0	0	0																																																																												
8B	READ_VOUT	<div>Returns the value of the output voltage of the module</div> <table><tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Function</td><td colspan="8">Mantissa</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Function</td><td colspan="8">Mantissa</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	Format	Linear, two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Mantissa								Default Value	0	0	0	0	0	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Mantissa								Default Value	0	0	0	0	0	0	0	0	
Format	Linear, two's complement binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	Mantissa																																																																																			
Default Value	0	0	0	0	0	0	0	0																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	Mantissa																																																																																			
Default Value	0	0	0	0	0	0	0	0																																																																												
8C	READ_IOUT	<div>Returns the value of the output current of the module</div> <table><tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Function</td><td colspan="5">Exponent</td><td colspan="3">Mantissa</td></tr><tr><td>Default Value</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Function</td><td colspan="8">Mantissa</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	Format	Linear, two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Exponent					Mantissa			Default Value	1	1	1	0	0	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Mantissa								Default Value	0	0	0	0	0	0	0	0	
Format	Linear, two's complement binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	Exponent					Mantissa																																																																														
Default Value	1	1	1	0	0	0	0	0																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	Mantissa																																																																																			
Default Value	0	0	0	0	0	0	0	0																																																																												
98	PMBUS_REVISION	<div>Returns one byte indicating the module is compliant to PMBus Spec. 1.1 (read only)</div> <table><tr><td>Format</td><td colspan="8">Unsigned Binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr></table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Default Value	0	0	0	1	0	0	0	1	YES																																													
Format	Unsigned Binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Default Value	0	0	0	1	0	0	0	1																																																																												

# FGMD12SR6020\*A

## Data Sheet

3-14.4Vdc Input, 20A, 0.45-5.5Vdc Output

Table 6 (continued)

Hex Code	Command	Brief Description	Non-Volatile Memory Storage																																																																																	
A0	MFR_VIN_MIN	<div>Returns the minimum input voltage the module is specified to operate at (read only)</div> <table><tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Function</td><td colspan="5">Exponent</td><td colspan="3">Mantissa</td></tr><tr><td>Default Value</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Function</td><td colspan="8">Mantissa</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr></table>	Format	Linear, two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Exponent					Mantissa			Default Value	1	1	1	1	0	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Mantissa								Default Value	0	0	0	0	1	1	0	0	YES
Format	Linear, two's complement binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	Exponent					Mantissa																																																																														
Default Value	1	1	1	1	0	0	0	0																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	Mantissa																																																																																			
Default Value	0	0	0	0	1	1	0	0																																																																												
A4	MFR_VOUT_MIN	<div>Returns the minimum output voltage possible from the module (read only)</div> <table><tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Function</td><td colspan="5">Exponent</td><td colspan="3">Mantissa</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Function</td><td colspan="8">Mantissa</td></tr><tr><td>Default Value</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr></table>	Format	Linear, two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Exponent					Mantissa			Default Value	0	0	0	0	0	0	1	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Mantissa								Default Value	0	1	1	0	0	1	1	0	YES
Format	Linear, two's complement binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	Exponent					Mantissa																																																																														
Default Value	0	0	0	0	0	0	1	0																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	Mantissa																																																																																			
Default Value	0	1	1	0	0	1	1	0																																																																												
D0	MFR_SPECIFIC_00	<div>Returns module name information (read only)</div> <table><tr><td>Format</td><td colspan="8">Unsigned Binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Function</td><td colspan="8">Reserved</td></tr><tr><td>Default Value</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Function</td><td colspan="6">Module Name</td><td colspan="2">Reserved</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr></table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Reserved								Default Value	1	1	1	0	1	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Module Name						Reserved		Default Value	0	0	0	0	1	0	1	0	YES
Format	Unsigned Binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	Reserved																																																																																			
Default Value	1	1	1	0	1	0	0	0																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	Module Name						Reserved																																																																													
Default Value	0	0	0	0	1	0	1	0																																																																												
D4	VOUT_CAL_OFFSET	<div>Applies an offset to the READ_VOUT command results to calibrate out offset errors in module measurements of the output voltage (between -125mV and +124mV)</div> <table><tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r/w</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr><tr><td>Function</td><td colspan="8">Mantissa</td></tr><tr><td>Default Value</td><td>V</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="8">Mantissa</td></tr><tr><td>Default Value</td><td>V</td><td>V</td><td>V</td><td>V</td><td>V</td><td>V</td><td>V</td><td>V</td></tr></table>	Format	Linear, two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r	r	r	r	r	r	r	Function	Mantissa								Default Value	V	0	0	0	0	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Mantissa								Default Value	V	V	V	V	V	V	V	V	YES
Format	Linear, two's complement binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r/w	r	r	r	r	r	r	r																																																																												
Function	Mantissa																																																																																			
Default Value	V	0	0	0	0	0	0	0																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w																																																																												
Function	Mantissa																																																																																			
Default Value	V	V	V	V	V	V	V	V																																																																												
D5	VOUT_CAL_GAIN	<div>Applies a gain correction to the READ_VOUT command results to calibrate out gain errors in module measurements of the output voltage (between -0.125 and 0.121)</div> <table><tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r/w</td></tr><tr><td>Function</td><td colspan="5">Exponent</td><td colspan="3">Mantissa</td></tr><tr><td>Default Value</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>V</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="8">Mantissa</td></tr><tr><td>Default Value</td><td>V</td><td>V</td><td>V</td><td>V</td><td>V</td><td>V</td><td>V</td><td>V</td></tr></table>	Format	Linear, two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r/w	Function	Exponent					Mantissa			Default Value	1	1	0	0	0	0	0	V	Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Mantissa								Default Value	V	V	V	V	V	V	V	V	YES
Format	Linear, two's complement binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r/w																																																																												
Function	Exponent					Mantissa																																																																														
Default Value	1	1	0	0	0	0	0	V																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w																																																																												
Function	Mantissa																																																																																			
Default Value	V	V	V	V	V	V	V	V																																																																												



**FGMD12SR6020\*A**
**Data Sheet**

3-14.4Vdc Input, 20A, 0.45-5.5Vdc Output

Table 6 (continued)

Hex Code	Command	Brief Description	Non-Volatile Memory Storage																																																																																	
D6	VIN_CAL_OFFSET	<p>Applies an offset correction to the READ_VIN command results to calibrate out offset errors in module measurements of the input voltage (between -2V and +1.968V)</p> <table><tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r/w</td><td>r</td><td>r</td><td>r/w</td></tr><tr><td>Function</td><td colspan="4">Exponent</td><td colspan="4">Mantissa</td></tr><tr><td>Default Value</td><td>1</td><td>1</td><td>0</td><td>1</td><td>V</td><td>0</td><td>0</td><td>V</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="8">Mantissa</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>V</td><td>V</td><td>V</td><td>V</td><td>V</td><td>V</td></tr></table>	Format	Linear, two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r/w	r	r	r/w	Function	Exponent				Mantissa				Default Value	1	1	0	1	V	0	0	V	Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w	Function	Mantissa								Default Value	0	0	V	V	V	V	V	V	YES
Format	Linear, two's complement binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r/w	r	r	r/w																																																																												
Function	Exponent				Mantissa																																																																															
Default Value	1	1	0	1	V	0	0	V																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w																																																																												
Function	Mantissa																																																																																			
Default Value	0	0	V	V	V	V	V	V																																																																												
D7	VIN_CAL_GAIN	<p>Applies a gain correction to the READ_VIN command results to calibrate out gain errors in module measurements of the input voltage (between -0.125 and 0.121)</p> <table><tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r/w</td><td>r</td><td>r</td><td>r/w</td></tr><tr><td>Function</td><td colspan="4">Exponent</td><td colspan="4">Mantissa</td></tr><tr><td>Default Value</td><td>1</td><td>1</td><td>0</td><td>0</td><td>V</td><td>0</td><td>0</td><td>V</td></tr><tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr><tr><td>Function</td><td colspan="8">Mantissa</td></tr><tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>V</td><td>V</td><td>V</td><td>V</td><td>V</td></tr></table>	Format	Linear, two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r/w	r	r	r/w	Function	Exponent				Mantissa				Default Value	1	1	0	0	V	0	0	V	Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r/w	r/w	r/w	r/w	r/w	Function	Mantissa								Default Value	0	0	0	V	V	V	V	V	YES
Format	Linear, two's complement binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r/w	r	r	r/w																																																																												
Function	Exponent				Mantissa																																																																															
Default Value	1	1	0	0	V	0	0	V																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r/w	r/w	r/w	r/w	r/w																																																																												
Function	Mantissa																																																																																			
Default Value	0	0	0	V	V	V	V	V																																																																												

# FGMD12SR6020\*A

3-14.4Vdc Input, 20A, 0.45-5.5Vdc Output

## Data Sheet

### Characterization

#### Overview

The converter has been characterized for several operational features, including efficiency, thermal derating (maximum available load current as a function of ambient temperature and airflow), ripple and noise, transient response to load step changes, start-up and shutdown characteristics.

Figures showing data plots and waveforms for different output voltages are presented in the following pages.

#### Thermal Considerations

Power modules operate in a variety of thermal environments; however, sufficient cooling should always be provided to help ensure reliable operation. Considerations include ambient temperature, airflow, module power dissipation, and the need for increased reliability. A reduction in the operating temperature of the module will result in an increase in reliability. The thermal data presented here is based on physical measurements taken in a wind tunnel. The test set-up is shown in Fig-13. The preferred airflow direction for the module is in Fig-14.

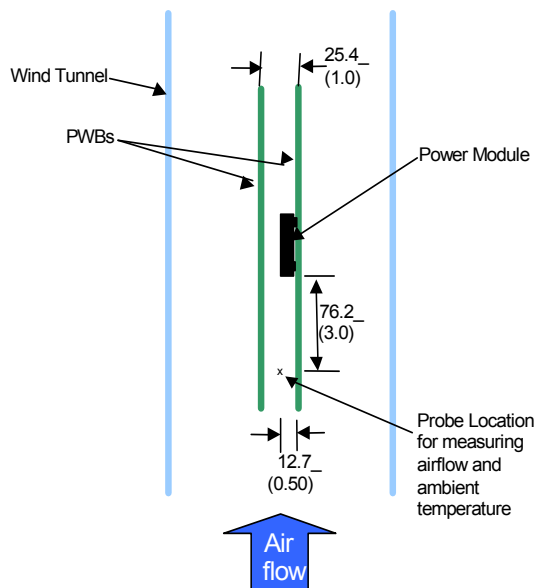


Fig-13: Thermal test set-up

The maximum available load current, for any given set of conditions, is defined as the lower of:

- The output current at which the temperature of any component reaches 130°C, or
- The current rating of the converter (20A)

A maximum component temperature of 120°C should not be exceeded in order to operate within the derating curves. Thus, the temperature at the thermocouple location shown in Fig-14 should not exceed 130°C in normal operation.

Note that continuous operation beyond the derated current as specified by the derating curves may lead to degradation in performance and reliability of the converter and may result in permanent damage.

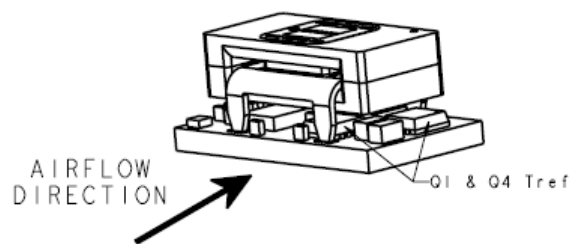


Fig-14: Preferred airflow direction and location of hot-spot of the module (Tref).

The main heat dissipation method of this converter is to transfer its heat to the system board. Thus, if the temperature of the system board goes high, even with the low ambient temperature, it may exceed the guaranteed temperature of components.

## FGMD12SR6020\*A

3-14.4Vdc Input, 20A, 0.45-5.5Vdc Output

## Data Sheet

### Characteristic Curves

The following figures provide typical characteristics for the 20A Digital **Tomodachi** at 5Vo and 25°C

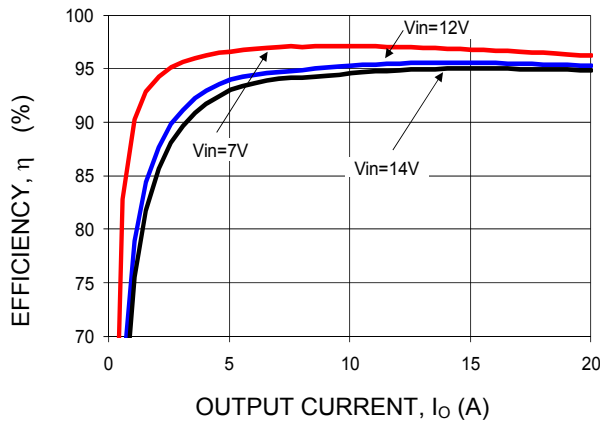


Fig-15. Converter Efficiency versus Output Current.

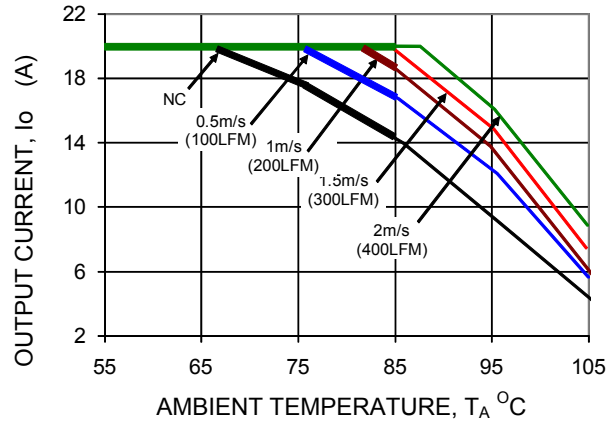


Fig-16. Derating Output Current versus Ambient Temperature and Airflow.

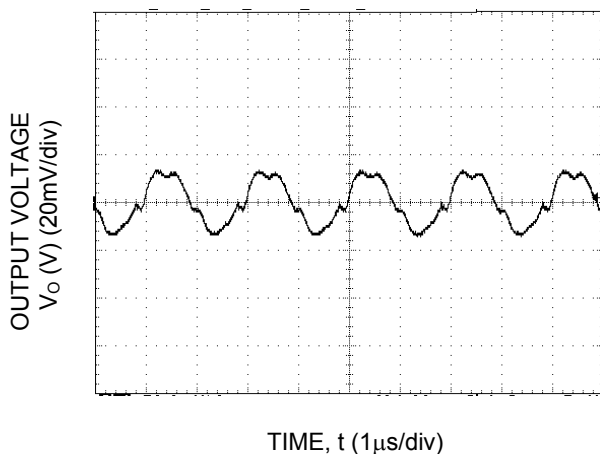


Fig-17. Typical output ripple and noise (CO=2x47uF ceramic, VIN = 12V, Io = Io,max, ).

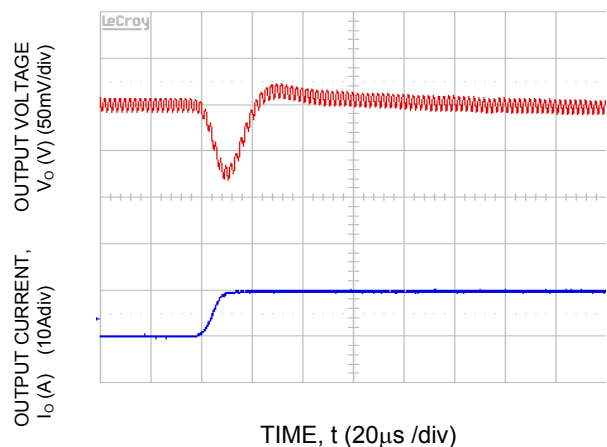


Fig-18. Transient Response to Dynamic Load Change from 50% to 100% at 12Vin, Cout= 8x47uF, CTune=1500pF & RTune=220ohms

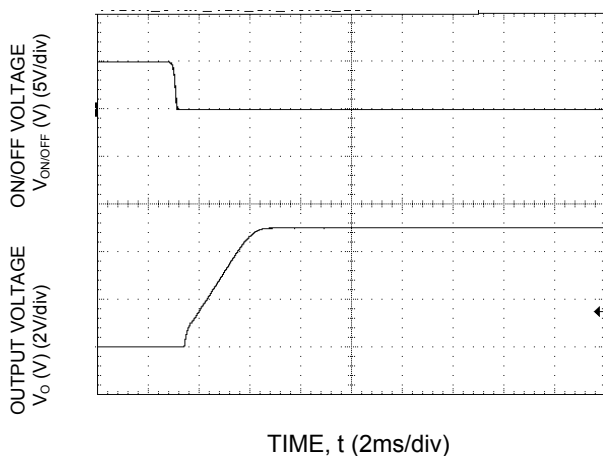


Fig-19. Typical Start-up Using On/Off Voltage (Io = Io,max).

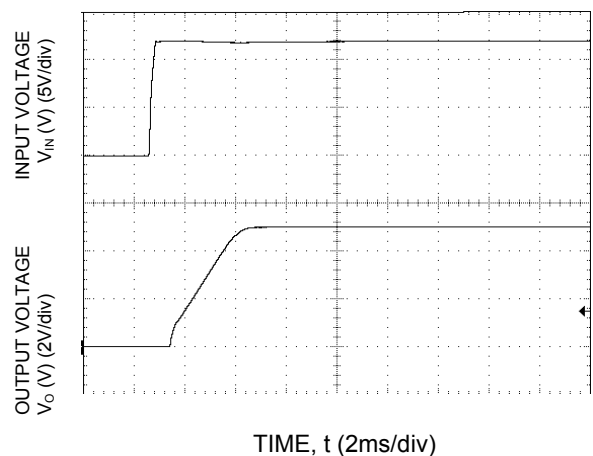


Fig-20. Typical Start-up Using Input Voltage (VIN = 12V, Io = Io,max).

## FGMD12SR6020\*A

3-14.4Vdc Input, 20A, 0.45-5.5Vdc Output

## Data Sheet

### Characteristic Curves

The following figures provide typical characteristics for the 20A Digital **Tomodachi** at 3.3V<sub>o</sub> and 25°C

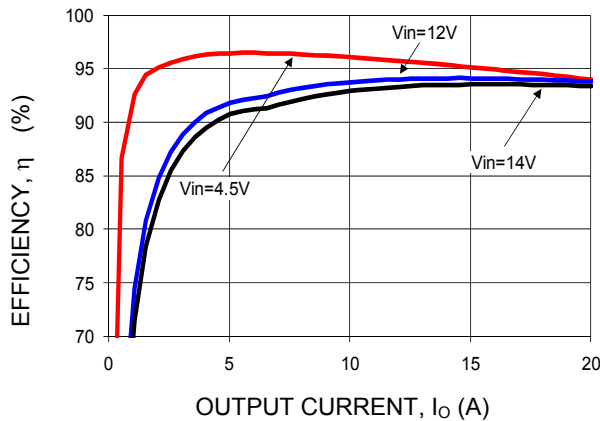


Fig-21. Converter Efficiency versus Output Current.

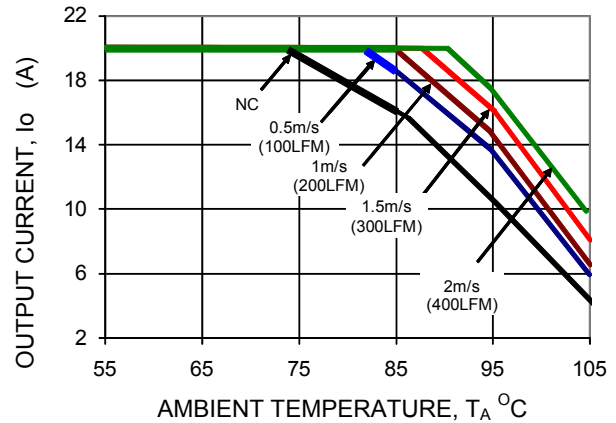


Fig-22. Derating Output Current versus Ambient Temperature and Airflow.

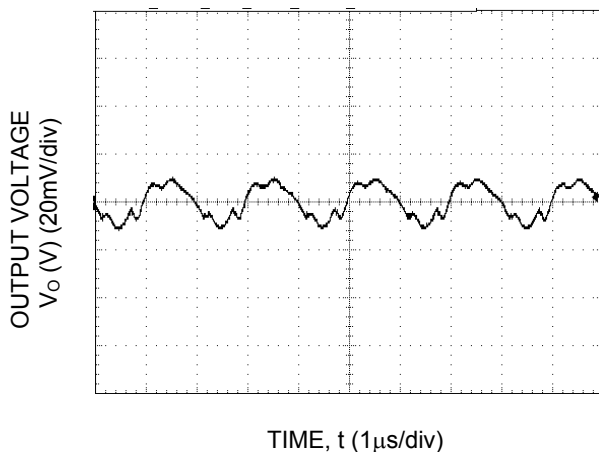


Fig-23. Typical output ripple and noise (C<sub>O</sub>=2x47uF ceramic, V<sub>IN</sub> = 12V, I<sub>o</sub> = I<sub>o,max</sub> ).

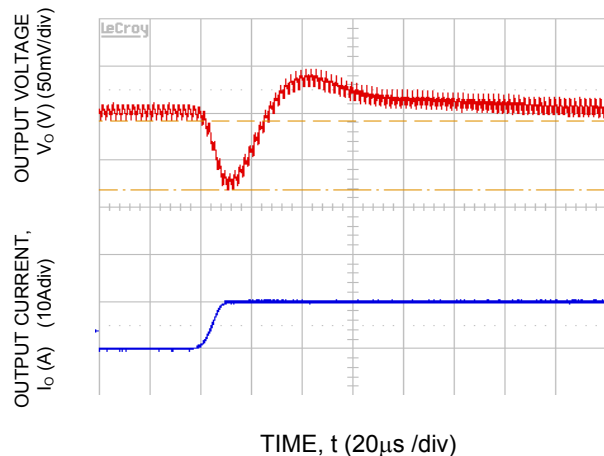


Fig-24. Transient Response to Dynamic Load Change from 50% to 100% at 12V<sub>in</sub>, C<sub>out</sub>= 5x47uF+1x330uF, C<sub>Tune</sub>=2200pF & R<sub>Tune</sub>=220ohms

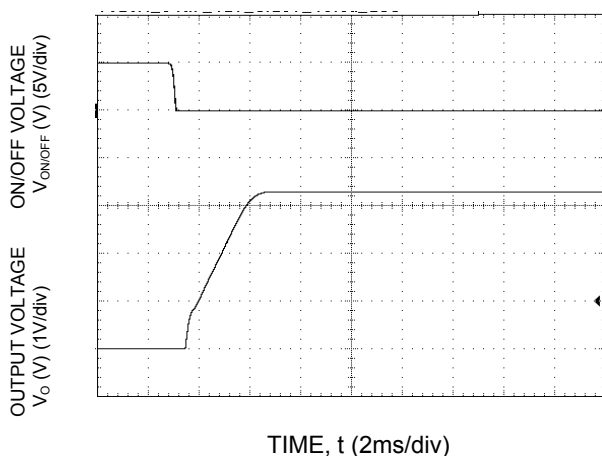


Fig-25. Typical Start-up Using On/Off Voltage (I<sub>o</sub> = I<sub>o,max</sub>).

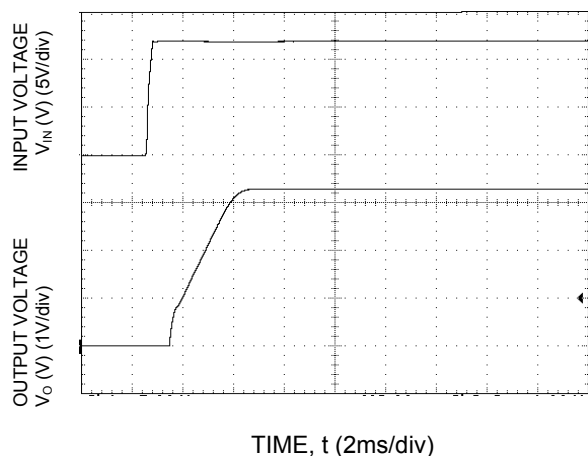


Fig-26. Typical Start-up Using Input Voltage (V<sub>IN</sub> = 12V, I<sub>o</sub> = I<sub>o,max</sub>).

## FGMD12SR6020\*A

3-14.4Vdc Input, 20A, 0.45-5.5Vdc Output

## Data Sheet

### Characteristic Curves

The following figures provide typical characteristics for the 20A Digital **Tomodachi** at 2.5V<sub>o</sub> and 25°C

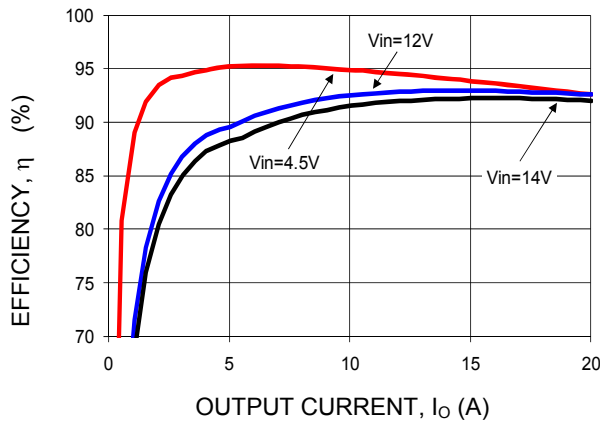


Fig-27. Converter Efficiency versus Output Current.

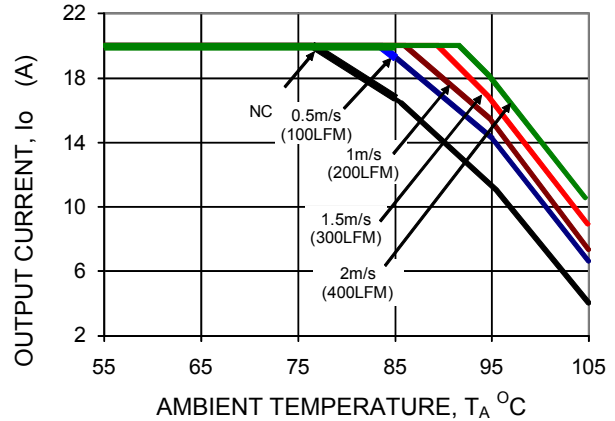


Fig-28. Derating Output Current versus Ambient Temperature and Airflow.

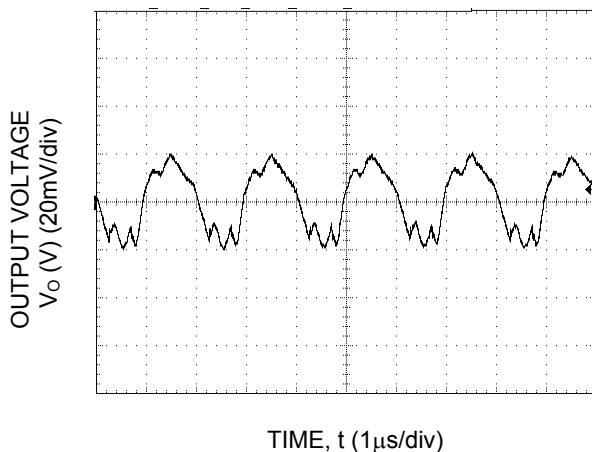


Fig-29. Typical output ripple and noise (C<sub>O</sub>=2x47uF ceramic, V<sub>IN</sub> = 12V, I<sub>o</sub> = I<sub>o,max</sub> ).

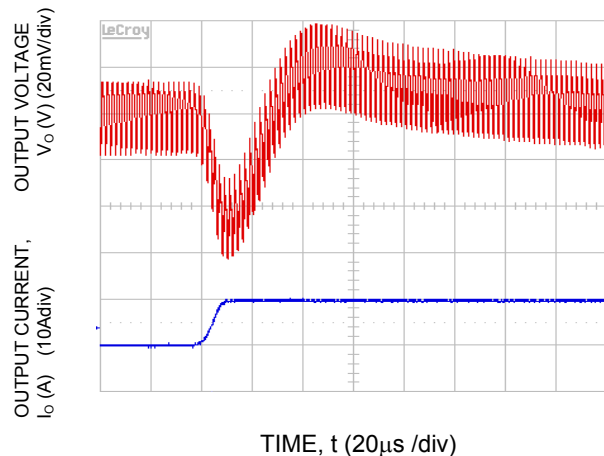


Fig-30. Transient Response to Dynamic Load Change from 50% to 100% at 12V<sub>in</sub>, C<sub>out</sub>= 2x47uF+2x330uF, C<sub>Tune</sub>=3300pF & R<sub>Tune</sub>=220ohms

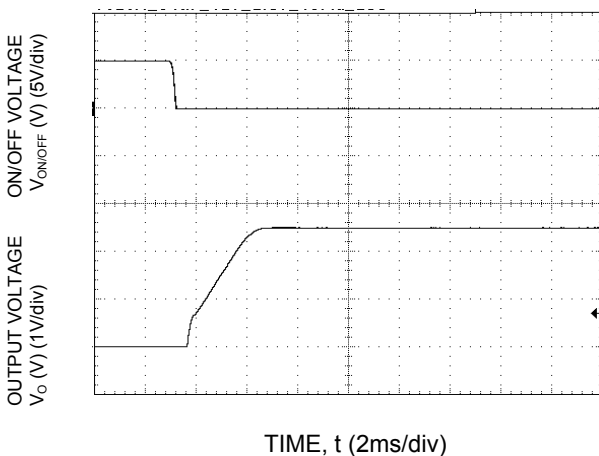


Fig-31. Typical Start-up Using On/Off Voltage (I<sub>o</sub> = I<sub>o,max</sub>).

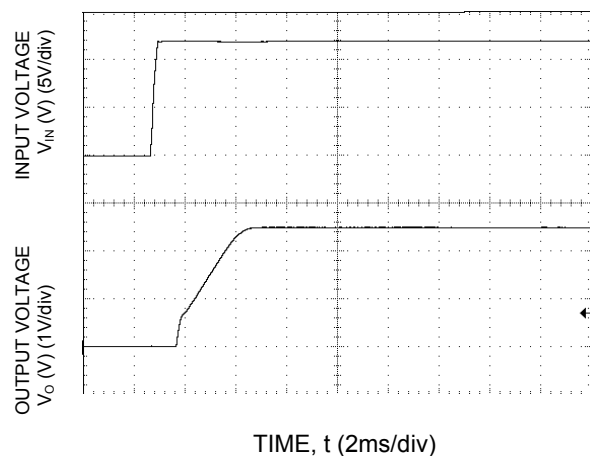


Fig-32. Typical Start-up Using Input Voltage (V<sub>IN</sub> = 12V, I<sub>o</sub> = I<sub>o,max</sub>).

## FGMD12SR6020\*A

3-14.4Vdc Input, 20A, 0.45-5.5Vdc Output

## Data Sheet

### Characteristic Curves

The following figures provide typical characteristics for the 20A Digital **Tomodachi** at 1.8V<sub>o</sub> and 25°C

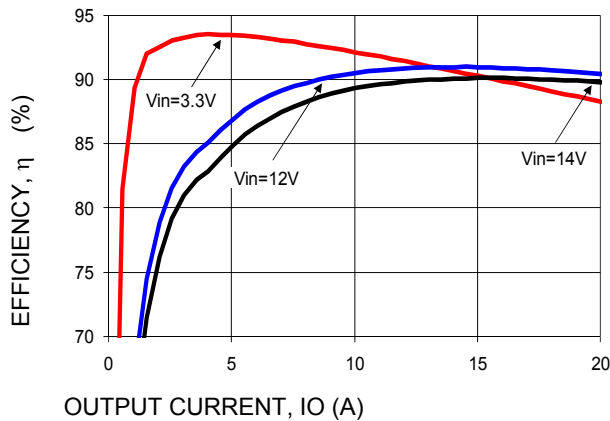


Fig-33. Converter Efficiency versus Output Current.

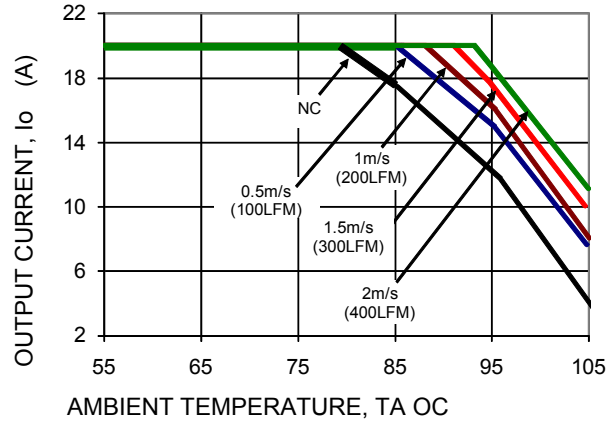


Fig-34. Derating Output Current versus Ambient Temperature and Airflow.

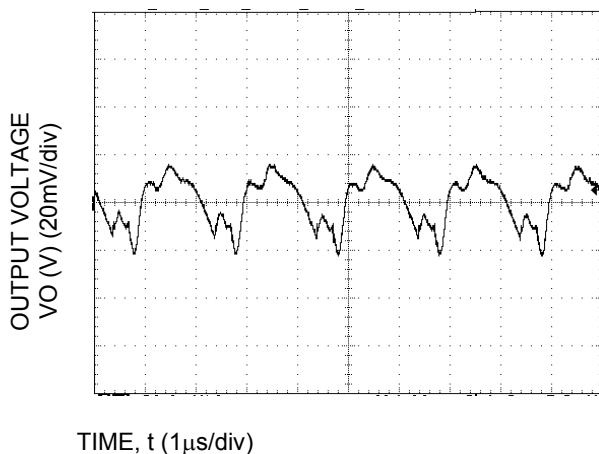


Fig-35. Typical output ripple and noise (C<sub>O</sub>=2x47μF ceramic, V<sub>IN</sub> = 12V, I<sub>O</sub> = I<sub>O,max</sub> ).

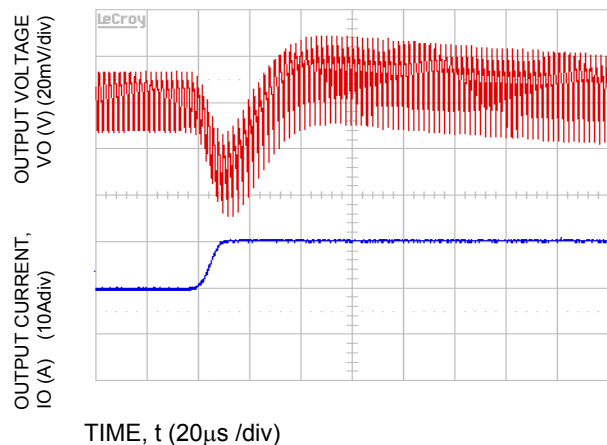


Fig-36. Transient Response to Dynamic Load Change from 50% to 100% at 12V<sub>in</sub>, C<sub>out</sub>= 2x47μF+3x330μF, C<sub>Tune</sub>=5600pF & R<sub>Tune</sub>=220ohms

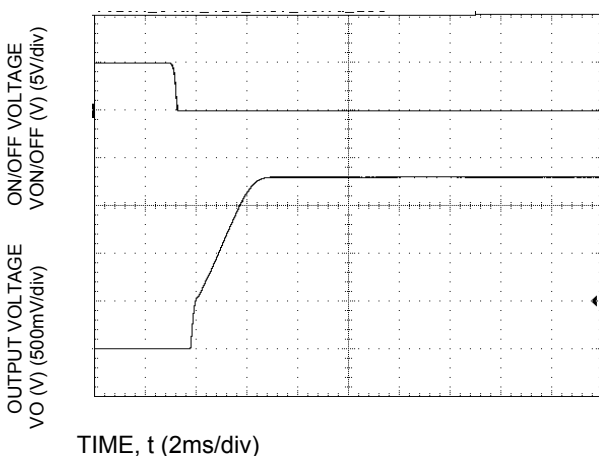


Fig-37. Typical Start-up Using On/Off Voltage (I<sub>O</sub> = I<sub>O,max</sub>).

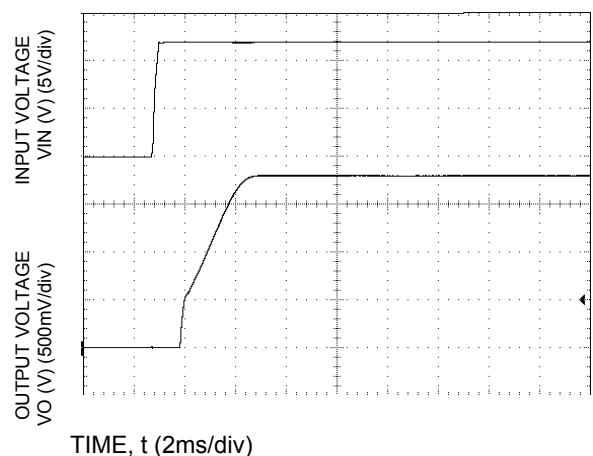


Fig-38. Typical Start-up Using Input Voltage (V<sub>IN</sub> = 12V, I<sub>O</sub> = I<sub>O,max</sub>).



## FGMD12SR6020\*A

3-14.4Vdc Input, 20A, 0.45-5.5Vdc Output

## Data Sheet

### Characteristic Curves

The following figures provide typical characteristics for the 20A Digital **Tomodachi** at 1.2V<sub>o</sub> and 25°C

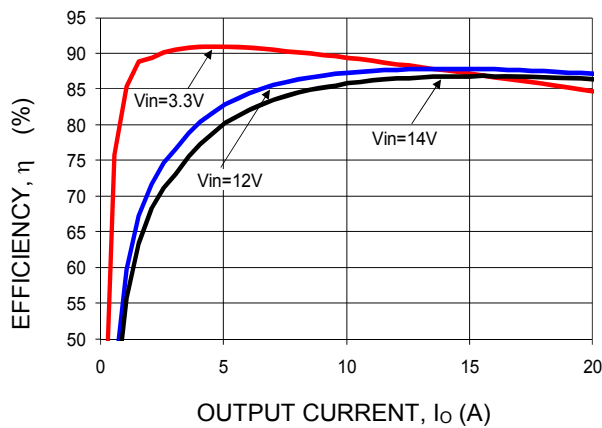


Fig-39. Converter Efficiency versus Output Current.

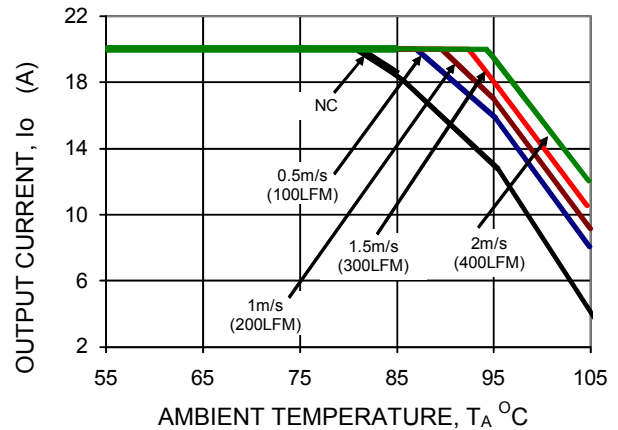


Fig-40. Derating Output Current versus Ambient Temperature and Airflow.

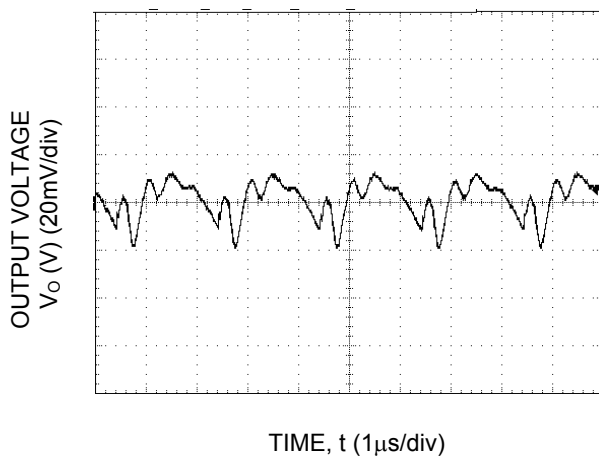


Fig-41. Typical output ripple and noise (C<sub>O</sub>=2x47uF ceramic, V<sub>IN</sub> = 12V, I<sub>o</sub> = I<sub>o,max</sub> ).

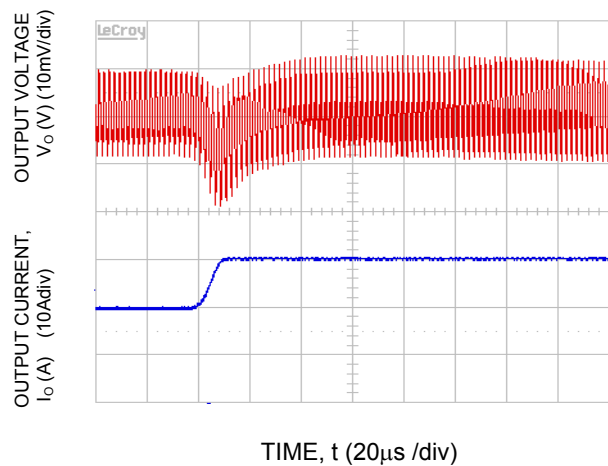


Fig-42. Transient Response to Dynamic Load Change from 50% to 100% at 12V<sub>in</sub>, C<sub>out</sub>= 1x47uF+5x330uF, C<sub>Tune</sub>=10nF & R<sub>Tune</sub>=178ohms

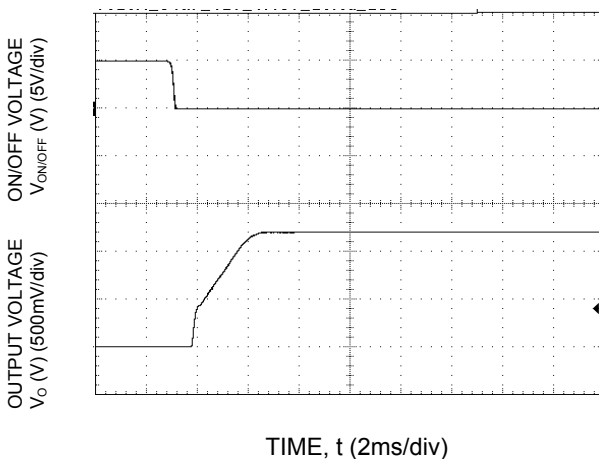


Fig-43. Typical Start-up Using On/Off Voltage (I<sub>o</sub> = I<sub>o,max</sub>).

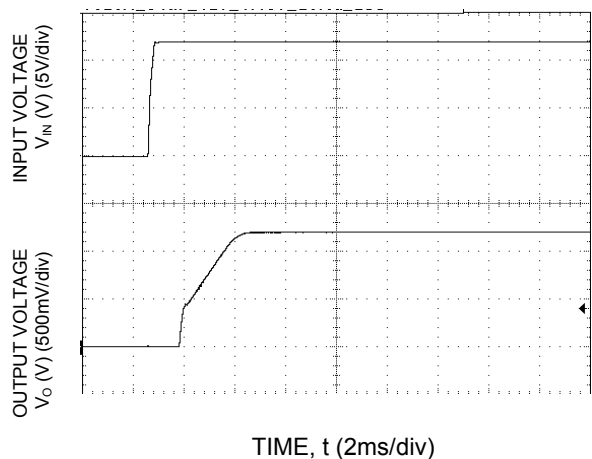


Fig-44. Typical Start-up Using Input Voltage (V<sub>IN</sub> = 12V, I<sub>o</sub> = I<sub>o,max</sub>).

## FGMD12SR6020\*A

3-14.4Vdc Input, 20A, 0.45-5.5Vdc Output

## Data Sheet

### Characteristic Curves

The following figures provide typical characteristics for the 20A Digital **Tomodachi** at 0.6V<sub>o</sub> and 25°C

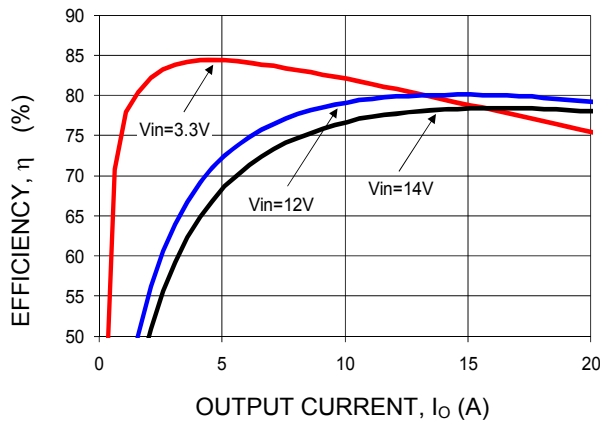


Fig-45. Converter Efficiency versus Output Current.

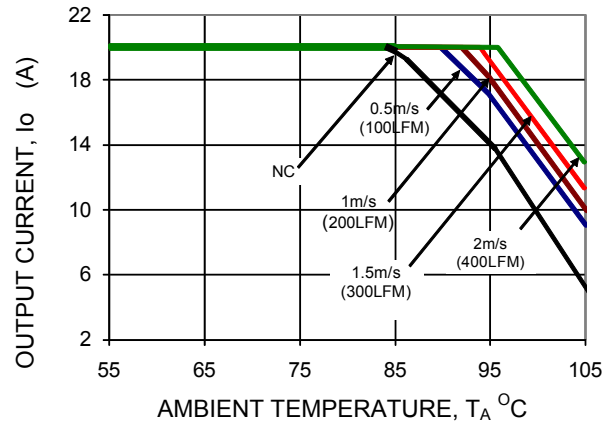


Fig-46. Derating Output Current versus Ambient Temperature and Airflow.

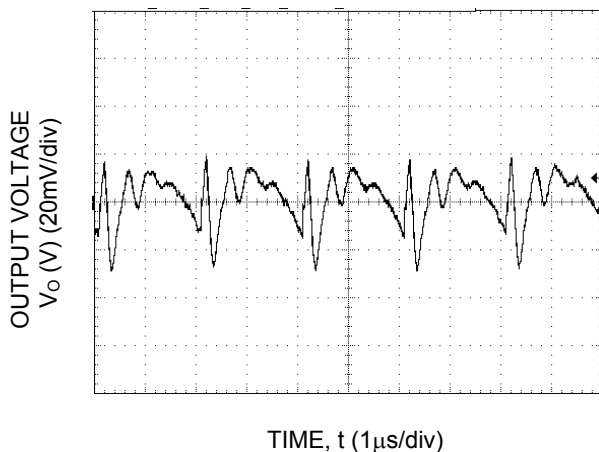


Fig-47. Typical output ripple and noise (C<sub>O</sub>=2x47uF ceramic, V<sub>IN</sub> = 12V, I<sub>o</sub> = I<sub>o,max</sub> ).

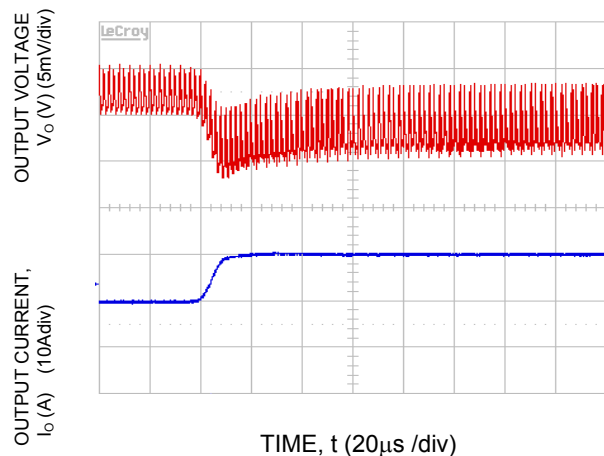


Fig-48. Transient Response to Dynamic Load Change from 50% to 100% at 12Vin, C<sub>out</sub>= 1x47uF+11x330uF, C<sub>Tune</sub>=47nF, R<sub>Tune</sub>=178ohms

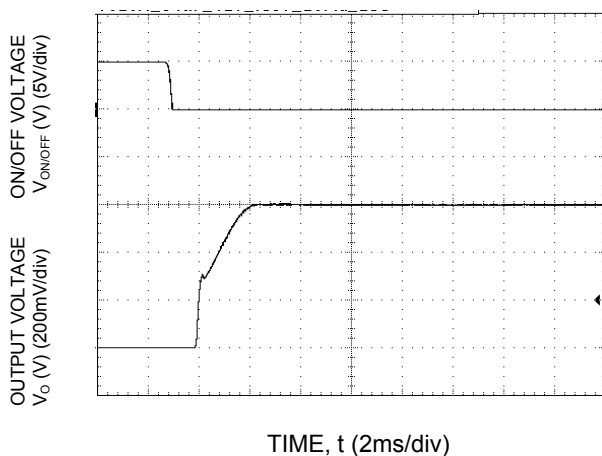


Fig-49. Typical Start-up Using On/Off Voltage (I<sub>o</sub> = I<sub>o,max</sub>).

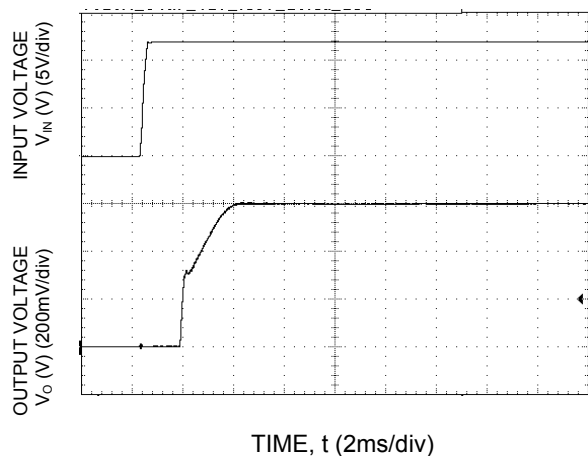


Fig-50. Typical Start-up Using Input Voltage (V<sub>IN</sub> = 12V, I<sub>o</sub> = I<sub>o,max</sub>).

# FGMD12SR6020\*A

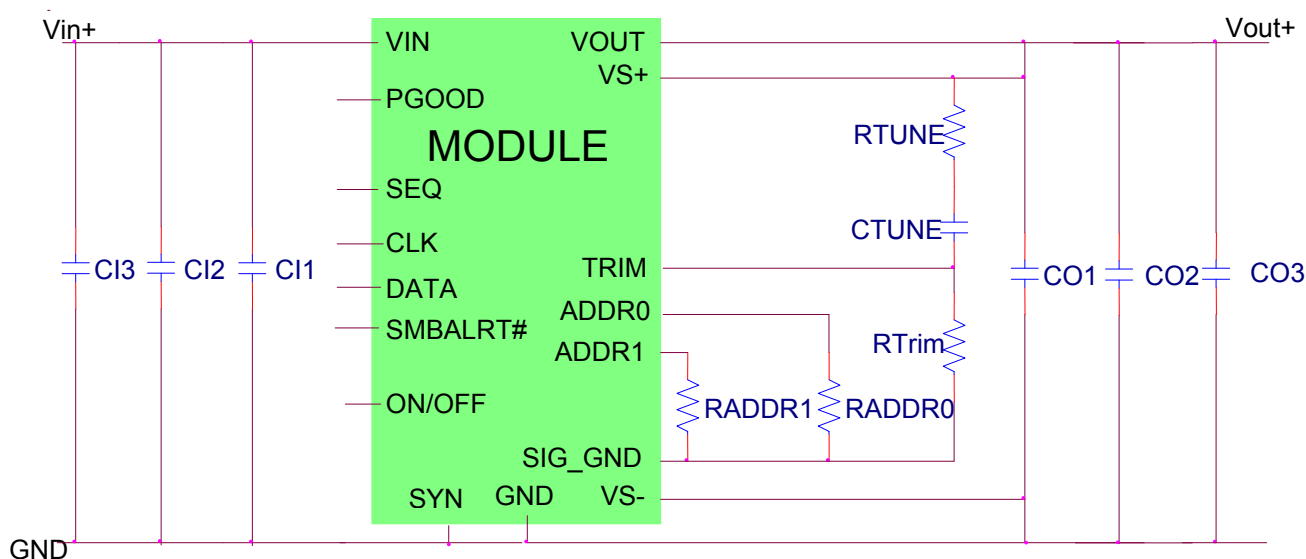
## Data Sheet

3-14.4Vdc Input, 20A, 0.45-5.5Vdc Output

### Example Application Circuit

#### Requirements:

Vin: 12V  
 Vout: 1.8V  
 Iout: 15A max., worst case load transient is from 10A to 15A  
 $\Delta V_{out}$ : 1.5% of Vout (27mV) for worst case load transient  
 Vin, ripple: 1.5% of Vin (180mV, p-p)



CI1	Decoupling cap - 1x0.047uF/16V ceramic capacitor (e.g. Murata LLL185R71C473MA01)
CI2	3x22uF/16V ceramic capacitor (e.g. Murata GRM32ER61C226KE20)
CI3	47uF/16V bulk electrolytic
Co1	Decoupling cap - 1x0.047uF/16V ceramic capacitor (e.g. Murata LLL185R71C473MA01)
Co2	N/A
Co3	3 x 330uF/6.3V Polymer (e.g. Sanyo Poscap)
C <sub>TUNE</sub>	4700pF ceramic capacitor (can be 1206, 0805 or 0603 size)
R <sub>TUNE</sub>	330 ohms SMT resistor (can be 1206, 0805 or 0603 size)
R <sub>Trim</sub>	10kΩ SMT resistor (can be 1206, 0805 or 0603 size, recommended tolerance of 0.1%)

**Note:** The DATA, CLK and SMBALRT pins do not have any pull-up resistors inside the module. Typically, the SMBus master controller will have the pull-up resistors as well as provide the driving source for these signals.

## FGMD12SR6020\*A

## Data Sheet

3-14.4Vdc Input, 20A, 0.45-5.5Vdc Output

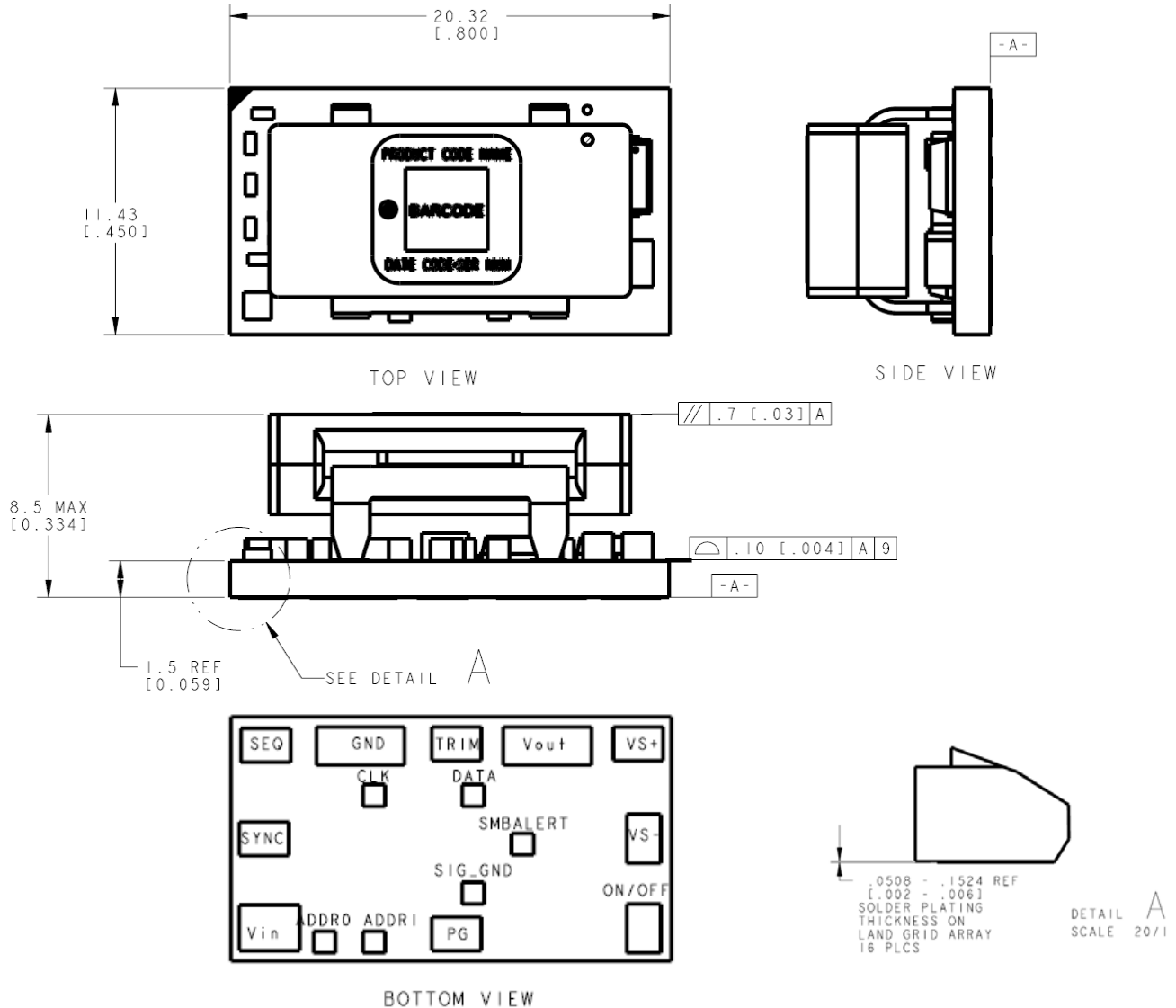
### Mechanical Drawing

All dimensions are in millimeters (inches)

Tolerances:

x.x mm  $\pm$  0.5 mm (x.xx in.  $\pm$  0.02 in.) [unless otherwise indicated]

x.xx mm  $\pm$  0.25 mm (x.xxx in  $\pm$  0.010 in.)



Pin Connections			
Pin #	Function	Pin #	Function
1	ON/OFF	10	SYNC *1
2	Vin	11	CLK
3	SEQ	12	DATA
4	GND	13	SMBALERT#
5	TRIM	14	SIG_GND
6	Vout	15	ADDR1
7	VS+	16	ADDR0
8	VS-		
9	PGood		

\*1 if not used, connect to Ground

# FGMD12SR6020\*A

## Data Sheet

3-14.4Vdc Input, 20A, 0.45-5.5Vdc Output

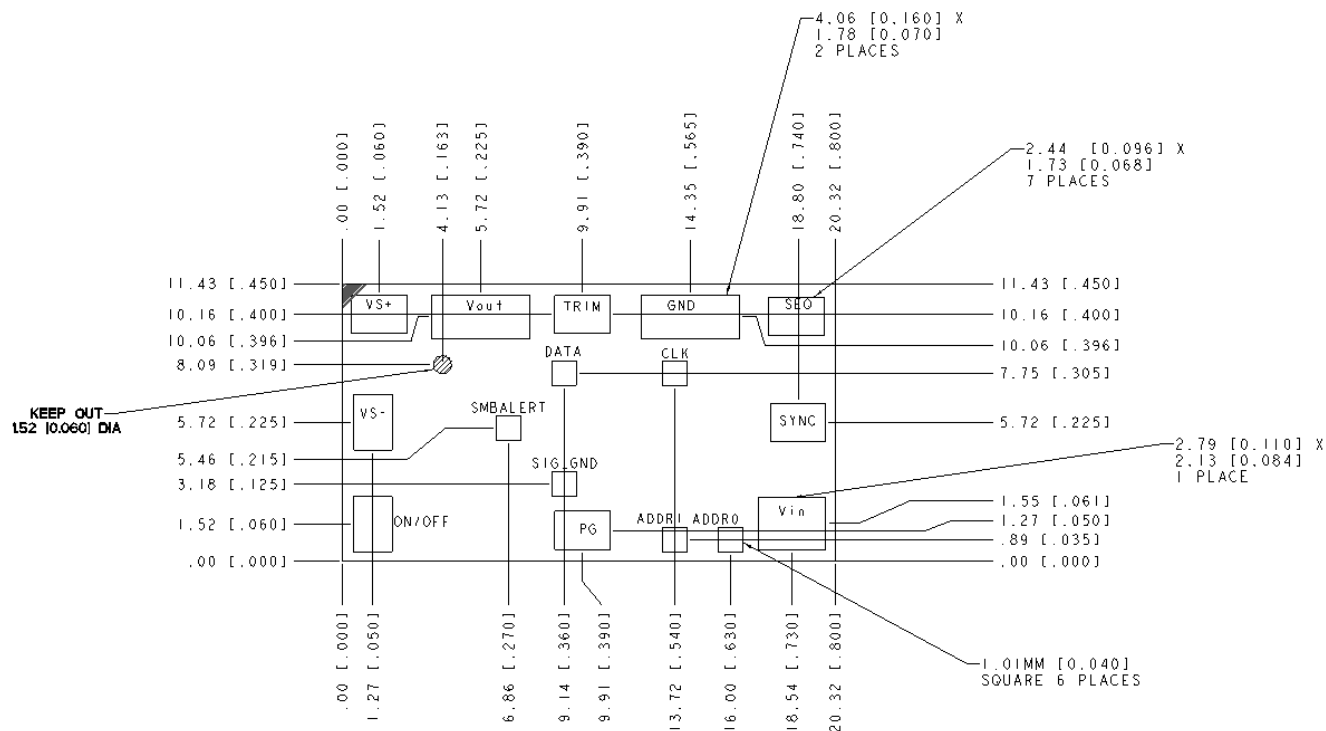
### Recommended Pad Layout

All dimensions are in millimeters (inches)

Tolerances:

x.x mm  $\pm$  0.5 mm (x.xx in.  $\pm$  0.02 in.) [unless otherwise indicated]

x.xx mm  $\pm$  0.25 mm (x.xxx in.  $\pm$  0.010 in.)



RECOMMENDED FOOTPRINT  
-THROUGH THE BOARD-

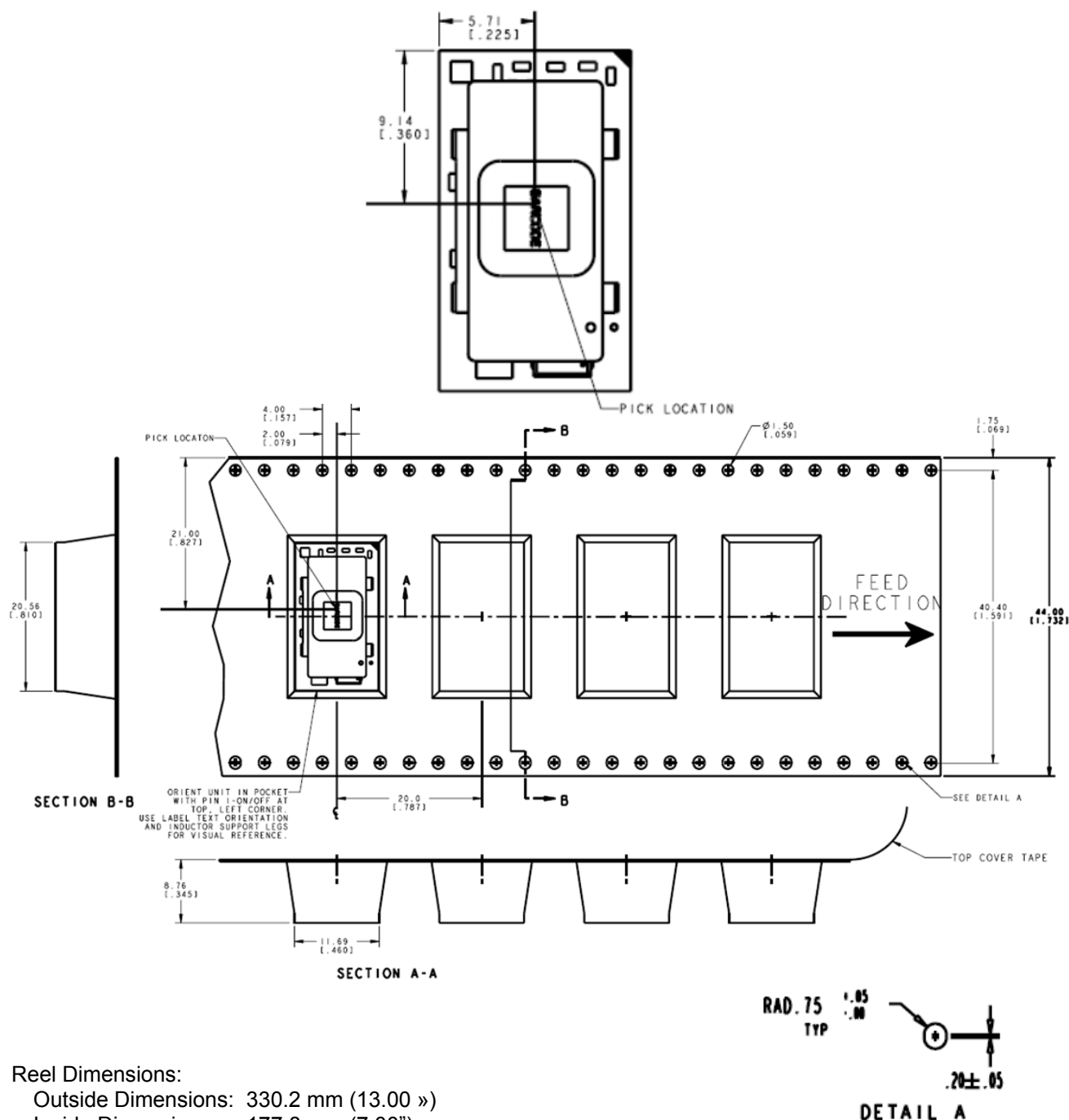
Pin Connections			
Pin #	Function	Pin #	Function
1	ON/OFF	10	SYNC <sup>*1</sup>
2	Vin	11	CLK
3	SEQ	12	DATA
4	GND	13	SMBALERT#
5	TRIM	14	SIG_GND
6	Vout	15	ADDR1
7	VS+	16	ADDR0
8	VS-		
9	PGood		

\*1 If not used, connect to Ground

## Data Sheet

## Packaging Details

All Dimensions are in millimeters and (in inches).



Outside Dimensions: 330.2 mm (13.00 »)  
Inside Dimensions: 177.8 mm (7.00")  
Tape Width: 44.00 mm (1.732")



## FGMD12SR6020\*A

3-14.4Vdc Input, 20A, 0.45-5.5Vdc Output

## Data Sheet

### Surface Mount Information

#### Pick and Place

The 20A Digital **Tomodachi** modules use an open frame construction and are designed for a fully automated assembly process. The modules are fitted with a label designed to provide a large surface area for pick and place operations. The label meets all the requirements for surface mount processing, as well as safety standards, and is able to withstand reflow temperatures of up to 300°C. The label also carries product information such as product code, serial number and the location of manufacture.

#### Nozzle Recommendations

The module weight has been kept to a minimum by using open frame construction. Variables such as nozzle size, tip style, vacuum pressure and placement speed should be considered to optimize this process. The minimum recommended inside nozzle diameter for reliable operation is 3mm. The maximum nozzle outer diameter, which will safely fit within the allowable component spacing, is 7mm.

#### Bottom Side / First Side Assembly

This module is not recommended for assembly on the bottom side of a customer board. If such an assembly is attempted, components may fall off the module during the second reflow process.

#### Lead Free Soldering

The modules are lead-free (Pb-free) and RoHS compliant and fully compatible in a Pb-free soldering process. Failure to observe the instructions below may result in the failure of or cause damage to the modules and can adversely affect long-term reliability.

#### Pb-free Reflow Profile

Power Systems will comply with J-STD-020 Rev. C (Moisture / Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices) for both Pb-free solder profiles and MSL classification procedures. This standard provides a recommended forced-air-convection reflow profile based on the volume and thickness of the package (table 4-2). The suggested Pb-free solder paste is Sn/Ag/Cu (SAC). For questions regarding Land grid array (LGA) soldering, solder volume; please contact Lineage Power for special manufacturing process instructions. The recommended linear reflow profile

using Sn/Ag/Cu solder is shown in Fig-51. Soldering outside of the recommended profile requires testing to verify results and performance.

#### MSL Rating

The 20A Digital **Tomodachi** modules have a MSL rating of 2a.

#### Storage and Handling

The recommended storage environment and handling procedures for moisture-sensitive surface mount packages is detailed in J-STD-033 Rev. A (Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices). Moisture barrier bags (MBB) with desiccant are required for MSL ratings of 2 or greater. These sealed packages should not be broken until time of use. Once the original package is broken, the floor life of the product at conditions of  $\leq 30^{\circ}\text{C}$  and 60% relative humidity varies according to the MSL rating (see J-STD-033A). The shelf life for dry packed SMT packages will be a minimum of 12 months from the bag seal date, when stored at the following conditions:  $< 40^{\circ}\text{C}$ ,  $< 90\%$  relative humidity.

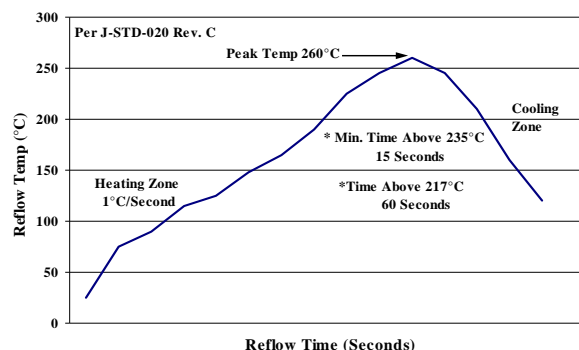


Fig-51: Recommended linear reflow profile using Sn/Ag/Cu solder.

#### Post Solder Cleaning and Drying Considerations

Post solder cleaning is usually the final circuit-board assembly process prior to electrical board testing. The result of inadequate cleaning and drying can affect both the reliability of a power module and the testability of the finished circuit-board assembly. For guidance on appropriate soldering, cleaning and drying procedures, refer to *Board Mounted Power Modules: Soldering and Cleaning Application Note (AN04-001)*.

**FGMD12SR6020\*A****Data Sheet**

3-14.4Vdc Input, 20A, 0.45-5.5Vdc Output

Part Number System

Product Series	Shape	Regulation	Input Voltage	Mounting Scheme	Output Voltage	Rated Current	ON/OFF Logic	Pin Shape
<b>FG</b>	<b>M</b>	<b>D</b>	<b>12</b>	<b>S</b>	<b>R60</b>	<b>20</b>	<b>*</b>	<b>A</b>
Series Name	Medium	D: Digital Feature	Typ=12V	Surface Mount	0.6V (Programmable: See page 9)	20A	N: Negative P: Positive	Standard

## Cautions

NUCLEAR AND MEDICAL APPLICATIONS: FDK Corporation products are not authorized for use as critical components in life support systems, equipment used in hazardous environments, or nuclear control systems without the written consent of FDK Corporation.

SPECIFICATION CHANGES AND REVISIONS: Specifications are version-controlled, but are subject to change without notice.

# AMEYA360

## Components Supply Platform

Authorized Distribution Brand :



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