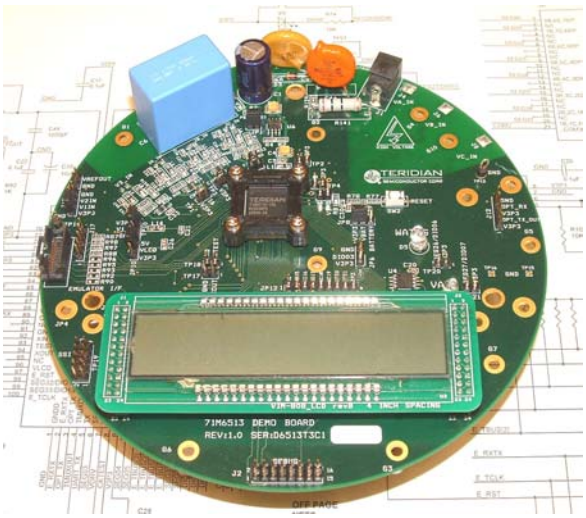
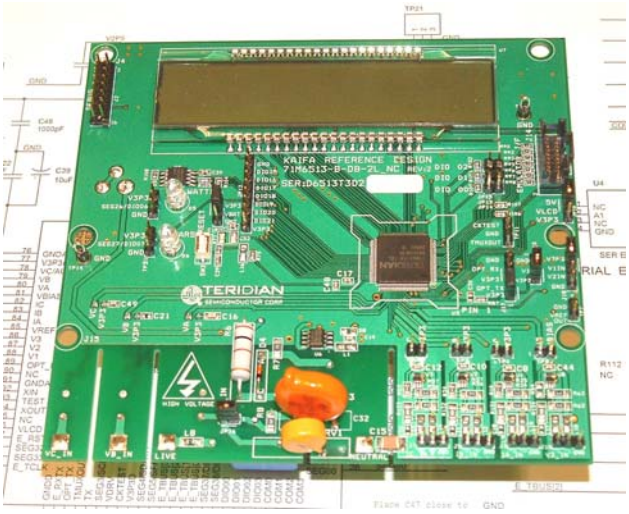
71M6513/71M6513H Demo Board

USER'S MANUAL





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Revision 5.6

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71M6513/71M6513H

3-Phase Energy Meter IC

DEMO BOARD

USER'S MANUAL

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1 GETTING STARTED

1.1 GENERAL

The TERIDIAN Semiconductor Corporation (TSC) 71M6513/71M6513H Demo Board is a demonstration board for evaluating the 71M6513/71M6513H device for 3-phase electronic power metering applications. It incorporates a 71M6513 or 71M6513H integrated circuit, peripheral circuitry such as a serial EEPROM, emulator port, and on board power supply as well as a companion Debug Board that allows a connection to a PC through a RS232 port. The demo board allows the evaluation of the 71M6513 or 71M6513H energy meter chip for measurement accuracy and overall system use.

The board is pre-programmed with a Demo Program (file name 6513_demo.hex) in the FLASH memory of the 71M6513/6513H IC. This embedded application is developed to exercise all low-level function calls to directly manage the peripherals, flash programming, and CPU (clock, timing, power savings, etc.).

The 71M6513/6513H IC on the Demo Board is pre-programmed with default calibration factors.

1.2 SAFETY AND ESD NOTES

Connecting live voltages to the demo board system will result in potentially hazardous voltages on the demo board.

BEFORE OPERATING THE DEMO BOARD, THE JUMPERS ON JP2 AND JP3 (IF INSTALLED) SHOULD BE REMOVED! IT IS RECOMMENDED TO OPERATE THE DEBUG BOARD WITH ITS OWN POWER SUPPLY.

THE DEMO SYSTEM IS ESD SENSITIVE! ESD PRECAUTIONS SHOULD BE TAKEN WHEN HANDLING THE DEMO BOARD!

EXTREME CAUTION SHOULD BE TAKEN WHEN HANDLING THE DEMO BOARD ONCE IT IS CONNECTED TO LIVE VOLTAGES!

1.3 DEMO KIT CONTENTS

- Demo Board with 71M6513/71M6513H IC and pre-loaded demo program:
  - D6513T3B2 Demo Board (standard poly-phase), or
  - D6513T3C1 Demo Board (poly-phase w/ added neutral current capability)
- Debug Board
- Two 5VDC/1,000mA universal wall transformers with 2.5mm plug (Switchcraft 712A compatible)
- Serial cable, DB9, Male/Female, 2m length (Digi-Key AE1020-ND)
- CD-ROM containing documentation (data sheet, board schematics, BOM, layout), Demo Code (sources and executable), and utilities

The CD-ROM contains a file named **readme.txt** that specifies all files found on the media and their purpose.

1.4 DEMO BOARD VERSIONS

The following versions of the Demo Board are available:

- Demo Board D6513T3B2 (standard)
- Demo Board D6513T3C1 (with neutral current detection capability)
- Demo Board D6513T3D2 (two layer PCB, with neutral current detection capability)

1.5 COMPATIBILITY

This manual applies to the following hardware and software revisions:

- 71M6513 or 71M6513H chip revision B03
- Demo Kit firmware revision 3.04 and 3.05 or later
- Demo Boards D6513T3B2, D6513T3C1 and D6513T3D2

1.6 SUGGESTED EQUIPMENT NOT INCLUDED

For functional demonstration:

- PC w/ MS-Windows® versions XP, ME, or 2000, equipped with RS232 port (COM port) via DB9 connector

For software development (MPU code):

- Signum ICE (In Circuit Emulator): ADM-51

  http://www.signum.com

- Keil 8051 "C" Compiler kit: CA51

  http://www.keil.com/c51/ca51kit.htm, http://www.keil.com/product/sales.htm

1.7 DEMO BOARD TEST SETUP

Figure 1-1 shows the basic connections of the Demo Board plus Debug Board with the external equipment for desktop testing, i.e. without live power applied. For desktop testing, both the Demo and Debug board may be powered with just the 5VDC power supplies.

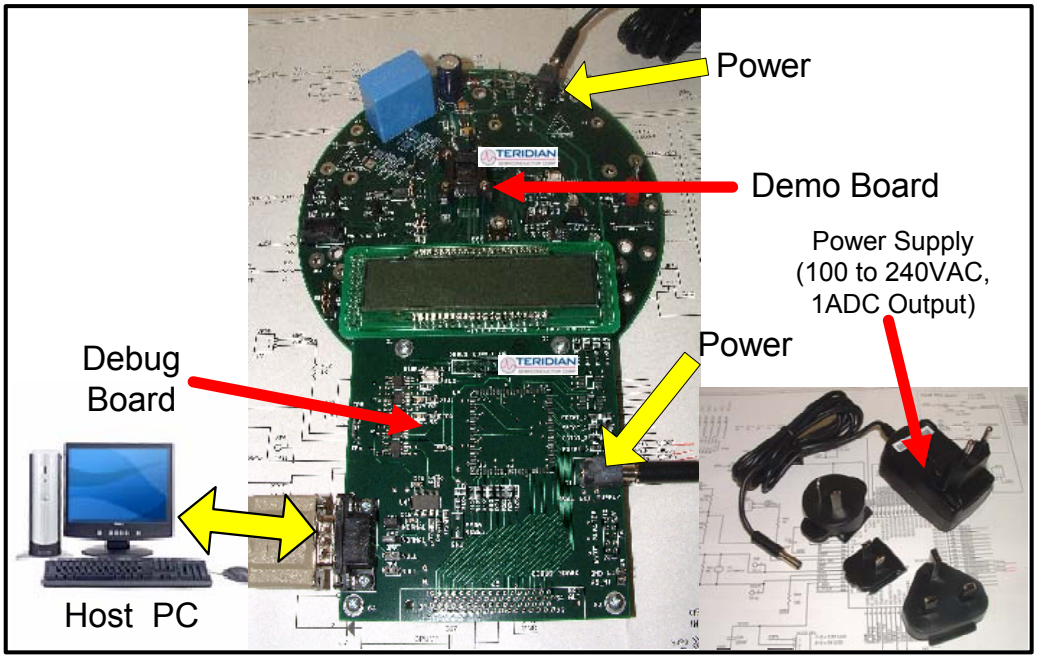


Figure 1-1: TERIDIAN D6513T3B2 Demo Board with Debug Board: Basic Connections

The D6513/T3B2 Demo Board block diagram is shown in Figure 1-2. It consists of a stand-alone (round) meter Demo Board and an optional Debug Board. The Demo Board contains all circuits necessary for operation as a meter, including display, calibration LED, and internal power supply. The Debug Board, when using a separate power supply, is optically isolated from the meter and interfaces to a PC through a 9 pin serial port. For serial communication between the PC and the TERIDIAN 71M6513/71M6513H, the Debug Board needs to be plugged with its connector J3 into connector J2 of the Demo Board.

The D6513/T3C1 Demo Board System is shown in Figure 1-3. It is almost identical to the D6513T3B2, except that the neutral current input is added and the optional power and ground connections from the Demo Board to the Debug Board were removed.

Connections to the external signals to be measured, i.e. scaled AC voltages and current signals derived from shunt resistors or current transformers, are provided on the rear side of the demo board.

Caution: It is recommended to set up the demo board with no live AC voltage connected, and to connect live AC voltages only after the user is familiar with the demo system.

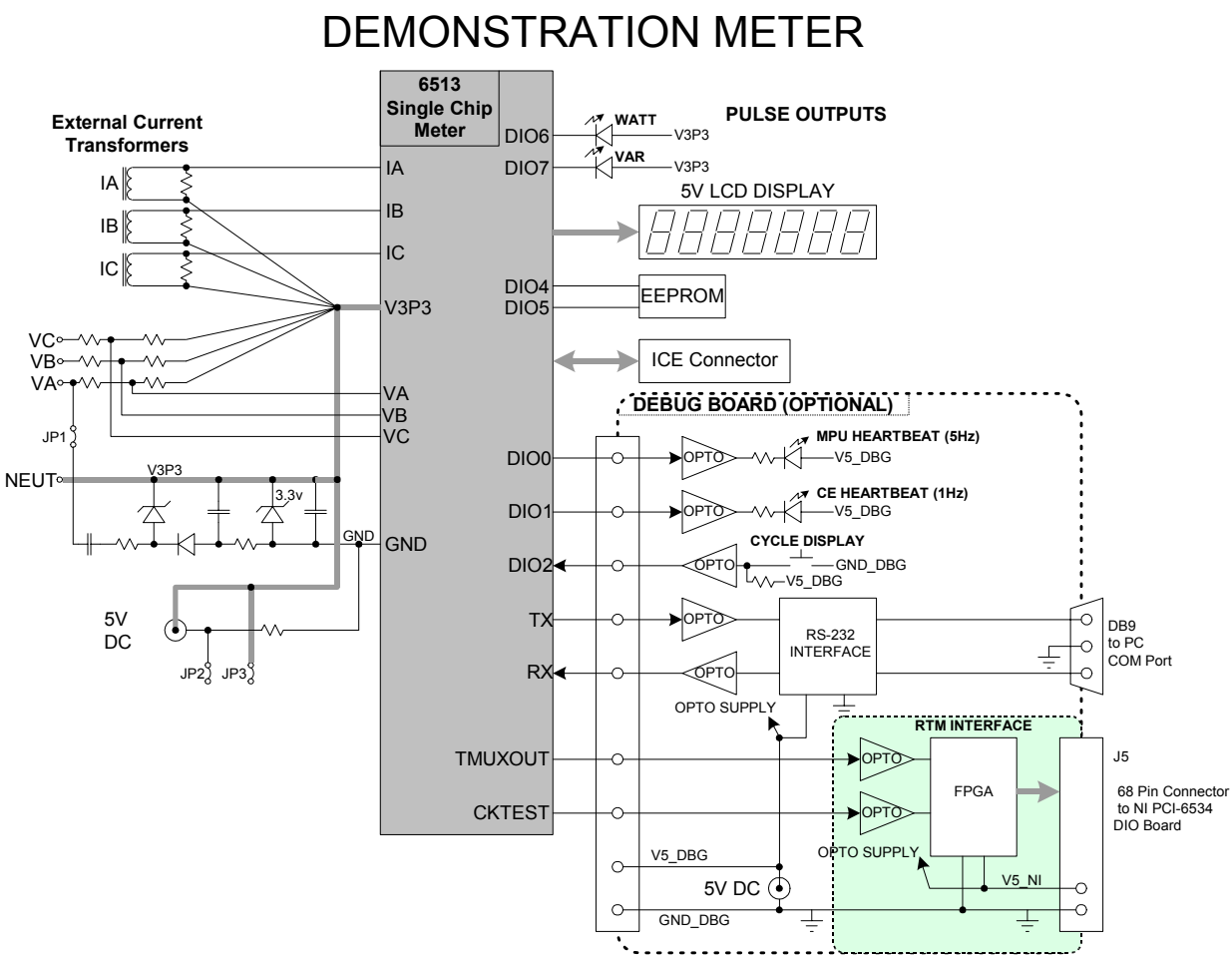


Figure 1-2: Block diagram for the TERIDIAN D6513T3B2 Demonstration Meter with Debug Board

All input signals are referenced to the V3P3 (3.3V power supply to the chip).

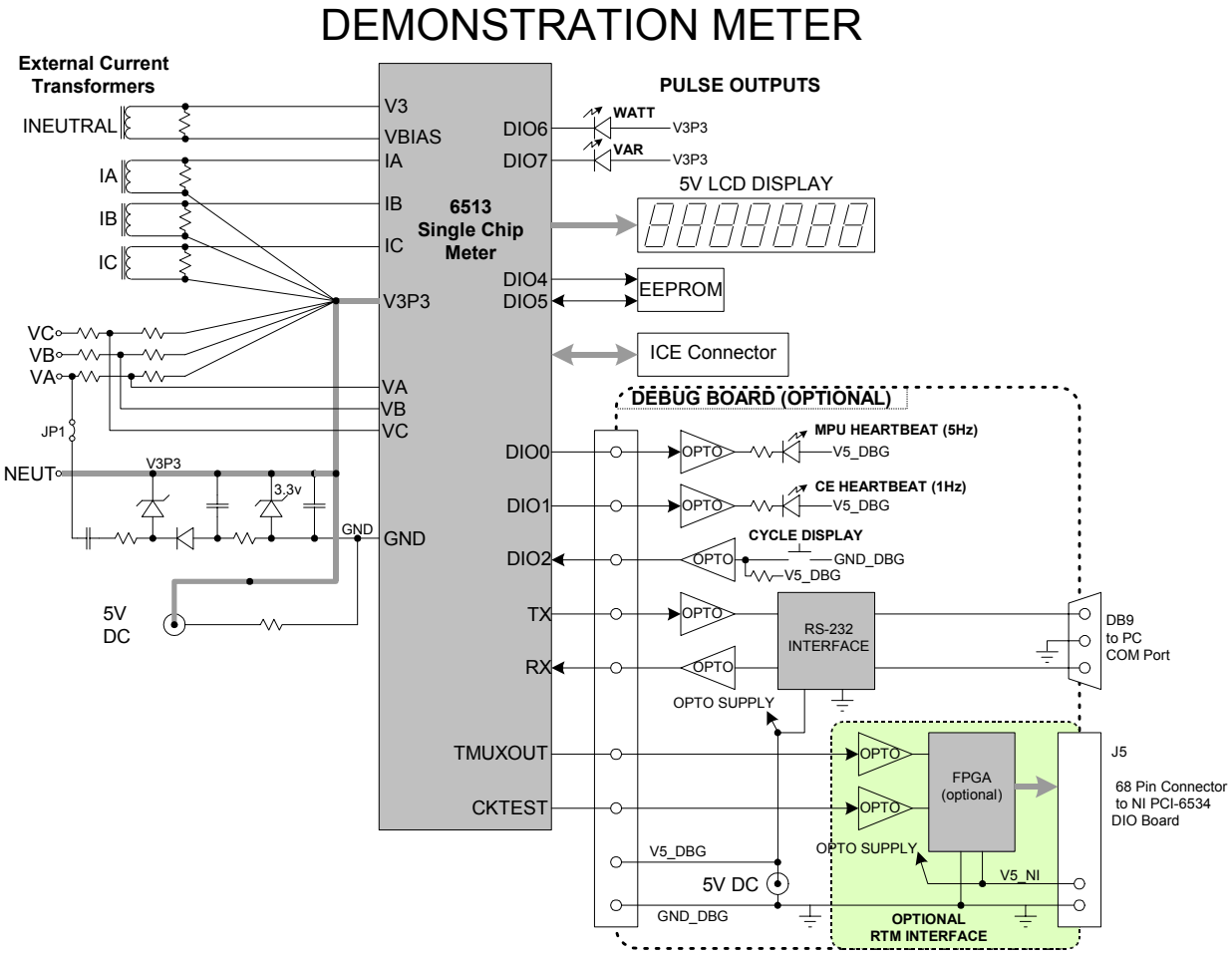


Figure 1-3: Block diagram for the TERIDIAN D6513T3C1 and D6513T3D2 Demo Boards with Debug Board

1.7.1 POWER SUPPLY SETUP

There are several choices for meter power supply:

- Internal (using phase A of the AC line voltage). The internal power supply is only suitable when phase A exceeds 220V RMS.
- External 5VDC connector (J1) on the Demo Board
- External 5VDC connector (J1) on the Debug Board.

The three power supply jumpers, JP1, JP2, and JP3 (JP2/JP3 is only provided on the D6513T3B2 Demo Board), must be consistent with the power supply choice. JP1 connects the AC line voltage to the internal power supply. This jumper should usually be left in place. **JP2 and JP3 should be left open (unconnected).**

1.7.2 CABLE FOR SERIAL CONNECTION (DEBUG BOARD)

For connection of the DB9 serial port to a PC, either a straight or a so-called "null-modem" cable may be used. JP1 and JP2 are plugged in for the straight cable, and JP3/JP4 are empty. The jumper configuration is reversed for the null-modem cable, as shown in Table 1-1.

Cable Configuration	Mode	Jumpers on Debug Board			
		JP1	JP2	JP3	JP4
Straight Cable	**Default**	Installed	Installed	--	--
Null-Modem Cable	Alternative	--	--	Installed	Installed

Table 1-1: Jumper settings on Debug Board

JP1 through JP4 can also be used to alter the connection when the PC is not configured as a DCE device. Table 1-2 shows the connections necessary for the straight DB9 cable and the pin definitions.

PC Pin	Function	Demo Board Pin
2	TX	2
3	RX	3
5	Signal Ground	5

Table 1-2: Straight cable connections

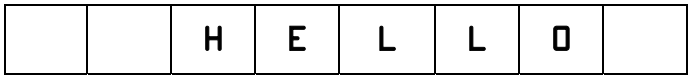
Table 1-3 shows the connections necessary for the null-modem DB9 cable and the pin definitions.

PC Pin	Function	Demo Board Pin
2	TX	3
3	RX	2
5	Signal Ground	5

Table 1-3: Null-modem cable connections

1.7.3 CHECKING OPERATION

A few seconds after power up, the LCD display on the Demo Board should display this brief greeting:



The "HELLO" message should be followed by the display of accumulated energy:

3.				0.	0	0	1

The decimal dot in the leftmost segment will be blinking, indicating activity of the MPU inside the 71M6513/6513H.

If contacts 3 and 5 of J2 are shorted with a jumper (or if the "DISPLAY SEL" switch SW2 on the Debug Board is pressed and held down), the display will show a series of incrementing numbers (1 through 12) in the leftmost digit(s) followed by the default date (2001.01.01) at number 10.

Once, the Debug Board is plugged into J2 of the Demo Board, LED DIO1 on the Debug Board will flash with a frequency of 1Hz, indicating CE activity. The LED DIO0 will flash with a frequency of 5Hz, indicating MPU activity.

1.7.4 SERIAL CONNECTION SETUP

After connecting the DB9 serial port to a PC, start the HyperTerminal application and create a session using the following parameters:

Port Speed: 9600 baud

Data Bits: 8

Parity: None

Stop Bits: 1

Flow Control: XON/XOFF

HyperTerminal can be found by selecting Programs →Accessories → Communications from the Windows© start menu. The connection parameters are configured by selecting File → Properties and then by pressing the Configure button. Port speed and flow control are configured under the General tab (Figure 1-5, left), bit settings are configured by pressing the Configure button (Figure 1-6, right), as shown below. A setup file (file name "Demo Board Connection.ht") for HyperTerminal that can be loaded with File → Open is also provided with the tools and utilities.

Port parameters can only be adjusted when the connection is not active. The disconnect button, as shown in Figure 1-4 must be clicked in order to disconnect the port.

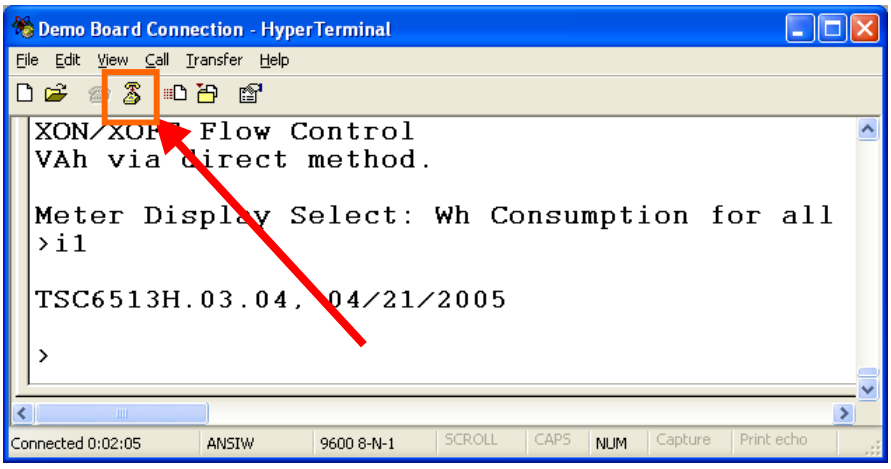


Figure 1-4: Hyperterminal Sample Window with Disconnect Button (Arrow)

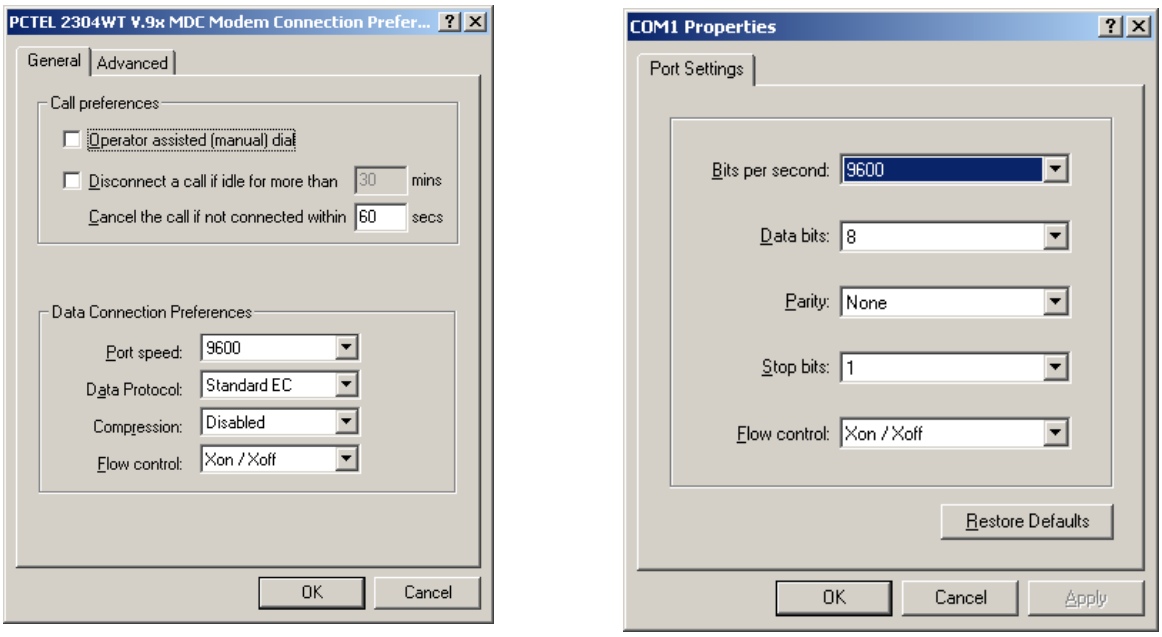


Figure 1-5: Port Speed and Handshake Setup (left) and Port Bit setup (right)

Once, the connection to the demo board is established, press <CR> and the prompt, **>**, should appear. Type **>?** to see the **Demo Code** help menu. Type **>i1** to verify that the demo code revision is 3.04 or later.

1.8 USING THE DEMO BOARD

The 71M6513/6513H Demo Board is a ready-to-use meter prepared for use with an external current transformer.

Using the Demo Board involves communicating with the Demo Code via the command line interface (CLI). The CLI allows all sorts of manipulations to the metering parameters, access to the EEPROM, initiation of auto-cal sequences, selection of the displayed parameters, changing calibration factors and many more operations.

Before evaluating the 71M6513/6513H on the Demo Board, users should get familiar with the commands and responses of the CLI. A complete description of the CLI is provided in section 1.8.1.

1.8.1 SERIAL COMMAND LANGUAGE

The Demo Code residing in the flash memory of the 71M6513/6513H provides a convenient way of examining and modifying key meter parameters. Once the Demo Board is connected to a PC or terminal per the instructions given in Section 1.7.2 and 1.7.4, typing '?' will bring up the list of commands shown in Figure 1-6.

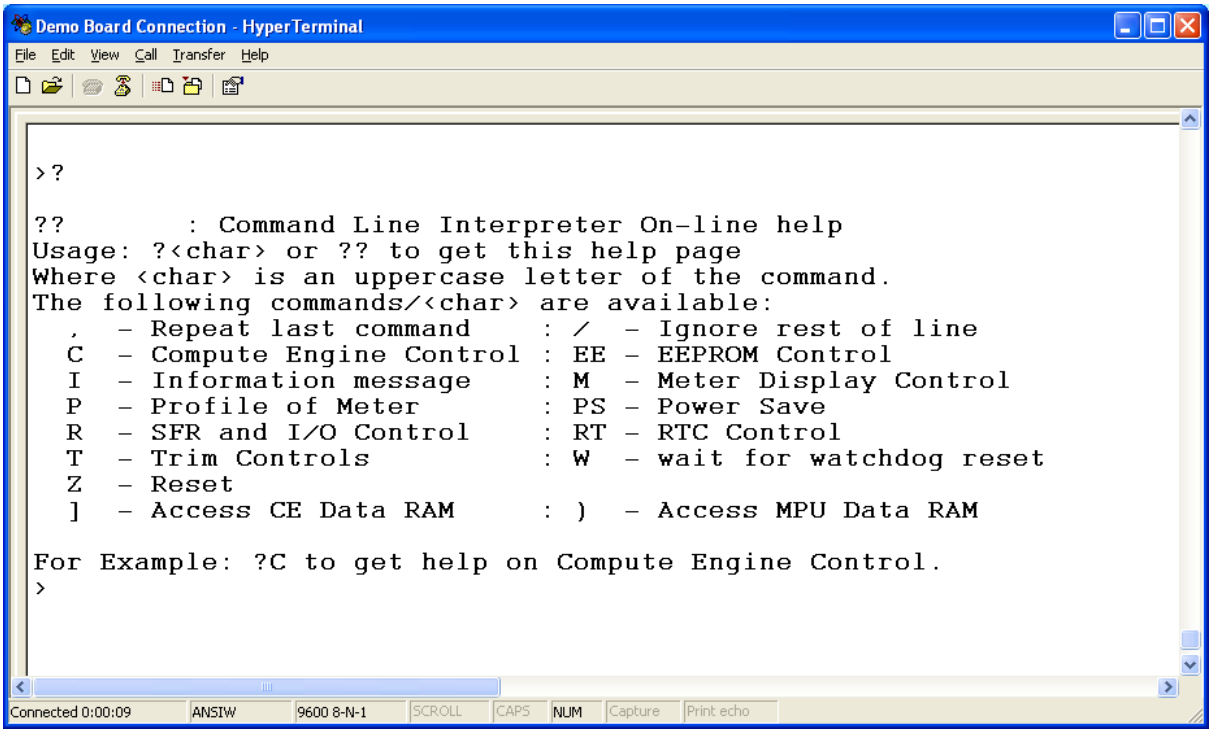


Figure 1-6: Command Line Help Display

The tables in this chapter describe the commands in detail.

Demo Code revision 3.05 offers more commands than revision 3.04. Commands only available on 3.05 are marked in the tables presented in this chapter.

Commands to Display Help on the CLI Commands:

?	HELP	
Description:	Command help available for each of the options below.	
Command combinations:	?	Command line interpreter help menu.
	?]	Display help on access CE data RAM
	?)	Display help on access MPU RAM
	?,	Display help on repeat last command
	?/	Display help on ignore rest of line
	?C	Display help on compute engine control and calibration. **In 3.05, pulse counter functions are offered.**
	?EE	Display help on EEPROM control
	?I	Display help on information message
	?M	Display help on meter display control
	?P	Display help on profile of meter
	?R	Display help on SFR control
	?RT	Display help on RTC control
	?T	Display help on trim control
	?W	**Display help on the wait/reset command – 3.05 only**
	?Z	Display help on reset
Examples:	??	Display the command line interpreter help menu.
	?C	Displays compute engine control help.

Commands for CE Data Access:

]	CE DATA ACCESS	
Description:	Allows user to read from and write to CE data space.	
Usage:	] [Starting CE Data Address] [option]…[option]	
Command combinations:	]A???	Read consecutive 16-bit words in Decimal, starting at address A
	]A$$$	Read consecutive 16-bit words in Hex, starting at address A
	]A=n=n	Write consecutive memory values, starting at address A
	]U	Update default version of CE Data in flash memory
Example:	]40$$$	Reads CE data words 0x40, 0x41 and 0x42.
	]7E=12345678=9876ABCD	Writes two words starting @ 0x7E

CE data space is the address range for the CE DRAM (0x1000 to 0x13FF). All CE data words are in 4-byte (32-bit) format. The offset of 0x1000 does not have to be entered when using the] command, thus typing]A? will access the 32-bit word located at the byte address 0x1000 + 4 * A = 0x1028.

Commands for MPU/XDATA Access:

)	MPU DATA ACCESS	
Description:	Allows user to read from and write to MPU data space.	
Usage:	) [Starting MPU Data Address] [option]…[option]	
Command combinations:	)A???	Read three consecutive 32-bit words in Decimal, starting at address A
	)A$$$	Read three consecutive 32-bit words in Hex, starting at address A
	)A=n=m	Write the values n and m to two consecutive addresses starting at address A
Example:	)08$$$$	Reads data words 0x08, 0x0C, 0x10, 0x14
	)04=12345678=9876ABCD	Writes two words starting @ 0x04

MPU or XDATA space is the address range for the MPU XRAM (0x0000 to 0x3FF). All MPU data words are in 4-byte (32-bit) format. Typing]A? will access the 32-bit word located at the byte address 4 * A = 0x28. The energy accumulation registers of the Demo Code can be accessed by typing two Dollar signs ("$$"), typing question marks will display negative decimal values if the most significant bit is set.

RAM access is limited to the lower 1KB address range. Read and write operations will "wrap around" at higher addresses, i.e.)200? will yield the same result as)0?

Commands for DIO RAM (Configuration RAM) and SFR Control:

R	DIO AND SFR CONTROL	
Description:	Allows the user to read from and write to DIO RAM and special function registers (SFRs).	
Usage:	R [option] [register] … [option]	
Command combinations:	RIx…	Select I/O RAM location x (0x2000 offset is automatically added)
	Rx…	Select internal SFR at address x
	Ra???...	Read consecutive SFR registers in Decimal, starting at address a
	Ra$$$...	Read consecutive registers in Hex, starting at address a
	Ra=n=m…	Set values of consecutive registers to n and m starting at address a
Example:	RI2$$$	Read DIO RAM registers 2, 3, and 4 in Hex.

DIO or Configuration RAM space is the address range 0x2000 to 0x20FF. This RAM contains registers used for configuring basic hardware and functional properties of the 71M6513/6513H and is organized in bytes (8 bits). The 0x2000 offset is automatically added when the command RI is typed.

The SFRs (special function registers) are located in internal RAM of the 80515 core, starting at address 0x80.

Commands for EEPROM Control:

EE	EEPROM CONTROL	
Description:	Allows user to enable read and write to EEPROM.	
Usage:	EE [option] [arguments]	
Command combinations:	EECn	EEPROM Access (1 → Enable, 0 → Disable)
	EERa.b	Read EEPROM at address 'a' for 'b' bytes.
	EESabc..xyz	Write characters to buffer (sets Write length)
	EETa	Transmit buffer to EEPROM at address 'a'.
	EEWa.b...z	Write values to buffer
Example:	EEShello EET$0210	Writes 'hello' to buffer, then transmits buffer to EEPROM starting at address 0x210.

Due to buffer size restrictions, the maximum number of bytes handled by the EEPROM command is 0x40.

Auxiliary Commands:

Typing a comma (",") repeats the command issued from the previous command line. This is very helpful when examining the value at a certain address over time, such as the CE DRAM address for the temperature (0x40).

The slash ("/") is useful to separate comments from commands when sending macro text files via the serial interface. All characters in a line after the slash are ignored.

Commands controlling the CE, TMUX and the RTM:

C	COMPUTE ENGINE CONTROL	
Description:	Allows the user to enable and configure the compute engine.	
Usage:	C [option] [argument]	
Command combinations:	CEn	Compute Engine Enable (1 → Enable, 0 → Disable)
	CTn	Select input n for TMUX output pin. n is interpreted as a decimal number.
	CREn	RTM output control (1 → Enable, 0 → Disable)
	CRSa.b.c.d	Selects CE addresses for RTM output
Example:	CE0	Disables CE, followed by "CE OFF" display on LCD. The Demo Code will reset if the WD timer is enabled.
	CT3	Selects the VBIAS signal for the TMUX output pin

Commands controlling the Auto-Calibration Function:

CL	AUTO-CALIBRATION CONTROL	
Description:	Allows the user to initiate auto-calibration and to store calibration values.	
Usage:	CL [option]	
Command combinations:	CLB	Begin auto-calibration. Prior to auto-calibration, the calibration coefficients are automatically restored from flash memory. If the coefficients are not unity gain (0x4000), auto-calibration will yield poor results.
	CLS	Save calibration coefficients to EEPROM starting at address 0x0004
	CLR	Restore calibration coefficients from EEPROM
	CLD	Restore coefficients from flash memory
Example:	CLB	Starts auto-calibration

Before starting the auto-calibration process, target values for voltage and current must be entered in I/O RAM prior to calibration (V at 0x2029, I at 0x202A, duration in accumulation intervals at 0x2028), and the target voltage and current must be applied constantly during calibration. No phase adjustment will be performed. Coefficients can be saved to EEPROM using the CLS command.

Commands controlling the Pulse Counter Function (Demo Code Revision 3.05 only)

CP	PULSE-COUNT CONTROL	
Description:	Allows the user to control the pulse count functions.	
Usage:	CP [option]	
Command combinations:	CPA	Start pulse counting for time period defined with the CPD command. Pulse counts will display with commands M15.2, M16.2
	CPC	Clear the absolute pulse count displays (shown with commands M15.1, M16.1)
	CPDn	Set time window for pulse counters to n seconds, n is interpreted as a decimal number.
Example:	CPD60	Set time window to 60 seconds.

Pulse counts accumulated over a time window defined by the CPD command will be displayed by M15.2 or M16.2 **after** the defined time has expired.

Commands M15.1 and M16.1 will display the **absolute** pulse count for the W and VAR outputs. These displays are reset to zero with the CPC command (or the XRAM write)1=2). Commands M15.2 and M16.2 will display the number of pulses counted during the interval defined by the CPD command. These displays are reset only after a new reading, as initiated by the CPA command.

Commands for Identification and Information:

I	INFORMATION MESSAGES	
Description:	Allows user to read and write information messages.	
Usage:	I [option] [argument]	
Command combinations:	I0	Displays complete version information
	I1	Displays Demo Code version string
	I1=abcdef	Change Demo Code version string
	I2	Displays Copyright string
	I3	CE Version string
	I3=abcdef	Change CE Code version string
Example:	I1	Returns Demo Code version

The I commands are mainly used to identify the revisions of Demo Code and the contained CE code.

P	PROFILE OF METER	
Description:	Returns current meter configuration profile	
Usage:	P	

The profile of the meter is a summary of the important settings of the I/O RAM registers.

Commands for Controlling the Metering Values Shown on the LCD Display:

M	**METER DISPLAY CONTROL (LCD)**	
Description:	Allows user to select internal variables to be displayed.	
Usage:	M [option]. [option]	
Command combinations:	M	Displays "HELLO" message
	M0	Disables display updates
	M1	Temperature (C° delta from nominal)
	M2	Frequency (Hz)
	M3. [phase]	Wh Total Consumption (display wraps around at 999.999)
	M4. [phase]	Wh Total Inverse Consumption (display wraps around at 999.999)
	M5. [phase]	VARh Total Consumption (display wraps around at 999.999)
	M6. [phase]	VARh Total Inverse Consumption (display wraps around at 999.999)
	M7. [phase]	VAh Total (display wraps around at 999.999)
	M8	Operating Time (in hours)
	M9	Real Time Clock
	M10	Calendar Date
	M11. [phase]	V/I Angle at Phase (degrees)
	M13.1	Main edge count (accumulated) – zero transitions of the input signal
	M13.2	CE main edge count for the last accumulation interval
	M14.1	Absolute count for W pulses. Reset with CPC command. **Demo Code revision 3.05 only.**
	M14.2	Count for W pulses in time window defined by the CPD command. **Demo Code revision 3.05 only.**
	M15.1	Absolute count for VAR pulses. Reset with CPC command. **Demo Code revision 3.05 only.**
	M15.2	Count for W pulses in time window defined by the CPD command. **Demo Code revision 3.05 only.**
Example:	M3.3	Displays Wh total consumption of phase C.
	M5.0	Displays VARh total consumption for all phases.

Displays for total consumption wrap around at 999.999Wh (or VARh, VAh) due to the limited number of available display digits. Internal registers (counters) of the Demo Code are 64 bits wide and do not wrap around.

When entering the phase parameter, use 1 for phase A, 2 for phase B, 3 for phase C, and 0 for all phases.

Commands for Controlling the RMS Values Shown on the LCD Display:

MR	METER RMS DISPLAY CONTROL (LCD)	
Description:	Allows user to select meter RMS display for voltage or current.	
Usage:	MR [option]. [option]	
Command combinations:	MR1. [phase]	Displays instantaneous RMS current
	MR2. [phase]	Displays instantaneous RMS voltage
Example:	MR1.3	Displays phase C RMS current.

On the D6513T3C1 Demo Boards, phase 4 is the measured neutral current.

No error message is issued when an invalid parameter is entered, e.g. MR1.8.

Commands for Controlling the MPU Power Save Mode:

PS	POWER SAVE MODE	
Description:	Enters power save mode	Disables CE, ADC, CKOUT, ECK, RTM, SSI, TMUX VREF, and serial port, sets MPU clock to 38.4KHz.
Usage:	PS	

Return to normal mode is achieved by resetting the MPU (Z command).

Commands for Controlling the RTC:

RT	REAL TIME CLOCK CONTROL	
Description:	Allows the user to read and set the real time clock.	
Usage:	RT [option] [value] … [value]	
Command combinations:	RTDy.m.d.w: Day of week	(year, month, day, weekday [1 = Sunday])
	RTR	Read Real Time Clock.
	RTTh.m.s	Time of day: (hr, min, sec).
	RTAs.t	Real Time Adjust: (start, trim). Allows trimming of the RTC. If s > 0, the speed of the clock will be adjusted by 't' parts per billion (PPB). If the CE is on, the value entered with 't' will be changing with temperature, based on Y_CAL, Y_CALC and Y_CALC2.
Example:	RTD05.03.17.5	Programs the RTC to Thursday, 3/17/2005
	RTA1.+1234	Speeds up the RTC by 1234 PPB.

The "Military Time Format" is used for the RTC, i.e. 15:00 is 3:00 PM.

Commands for Accessing the Trim Control Registers:

T	TRIM CONTROL	
Description:	Allows user to read trim and fuse values.	
Usage:	T [option]	
Command combinations:	T4	Read fuse 4 (TRIMM).
	T5	Read fuse 5 (TRIMBGA)
	T6	Read fuse 6 (TRIMBGB).
Example:	T4	Reads the TRIMM fuse.

These commands are only accessible for the 71M6513H (0.1%) parts. When used on a 71M6513 (0.5%) part, the results will be displayed as zero.

Reset Commands:

W, Z	RESET	
Description:	Soft Reset and watchdog control	
Usage:	W, Z	
Commands:	W	Halts the Demo Code program, thus suppressing the triggering of the hardware watchdog timer. This will cause a reset, if the watchdog timer is enabled. **Demo Code revision 3.05 only.**
	Z	Soft reset. This command acts like a hardware reset. The energy accumulators in XRAM will retain their values.

1.8.2 USING THE DEMO BOARD FOR ENERGY MEASUREMENTS

The 71M6513/6513H Demo Board was designed for use with current transformers (CT).

The Demo Board may immediately be used with current transformers having 2,000:1 winding ratio and is programmed for a Kh factor of 3.2 and (see Section 1.8.4 for adjusting the Demo Board for transformers with different turns ratio).

Once, voltage is applied and load current is flowing, the red LED D5 will flash each time an energy sum of 3.2 Wh is collected. The LCD display will show the accumulated energy in Wh when set to display mode 3 (command >**M3** via the serial interface).

Similarly, the red LED D6 will flash each time an energy sum of 3.2 VARh is collected. The LCD display will show the accumulated energy in VARh when set to display mode 5 (command >**M5** via the serial interface).

1.8.3 ADJUSTING THE KH FACTOR FOR THE DEMO BOARD

The 71M6513/6513H Demo Board is shipped with a pre-programmed scaling factor Kh of 3.2, i.e. 3.2Wh per pulse. In order to be used with a calibrated load or a meter calibration system, the board should be connected to the AC power source using the spade terminals on the bottom of the board. The current transformers should be connected to the dual-pin headers on the bottom of the board.

The Kh value can be derived by reading the values for IMAX and VMAX (i.e. the RMS current and voltage values that correspond to the 250mV maximum input signal to the IC), and inserting them in the following equation for Kh:

Kh = *IMAX* * *VMAX* * 66.1782 / (In_8 * *WRATE* * N_{ACC} * X) = 3.19902 Wh/pulse.

The small deviation between the adjusted Kh of 3.19902 and the ideal Kh of 3.2 is covered by calibration. The default values used for the 71M6513/6513H Demo Board are:

WRATE:	683	
IMAX:	208	
VMAX:	600	
In_8:	1	(controlled by *IA_SHUNT* = -15)
N_{ACC}:	2520	
X:	1.5	

Explanation of factors used in the Kh calculation:

WRATE: The factor input by the user to determine Kh

IMAX: The current input scaling factor, i.e. the input current generating 177mVrms at the IA/IB/IC input pins of the 71M6513. 177mV rms is equivalent to 250mV peak.

VMAX: The voltage input scaling factor, i.e. the voltage generating 177mVrms at the VA/VB/VC input pins of the 71M6513

In_8: The setting for the additional ADC gain (8 or 1) determined by the CE register *IA_SHUNT*

N_{ACC}: The number of samples per accumulation interval, i.e. *PRE_SAMPS* *SUM_CYCLES*

X: The pulse rate control factor determined by the CE registers *PULSE_SLOW* and *PULSE_FAST*

Almost any desired Kh factor can be selected for the Demo Board by resolving the formula for WRATE:

***WRATE* = (IMAX * VMAX * 66.1782) / (Kh * In_8 * N_{ACC} * X)**

For the Kh of 3.2Wh, the value 683 (decimal) should be entered for WRATE at location 2D (using the CLI command >**]2D=+683**).

1.8.4 ADJUSTING THE DEMO BOARDS TO DIFFERENT CURRENT TRANSFORMERS

The Demo Board is prepared for use with 2000:1 current transformers (CTs). This means that for the unmodified Demo Board, 208A on the primary side at 2000:1 ratio result in 104mA on the secondary side, causing 177mV at the 1.7Ω resistor pairs R24/R25, R36/R37, R56/R57 (2 x 3.4Ω in parallel).

In general, when *IMAX* is applied to the primary side of the CT, the voltage V_{in} at the IA, IB, or IC input of the 71M6513 IC is determined by the following formula:

$V_{in} = R * I = R * IMAX/N$
where N = transformer winding ratio, R = resistor on the secondary side

If, for example, *IMAX* = 208A are applied to a CT with a 2500:1 ratio, only 83.2mA will be generated on the secondary side, causing only 141mV. The steps required to adapt a 71M6513 Demo Board to a transformer with a winding ratio of 2500:1 are outlined below:

1) The formula R_x = 177mV/(IMAX/N) is applied to calculate the new resistor R_x. We calculate Rx to 2.115Ω

2) **Changing the resistors R24/R25, R106/R107 to a combined resistance of 2.115Ω** (for each pair) will cause the desired voltage drop of 177mV appearing at the IA, IB, or IC inputs of the 71M6513 IC.

3) *WRATE* should be adjusted to achieve the desired Kh factor, as described in 1.8.3.

Simply scaling *IMAX* is not recommended, since peak voltages at the 71M6513 inputs should always be in the range of 0 through ±250mV (equivalent to 177mV rms). If a CT with a much lower winding ratio than 1:2,000 is used, higher secondary currents will result, causing excessive voltages at the 71M6513 inputs. Conversely, CTs with much higher ratio will tend to decrease the useable signal voltage range at the 71M6513 inputs and may thus decrease resolution.

1.8.5 ADJUSTING THE DEMO BOARDS TO DIFFERENT VOLTAGE DIVIDERS

The 71M6513 Demo Board comes equipped with its own network of resistor dividers for voltage measurement mounted on the PCB. The resistor values (for the D6513T3B2 Demo Board) are 2.5477MΩ (R15-R21, R26-R31 combined) and 750Ω (R32), resulting in a ratio of 1:3,393.933. This means that *VMAX* equals 176.78mV*3,393.933 = 600V. A large value for *VMAX* has been selected in order to have headroom for overvoltages. This choice need not be of concern, since the ADC in the 71M6513 has enough resolution, even when operating at 120Vrms or 240Vrms.

If a **different set of voltage dividers** or an external voltage transformer (potential transformer) is to be used, scaling techniques similar to those applied for the current transformer should be used.

In the following example we assume that the line voltage is not applied to the resistor divider for VA formed by R15-R21, R26-R31, and R32, but to a voltage transformer with a ratio N of 20:1, followed by a simple resistor divider. We also assume that we want to maintain the value for *VMAX* at 600V to provide headroom for large voltage excursions.

When applying VMAX at the primary side of the transformer, the secondary voltage V_s is:

$V_s = VMAX / N$

V_s is scaled by the resistor divider ratio R_R. When the input voltage to the voltage channel of the 71M6513 is the desired 177mV, V_s is then given by:

$V_s = R_R * 177mV$

Resolving for R_R, we get:

$R_R = (VMAX / N) / 177mV = (600V / 30) / 177mV = 170.45$

This divider ratio can be implemented, for example, with a combination of one 16.95kΩ and one 100Ω resistor.

If potential transformers (PTs) are used instead of resistor dividers, phase shifts will be introduced that will require negative phase angle compensation. TERIDIAN can supply Demo Code that accepts negative calibration factors for phase.

1.9 CALIBRATION PARAMETERS

1.9.1 GENERAL CALIBRATION PROCEDURE

Any calibration method can be used with the 71M6513/6513H chips. This Demo Board User's Manual presents calibration methods with three or five measurements as recommended methods, because they work with most manual calibration systems based on counting "pulses" (emitted by LEDs on the meter).

Naturally, a meter in mass production will be equipped with special calibration code offering capabilities beyond those of the Demo Code. It is basically possible to calibrate using voltage and current readings, with or without pulses involved. For this purpose, the MPU Demo Code can be modified to display averaged voltage and current values (as opposed to momentary values). Also, automated calibration equipment can communicate with the Demo Boards via the serial interface and extract voltage and current readings. This is possible even with the unmodified Demo Code.

A complete calibration procedure is given in section 0 of this manual.

Regardless of the calibration procedure used, parameters (calibration constants) will result that will have to be applied to the 71M6513/6513H chip in order to make the chip apply the modified gains and phase shifts necessary for accurate operation. Table 1-4 shows the names of the calibration constants, their function, and their location in the CE RAM.

Again, the command line interface can be used to store the calibration constants in their respective CE RAM addresses. For example, the command

```
>]8=+16302
```

stores the decimal value 16302 in the CE RAM location controlling the gain of the current channel (*CAL_IA*) for phase A.

The command

```
>]9=4005
```

stores the hexadecimal value 0x4005 (decimal 16389) in the CE RAM location controlling the gain of the voltage channel for phase A (*CAL_VA*).

Constant	CE Address (hex)	Description
CAL_VA *CAL_VB* *CAL_VC*	0x09 0x0B 0x0D	Adjusts the gain of the voltage channels. +16384 is the typical value. The gain is directly proportional to the CAL parameter. Allowed range is 0 to 32767. If the gain is 1% slow, CAL should be increased by 1%.
CAL_IA *CAL_IB* *CAL_IC*	0x08 0x0A 0x0C	Adjusts the gain of the current channels. +16384 is the typical value. The gain is directly proportional to the CAL parameter. Allowed range is 0 to 32767. If the gain is 1% slow, CAL should be increased by 1%.
PHADJ_A *PHADJ_B* *PHADJ_C*	0x0E 0x0F 0x10	This constant controls the CT phase compensation. No compensation occurs when PHADJ=0. As PHADJ is increased, more compensation is introduced.
TEMP_NOM	0x11	*TEMP_RAW* reading

Table 1-4: CE RAM Locations for Calibration Constants

1.9.2 CALIBRATION MACRO FILE

The macro file in Figure 1-7 contains a sequence of the serial interface commands. It is a simple text file and can be created with Notepad or an equivalent ASCII editor program. The file is executed with HyperTerminal's *Transfer->Send Text File* command.

```
]8=+16022/  CAL_IA (gain=CAL_IA/16384)
]9=+16381/  CAL_VA (gain=CAL_VA/16384)
]a=+16019/  CAL_IB (gain=CAL_IB/16384)
]b=+16370/  CAL_VB (gain=CAL_VB/16384)
]c=+15994/  CAL_IC (gain=CAL_IC/16384)
]d=+16376/  CAL_VC (gain=CAL_VC/16384)
]e=+115/    PHADJ_A (default 0)
]f=+113/    PHADJ_B (default 0)
]10=+109/   PHADJ_C (default 0)
ce1
```

Figure 1-7: Typical Calibration Macro file

It is possible to send the calibration macro file to the 71M6513/71M6513H for "temporary" calibration. This will temporarily change the CE data values. Upon power up, these values are refreshed back to the default values stored in flash memory. Thus, until the flash memory is updated, the macro file must be loaded each time the part is powered up. The macro file is run by first issuing the ce0 command to turn off the compute engine and then sending the file with the *transfer → send text file* procedure.

Use the *Transfer → Send Text File* command!

1.9.3 UPDATING THE 6513_DEMO.HEX FILE

The io_merge program updates the 6513_demo.hex file with the values contained in the macro file. This program is executed from a DOS command line window. Executing the io_merge program with no arguments will display the syntax description. To merge macro.txt and old_6513_demo.hex into new_6513_demo.hex, use the command:

```
io_merge old_6513_demo.hex macro.txt new_6513_demo.hex
```

The new hex file can be written to the 71M6513/71M6513H through the ICE port using the ADM51 in-circuit emulator. This step makes the calibration to the meter permanent.

1.9.4 UPDATING CALIBRATION DATA IN FLASH MEMORY WITHOUT USING THE ICE OR A PROGRAMMER

It is possible to make data permanent that had been entered temporarily into the CE RAM. The transfer to flash memory is done using the following serial interface command:

```
>]U
```

Thus, after transferring calibration data with manual serial interface commands or with a macro file, all that has to be done is invoking the U command.

Similarly, calibration data can also stored in EEPROM using the CLS command.

After reset, calibration data is copied from the EEPROM, if present. Otherwise, calibration data is copied from the flash memory. Writing 0xFF into the first few bytes of the EEPROM deactivates any calibration data previously stored to the EEPROM.

1.9.5 AUTOMATIC GAINS CALIBRATION

Starting with Demo Code revision 3.04, it is possible to perform a simple automatic calibration. This calibration is performed for resistive loads only and will not correct phase angle. The steps required for the calibration are:

1. Enter operating values for voltage and current in I/O RAM. The voltage is entered at address 0x2029 (e.g. with the command **)29=+2400** for 240V), the current is entered at 0x202A (e.g. with the command **)2A=+300** for 30A) and the duration measured in accumulation intervals is entered at 0x2028.
2. The operating voltage and current defined in step 1 must be applied to the meter (Demo Board).
3. The CLB (Begin Calibration) command must be entered via the serial interface. The operating voltage and current must be maintained accurately while the calibration is being performed.
4. The calibration procedure will automatically reset CE addresses 08, 09, 0x0A, 0x0B, 0x0C, and 0x0D to nominal values (0x4000), and 0x0E, 0x0F and 0x10 to zero prior to starting the calibration. Automatic calibration also reads the chip temperature and enters it in CE location 0x11 for proper temperature compensation.
5. The LCD showing the "HELLO" message will signal completion of the automatic calibration. Enter M3 or another serial interface command to bring the display back to normal.
6. CE addresses 08, 09, 0x0A, 0x0B, 0x0C, and 0x0D will now show values other than 0x4000. These values can be stored in EEPROM by issuing the CLS command.

Tip: Current transformers of a given type usually have very similar phase angle for identical operating conditions. If the phase angle is accurately determined for one current transformer, the corresponding phase adjustment coefficient PHADJ_X can be entered for all calibrated units.

1.9.6 LOADING THE 6513_DEMO.HEX FILE INTO THE DEMO BOARD

Hardware Interface for Programming: The 71M6513/6513H IC provides an interface for loading code into the internal flash memory. This interface consists of the following signals:

E_RXTX (data)

E_TCLK (clock)

E_RST (reset)

These signals, along with V3P3 and GND are available on the emulator header J14. Production meters may be equipped with much simpler programming connectors, e.g. a 5x1 header.

Programming of the flash memory requires a specific in-circuit emulator, the ADM51 by Signum Systems (http//www.signumsystems.com) or the Flash Programmer (TFP-1) provided by TERIDIAN Semiconductor. A gang programmer is available for high-volume production.

In-Circuit Emulator: If firmware exists in the 71M6513/6513H flash memory, this memory has to be erased before loading a new file into memory. Figure 1-8 and Figure 1-9 show the emulator software active. In order to erase the flash memory, the RESET button of the emulator software has to be clicked followed by the ERASE button (Figure 1-8).

Once the flash memory is erased, the new file can be loaded using the commands File followed by Load. The dialog box shown in Figure 1-9 will then appear making it possible to select the file to be loaded by clicking the Browse button. Once the file is selected, pressing the OK button will load the file into the flash memory of the 71M6513/6513H IC.

At this point, the emulator probe (cable) can be removed. Once the 71M6513/6513H IC is reset using the reset button on the Demo Board, the new code starts executing.

Flash Programmer Module (TFP-1): Follow the instructions given in the User Manual for the TFP-1.

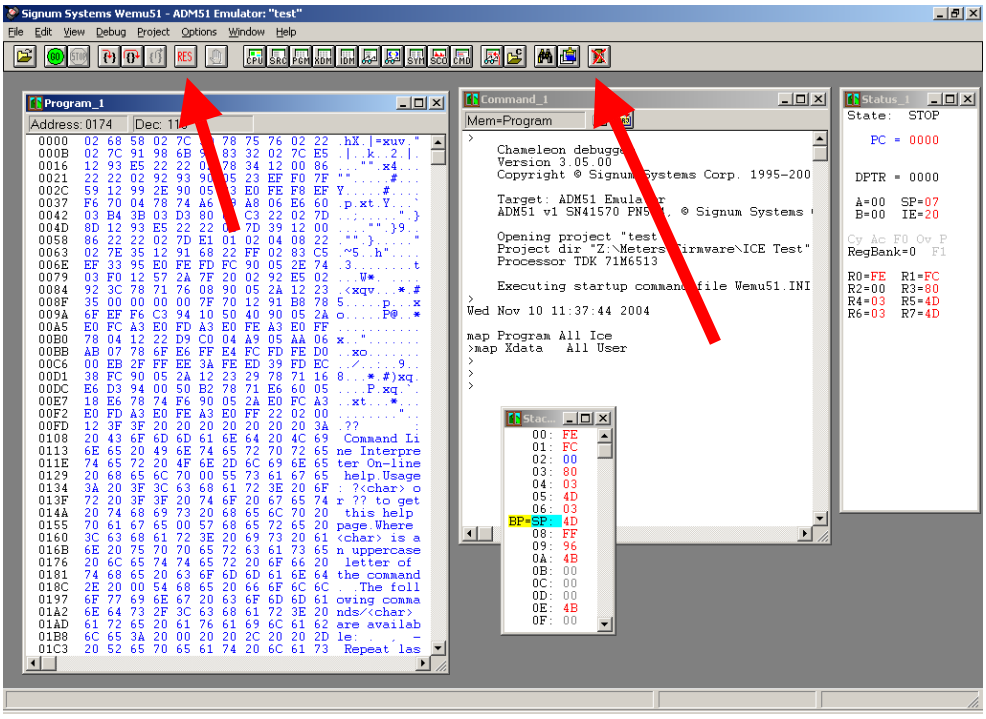


Figure 1-8: Emulator Window Showing Reset and Erase Buttons (see Arrows)

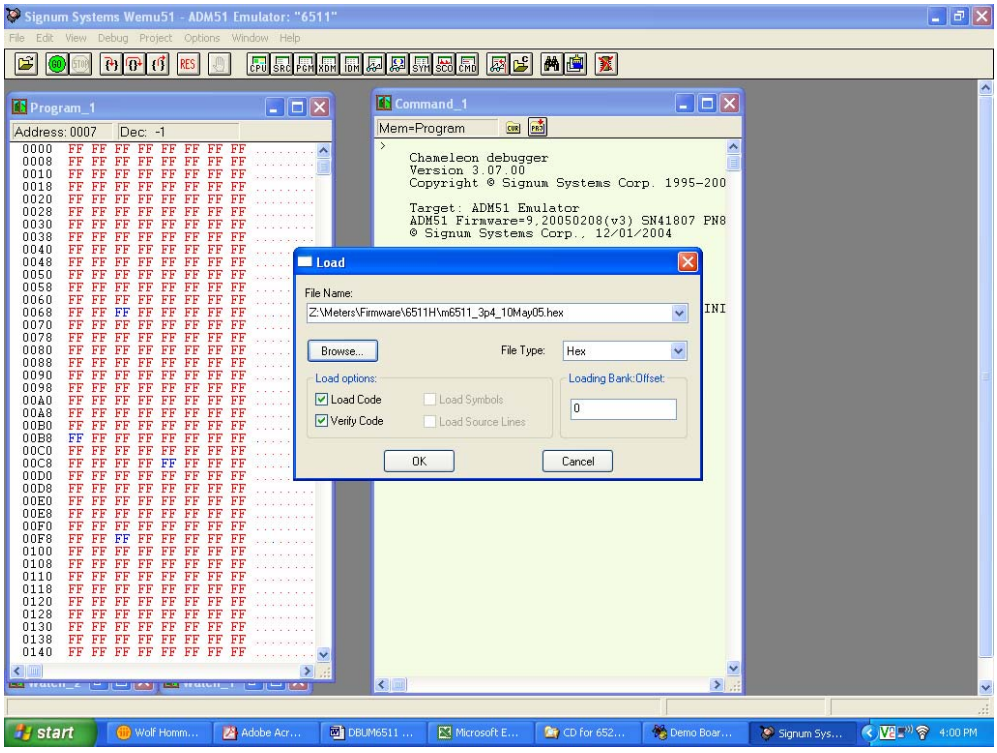


Figure 1-9: Emulator Window Showing Erased Flash Memory and File Load Menu

1.9.7 THE PROGRAMMING INTERFACE OF THE 71M6513/6513H

Flash Downloader/ICE Interface Signals

The signals listed in Table 1-5 are necessary for communication between the Flash Downloader or ICE and the 71M6513/6513H.

Signal	Direction	Function
E_TCLK	Output from 71M6513/6513H	Data clock
E_RXTX	Bi-directional	Data input/output
E_RST	Bi-directional	Flash Downloader Reset (active low)

Table 1-5: Flash Programming Interface Signals

The other signals accessible at the emulator interface connector J14 (E_TBUS[0]-E_TBUS[3], E_ISYNC/BRKRQ) are used for the trace debugger, if available.

The E_RST signal should only be driven by the Flash Downloader when enabling these interface signals. The Flash Downloader must release E_RST at all other times.

1.10 DEMO CODE

1.10.1 DEMO CODE DESCRIPTION

The Demo Board is shipped preloaded with Demo Code revision 3.0.4 or later in the 71M6513 or 71M6513H chip. The code revision can easily be verified by entering the command >**i1** via the serial interface (see section 1.8.1). Check with your local TERIDIAN representative or FAE for the latest revision.

Some Demo Boards are shipped with Demo Code 3.03. These boards can be updated to revision 3.04 or later using either an in-circuit emulator (ICE) or the Flash Programmer (TFP-1), as described in section 1.9.6.

The Demo Code is useful due to the following features:

- It provides basic metering functions such as pulse generation, display of accumulated energy, frequency, date/time, and enables the user to evaluate the parameters of the metering IC such as accuracy, harmonic performance, etc.
- It maintains and provides access to basic household functions such as real-time clock (RTC).
- It provides access to control and display functions via the serial interface, enabling the user to view and modify a variety of meter parameters such as Kh, calibration coefficients, temperature compensation etc.
- It provides libraries for access of low-level IC functions to serve as building blocks for code development.

A detailed description of the Demo Code can be found in the Software User's Guide (SUG). In addition, the comments contained in the library provided with the Demo Kit can serve as useful documentation.

The Software User's Guide contains the following information:

- Design guide
- Design reference for routines
- Tool Installation Guide
- List of library functions
- 80515 MPU Reference (hardware, instruction set, memory, registers)
- Description of serial interface commands

1.10.2 DEMO CODE MPU PARAMETERS

In the Demo Code, certain MPU **XRAM** parameters have been given fixed addresses in order to permit easy external access. These variables can be read via the serial interface, as described in section 1.7.1, with the **)n$** command and written with the **)n=xx** command where n is the word address. Note that accumulation variables are 64 bits long and are accessed with **)n$$** (read) and **)n=hh=ll** (write) in the case of accumulation variables. Default values are the values assigned by the Demo Code on start-up.

MPU INPUT PARAMETERS

All MPU Input Parameters are loaded by the MPU at startup and should not need adjustment during meter calibration.

MPU Input Parameters for Metering

XRAM Word Address	Default Value	Name	Description
0x00	5917	*WCREEP_THR*	For each element, if *WSUM_X* or *VARSUM_X* of that element exceeds *WCREEP_THR*, the sample values for that element are not zeroed. Otherwise, the accumulators for Wh, VARh, and VAh are not updated and the instantaneous value of IRMS for that element is zeroed. LSB = $9.4045*10^{-13}$ VMAX IMAX Wh Demo Code revision 3.04: The default value is 1536. **Demo Code revision 3.05:** The default value 5917 is equivalent to 2.5Wh/h.
0x01	0	*CONFIG*	Bit 0: Sets VA calculation mode. 0: $V_{RMS}*A_{RMS}$ 1: $\sqrt{W^2 + VAR^2}$ Bit 1: Clears accumulators for Wh, VARh, VAh. This bit need not be reset.
0x02	136105056	*PK_VTHR*	Demo Code revision 3.04: Not implemented (default = 0) **Demo Code revision 3.05:** When the voltage exceeds this value, bit 5 in the MPU status word is set, and the MPU might choose to log a warning. Event logs are not implemented in Demo Code. LSB = $9.4045*10^{-13}$*VMAX^2 V^2h_{RMS} The default value of 136105056 is equivalent to $407.3V_{RMS}$ if VMAX = 600V and a 1-second accumulation interval is used.
0x03	17695797	*PK_ITHR*	Demo Code revision 3.04: Not implemented (default = 0) **Demo Code revision 3.05:** When the current exceeds this value, bit 6 in the MPU status word is set, and the MPU might choose to log a warning. Event logs are not implemented in Demo Code. LSB = $9.4045*10^{-13}$*IMAX^2 V^2h_{RMS} The default value of 17695797 is equivalent to $50.9A_{RMS}$ if IMAX = 208A and a 1-second accumulation interval is used.

0x09	6000	*VMAX*	The nominal external RMS voltage that corresponds to 250mV peak at the ADC input. The meter uses this value to convert internal quantities to external. LSB=0.1V
0x0A	2080	*IMAX*	The nominal external RMS current that corresponds to 250mv peak at the ADC input. The meter uses this value to convert internal quantities to external. LSB=0.1A
0x0F	10	*ALT_MUX_RATE*	Sample rate control for neutral current detection (D6513T3C1 Demo Boards only). The frequency of alternative multiplexer cycles (measuring V3 and temperature) is given by: $f = \frac{2520.6}{ALT\_MUX\_RATE}$ The default setting results in a frequency of 252Hz. See section 1.10.4 for details. **This address is only used by the "Neutral Current" Demo Code. For other Demo Code revisions, XRAM word address 0x0F is a reserved location.**
0x13	44	*ICREEP_THR*	For each element, if *ISQSUM_X* of that element exceeds *ICREEP_THR*, the sample values for that element are not zeroed. Otherwise, the accumulators for Wh, VARh, and VAh are not updated and the instantaneous value of IRMS for that element is zeroed. LSB = $9.4045*10^{-13}$ $IMAX^2$ Wh **Demo Code revision 3.05:** The default value 44 is equivalent to $0.00644A^2$.

Table 1-6: MPU Input Parameters for Metering

MPU Input Parameters for Temperature Compensation

XDATA Word Address	Default Value	Name	Description
0x04	0	*Y_CAL*	Implement RTC trim. $CORRECTION(ppm) = \frac{Y\_CAL}{10} + T \cdot \frac{Y\_CALC}{100} + T^2 \cdot \frac{Y\_CALC2}{1000}$
0x05	0	*Y_CALC*	
0x06	0	*Y_CALC2*	
0x0B	0	*PPMC*	PPM/C*26.84. Linear temperature compensation. A positive value will cause the meter to run faster when hot. This is applied to both V and I and will therefore have a double effect on products. Default is 0.
0x0C	0	*PPMC2*	PPM/C^2*1374. Square law compensation. A positive value will cause the meter to run faster when hot. This is applied to both V and I and will therefore have a double effect on products. Default is 0.
0x0D	22721	*DEGSCALE*	Scale factor for TEMP_X. TEMP_X=DEGSCALE*2^{-22}*(TEMP_RAW_X-TEMP_NOM).

Y_CAL, Y_CALC, Y_CALC2 are 16-bit signed integers, i.e. the range is –32,767 to +32,768

Table 1-7: MPU Input Parameters for Temperature Compensation

MPU Input Parameters for Pulse Generation

XDATA Word Address	Default Value	Name	Description
0x07	0	*PULSEW_SRC*	This address contains a number that points to the selected pulse source. Selectable pulse sources are listed in Table 1-9.
0x08	4	*PULSER_SRC*	This address contains a number that points to the selected pulse source. Selectable pulse sources are listed in Table 1-9.

Table 1-8: MPU Parameters for Pulse Source Selection

Any of the values listed in Table 1-9 can be selected for as a source for PULSEW and PULSER. The designation "source_I" refers to values imported by the consumer, "source_E" refers to energy exported by the consumer (energy generation).

Number	Pulse Source	Description
0	***WSUM***	***Default for PULSEW_SRC***
1	*W0SUM*	
2	*W1SUM*	
3	*W2SUM*	
4	***VARSUM***	***Default for PULSER_SRC***
5	*VAR0SUM*	
6	*VAR1SUM*	
7	*VAR2SUM*	
8	*I0SQSUM*	
9	*I1SQSUM*	
10	*I2SQSUM*	
11	*INSQSUM*	
12	*V0SQSUM*	
13	*V1SQSUM*	
14	*V2SQSUM*	
15	*VASUM*	
16	*VA0SUM*	
17	*VA1SUM*	

Number	Pulse Source	Description
18	*VA2SUM*	
19	*WSUM_I*	Sum of imported real energy
20	*W0SUM_I*	Imported real energy on element A
21	*W1SUM_I*	Imported real energy on element B
22	*W2SUM_I*	Imported real energy on element C
23	*VARSUM_I*	Sum of imported reactive energy
24	*VAR0SUM_I*	Imported reactive energy on element A
25	*VAR1SUM_I*	Imported reactive energy on element B
26	*VAR1SUM_I*	Imported reactive energy on element C
27	*WSUM_E*	Sum of exported real energy
28	*W0SUM_E*	Exported real energy on element A
29	*W1SUM_E*	Exported real energy on element B
30	*W2SUM_E*	Exported real energy on element C
31	*VARSUM_E*	Sum of exported reactive energy
32	*VAR0SUM_E*	Exported reactive energy on element A
33	*VAR1SUM_E*	Exported reactive energy on element B
34	*VAR2SUM_E*	Exported reactive energy on element C

Table 1-9: Selectable Pulse Sources

MPU INSTANTANEOUS OUTPUT VARIABLES

The Demo Code processes CE outputs after each accumulation interval. It calculates instantaneous values such as VRMS, IRMS, W and VA as well as accumulated values such as Wh, VARh, and VAh. Table 1-10 lists the calculated instantaneous values.

XRAM Word Address	Name	DESCRIPTION
0x14 0x15 0x16	Vrms_A Vrms_B* Vrms_C*	V_{rms} from element 0, 1, 2. $LSB = \frac{4.4575 \cdot 10^{-8} VMAX}{\sqrt{Nacc}}$
0x17 0x18 0x19	Irms_A Irms_B Irms_C*	I_{rms} from element 0, 1, 2. $LSB = \frac{4.4575 \cdot 10^{-8} IMAX\ In8}{\sqrt{Nacc}}$
0x1A 0x1B 0x1C	IPhase_A IPhase_B* IPhase_C*	In-Vn phase from element n. The number of degrees In lags Vn. LSB=0.001°. Range = -180 to +180.
0x1D	Frequency	Frequency of voltage selected by CE input. If the selected voltage is below the sag threshold, Frequency=0. LSB $\equiv \frac{F_S}{2^{32}} \approx 0.587 \cdot 10^{-6}$ Hz
0x1E	Delta_T	Deviation from Calibration temperature. LSB = 0.1 ^{0}C.
0x1F 0x20	VPhase_AB* VPhase_BC*	Amount phase B lags phase A and amount phase B lags phase C. LSB=1° (0,360). If V_{rms}_A<5% of VMAX, VPhase_AB and VPhase BC are cleared to 0.

Table 1-10: MPU Instantaneous Output Variables

MPU STATUS WORD

The MPU maintains the status of certain meter and I/O related variables in the Status Word. The Status Word is located at address 0x21. The bit assignments are listed in Table 1-11.

Status Word Bit	Name	DESCRIPTION
0	Reserved	
1	SAGA	Reserved for sag flag phase A – not implemented[1]
2	SAGB	Reserved for sag flag phase B – not implemented[1]
3	SAGC	Reserved for sag flag phase C – not implemented[1]
4	F0	Reconstructed line signal flag
5	MAXV	Overvoltage. 1 when overvoltage is detected.
6	MAXI	Overcurrent. 1 when overcurrent is detected.
7	ONE_SEC	Reserved
8	VXEDGE	Reserved
9	Reserved	
10	Reserved	
11	XFER	Reserved
12	CREEP	Creep bit. This bit is 1 when creep is detected. This bit is only set if a creep condition is detected in all phases.
13-31	Reserved	

Note: [1]: Not implemented in Demo Code revision 3.04

Table 1-11: MPU Status Word Bit Assignment

MPU ACCUMULATION OUTPUT VARIABLES

Accumulation values are accumulated from XFER cycle to XFER cycle (see Table 1-12). They are all in 64-bit format. The 6513 has an LSB of $9.4045*10^{-13}$*VMAX*IMAX*In_8 Wh. Accumulated values are calculated by summing the CE XFER outputs into 64 bit variables. Thus, the accumulators will hold at least 136 years of data when XFER rate is 1Hz.

The CLI commands with two Dollar signs e.g. **)39$$** should be used to read the variables. When using the commands with two question marks, e.g. **)39??** , negative decimal values will be displayed when the most significant bit is set.

XRAM Word Address	Name	Description
0x2F	*Wh*	Total Watt hours consumed (imported)
0x31	*Whe*	Total Watt hours generated (exported)
0x33	*VARh*	Total VAR hours consumed
0x35	*VARhe*	Total VAR hours generated (inverse consumed)
0x37	*VAh*	Total VA hours
0x39	*Wh_A*	Total Watt hours consumed through element 0
0x3B	*Whe_A*	Total Watt hours generated (inverse consumed) through element 0
0x3D	*VARh_A*	Total VAR hours consumed through element 0
0x3F	*VARhe_A*	Total VAR hours generated (inverse consumed) through element 0
0x41	*VAh_A*	Total VA hours in element 0
0x43	*Wh_B*	Total Watt hours consumed through element 1
0x45	*Whe_B*	Total Watt hours generated (inverse consumed) through element 1
0x47	*VARh_B*	Total VAR hours consumed through element 1
0x49	*VARhe_B*	Total VAR hours generated (inverse consumed) through element 1
0x4B	*VAh_B*	Total VA hours in element 1
0x4D	*Wh_C*	Total Watt hours consumed through element 2
0x4F	*Whe_C*	Total Watt hours generated (inverse consumed) through element 2
0x51	*VARh_C*	Total VAR hours consumed through element 2
0x53	*VARhe_C*	Total VAR hours generated (inverse consumed) through element 2
0x55	*VAh_C*	Total VA hours in element 2

Table 1-12: MPU Accumulation Output Variables

1.10.3 USEFUL CLI COMMANDS INVOLVING THE MPU AND CE

Table 1-13 shows a few essential commands involving MPU data memory.

Command	Description
>)1=2	Clears the accumulators for Wh, VARh, and VAh by setting bit 1 of the *CONFIG* register.
>)A=+2080	Applies the value 208A to the IMAX register
>)9=+6000	Applies the value 600V to the VMAX register
>)22?	Displays the operating time since the last power up (in 1/100 of hours)
>)2F$$	Displays the total accumulated imported Wh energy (two $$ used for full 64 bit hex display)
>MR2.1	Displays the current RMS voltage in phase A
>MR1.2	Displays the current RMS current in phase B
>RI5=26	Disables the emulator clock by setting bit 5 in I/O RAM address 0x05.
>RI5=6	Re-enables the emulator clock by clearing bit 5 in I/O RAM address 0x05.
>RI1C=1	Increments the RTC clock by one second.
]U	Stores the current CE RAM variables in flash memory. The stored variables will be applied by the MPU at the next reset or power-up if no valid data is available from the EEPROM.
>CLS	Stores the current CE RAM variables in EEPROM memory. The stored variables will be applied by the MPU at the next reset or power-up.

Table 1-13: CLI Commands for MPU Data Memory

1.10.4 DEMO CODE FOR NEUTRAL DETECTION (DEMO BOARD D6513T3C1)

Normally a high neutral current indicates tampering, perhaps from a grounded or bypassed power conductor.

The Neutral Current measurement is performed by acquiring the signal from a fourth current transformer that is connected to the auxiliary analog input, the V3 pin (pin 86). The analog data measured on this pin is referenced to the VBIAS pin (pin 81).

The ICs supplied with the 71M6513/6513H Demo Kits may contain firmware versions with and without neutral current. On the CD-ROM containing the firmware sources and documentation, the files supporting neutral current code end with "NC".

Neutral current is read using alternate multiplexer cycles, as controlled by the *MUX_ALT* bit in I/O RAM. While the TERIDIAN standard Demo Code revision 3.04 performs one alternate multiplexer cycle per second, the neutral current-capable Demo Code can perform alternate multiplexer cycles more frequently. When the alternate multiplexer cycle is triggered once every 10th CE_BUSY interrupt (i.e. every 3.97ms, or 252Hz), no interference with regular power measurement occurs, and the neutral current is still measured with an accuracy of about 1.5%.

The sampling rate for the neutral current can be changed by changing the MPU (XDATA) address *ALT_MUX_RATE*, which is located at CE DRAM address 0x0F. The sample rate (2520.6), divided by the value entered into *ALT_MUX_RATE* controls the number of neutral current samples per second:

$$f = \frac{2520.6}{ALT\_MUX\_RATE}$$

When the value of *ALT_MUX_RATE* decreased, the sample rate for the neutral current increases. The Minimum value for *ALT_MUX_RATE* is 10, i.e. 252Hz is the maximum recommended sample rate for neutral current.

On Demo Code without neutral current, MPU XDATA address 0x0F accesses a reserved (and unused) memory location.

The neutral current is available for display. The help text for the MR command describes how to display neutral current on the display. For the "M" command of the CLI for current, phase 4 signifies the neutral current.

The accuracy data collected for several *ALT_MUX_RATE* settings is given in Table 1-14:

Test Number	Applied Current	ALT_MUX_RATE = 10 (252Hz)		ALT_MUX_RATE = 25 (100Hz)		ALT_MUX_RATE = 50 (51Hz)	
		measured current	error [%]	measured current	error [%]	measured current	error [%]
1	200	200.66	0.33	201.15	0.575	202.335	1.168
2	150	150.63	0.42	150.778	0.519	150.824	0.549
3	100	99.82	-0.18	99.765	-0.235	100.221	0.221
4	50	49.859	-0.282	49.76	-0.48	49.333	-1.334
5	25	24.889	-0.444	24.861	-0.556	24.951	-0.196
6	10	10.042	0.42	10.134	1.34	10.193	1.93
7	5	4.988	-0.24	5.132	2.64	5.155	3.1
8	2.5	2.486	-0.56	2.459	-1.64	2.535	1.4
9	1	1.036	3.6	1.067	6.7	1.071	7.1
10	0.5	0.564	12.8	0.581	16.2	0.592	18.4
11	0.25	0.324	29.6	0.328	31.2	0.334	33.6

Table 1-14: Neutral Current Accuracy at Various Sampling Frequencies

MPU (XDATA) address 0x027 represents the neutral current (RMS value). For the standard Demo Code (revision 3.04), this address is a reserved location.

In the CE interface, the CE address 0x56 represents the 32-bit neutral current value, I3SQSUM. It has different units than the current registers derived from the regular inputs IA, IB, and IC, because it is sampled at a different rate (default = 1/10) than the other current channels, and because the reference is not VREF, but VBIAS.

If one accumulates data for 250 samples (with XDATA address 0x0F=10) the accumulated data is transferred to the MPU as one register on each XFER_BUSY interrupt. The values in between samples are equivalent to the previous acquired sample value.

The actual LSB value for the neutral current measurement is computed from the following formula

$$LSB_{NC} = \frac{IMAX^2}{431 \cdot 10^3 \cdot N_{ACC} \cdot A^2 h}$$

where:

IMAX is the numerical value of the current corresponding to 176mV RMS at the IC input,
NACC is the product of *SUM_CYCLES* and *PRE_SAMPS*,

With IMAX = 208A and N_{ACC} = 2520, LSB_{NC} becomes $39.8*10^{-6}/A^2h$.

2

2 APPLICATION INFORMATION

2.1 CALIBRATION THEORY

A typical meter has phase and gain errors as shown by ϕ_S, A_{XI}, and A_{XV} in Figure 2-1. Following the typical meter convention of current phase being in the lag direction, the small amount of phase lead in a typical current sensor is represented as $-\phi_S$. The errors shown in Figure 2-1 represent the sum of all gain and phase errors. They include errors in voltage attenuators, current sensors, and in ADC gains. In other words, no errors are made in the 'input' or 'meter' boxes.

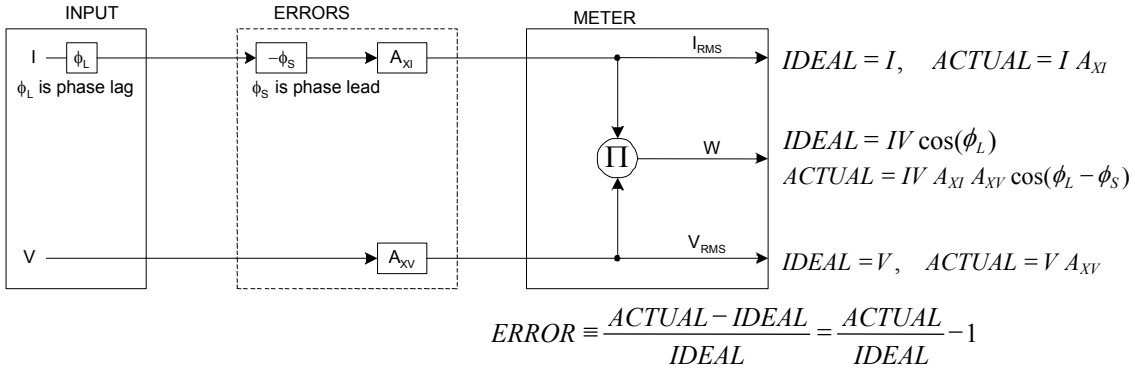


Figure 2-1: Watt Meter with Gain and Phase Errors.

During the calibration phase, we measure errors and then introduce correction factors to nullify their effect. With three unknowns to determine, we must make at least three measurements. If we make more measurements, we can average the results.

2.1.1 CALIBRATION WITH THREE MEASUREMENTS

The simplest calibration method is to make three measurements. Typically, a voltage measurement and two Watt-hour (Wh) measurements are made. A voltage display can be obtained for test purposes via the command >**MR2.1** in the serial interface.

Let's say the voltage measurement has the error E_V and the two Wh measurements have errors E_0 and E_{60}, where E_0 is measured with $\phi_L = 0$ and E_{60} is measured with $\phi_L = 60$. These values should be simple ratios—not percentage values. They should be zero when the meter is accurate and negative when the meter runs slow. The fundamental frequency is f_0. T is equal to $1/f_S$, where f_S is the sample frequency (2560.62Hz). Set all calibration factors to nominal: *CAL_IA* = 16384, *CAL_VA* = 16384, *PHADJA* = 0.

From the voltage measurement, we determine that

1.➔ $$A_{XV} = E_V + 1$$

We use the other two measurements to determine ϕ_S and A_{XI}.

2. $$E_0 = \frac{IV\ A_{XV}\ A_{XI}\cos(0-\phi_S)}{IV\cos(0)} - 1 = A_{XV}\ A_{XI}\cos(\phi_S) - 1$$

2a. $$A_{XV}A_{XI} = \frac{E_0 + 1}{\cos(\phi_S)}$$

3. $$E_{60} = \frac{IV\ A_{XV}\ A_{XI}\cos(60-\phi_S)}{IV\cos(60)} - 1 = A_{XV}\ A_{XI}\frac{\cos(60-\phi_S)}{\cos(60)} - 1$$

3a. $$E_{60} = \frac{A_{XV}A_{XI}\left[\cos(60)\cos(\phi_S) + \sin(60)\sin(\phi_S)\right]}{\cos(60)} - 1$$

$$= A_{XV}A_{XI}\cos(\phi_S) + A_{XV}A_{XI}\tan(60)\sin(\phi_S) - 1$$

Combining 2a and 3a:

4. $$E_{60} = E_0 + (E_0 + 1)\tan(60)\tan(\phi_S)$$

5. $$\tan(\phi_S) = \frac{E_{60} - E_0}{(E_0 + 1)\tan(60)}$$

6.➔ $$\phi_S = \tan^{-1}\left(\frac{E_{60} - E_0}{(E_0 + 1)\tan(60)}\right)$$

and from 2a:

7.➔ $$A_{XI} = \frac{E_0 + 1}{A_{XV}\cos(\phi_S)}$$

Now that we know the A_{XV}, A_{XI}, and ϕ_S errors, we calculate the new calibration voltage gain coefficient from the previous ones:

$$CAL\_V_{NEW} = \frac{CAL\_V}{A_{XV}}$$

We calculate PHADJ from ϕ_S, the desired phase lag:

$$PHADJ = 2^{20}\left[\frac{\tan(\phi_S)\left[1 + (1-2^{-9})^2 - 2(1-2^{-9})\cos(2\pi f_0 T)\right]}{(1-2^{-9})\sin(2\pi f_0 T) - \tan(\phi_S)\left[1 - (1-2^{-9})\cos(2\pi f_0 T)\right]}\right]$$

And we calculate the new calibration current gain coefficient, including compensation for a slight gain increase in the phase calibration circuit.

$$CAL\_I_{NEW} = \frac{CAL\_I}{A_{XI}} \frac{1}{\sqrt{1 + \frac{2^{-20} PHADJ(2 + 2^{-20} PHADJ - 2(1 - 2^{-9})\cos(2\pi f_0 T))}{1 - 2(1 - 2^{-9})\cos(2\pi f_0 T) + (1 - 2^{-9})^2}}}$$

2.1.2 CALIBRATION WITH FIVE MEASUREMENTS

The five measurement method provides more orthogonality between the gain and phase error derivations. This method involves measuring E_V, E_0, E_{180}, E_{60}, and E_{300}. Again, set all calibration factors to nominal, i.e. *CAL_IA* = 16384, *CAL_VA* = 16384, *PHADJA* = 0.

First, calculate A_{XV} from E_V:

1.➔ $A_{XV} = E_V + 1$

Calculate A_{XI} from E_0 and E_{180}:

2. $E_0 = \frac{IV\ A_{XV}\ A_{XI} \cos(0 - \phi_S)}{IV \cos(0)} - 1 = A_{XV}\ A_{XI} \cos(\phi_S) - 1$

3. $E_{180} = \frac{IV\ A_{XV}\ A_{XI} \cos(180 - \phi_S)}{IV \cos(180)} - 1 = A_{XV}\ A_{XI} \cos(\phi_S) - 1$

4. $E_0 + E_{180} = 2A_{XV} A_{XI} \cos(\phi_S) - 2$

5. $A_{XV} A_{XI} = \frac{E_0 + E_{180} + 2}{2\cos(\phi_S)}$

6.➔ $A_{XI} = \frac{(E_0 + E_{180})/2 + 1}{A_{XV} \cos(\phi_S)}$

Use above results along with E_{60} and E_{300} to calculate ϕ_S.

7. $E_{60} = \frac{IV\ A_{XV}\ A_{XI} \cos(60 - \phi_S)}{IV \cos(60)} - 1$

$= A_{XV} A_{XI} \cos(\phi_S) + A_{XV} A_{XI} \tan(60) \sin(\phi_S) - 1$

8. $E_{300} = \frac{IV\ A_{XV}\ A_{XI} \cos(-60 - \phi_S)}{IV \cos(-60)} - 1$

$= A_{XV} A_{XI} \cos(\phi_S) - A_{XV} A_{XI} \tan(60) \sin(\phi_S) - 1$

Subtract 8 from 7

9. $E_{60} - E_{300} = 2A_{XV} A_{XI} \tan(60) \sin(\phi_S)$

use equation 5:

10. $$E_{60} - E_{300} = \frac{E_0 + E_{180} + 2}{\cos(\phi_S)} \tan(60) \sin(\phi_S)$$

11. $$E_{60} - E_{300} = (E_0 + E_{180} + 2) \tan(60) \tan(\phi_S)$$

12.➔ $$\phi_S = \tan^{-1}\left(\frac{(E_{60} - E_{300})}{\tan(60)(E_0 + E_{180} + 2)} \right)$$

Now that we know the A_{XV}, A_{XI}, and ϕ_S errors, we calculate the new calibration voltage gain coefficient from the previous ones:

$$CAL\_V_{NEW} = \frac{CAL\_V}{A_{XV}}$$

We calculate PHADJ from ϕ_S, the desired phase lag:

$$PHADJ = 2^{20}\left[\frac{\tan(\phi_S)\left[1 + (1-2^{-9})^2 - 2(1-2^{-9})\cos(2\pi f_0 T)\right]}{(1-2^{-9})\sin(2\pi f_0 T) - \tan(\phi_S)\left[1 - (1-2^{-9})\cos(2\pi f_0 T)\right]} \right]$$

And we calculate the new calibration current gain coefficient, including compensation for a slight gain increase in the phase calibration circuit.

$$CAL\_I_{NEW} = \frac{CAL\_I}{A_{XI}} \frac{1}{\sqrt{1 + \frac{2^{-20} PHADJ(2 + 2^{-20} PHADJ - 2(1-2^{-9})\cos(2\pi f_0 T))}{1 - 2(1-2^{-9})\cos(2\pi f_0 T) + (1-2^{-9})^2}}}$$

2.2 CALIBRATION PROCEDURES

Calibration requires that a calibration system is used, i.e. equipment that applies accurate voltage, load current and load angle to the unit being calibrated, while measuring the response from the unit being calibrated in a repeatable way. By repeatable we mean that the calibration system is synchronized to the meter being calibrated. Best results are achieved when the first pulse from the meter opens the measurement window of the calibration system. This mode of operation is opposed to a calibrator that opens the measurement window at random time and that therefore may or may not catch certain pulses emitted by the meter.

It is essential for a valid meter calibration to have the voltage stabilized a few seconds before the current is applied. This enables the Demo Code to initialize the 71M6513/6513H and to stabilize the PLLs and filters in the CE. This method of operation is consistent with meter applications in the field as well as with metering standards.

Each meter phase must be calibrated individually. The procedures below show how to calibrate a meter phase with either three or five measurements. The PHADJ equations apply only when a current transformer is used for the phase in question. Note that positive load angles correspond to lagging current (see Figure 2-2).

During calibration of any phase, a stable mains voltage has to be present on phase A. This enables the CE processing mechanism of the 71M6513/6513H necessary to obtain a stable calibration.

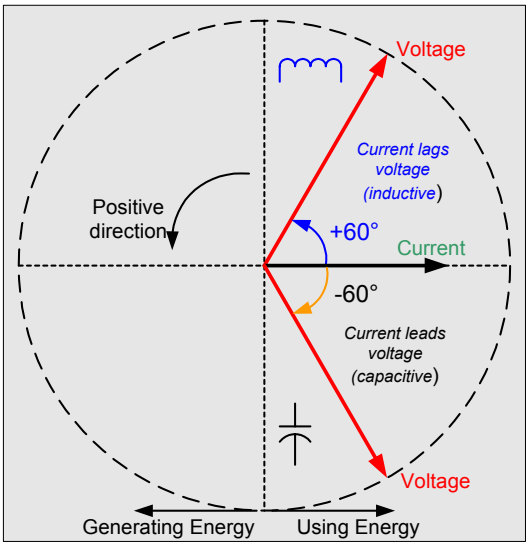


Figure 2-2: Phase Angle Definitions

The calibration procedures described below should be followed after interfacing the voltage and current sensors to the 71M6513/6513H chip. When properly interfaced, the V3P3 power supply is connected to the meter neutral and is the DC reference for each input. Each voltage and current waveform, as seen by the 71M6513/6513H, is scaled to be less than 250mV (peak).

2.2.1 CALIBRATION PROCEDURE WITH THREE MEASUREMENTS

The calibration procedure is as follows:

1) All calibration factors are reset to their default values, i.e. CAL_IA = CAL_VA = 16384, and PHADJ_A = 0.

2) An RMS voltage V_{ideal} consistent with the meter's nominal voltage is applied, and the RMS reading V_{actual} of the meter is recorded. The voltage reading error Axv is determined as

   $Axv = (V_{actual} - V_{ideal}) / V_{ideal}$

3) Apply the nominal load current at phase angles 0° and 60°, measure the Wh energy and record the errors E_0 AND E_{60}.

4) Calculate the new calibration factors CAL_IA, CAL_VA, and PHADJ_A, using the formulae presented in section 2.1.1 or using the spreadsheet presented in section 2.2.4.

5) Apply the new calibration factors CAL_IA, CAL_VA, and PHADJ_A to the meter. The memory locations for these factors are given in section 1.9.1.

6) Test the meter at nominal current and, if desired, at lower and higher currents and various phase angles to confirm the desired accuracy.

7) Store the new calibration factors CAL_IA, CAL_VA, and PHADJ_A in the flash memory of the meter. If the calibration is performed on a TERIDIAN Demo Board, the methods shown in sections 1.9.3 and 1.9.4 can be used.

8) Repeat the steps 1 through 7 for each phase.

9) For added temperature compensation, read the value in CE RAM location 0x54 and write it to CE RAM location 0x11. If Demo Code 3.05 or later is used, this will automatically calculate the correction coefficients PPMC and PPMC2 from the nominal temperature entered in CE location 0x11 and from the characterization data contained in the on-chip fuses.

Tip: Step 2 and the energy measurement at 0° of step 3 can be combined into one step.

2.2.2 CALIBRATION PROCEDURE WITH FIVE MEASUREMENTS

The calibration procedure is as follows:

1) All calibration factors are reset to their default values, i.e. CAL_IA = CAL_VA = 16384, and PHADJ_A = 0.

2) An RMS voltage V_{ideal} consistent with the meter's nominal voltage is applied, and the RMS reading V_{actual} of the meter is recorded. The voltage reading error Axv is determined as

   $Axv = (V_{actual} - V_{ideal}) / V_{ideal}$

3) Apply the nominal load current at phase angles 0°, 60°, 180° and –60° (-300°). Measure the Wh energy each time and record the errors E_0, E_{60}, E_{180}, and E_{300}.

4) Calculate the new calibration factors CAL_IA, CAL_VA, and PHADJ_A, using the formulae presented in section 2.1.2 or using the spreadsheet presented in section 2.2.4.

5) Apply the new calibration factors CAL_IA, CAL_VA, and PHADJ_A to the meter. The memory locations for these factors are given in section 1.9.1.

6) Test the meter at nominal current and, if desired, at lower and higher currents and various phase angles to confirm the desired accuracy.

7) Store the new calibration factors CAL_IA, CAL_VA, and PHADJ_A in the flash memory of the meter. If a Demo Board is calibrated, the methods shown in sections 1.9.3 and 1.9.4 can be used.

8) Repeat the steps 1 through 7 for each phase.

9) For added temperature compensation, read the value in CE RAM location 0x54 and write it to CE RAM location 0x11. If Demo Code 3.05 or later is used, this will automatically calculate the correction coefficients PPMC and PPMC2 from the nominal temperature entered in CE location 0x11 and from the characterization data contained in the on-chip fuses.

Tip: Step 2 and the energy measurement at 0° of step 3 can be combined into one step.

2.2.3 CALIBRATION PROCEDURE FOR ROGOWSKI COIL SENSORS

Demo Code containing CE code that is compatible with Rogowski coils is available from TERIDIAN Semiconductor.

Rogowski coils generate a signal that is the derivative of the current. The CE code implemented in the Rogowski CE image digitally compensates for this effect and has the usual gain and phase calibration adjustments. Additionally, calibration adjustments are provided to eliminate voltage coupling from the sensor input.

Current sensors built from Rogowski coils have a relatively high output impedance that is susceptible to capacitive coupling from the large voltages present in the meter. The most dominant coupling is usually capacitance between the primary of the coil and the coil's output. This coupling adds a component proportional to the derivative of voltage to the sensor output. This effect is compensated by the voltage coupling calibration coefficients.

As with the CT procedure, the calibration procedure for Rogowski sensors uses the meter's display to calibrate the voltage path and the pulse outputs to perform the remaining energy calibrations. The calibration procedure must be done to each phase separately, making sure that the pulse generator is driven by the accumulated real energy for just that phase. In other words, the pulse generator input should be set to WhA, WhB, or WhC, depending on the phase being calibrated.

In preparation of the calibration, all calibration parameters are set to their default values. *VMAX* and *IMAX* are set to reflect the system design parameters. *WRATE* and *PUSE_SLOW*, *PULSE_FAST* are adjusted to obtain the desired Kh.

Step 1: Basic Calibration: After making sure *VFEED_A*, *VFEED_B*, and *VFEED_C* are zero, perform either the three measurement procedure (2.2.1) or the five measurement calibration procedure (2.2.2) described in the CT section. Perform the procedure at a current large enough that energy readings are immune from voltage coupling effects.

The one exception to the CT procedure is the equation for PHADJ—after the phase error, ϕs, has been calculated, use the PHADJ equation shown below. Note that the default value of PHADJ is not zero, but rather –3973.

$$PHADJ = PHADJ_{PREVIOUS} - \phi_S 1786 \frac{50}{f_0}$$

If voltage coupling at low currents is introducing unacceptable errors, perform step 2 below to select non-zero values for *VFEED_A*, *VFEED_B*, and *VFEED_C*.

Step 2: Voltage Cancellation: Select a small current, I_{RMS}, where voltage coupling introduces at least 1.5% energy error. At this current, measure the errors E_0 and E_{180} to determine the coefficient *VFEED* .

$$VFEED = \frac{E_0 - E_{180}}{2} 2^{25} \frac{I_{RMS}\ V_{MAX}}{I_{MAX}\ V_{RMS}} - VFEED_{PREVIOUS}$$

2.2.4 CALIBRATION SPREADSHEETS

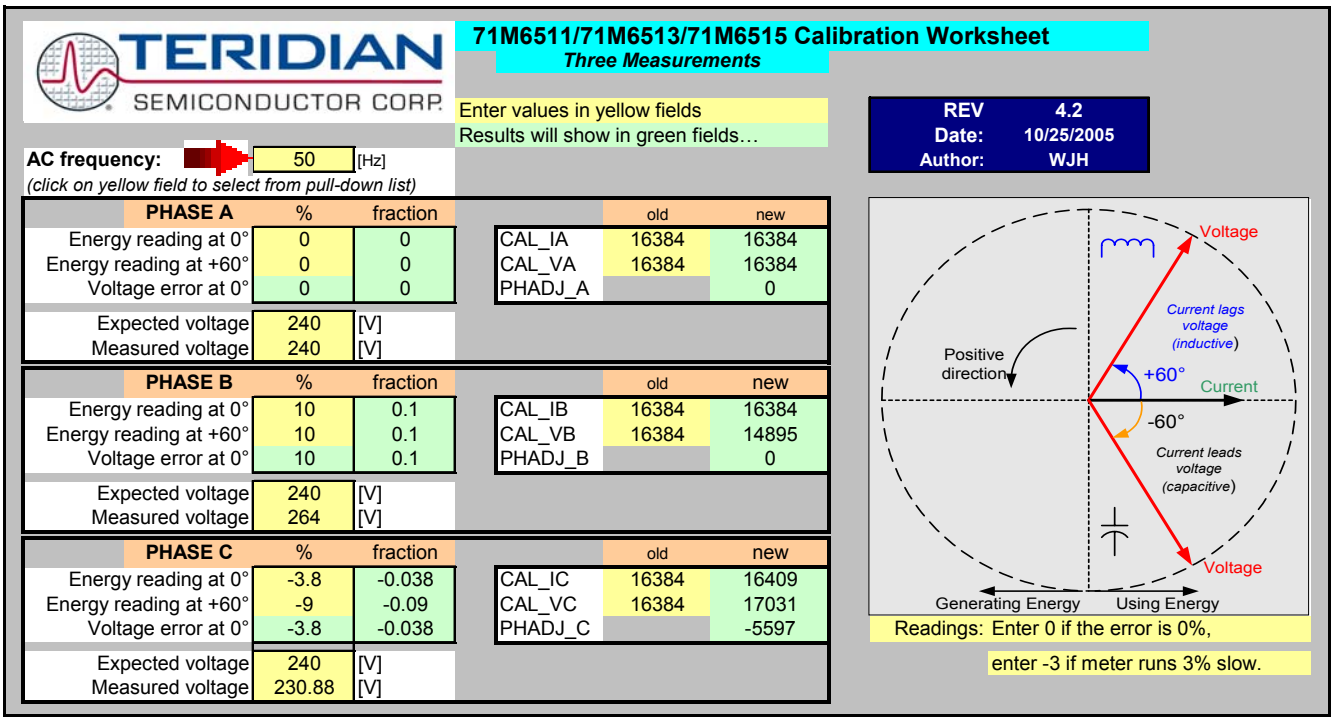
Calibration spreadsheets are available from TERIDIAN Semiconductor. They are also included in the CD-ROM shipped with any Demo Kit. Figure 2-3 shows the spreadsheet for three measurements. Figure 2-4 shows the spreadsheet for five measurements with three phases.

For CT and shunt calibration, data should be entered into the calibration spreadsheets as follows:

1. Calibration is performed one phase at a time.
2. Results from measurements are generally entered in the yellow fields. Intermediate results and calibration factors will show in the green fields.
3. The line frequency used (50 or 60Hz0 is entered in the yellow field labeled AC frequency.
4. After the voltage measurement, measured (observed) and expected (actually applied) voltages are entered in the yellow fields labeled "Expected Voltage" and "Measured Voltage". The error for the voltage measurement will then show in the green field above the two voltage entries.
5. The relative error from the energy measurements at 0° and 60° are entered in the yellow fields labeled "Energy reading at 0°" and "Energy reading at 60°". The corresponding error, expressed as a fraction will then show in the two green fields to the right of the energy reading fields.
6. The spreadsheet will calculate the calibration factors CAL_IA, CAL_VA, and PHADJ_A from the information entered so far and display them in the green fields in the column underneath the label "new".
7. If the calibration was performed on a meter with non-default calibration factors, these factors can be entered in the yellow fields in the column underneath the label "old".
   For a meter with default calibration factors, the entries in the column underneath "old" should be at the default value (16384).

A spreadsheet is also available for Rogowski coil calibration (see Figure 2-5). Data entry is as follows:

1. All nominal values are entered in the fields of step one.
2. The applied voltage is entered in the yellow field labeled "Input Voltage Applied" of step 2. The entered value will automatically show in the green fields of the two other channels.
3. After measuring the voltages displayed by the meter, these are entered in the yellow fields labeled "Measured Voltage". The spreadsheet will show the calculated calibration factors for voltage in the green fields labeled "CAL_Vx".
4. The default values (-3973) for PHADJ_x are entered in the yellow fields of step 3. If the calibration factors for the current are not at default, their values are entered in the fields labeled "Old CAL_Ix".
5. The errors of the energy measurements at 0°, 60°, -60°, and 180° are entered in the yellow fields labeled "% Error …". The spreadsheet will then display phase error, the current calibration factor and the PHADJ_x factor in the green fields, one for each phase.
6. If a crosstalk measurement is necessary, it should be performed at a low current, where the effects of crosstalk are noticeable. First, if (old) values for VFEEDx exist in the meter, they are entered in the spreadsheet in the row labeled "Old VFEEDx", one for each phase. If these factors are zero, "0" is entered for each phase.
7. Test current and test voltage are entered in the yellow fields labeled VRMS and IRMS.
8. The crosstalk measurement is now conducted at a low current with phase angles of 0° and 180°, and the percentage errors are entered in the yellow fields labeled "% error, 0 deg" and "% error, 180 deg", one pair of values for each phase. The resulting VFEEDx factors are then displayed in the green fields labeled VFEEDx.



TERIDIAN SEMICONDUCTOR CORP.

71M6511/71M6513/71M6515 Calibration Worksheet

Three Measurements

Enter values in yellow fields
Results will show in green fields…

REV	4.2
Date:	10/25/2005
Author:	WJH

AC frequency: 50 [Hz]
(click on yellow field to select from pull-down list)

PHASE A	%	fraction
Energy reading at 0°	0	0
Energy reading at +60°	0	0
Voltage error at 0°	0	0
Expected voltage	240	[V]
Measured voltage	240	[V]

	old	new
CAL_IA	16384	16384
CAL_VA	16384	16384
PHADJ_A		0

PHASE B	%	fraction
Energy reading at 0°	10	0.1
Energy reading at +60°	10	0.1
Voltage error at 0°	10	0.1
Expected voltage	240	[V]
Measured voltage	264	[V]

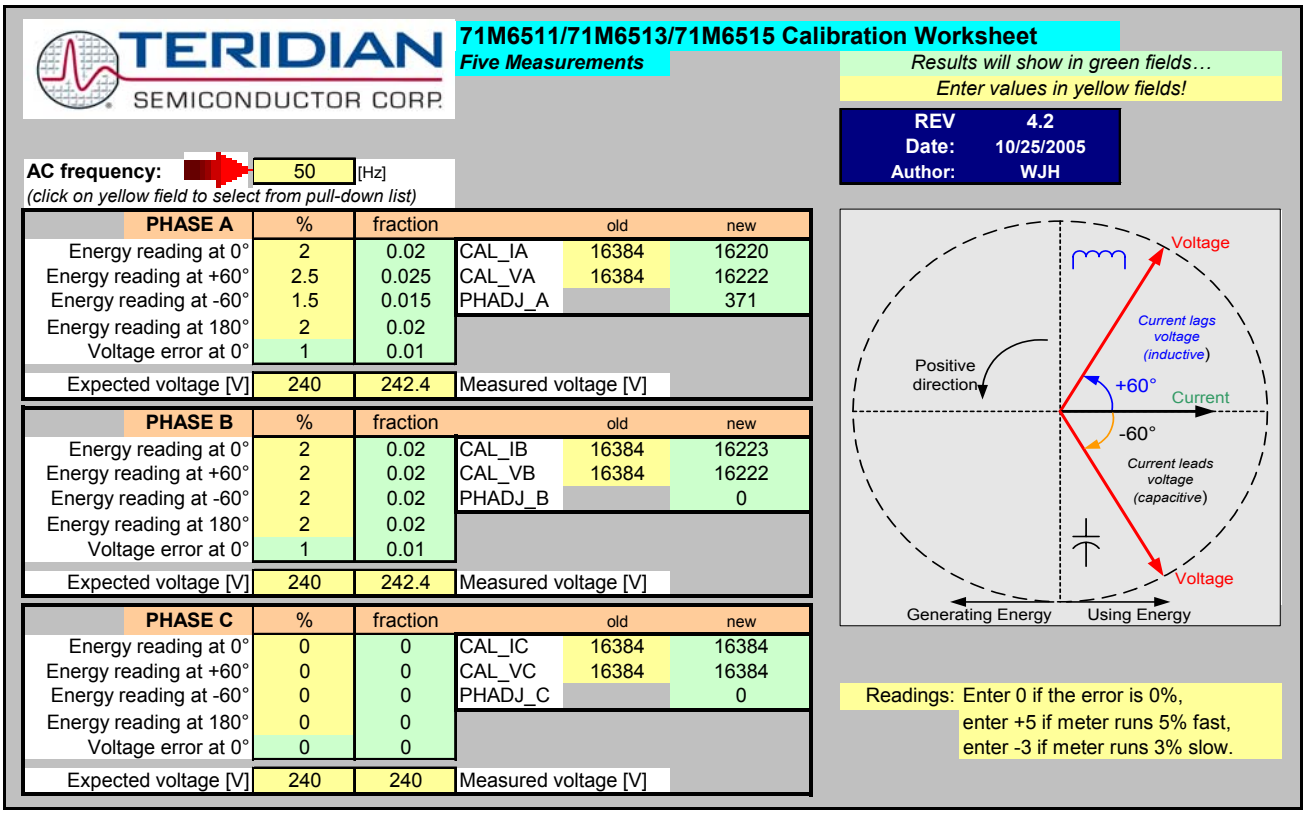
	old	new
CAL_IB	16384	16384
CAL_VB	16384	14895
PHADJ_B		0

PHASE C	%	fraction
Energy reading at 0°	-3.8	-0.038
Energy reading at +60°	-9	-0.09
Voltage error at 0°	-3.8	-0.038
Expected voltage	240	[V]
Measured voltage	230.88	[V]

	old	new
CAL_IC	16384	16409
CAL_VC	16384	17031
PHADJ_C		-5597

Readings: Enter 0 if the error is 0%,
enter -3 if meter runs 3% slow.

Figure 2-3: Calibration Spreadsheet for Three Measurements



TERIDIAN SEMICONDUCTOR CORP.

71M6511/71M6513/71M6515 Calibration Worksheet

Five Measurements

Results will show in green fields…
Enter values in yellow fields!

REV	4.2
Date:	10/25/2005
Author:	WJH

AC frequency: 50 [Hz]
(click on yellow field to select from pull-down list)

PHASE A	%	fraction		old	new
Energy reading at 0°	2	0.02	CAL_IA	16384	16220
Energy reading at +60°	2.5	0.025	CAL_VA	16384	16222
Energy reading at -60°	1.5	0.015	PHADJ_A		371
Energy reading at 180°	2	0.02			
Voltage error at 0°	1	0.01			
Expected voltage [V]	240	242.4	Measured voltage [V]		

PHASE B	%	fraction		old	new
Energy reading at 0°	2	0.02	CAL_IB	16384	16223
Energy reading at +60°	2	0.02	CAL_VB	16384	16222
Energy reading at -60°	2	0.02	PHADJ_B		0
Energy reading at 180°	2	0.02			
Voltage error at 0°	1	0.01			
Expected voltage [V]	240	242.4	Measured voltage [V]		

PHASE C	%	fraction		old	new
Energy reading at 0°	0	0	CAL_IC	16384	16384
Energy reading at +60°	0	0	CAL_VC	16384	16384
Energy reading at -60°	0	0	PHADJ_C		0
Energy reading at 180°	0	0			
Voltage error at 0°	0	0			
Expected voltage [V]	240	240	Measured voltage [V]		

Readings: Enter 0 if the error is 0%,
enter +5 if meter runs 5% fast,
enter -3 if meter runs 3% slow.

Figure 2-4: Calibration Spreadsheet for Five Measurements

Calibration Procedure for Rogowski Coils

Enter values in yellow fields!
Results will show in green fields…

TERIDIAN SEMICONDUCTOR CORP.

Step 1: Enter Nominal Values:

Nominal CAL_V	16384
Nominal CAL_I	16384
PHADJ	-3973
WRATE	179
VMAX	600
Calibration Frequency [Hz]	50
IMAX (incl. ISHUNT)	30.000
PULSE_FAST	-1
PULSE_SLOW	-1
NACC	2520

Resulting Nominal Values: X	6	REV	4.3
Kh (Wh)	0.440	Date:	11/18/2005
		Author:	WJH

Angle Sensitivity (deg/LSB)
50Hz 5.60E-04

Step 2: VRMS Calibration:

	Phase A	Phase B	Phase C
Enter old CAL_VA	16384	16384	16384
Input Voltage Applied	240	240	240
Measured Voltage	235.612	236.55	234.72
CAL_Vx	16689	16623	16753

Step 3: Current Gain and Phase Calibration Deg/ct 5.60E-04

	Phase A	Phase B	Phase C
old PHADJ	-3973	-3973	-3973
Old CAL_Ix	16384	16384	16384
%Error, 60°	-3.712	-3.912	-5.169
%Error, -60°	-3.381	-2.915	-4.241
%Error, 0°	-3.591	-3.482	-4.751
%Error, 180°	-3.72	-3.56	-4.831
Phase Error (°)	0.0547319	0.1647659	0.1533716
PHADJ	-4070.74	-4267.22	-4246.88
CAL_Ix	17005.641	16981.934	17208.457

Step 4: Crosstalk Calibration (Equalize Gain for 0° and 180°)

VRMS	240
IRMS	0.30

	Phase A	Phase B	Phase C
Old VFEEDx	0	0	0
% Error, 0deg	1.542	1.61	1.706
%Error, 180deg	-1.634	-1.743	-1.884
VFEEDx	-13321	-14064	-15058

1. Rogowski coils have significant crosstalk from voltage to current. This contributes to gain and phase errors.
2. Therefore, before calibrating a Rogowski meter, a quick 0° load line should be run to determine at what current the crosstalk contributes at least 1% error.
3. Crosstalk calibration should be performed at this current or lower.
4. If crosstalk contributes an E0 error at current Ix, there will be a 0.1% error in E60 at 15*Ix.

Figure 2-5: Calibration Spreadsheet for Rogowski coil

2.2.5 COMPENSATING FOR NON-LINEARITIES

Nonlinearity is most noticeable at low currents, as shown in Figure 2-6, and can result from input noise and truncation. Nonlinearities can be eliminated using the *QUANT* variable.

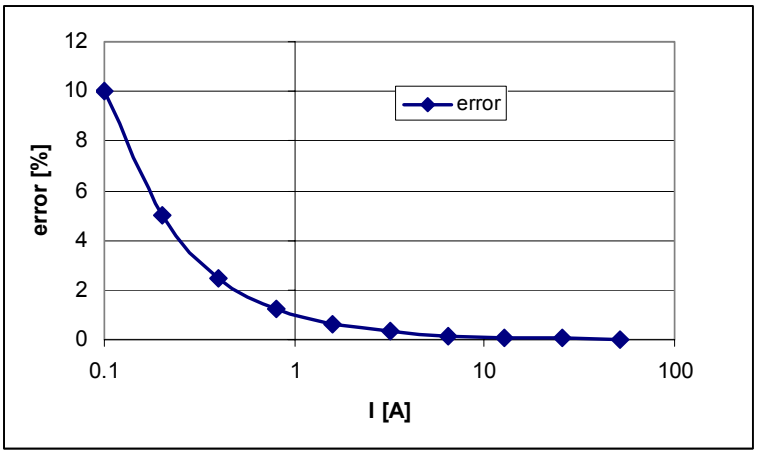


Figure 2-6: Non-Linearity Caused by Quantification Noise

The error can be seen as the presence of a virtual constant noise current. While 10mA hardly contribute any error at currents of 10A and above, the noise becomes dominant at small currents.

The value to be used for QUANT can be determined by the following formula:

$$QUANT = -\frac{\frac{error}{100} V \cdot I}{VMAX \cdot IMAX \cdot LSB}$$

Where error = observed error at a given voltage (V) and current (I),
VMAX = voltage scaling factor, as described in section 1.8.3,
IMAX = current scaling factor, as described in section 1.8.3,
LSB = QUANT LSB value = $7.4162*10^{-10}$W

Example: Assuming an observed error as in Figure 2-6, we determine the error at 1A to be +1%. If VMAX is 600V and IMAX = 208A, and if the measurement was taken at 240V, we determine QUANT as follows:

$$QUANT = -\frac{\frac{1}{100} 240 \cdot 1}{600 \cdot 208 \cdot 7.4162 \cdot 10^{-10}} = -11339$$

QUANT is to be written to the CE location 0x2F. It does not matter which current value is chosen as long as the corresponding error value is significant (5% error at 0.2A used in the above equation will produce the same result for *QUANT*).

Input noise and truncation can cause similar errors in the VAR calculation that can be eliminated using the *QUANT_VAR* variable. *QUANT_VAR* is determined using the same formula as *QUANT*.

2.3 POWER SAVING MEASURES

In many cases, especially when operating the TERIDIAN 71M6513/71M6513H from a battery, it is desirable to reduce the power consumed by the chip to a minimum. This can be achieved with the measures listed in Table 2-1.

Power Saving Measure	Software Control	Typical Savings
Disable the CE	CE_EN = 0	0.16mA
Disable the ADC	ADC_DIS = 1	1.8mA
Disable clock test output CKTEST	CKOUTDIS = 1	0.6mA
Disable emulator clock	ECK_DIS = 1	0.1mA
Set flash read pulse timing to 33 ns	FLASH66Z =1	0.04mA
Disable the LCD voltage boost circuitry	LCD_BSTEN = 0	0.9mA
Disable RTM outputs	RTM_EN = 0	0.01mA
Disable SSI output	SSI_EN = 0	
Select DGND for the multiplexer input	TMUX[3:0] = 0	
Disable reference voltage output	VREF_DIS = 1	
Reduce the clock for the MPU	MPU_DIV = 5	0.4mA

Table 2-1: Power Saving Measures

2.4 SCHEMATIC INFORMATION

In this section, hints on proper schematic design are provided that will help designing circuits that are functional and sufficiently immune to EMI (electromagnetic interference).

2.4.1 COMPONENTS FOR THE V1 PIN

The V1 pin of the 71M6513/6513H can never be left unconnected.

A voltage divider should be used to establish that V1 is in a safe range when the meter is in mission mode (V1 must be lower than 2.9V in all cases in order to keep the hardware watchdog timer enabled). For proper debugging or loading code into the 71M6513/6513H mounted on a PCB, it is necessary to have a provision like the header JP1 shown above R1 in Figure 2-7. A shorting jumper on this header pulls V1 up to V3P3 disabling the hardware watchdog timer.

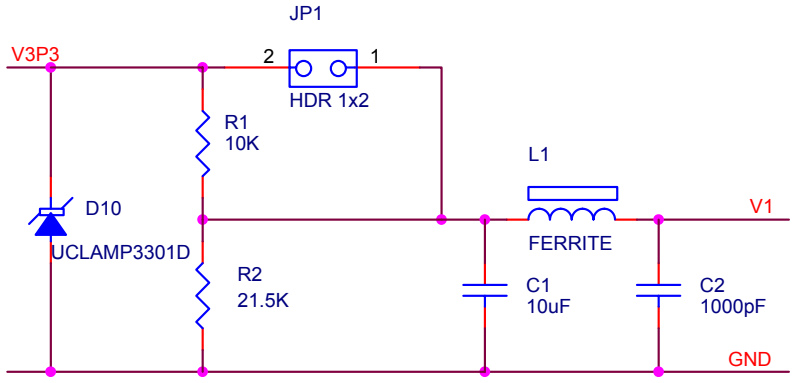


Figure 2-7: Voltage Divider for V1

On the 6513 Demo Boards this feature is implemented with resistors R83/R86, capacitor C31 (D6513T3C1 Demo Board) and TP10. See the board schematics in the Appendix for details.

2.4.2 RESET CIRCUIT

Even though a functional meter will not necessarily need a reset switch, the 71M6513 Demo Boards provide a reset pushbutton that can be used when prototyping and debugging software. When a circuit is used in an EMI environment, the RESETZ pin should be supported by the external components shown in Figure 2-8. R_1 should be in the range of 200Ω, R_2 should be around 10Ω. The capacitor C_1 should be 1nF. R1 and C1 should be mounted as close as possible to the IC. In cases where the trace from the pushbutton switch to the RESETZ pin poses a problem, R_2 can be removed.

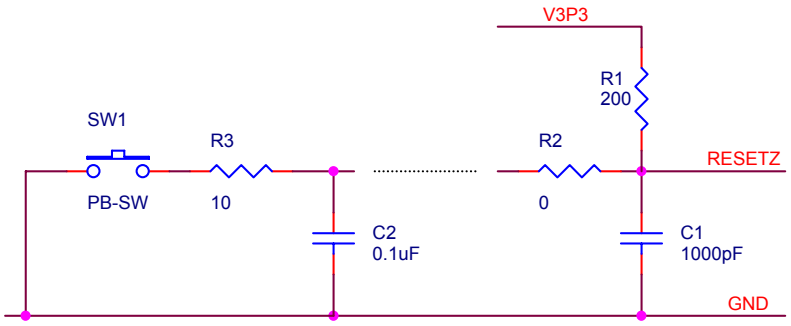


Figure 2-8: External Components for RESETZ

2.4.3 OSCILLATOR

The oscillator of the 71M6513 drives a standard 32.768kHz watch crystal (see Figure 2-9). Crystals of this type are accurate and do not require a high current oscillator circuit. The oscillator in the 71M6513 has been designed specifically to handle watch crystals and is compatible with their high impedance and limited power handling capability. The oscillator power dissipation is very low to maximize the lifetime of any battery backup device attached to the VBAT pin.

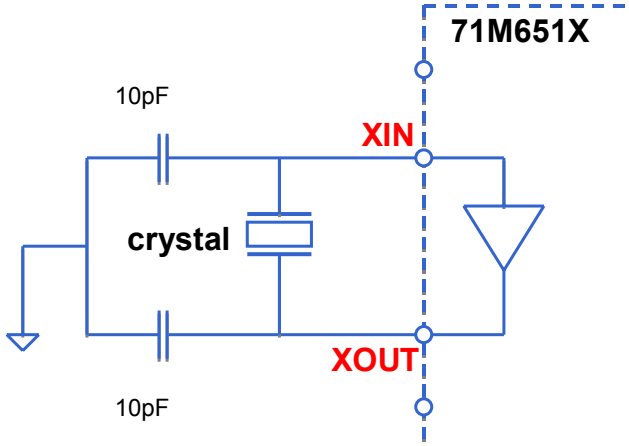


Figure 2-9: Oscillator Circuit

It is not necessary to place an external resistor across the crystal, i.e. R91 on the D6513T3B2 Demo Board must not be populated.

Capacitor values for the crystal must be <15pF.

2.4.4 EEPROM

EEPROMs should be connected to the pins DIO4 and DIO5 (see Figure 2-10). These pins can be switched from regular DIO to implement an I2C interface by setting the I/O RAM register DIO_EEX (0x2008[4]) to 1. Pull-up resistors of 3kΩ must be provided for both the SCL and SDA signals.

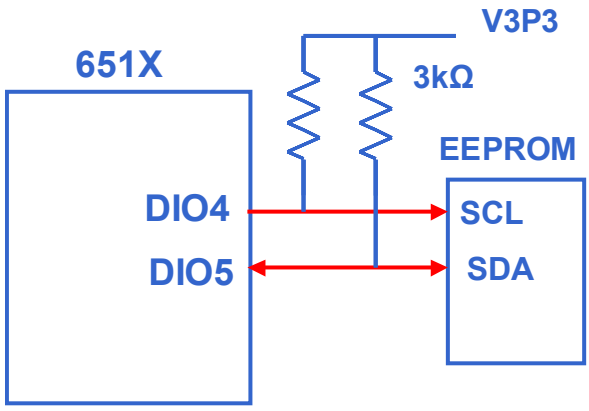


Figure 2-10: EEPROM Circuit

2.4.5 LCD

The 71M6513 has an on-chip LCD controller capable of controlling static or multiplexed LCDs. Figure 2-11 shows the basic connection for LCDs. Note that the LCD module itself has no power connection.

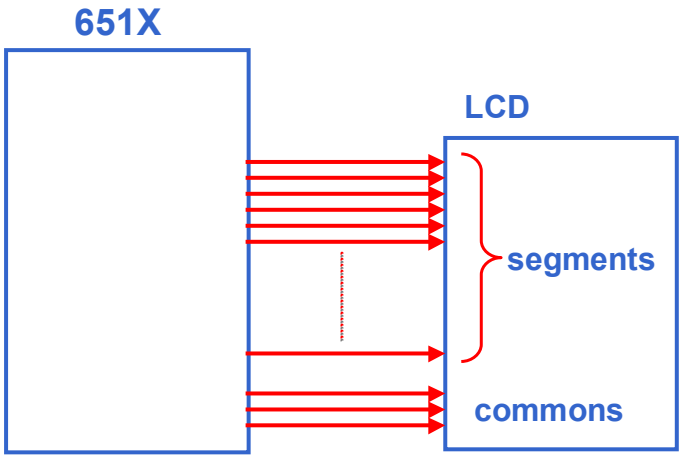


Figure 2-11: LCD Connections

Figure 2-12 shows how 5V LCDs can be operated even when a 5V supply is not available. Setting the I/O RAM register *LCD_BSTEN* to 1 starts the on-chip boost circuitry that will output an AC frequency on the VDRV pin. Using a small coupling capacitor, two general-purpose diodes and a reservoir capacitor, a 5VDC voltage is generated which can be fed back into the VLCD pin of the 71M6513. The LCD drivers are enabled with the I/O register *LCD_ON*; I/O register *LCD_FS* is used to adjust contrast, and *LCD_MODE* selects the operation mode (LCD type).

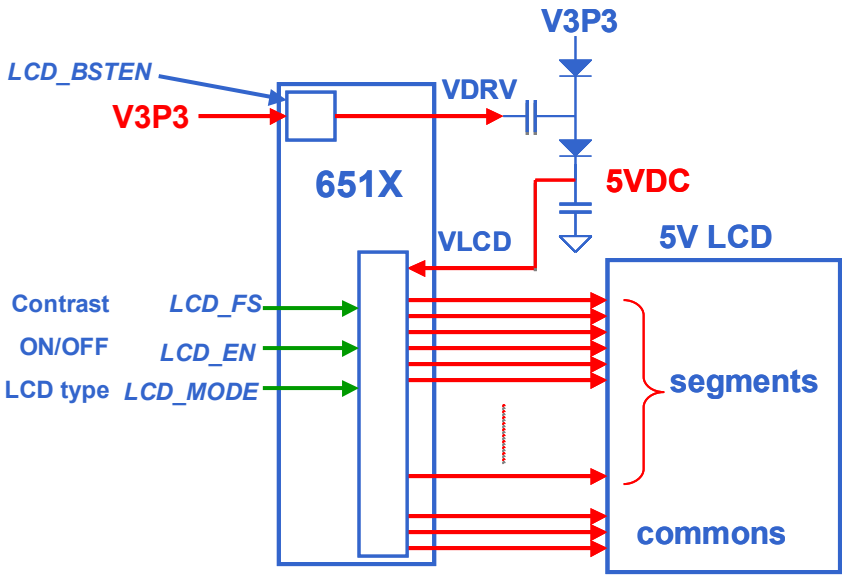


Figure 2-12: LCD Boost and LCD Control Registers

2.4.6 OPTICAL INTERFACE

The 71M6513 IC is equipped with two pins supporting the optical interface: OPT_TX and OPT_RX. The OPT_TX pin can be used to drive a visual or IR light LED with up to 20mA, a series resistor (R_2 in Figure 2-13) helps limiting the current). The OPT_RX pin can be connected to the collector of a photo-transistor, as shown in Figure 2-13.

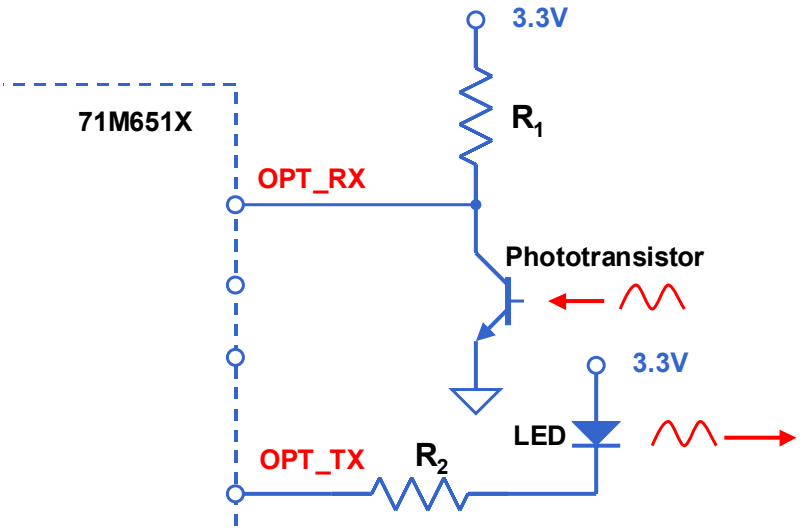


Figure 2-13: Optical Interface Block Diagram

On both the D6513T3B2 and D6513T3C1 Demo Boards, the current limiting resistor R79 is provided in between the OPT_TX pin of the chip and pin 2 of J12 (Figure 2-14). C21 on the D6513T3B2 Demo Boards should be shorted to create a DC path from the collector of the photo-transistor to the OPT_RX pin.

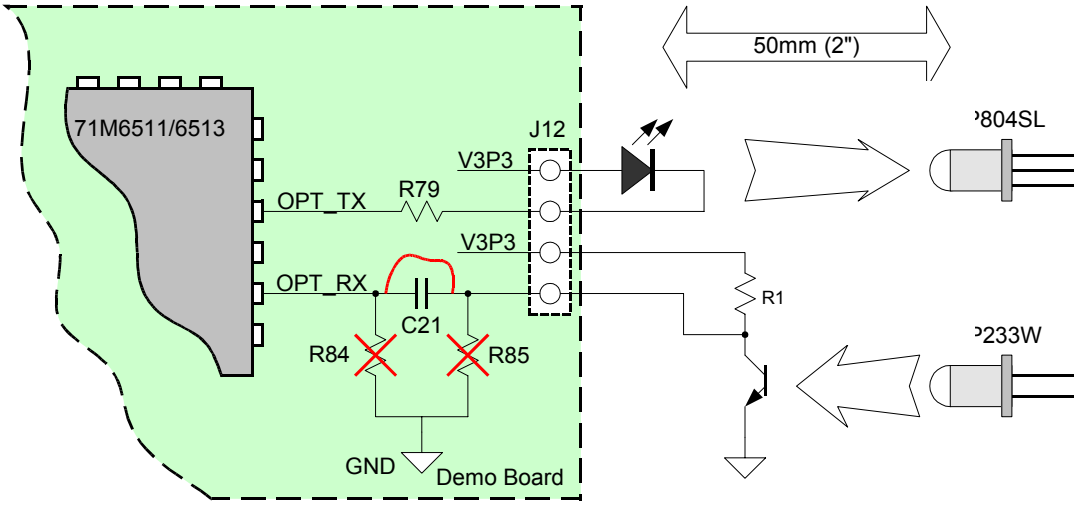


Figure 2-14: Optical Port Circuitry on the D6513T3B2 Demo Board

The IR diode should be connected between terminal 2 of header J12 on the Demo Board (cathode) and the V3P3 voltage (anode), which is accessible at terminal 1 of header J12 (see Figure 3). The value of R79 may be increased or decreased in order to vary the diode current. R84 and R85 (D6513T3B2 only) should be removed when operating the photo-transistor in the configuration shown.

J12 on the D6513T3C1 Demo Boards has all the provisions for connecting the IR LED and photo-transistor (see Figure 2-15). Depending on the required LED current, R79 may have to be scaled. Similarly, R84 may be scaled or removed, depending on the current generated by the photo-transistor.

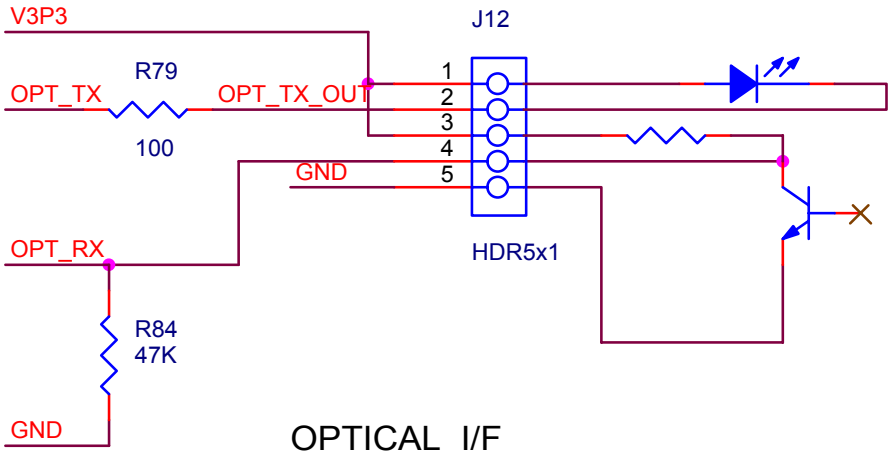


Figure 2-15: Optical Port Circuitry on the D6513T3C1 Demo Board

2.4.7 CONNECTING THE RX PIN

Due to unique circuitry on the RX input, its behavior is slightly different from the other digital inputs of the 651X family of metering ICs.

The Rx pin (serial port receive pin) of the 71M6513/6513H is internally clamped to the V3P3 supply as shown in Figure 2-16. This means, the voltage of signals applied to this pin will be clamped to V3P3D + 0.6V, i.e. nominally 3.9V. Note that this clamp voltage exceeds the 3.6V Absolute Maximum Rating of the RX input.

Inputs above 1.6V (V_{IL}) are guaranteed to be recognized as logic 1. Inputs below 0.8V (V_{IL}) are guaranteed to be recognized as logic 0. Input voltages between 0.8V and 1.6V must be avoided.

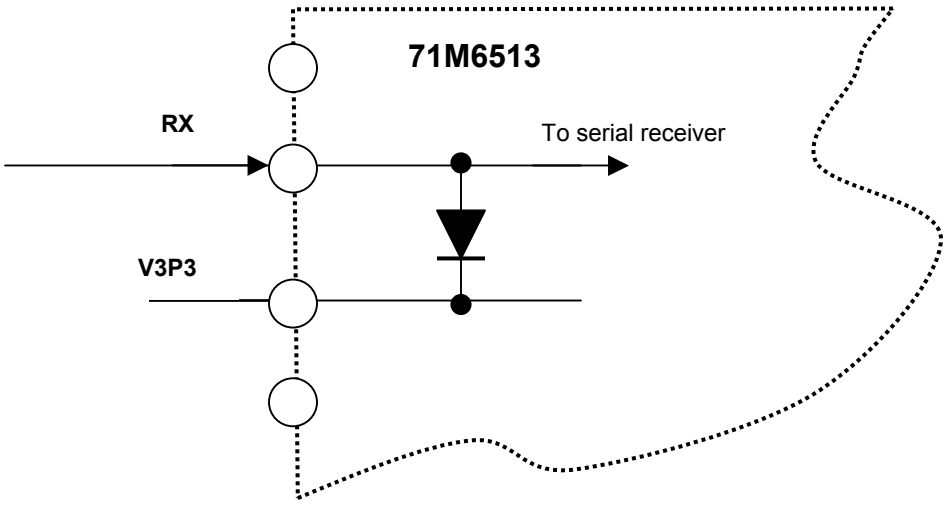


Figure 2-16: Internal Diode Clamp on the RX Pin

If inputs higher than 3.6V are expected at the RX pin, e.g. when interfacing to 5V-based driving circuitry such as RS-232 transceivers/receivers, TTL or CMOS logic, a resistor attenuator should be used in order to restrict the RX input voltage.

Figure 2-17 shows the recommended resistor network consisting of R1 (17kΩ) and R2 (33kΩ). This network scales the input voltage V_{IN} of 5.5V to 3.6V, and an input voltage of 2.5V will be scaled to 1.6V. For the low voltage level, V_{IN} voltages below 1.2V will be scaled to 0.8V. The maximum current at 5.5V input voltage is 5.5V/(50kΩ) + I_{IH} = 110µA + 1µA = 111µA.

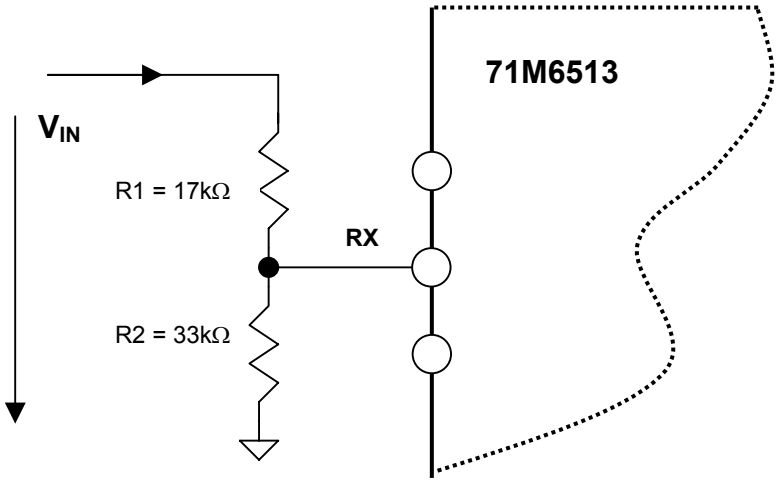


Figure 2-17: Resistor Network for RX

2.4.8 CONNECTING THE V3 PIN

If not used for sensing or measuring purposes, the V3 pin should be either left unconnected (floating) or connected to the VREF pin.

2.5 TESTING THE DEMO BOARD

This section will explain how the 71M6513/6513H IC and the peripherals can be tested. Hints given in this section will help evaluating the features of the Demo Board and understanding the IC and its peripherals.

2.5.1 FUNCTIONAL METER TEST

This is the test that every Demo Board has to pass before being integrated into a Demo Kit. Before going into the functional meter test, the Demo Board has already passed a series of bench-top tests, but the functional meter test is the first test that applies realistic high voltages (and current signals from current transformers) to the Demo Board.

Figure 2-18 shows a meter connected to a typical calibration system. The calibrator supplies calibrated voltage and current signals to the meter. It should be noted that the current flows through the CT or CTs that are not part of the Demo Board. The Demo Board rather receives the voltage output signals fro the CT. An optical pickup senses the pulses emitted by the meter and reports them to the calibrator. Some calibration systems have electrical pickups. The calibrator measures the time between the pulses and compares it to the expected time, based on the meter Kh and the applied power.

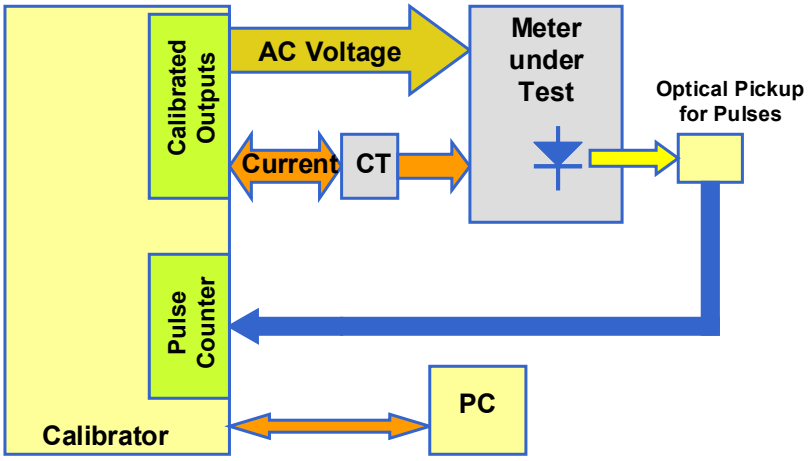


Figure 2-18: Meter with Calibration System

TERIDIAN Demo Boards are not calibrated prior to shipping. However, the Demo Board pulse outputs are tested and compared to the expected pulse output. Figure 2-19 shows the screen on the controlling PC for a typical Demo Board. The number in the red field under "As Found" represents the error measured for phase A, while the number in the red field under "As Left" represents the error measured for phase B. Both numbers are given in percent. This means that for the measured Demo Board, the sum of all errors resulting from tolerances of PCB components, CTs, and 71M6513/6513H tolerances was –2.8% and –3.8%, a range that can easily be compensated by calibration.

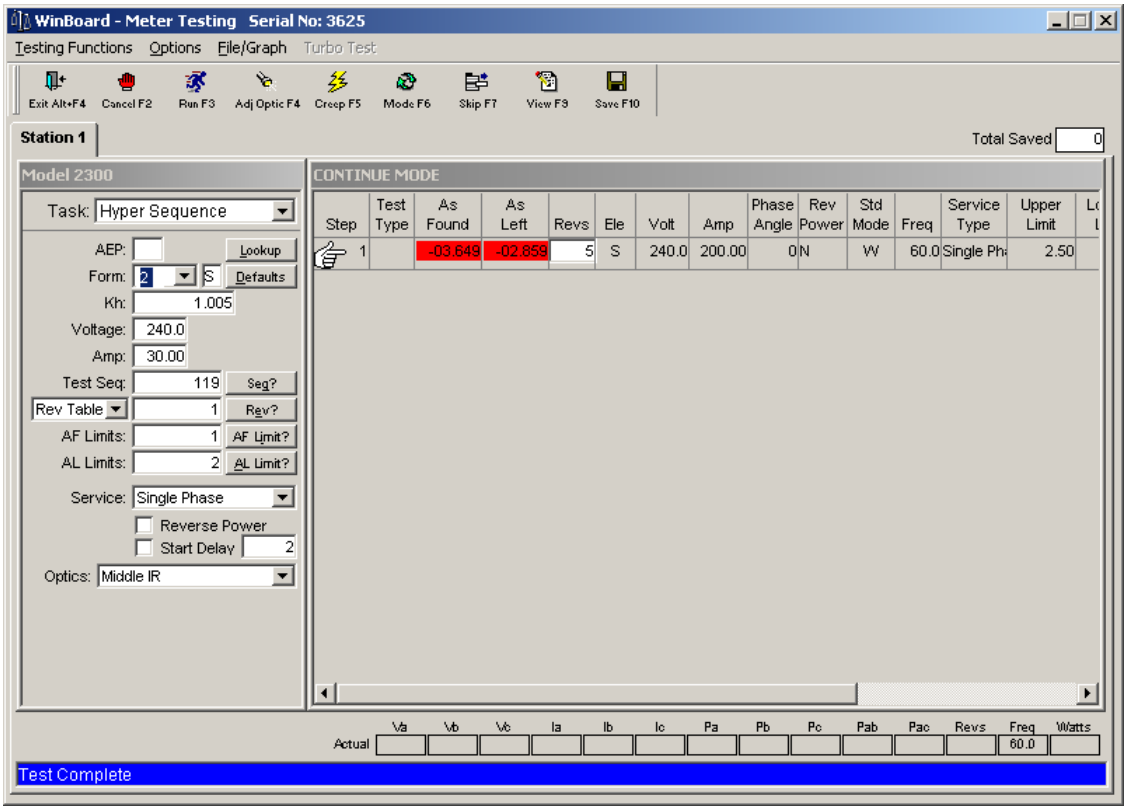


Figure 2-19: Calibration System Screen

2.5.2 EEPROM

Testing the EEPROM provided on the Demo Board is straightforward and can be done using the serial command line interface (CLI) of the Demo Code.

To write a string of text characters to the EEPROM and read it back, we apply the following sequence of CLI commands:

>EEC1 Enables the EEPROM

>EESthis is a test Writes text to the buffer

>EET80 Writes buffer to address 80

Written to EEPROM address 00000080 74 68 69 73 20 69 73 20 61 ….

Response from Demo Code

>EER80.E Reads text from the buffer

Read from EEPROM address 00000080 74 68 69 73 20 69 73 20 61 ….

Response from Demo Code

>EEC0 Disables the EEPROM

2.5.3 RTC

Testing the RTC inside the 71M6513/6513H IC is straightforward and can be done using the serial command line interface (CLI) of the Demo Code.

To set the RTC and check the time and date, we apply the following sequence of CLI commands:

>M10	LCD display to show calendar date
>RTD05.09.27.3	Sets the date to 9/27/2005 (Tuesday)
>M9	LCD display to show time of day
>RTT10.45.00	Sets the time to 10:45:00. AM/PM distinction: 1:22:33PM = 13:22:33

2.5.4 HARDWARE WATCHDOG TIMER

The hardware watchdog timer of the 71M6513/6513H is disabled when the voltage at the V1 pin is at 3.3V (V3P3). On the Demo Boards, this is done by plugging in a jumper at TP10 between the V1 and V3P3 pins.

Programming the flash memory or emulation using the ADM51 In-Circuit-Emulator can only be done when a jumper is plugged in at TP10 between V1 and V3P3.

Conversely, removing the jumper at TP10 will enable the hardware watchdog timer.

2.5.5 LCD

Various tests of the LCD interface can be performed with the Demo Board, using the serial command line interface (CLI):

Setting the LCD_EN register to 1 enables the display outputs.

Register Name	Address [bits]	R/W	Description
LCD_EN	2021[5]	R/W	Enables the LCD display. When disabled, VLC2, VLC1, and VLC0 are ground as are the COM and SEG outputs.

To access the *LCD_EN* register, we apply the following CLI commands:

>RI21$	Reads the hex value of register 0x2021
>25	Response from Demo Code indicating the bit 5 is set
>RI21=5	Writes the hex value 0x05 to register 0x2021 causing the display to be switched off
>RI21=25	Sets the *LCD_EN* register back to normal

The 71M6513/6513H provides a charge pump capable of boosting the 3.3VDC supply voltage up to 5.0VDC. The boost circuit is enabled with the *LCD_BSTEN* register. The 6513 Demo Boards have the boost circuit enabled by default.

Register Name	Address [bits]	R/W	Description
LCD_BSTEN	2020[7]	R/W	Enables the LCD voltage boost circuit.

To disable the LCD voltage boost circuit, we apply the following CLI commands:

>RI20$ Reads the hex value of register 0x2020

>8E Response from Demo Code indicating the bit 7 is set

>RI20=E Writes the hex value 0x0E to register 0x2020 causing the LCD boost to be switched off

>RI20=8E Enables the LCD boost circuit

The *LCD_CLK* register determines the frequency at which the COM pins change states. A slower clock means lower power consumption, but if the clock is too slow, visible flicker can occur. The default clock frequency for the 71M6513/6513H Demo Boards is 150Hz (*LCD_CLK* = 01).

Register Name	Address [bits]	R/W	Description
LCD_CLK[1:0]	2021[1:0]	R/W	Sets the LCD clock frequency, i.e. the frequency at which SEG and COM pins change states. f_w = CKADC/128 = 38,400 00: $f_w/2^9$, 01: $f_w/2^8$, 10: $f_w/2^7$, 11: $f_w/2^6$

To change the LCD clock frequency, we apply the following CLI commands:

>RI21$ Reads the hex value of register 0x2021

>25 Response from Demo Code indicating the bit 0 is set and bit 1 is cleared.

>RI21=24 Writes the hex value 0x24 to register 0x2021 clearing bit 0 – LCD flicker is visible now

>RI21=25 Writes the original value back to *LCD_CLK*

2.6 TERIDIAN APPLICATION NOTES

Please contact your local TERIDIAN sales representative for TERIDIAN Application Notes. Available application notes are listed below.

Number	Title
AN_651X_007	Rogowski Coil
AN_651X_008	Optical Port
AN_651X_009	Temperature Compensation
AN_651X_013	Emulator Upgrade
AN_651X_016	EMC/EMI Guidelines
AN_651X_017	LCD
AN_651X_018	Chop Enable
AN_651X_019	RX Pin
AN_651X_020	Calibration for Shunt and CT
AN_651X_022	Calibration Procedures
AN_6513_021	Neutral Current

3

3 HARDWARE DESCRIPTION

3.1 D6513T3B2 BOARD DESCRIPTION: JUMPERS, SWITCHES AND TEST POINTS

The items described in the following tables refer to the flags in Figure 3-1.

Item #	Reference Designator	Name	Use
1	JP1	PS_SEL[0]	Two-pin header. When the jumper is installed the on- board power supply (AC signal) is used to power the demo board. When not installed, the board must be powered by an external supply connect to J1. **Normally installed.**
2,5,6,7	J2, J5, J6, J7	Neutral, VA_IN, VB_IN, VC_IN 	VA_IN, VB_IN, and VC_IN are the line voltage inputs. Each point has a resistor divider that leads to the respective pin on the chip that is the voltage input to the A/D. These inputs come in from the bottom of the board. **Caution: High Voltage! Do not touch these pins!**
3	JP2, JP3	PS_SEL[1], PS_SEL[2]	Two-pin headers. When both jumpers are installed, external power is not required for the Debug Board that attaches to the 71M6513/71M6513H demo board at J2. Normally left open.  **Caution! When JP2/JP3 are plugged in, there is NO ISOLATION between the Demo Board and the Debug Board.**
4	J1	5 Volt external supply	Plug for connecting external 5 VDC power supply (wall wart)
8	TP2, TP4, TP6	VA, VB, and VC	Two pin header test points. One end is either the VA, VB or VC line voltage inputs to the IC and the other end is ground

Table 3-1: D6513T3B2 Demo Board Description

Item #	Reference Designator	Name	Use
9	SW2	RESET	Chip reset switch: The RESETZ pin has an internal pull up that allows normal chip operation. When the switch is pressed, the RESETZ pin is pulled low which resets the IC into a known state.
10	SW1	Pulse Rate Select	Switch connected to DIO3 (non-functional in Demo Code). SW1 should always be kept in the lower position.
11	JP9	EEPROM Write Protect	Three-pin header that allows selection of the write protection or read/write capability for the EEPROM (U4) on the demo board. **Default setting of the demo board is to place a jumper between pin 1 and 2 of JP9**.
12	J12	Supply and Optical Test Point	Four-pin header. Terminals 1 and 3 can be used to measure the supply voltage to the 71M6513/71M6513H IC. Terminal 2 monitors the TX_OPT output of the IC. Terminal 4 monitors the OPT_RX input to the IC.
13	JP12	DIO Test Point	7-pin test point. For monitoring DIO15 to DIO21.
14	J2	DEBUG	Connector for Debug Board. 2x8 pin male header.
15	J10, J11	LCD	LCD connection. The LCD daughter board connects between these two 2x12 header jumpers.
16	BT1	Battery Terminal	Two-pin header for connection of a 3.6V battery. The top pin is the positive terminal and the bottom pin is ground.
17	JP8	VBAT Selection	Three-pin header that allows selection of power to the VBAT pin. When the jumper is placed between pins 1 and 2 **(default setting of demo board)** VBAT is tied to the IC supply. When placed between terminals 2 and 3, VBAT is powered by an external battery.
18, 19	TP17, TP18	Test Points	TMUXOUT and CKTEST test point.
20	J14	EMULATOR I/F	2x10 emulator connector port for Signum ICE ADM-51.
21	J13	Voltage Connections	Five-pin header. **Connect jumper to the bottom two pins as the default**.
22	TP7	VREFOUT	Two-pin header. The top terminal is VREF, the bottom terminal is ground
23	TP10, TP9, TP8	V1, V2, V3 Test Points	Two-pin headers that are the comparator voltage input test points**. A jumper is required at TP10 from V3P3 to V1 for operation with emulator**.

Table 3-2: D6513T3B2 Demo Board Description

Item #	Reference Designator	Name	Use
24	JP10	VLCD Select	Three-pin header for selecting the voltage to the LCD. The top pin is 5V and the bottom pin is 3.3V. **The default setting for the jumper is 5V**.
25	TP11, TP12	XIN, XOUT	One-pin header test points that monitor the crystal inputs XIN and XOUT.
26	J3, J5, J7	IA_IN, IB_IN, IC_IN	Current shunt connections. Two-pin headers on bottom of the PCB. One terminal is 3.3V, the other is the shunt current.
27	TP1, TP3, TP5	IA, IB, IC	Two-pin headers that provide line current sense to the IC test points. One terminal is ground, the other is the respective line current sense input to the IC.
28	TP19	SSI	5x2 header. High-speed serial interface. One row is gnd.

Table 3-3: D6513T3B2 Demo Board Description

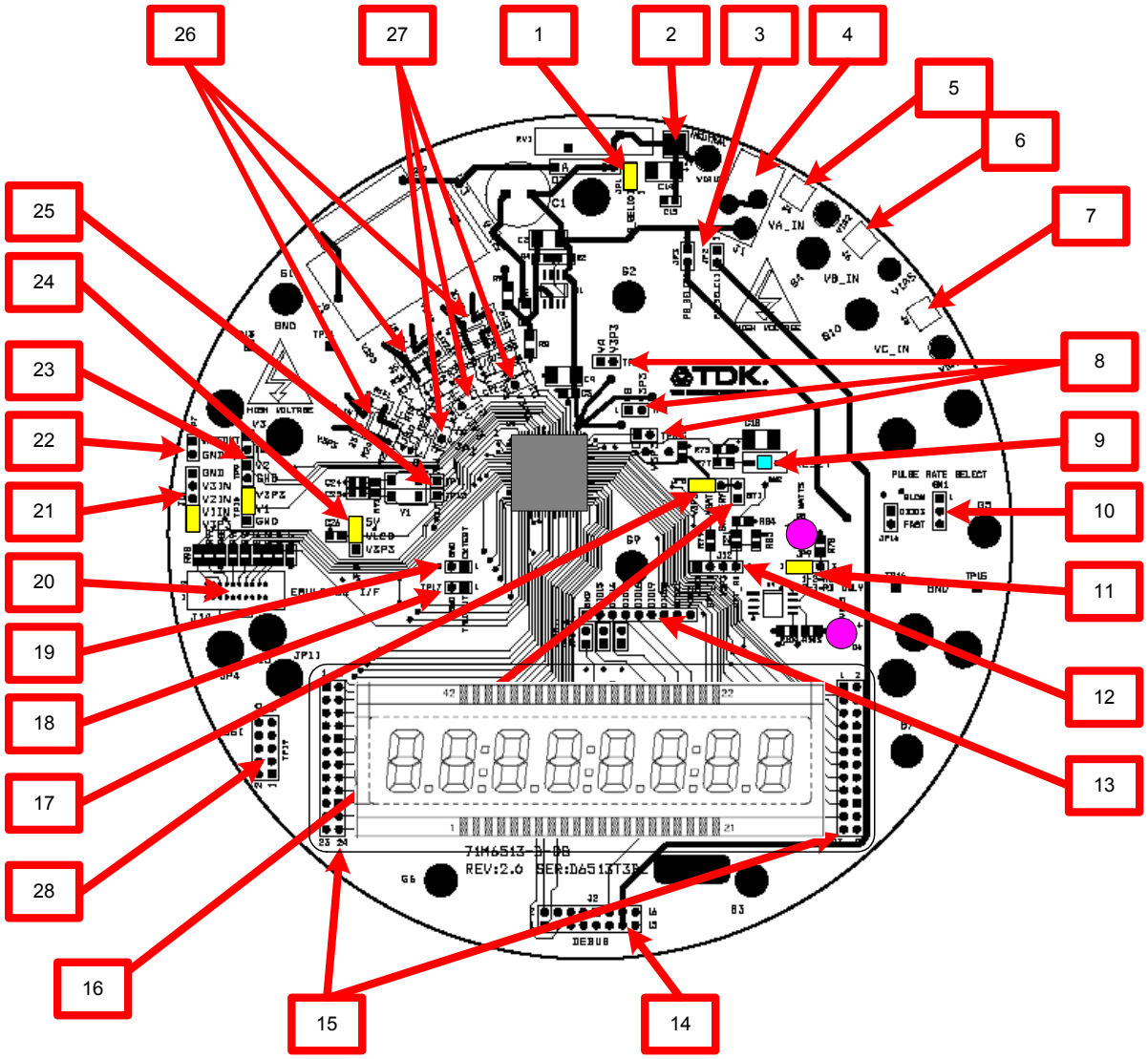


Figure 3-1: D6513T3B2 Demo Board - Board Description
(Default jumper settings indicated in yellow)

3.2 D6513T3C1 BOARD DESCRIPTION: JUMPERS, SWITCHES AND TEST POINTS

The items described in the following tables refer to the flags in Figure 3-2.

Item #	Reference Designator	Name	Use
1	JP1	PS_SEL[0]	Two-pin header. When the jumper is installed the on- board power supply (AC signal) is used to power the demo board. When not installed, the board must be powered by an external supply connected to J1. Normally installed.
2,8,9	TP2, TP4, TP6	VA, VB, and VC	Two pin header test points. One pin is the VA, VB or VC line voltage input to the IC and the other pin is ground.
3,5,6,7	J9, J4, J6, J8	Neutral, VA_IN, VB_IN, VC_IN 	VA_IN, VB_IN, and VC_IN are the line voltage inputs. Each point has a resistor divider that leads to the respective pin on the chip that is the voltage input to the ADC. These inputs are spade terminals on the bottom of the board. Caution: High Voltage! Do not touch these pins!
4	J1	5 Volt external supply	Plug for connecting the external 5 VDC power supply.
10	SW2	RESET	Chip reset switch: When the switch is pressed, the RESETZ pin is pulled low, which resets the IC into a known state.
11	J12	Test Point for the Optical Interface	Five-pin header allowing access to the OPT_RX and OPT_TX signals. Pins 1 and 2 can be used to connect a LED. Pins 3, 4, and 5 can be used to connect a photo-transistor.
12	D5	WATTS	Red LED. This LED functions as a pulse output for test and calibration (Wh).
13	JP6	GND, DIO3, V3P3	Three-pin header. This header can be used for general purpose DIO.
14	TP15, TP16	GND	GND test point
15	TP20	SEG26/DIO06	Two-pin header. This header can be used to pick up the signal for the VARS LED output.
16	TP21	SEG27/DIO07	Two-pin header. This header can be used to pick up the signal for the WATTS LED output.
17	D6	VARS	Red LED. This LED functions as a pulse output for test and calibration (VARh).
18,23	J11,J10	--	Two 2x12 headers for the LCD connection. The LCD daughter board plugs into the male (J10) and female (J11) headers.
19	JP12	DIO Test Point	9-pin header for monitoring DIO15 to DIO21.
20	JP13,JP14, JP15	DIO00, DIO01, DIO02	Three two-pin headers for monitoring the DIO00, DIO01, and DIO02 signals.

Table 3-4: D6513T3C1 Demo Board Description

Item #	Reference Designator	Name	Use
21	J2	DEBUG	2x8 pin male header for connecting the Debug Board.
22	TP17	TMUXOUT	Two-pin header. Pin 1 is the TMUXOUT signal.
24	TP19	SSI	5x2 header for access to the high-speed serial interface. One row is connected to GND.
25	TP18	CKTEST	Two-pin header. Pin 1 is the CKTEST signal.
26	JP8	V3P3, VBAT, BATTERY	Three-pin header that allows selection of power to the VBAT pin. When the jumper is placed between pins 1 and 2 **(default setting of the Demo Board),** VBAT is tied to the IC supply. When using an external battery, it must be connected to pin 2(+) and pin 3 (-).
27	JP10	5V, VLCD, V3P3	Three-pin header for selecting the voltage to the LCD. The top pin is 5V (supplied by the charge pump in the 71M6513/6513H) and the bottom pin is 3.3V. **The default setting for the jumper is 5V**.
28	J14	EMULATOR I/F	2x10 emulator connector compatible with the plug uses by the Signum ADM-51 ADM51 in-circuit emulator.
29	J17	EMULATOR I/F	Five-pin header providing an alternative connection for the Signum ADM51 in-circuit emulator.
30	J13	GND, V2IN, V1IN, V3P3	Four-pin header providing access to the V1 and V2 pins of the 71M6513/6513H. **Connect jumper to the bottom two pins as the default**.
31	TP7	VREFOUT	Two-pin header providing access to the VREF voltage of the 71M6513/6513H.
32	TP10	V3P3, V1_L, GND	Three-pin header providing access to the V1 pin of the 71M6513/6513H. Placing a jumper across pins 2 and 3 will disable the hardware watchdog timer of the 71M6513/6513H.
33	J16, J3, J5, J7	V3_IN, IA_IN, IB_IN, IC_IN	Two-pin headers mounted on the bottom side of the board. The signals from the current transformers should be connected to these headers. V3_IN is for connection of the CT used for the neutral current. IA_IN, IB_IN, IC_IN are V3P3-referenced, V3_IN is VBIAS referenced.
34	TP1,TP3,TP5	IA, IB, IC	

Table 3-5: D6513T3C1 Demo Board Description

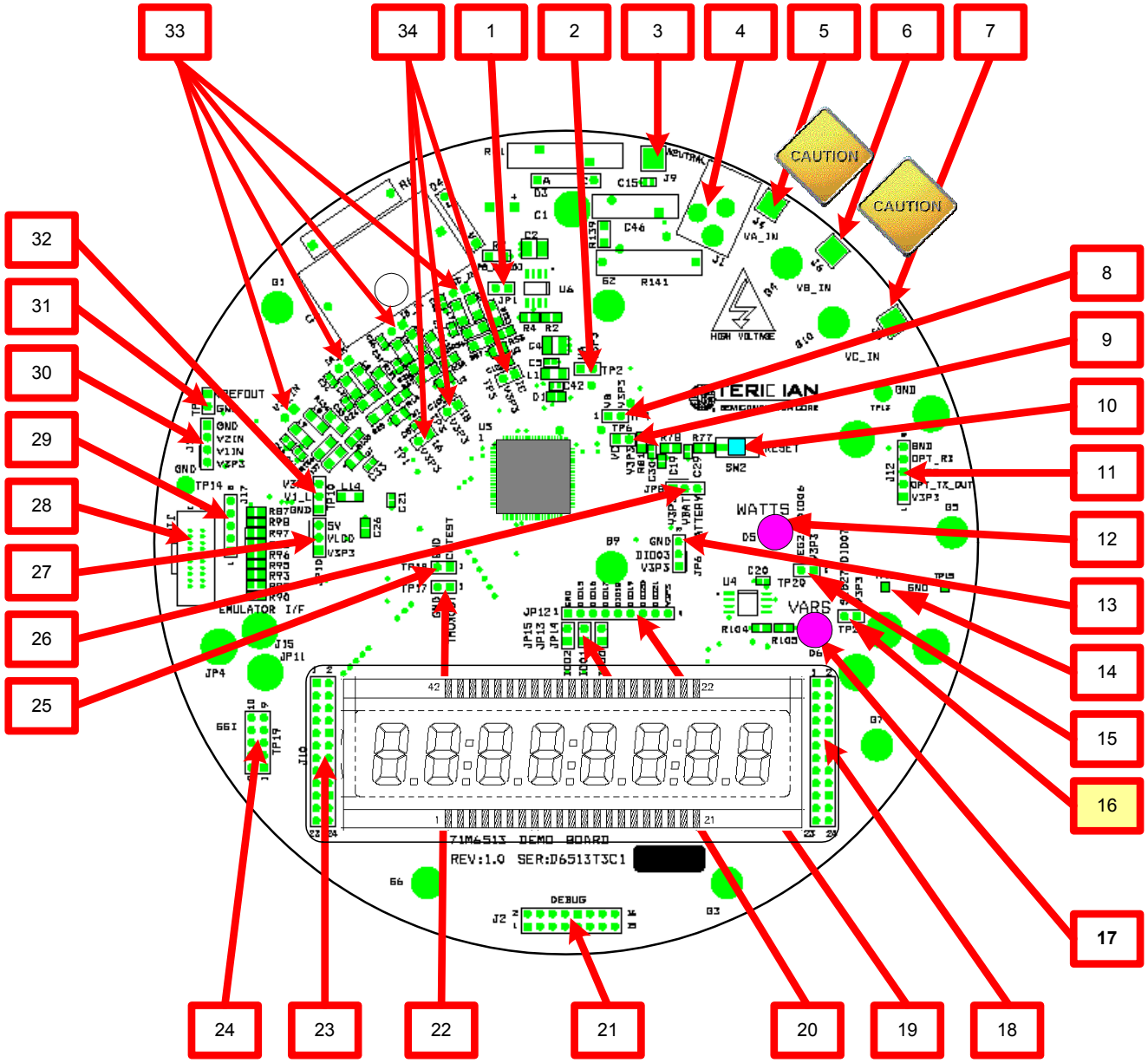


Figure 3-2: D6513T3C1 Demo Board - Board Description

3.3 D6513T3D2 BOARD DESCRIPTION: JUMPERS, SWITCHES AND TEST POINTS

The items described in the following tables refer to the flags in Table 3-6.

Item #	Reference Designator	Name	Use
1	U7	LCD	Display
2	U5	--	The 71M6513/71M6513H chip
3	--	--	Serial number field on silk screen
4	J17	Test Point for the Optical Interface	Five-pin header allowing access to the OPT_RX and OPT_TX signals. Pins 1 and 2 can be used to connect a LED. Pins 3, 4, and 5 can be used to connect a photo-transistor.
5	JP14	DIO 00	
6	JP13	DIO 01	
7	JP15	DIO 02	
8	TP13	GND	Ground test point
9	J14	EMULATOR I/F	Connector for emulator (ADM51) or programmer (TFP-1)
10	JP10	5V, VLCD, 3.3V	Voltage selector for LCD
11	TP11	CKTEST, GND TMUXOUT	Test header for accessing CKTEST and TMUXOUT pins
12	TP10	GND, V1, V3P3	Plugging a jumper between pins 2 and 3 disables the watch dog timer of the 71M6513 so that the emulator and/or flash programmer can be used.
13	J18	V3P3, V1IN, V2IN, GND	Plugging a jumper between pins 3 and 4 provides power to the resistor divider R83/R86 for V1.
14	TP7	GND, VREFOUT	This header provides access to the VREF pin.
15	TP8	V3, VBIAS	This header provides access to the signal of the current transformer used to measure the neutral current.
16	TP1	IA, V3P3	This header provides access to the signal of the current transformer used to measure the current in phase A.
17	TP3	IB, V3P3	This header provides access to the signal of the current transformer used to measure the current in phase B.
18	TP5	IC, V3P3	This header provides access to the signal of the current transformer used to measure the current in phase C.
19	J10	V3_IN	Three-pin header for connecting the CT of the neutral phase.
20	J3	IA_IN	Three-pin header for connecting the CT of the phase A. Pin 3 is GND and can be used to connect a cable shield.
21	J5	IB_IN	Three-pin header for connecting the CT of the phase B.

22	J7	IC_IN	Three-pin header for connecting the CT of the phase C.
Item #	**Reference Designator**	**Name**	**Use**
23	J9	NEUTRAL	Spade connector on the back side of the PCB for connecting the NEUTRAL wire.
24	JP16	VA_IN	Two-pin header. When the jumper is installed the on- board power supply (AC signal) is used to power the demo board. When not installed, the board must be powered by an external supply connected to J1. Normally installed.
25	J16 	LIVE	Line voltage input for phase C. This connector has a resistor divider that leads to the VC pin on the chip that is the voltage input to the ADC. This input is spade terminal on the bottom of the board. **Caution: High Voltage! Do not touch this pin!**
26	J6 	VB_IN	Line voltage input for phase B. This connector has a resistor divider that leads to the VB pin on the chip that is the voltage input to the ADC. This input is spade terminal on the bottom of the board. **Caution: High Voltage! Do not touch this pin!**
27	J8 	VA_IN	Line voltage input for phase A. This connector has a resistor divider that leads to the VA pin on the chip that is the voltage input to the ADC. This input is spade terminal on the bottom of the board. **Caution: High Voltage! Do not touch this pin!**
28	SW2	RESET	Chip reset switch: When the switch is pressed, the RESETZ pin is pulled low, which resets the IC into a known state.
29	D6	VARS	Red LED. This LED functions as a pulse output for test and calibration (VARh).
30	TP21	V3P3, DIO7, GND	This header provides access to the VARh pulse signal.
31	TP14	GND	Ground test point
32	TP20	V3P3, DIO6, GND	This header provides access to the Wh pulse signal.
33	D5	WATTS	Red LED. This LED functions as a pulse output for test and calibration (Wh).
34	J1	5 Volt external supply	DC plug for connecting the external 5 VDC power supply.
35	JP13,JP14, JP15	GND, DIO00, DIO01, …, DIO021	Nine-pin header for monitoring the DIO00, DIO01, … to DIO021 signals.
36	J4	DEBUG	8X2 header for connecting the Debug Board.

Table 3-6: D6513T3D2 Demo Board Description

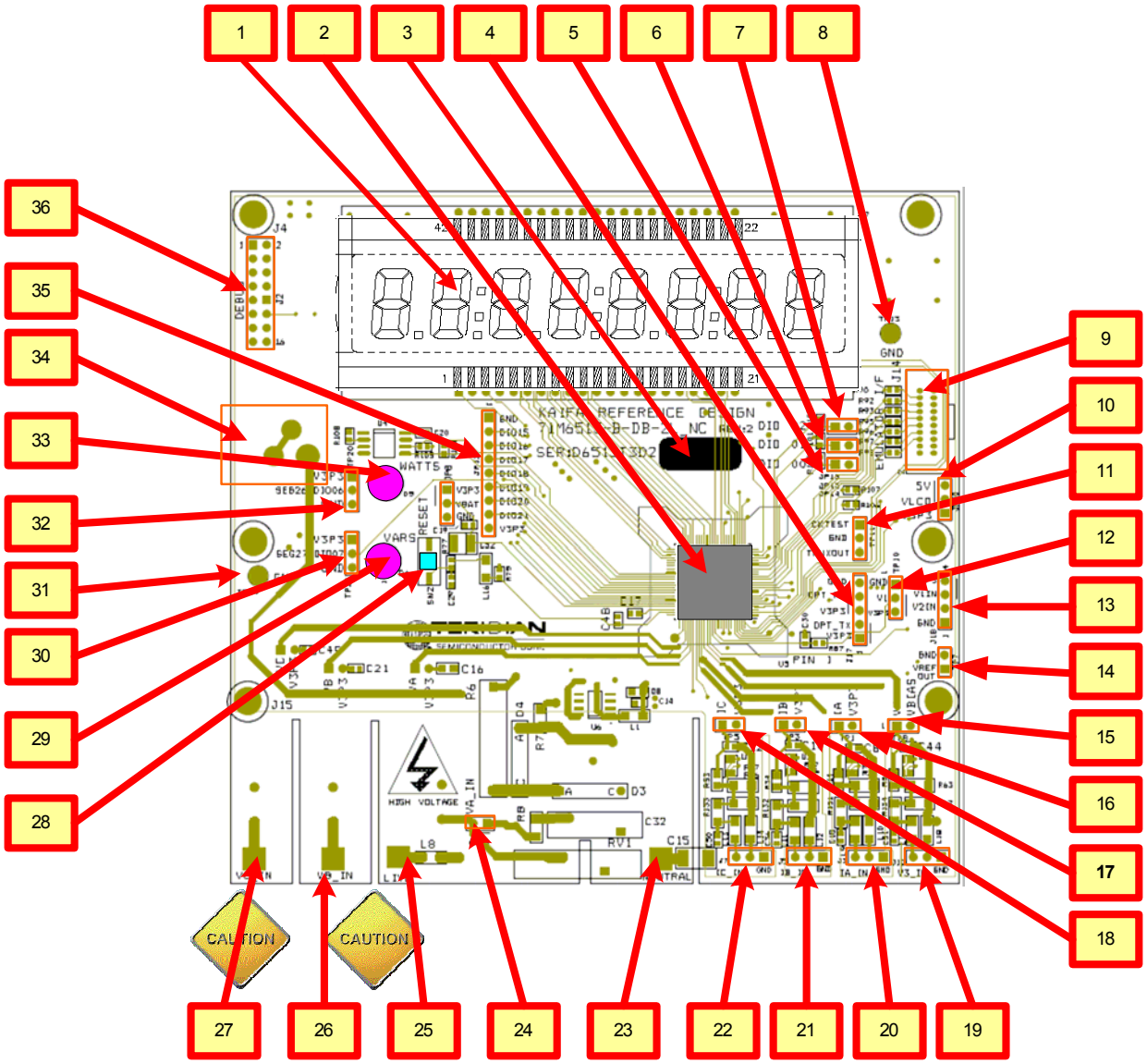


Figure 3-3: D6513T3D2 Demo Board - Board Description

3.4 BOARD HARDWARE SPECIFICATIONS (D6513T3B2, D6513T3C1)

PCB Dimensions

- Diameter 6.5" (165.1mm)
- Thickness 0.062" (1.6mm)
- Height w/ components and 3/8" spacers 1.5" (38.1mm)

Environmental

- Operating Temperature -40°…+85°C
  (function of crystal oscillator affected outside –10°C to +60°C)
- Storage Temperature -40°C…+100°C

Power Supply

- Using AC Input Signal 180V…700V rms
- DC Input Voltage (powered from DC supply) 5VDC ±0.5V
- Supply Current 25mA typical

Input Signal Range

- AC Voltage Signals (VA, VB, VC) 0…240V rms
- AC Current Signals (IA, IB, IC) from CT 0…0.25V p/p

Interface Connectors

- DC Supply Jack (J1) to Wall Transformer Concentric connector, 2.5mm
- Emulator (J14) 10x2 Header, 0.05" pitch
- Input Signals Spade Terminals and 0.1" headers on PCB bottom
- Debug Board (J2) 8x2 Header, 0.1" pitch
- Target Chip (U5) LQFP100 Socket
- SSI Connector (TP19) 5x2 Header, 0.1" pitch

Functional Specification

- Program Memory 64KByte FLASH memory
- NV memory 1Mbit serial EEPROM
- Time Base Frequency 32.768kHz, ±20PPM at 25°C
- Time Base Temperature Coefficient -0.04PPM/°C2 (max)

Controls and Displays

- Reset Button (SW2)
- Numeric Display 8-digit LCD, 8-segments per digit, 12.7mm character height, 89.0 x 17.7mm view area
- "Watts" red LED (D5)
- "VARS" red LED (D6)

Measurement Range

- Voltage 120…700 V rms (resistor division ratio 1:3,398)
- Current 1.7Ω termination for 2,000:1 CT input (200A)

3.5 BOARD HARDWARE SPECIFICATIONS (D6513T3D2)

PCB Dimensions

- Width, length — 5.25" x 5.0" (133.4mm x 127mm)
- Thickness — 0.062" (1.6mm)
- Height w/ components and 3/8" spacers — 1.5" (38.1mm)

Environmental

- Operating Temperature — -40°…+85°C
  (function of crystal oscillator affected outside –10°C to +60°C)
- Storage Temperature — -40°C…+100°C

Power Supply

- Using AC Input Signal — 180V…700V rms
- DC Input Voltage (powered from DC supply) — 5VDC ±0.5V
- Supply Current — 25mA typical

Input Signal Range

- AC Voltage Signals (VA, VB, VC) — 0…240V rms
- AC Current Signals (IA, IB, IC) from CT — 0…0.25V p/p

Interface Connectors

- DC Supply Jack (J1) to Wall Transformer — Concentric connector, 2.5mm
- Emulator (J14) — 10x2 Header, 0.05" pitch
- Input Signals — Spade Terminals and 0.1" headers on PCB bottom
- Debug Board (J2) — 8x2 Header, 0.1" pitch

Functional Specification

- Program Memory — 64KByte FLASH memory
- NV memory — 1Mbit serial EEPROM
- Time Base Frequency — 32.768kHz, ±20PPM at 25°C
- Time Base Temperature Coefficient — -0.04PPM/°C2 (max)

Controls and Displays

- Reset — Button (SW2)
- Numeric Display — 8-digit LCD, 8-segments per digit, 12.7mm character height, 89.0 x 17.7mm view area
- "WATTS" — red LED (D5)
- "VARS" — red LED (D6)

Measurement Range

- Voltage — 120…700 V rms (resistor division ratio 1:3,398)
- Current — 1.7Ω termination for 2,000:1 CT input (200A)

4

4 APPENDIX

This appendix includes the following documentation, tables and drawings:

71M6513/71M6513H Demo Board Description

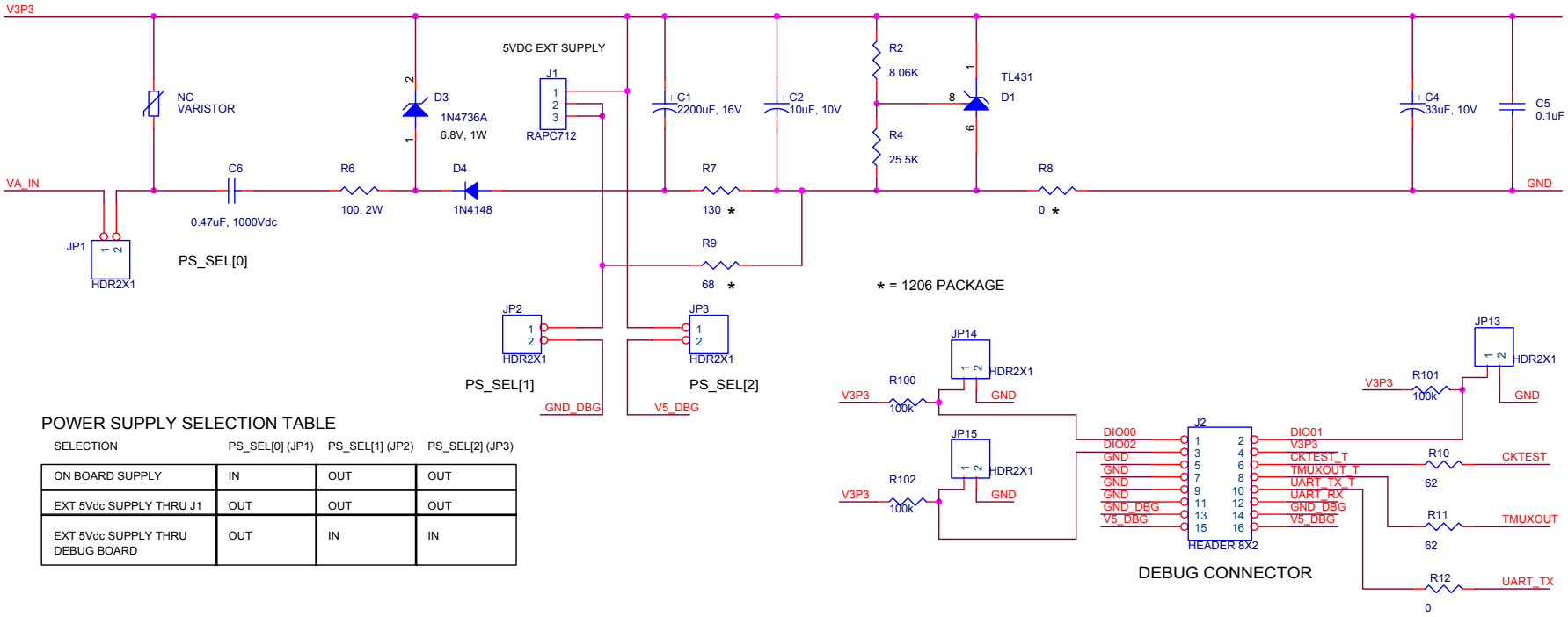
- D6513T3B2 Demo Board Electrical Schematic
- D6513T3B2 Demo Board Bill of Materials
- D6513T3B2 Demo Board PCB layers (copper, silk screen, top and bottom side)
- D6513T3C1 Demo Board Electrical Schematic
- D6513T3C1 Demo Board Bill of Materials
- D6513T3C1 Demo Board PCB layers (copper, silk screen, top and bottom side)
- D6513T3D2 Demo Board Electrical Schematic
- D6513T3D2 Demo Board Bill of Materials
- D6513T3D2 Demo Board PCB layers (copper, silk screen, top and bottom side)

Debug Board Description

- Debug Board Electrical Schematic
- Debug Board Bill of Materials
- Debug Board PCB layers (copper, silk screen, top and bottom side)

71M6513/71M6513H Description

- 71M6513/71M6513H Pin Description
- 71M6513/71M6513H Pin-out



POWER SUPPLY SELECTION TABLE

SELECTION	PS_SEL[0] (JP1)	PS_SEL[1] (JP2)	PS_SEL[2] (JP3)
ON BOARD SUPPLY	IN	OUT	OUT
EXT 5Vdc SUPPLY THRU J1	OUT	OUT	OUT
EXT 5Vdc SUPPLY THRU DEBUG BOARD	OUT	IN	IN

Figure 4-1: TERIDIAN D6513T3B2 Demo Board: Electrical Schematic 1/3

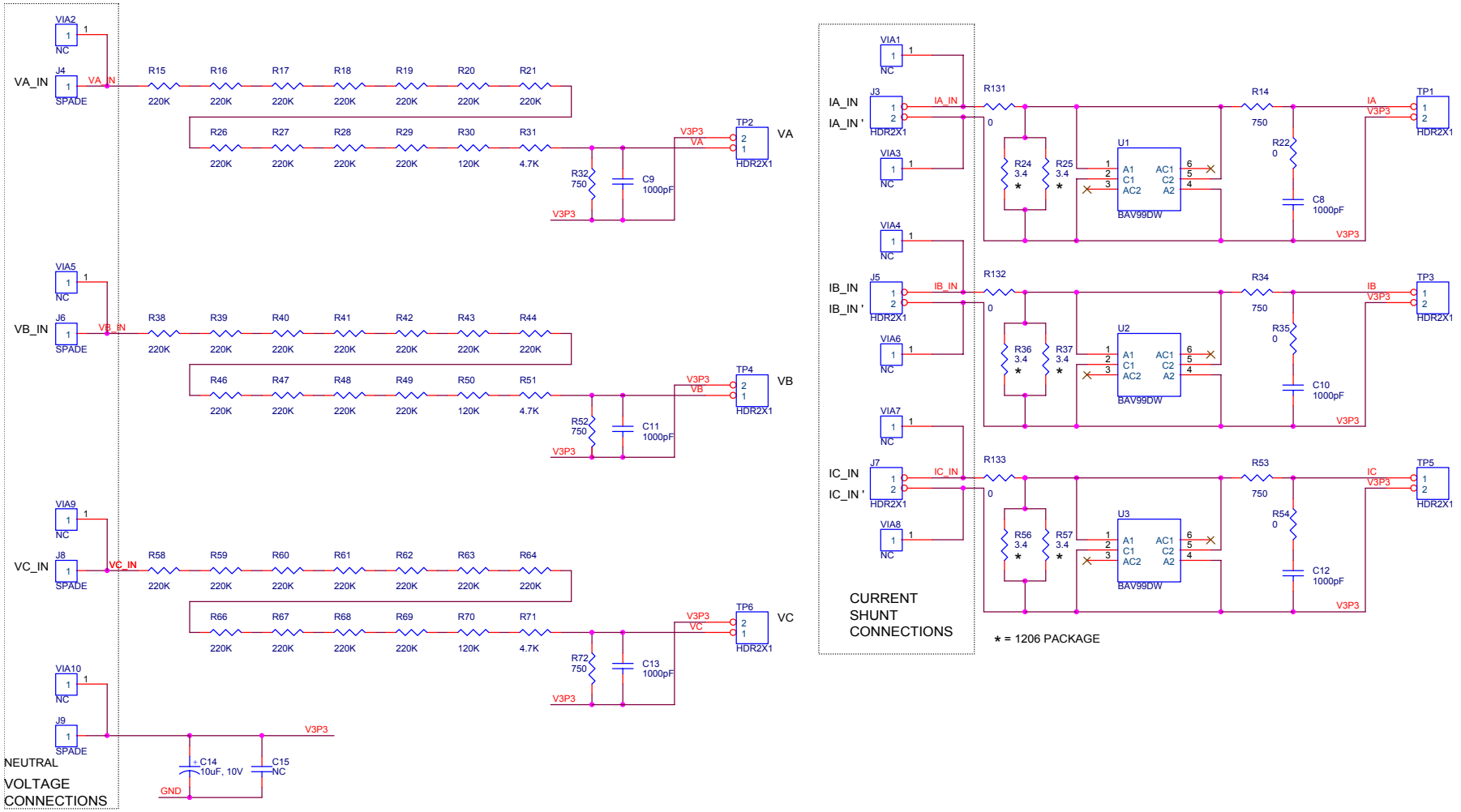


Figure 4-2: TERIDIAN D6513T3B2 Demo Board: Electrical Schematic 2/3

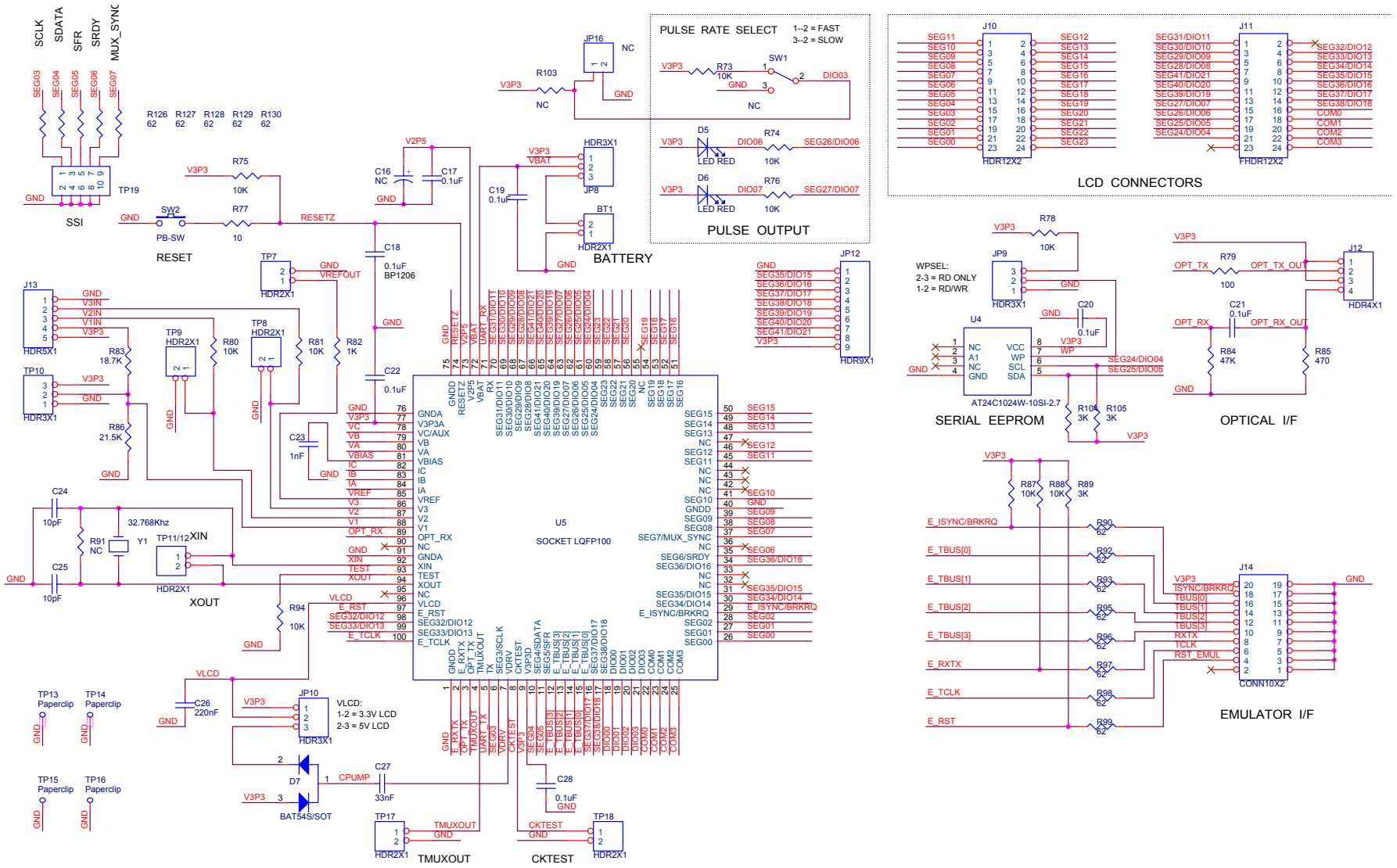


Figure 4-3: TERIDIAN D6513T3B2 Demo Board: Electrical Schematic 2/3

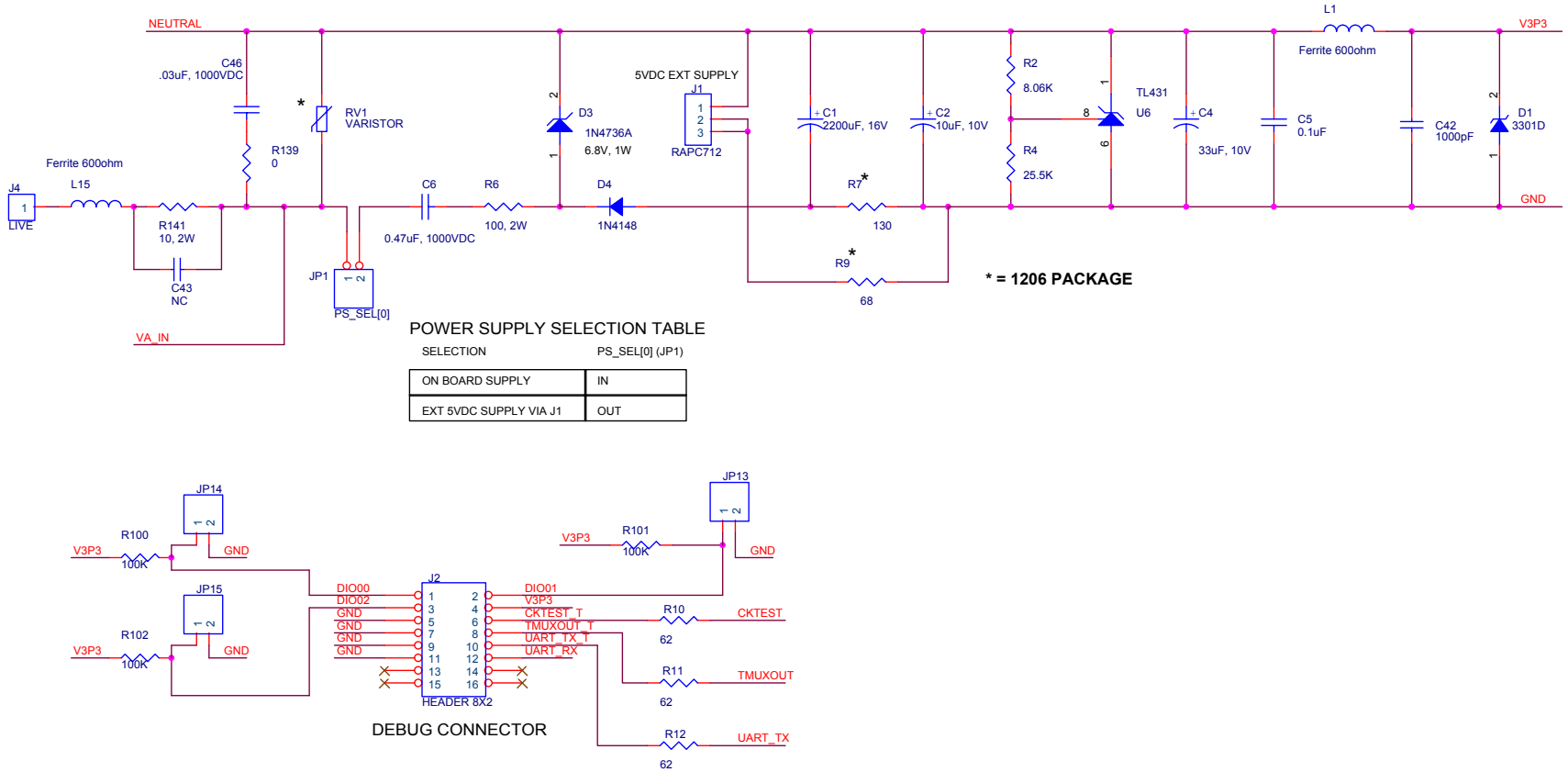


Figure 4-4: TERIDIAN D6513T3C1 Demo Board: Electrical Schematic 1/3

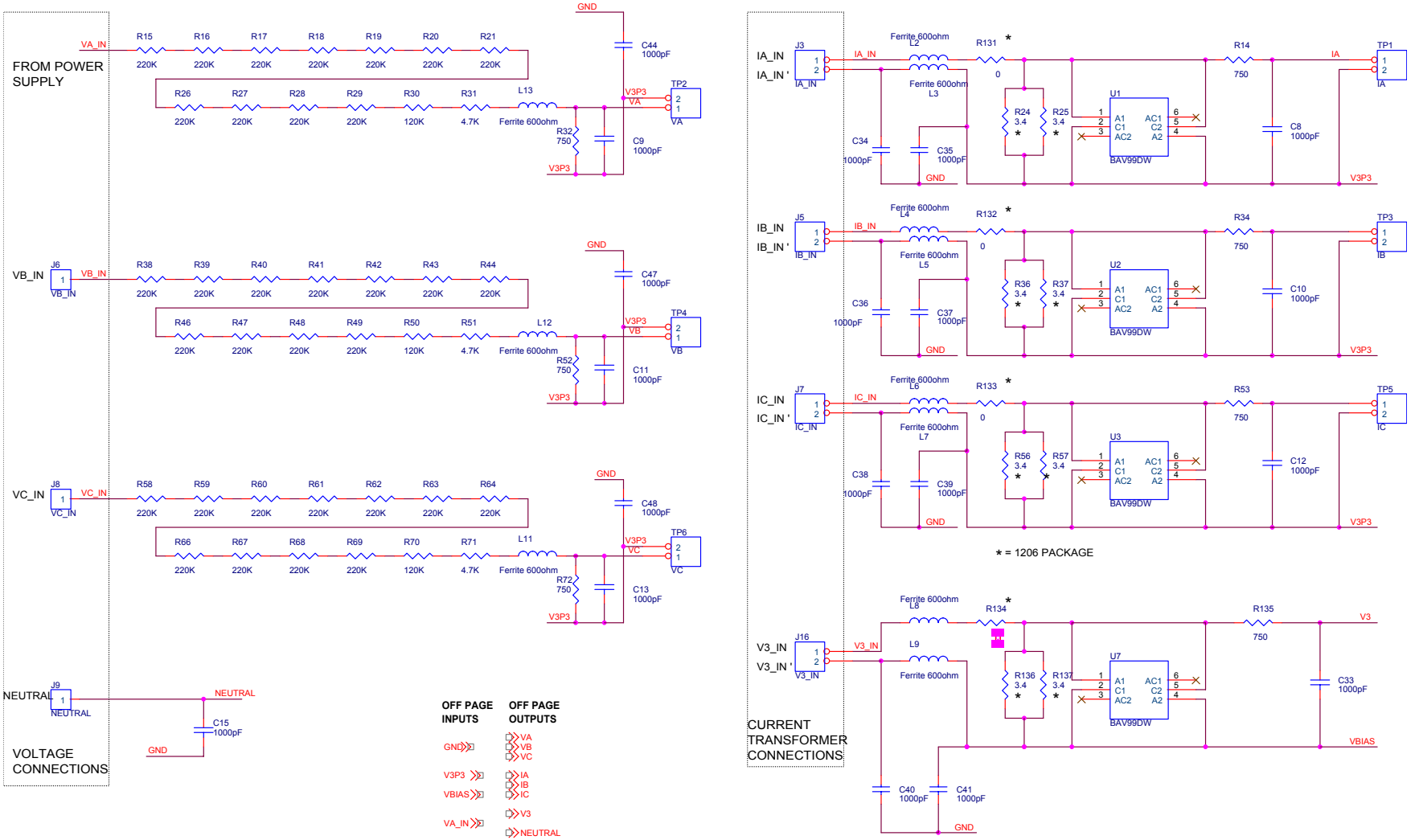


Figure 4-5: TERIDIAN D6513T3C1 Demo Board: Electrical Schematic 2/3

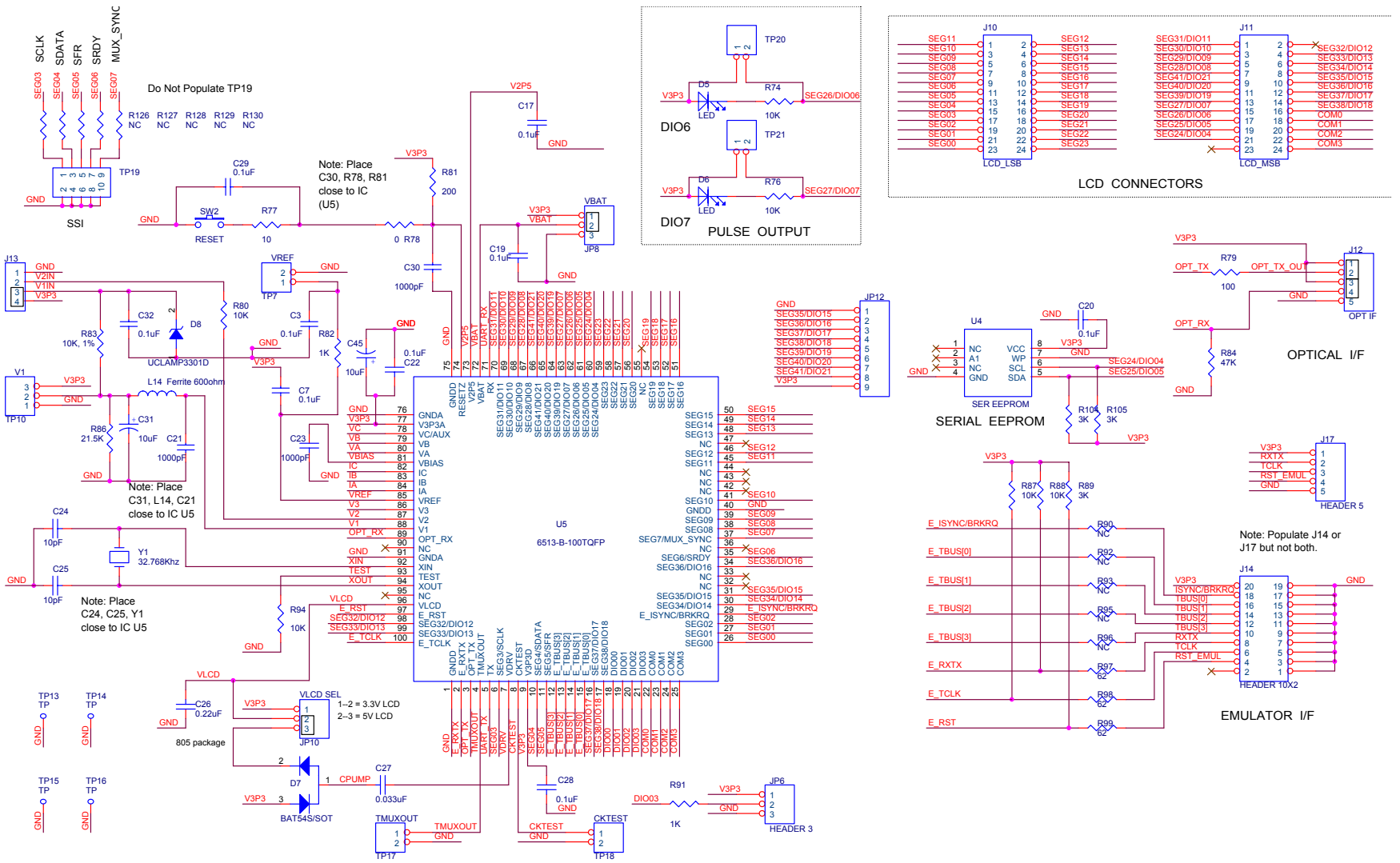


Figure 4-6: TERIDIAN D6513T3C1 Demo Board: Electrical Schematic 3/3

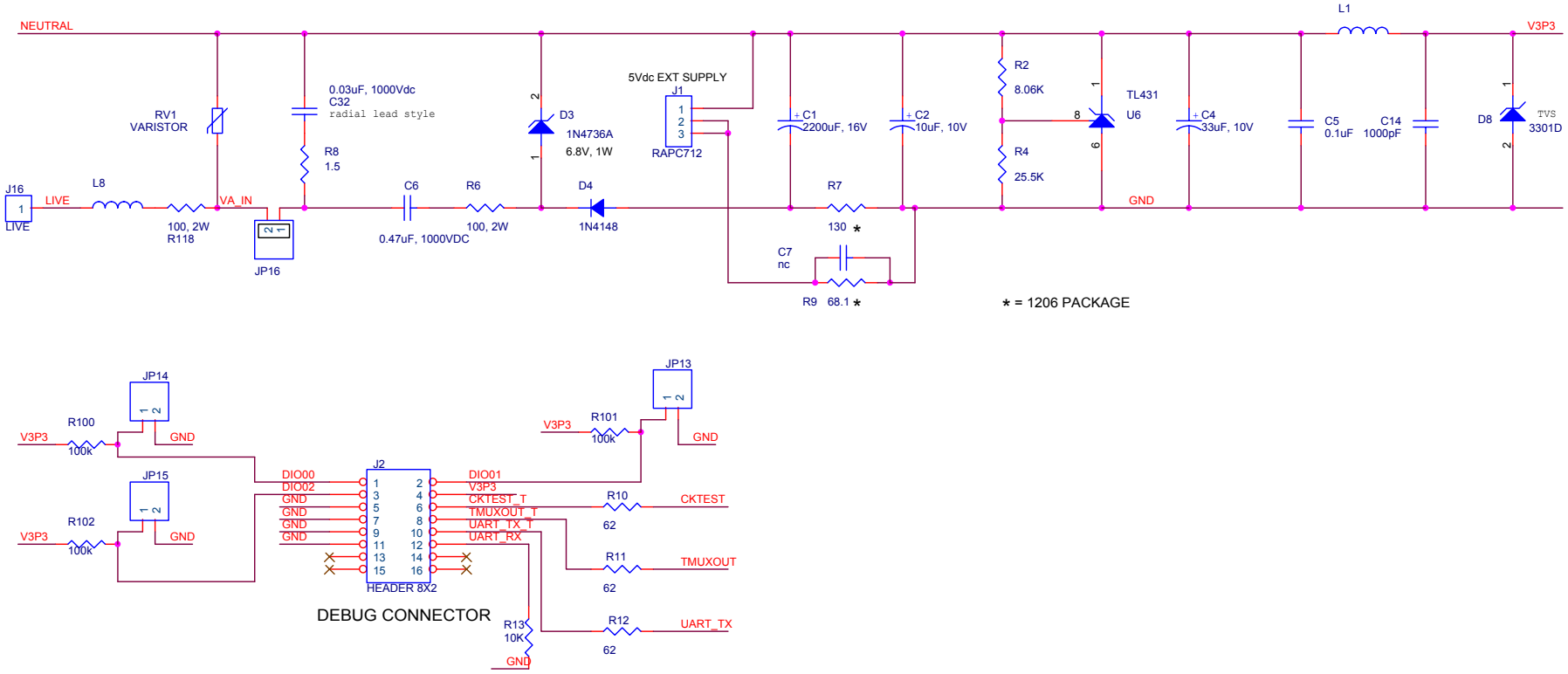


Figure 4-7: TERIDIAN D6513T3D2 Demo Board: Electrical Schematic 1/3

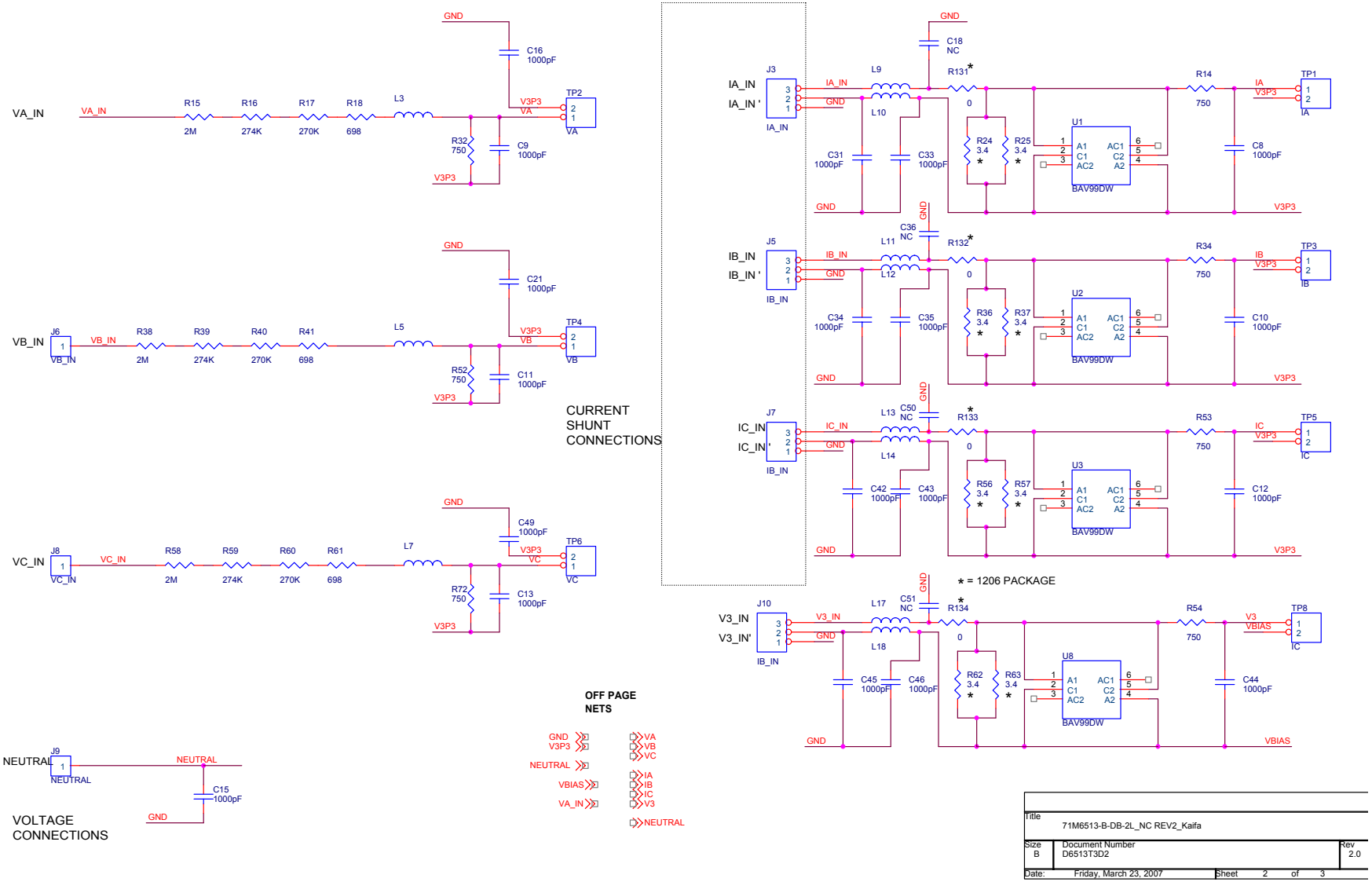


Figure 4-8: TERIDIAN D6513T3D2 Demo Board: Electrical Schematic 2/3

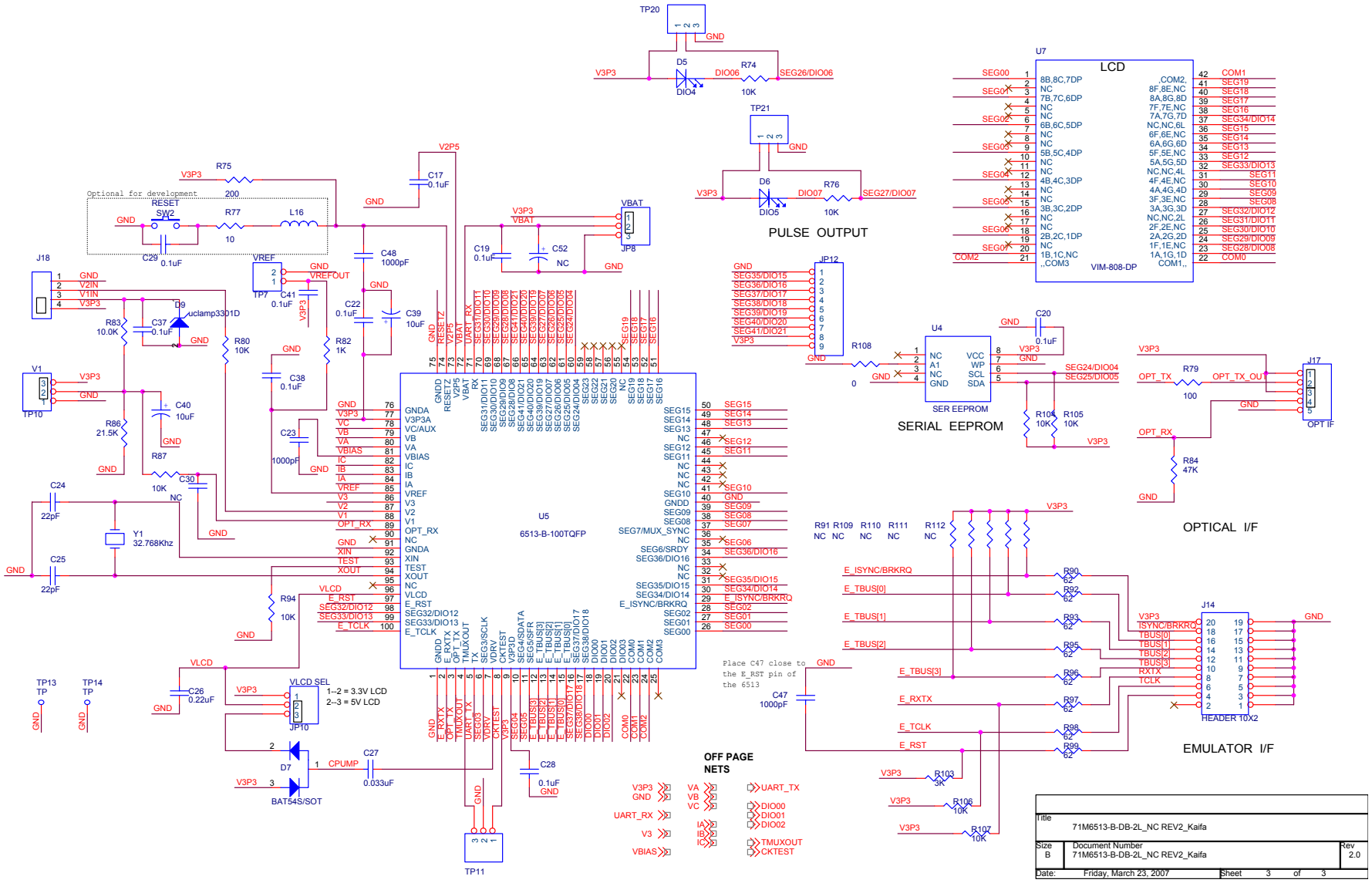


Figure 4-9: TERIDIAN D6513T3D2 Demo Board: Electrical Schematic 3/3

Item	Q	Reference	Part	PCB Footprint	Digi-Key/Mouser Part Number	Part Number	Manufacturer
1	1	C1	2200uF	radial	P5143-ND	ECA-1CM222	Panasonic
2	3	C2,C31,C45	10uF	RC1812	478-1672-1-ND	TAJB106K010R	AVX
3	10	C3,C5,C7,C17,C19,C20,	0.1uF	RC0603	445-1314-1-ND	C1608X7R1H104K	TDK
		C22,C28,C29,C32					
4	1	C4	33uF	RC1812	478-1688-1-ND	TAJB336K016R	AVX
5	1	C6	0.47uF		BC1918-ND	222 383 30474	BC Components
6	23	C8-C13,C15,C21,C23,C30,	1000pF	RC0603	445-1298-1-ND	C1608X7R2A102K	TDK
		C33-C42,C44,C47,C48					
7	2	C24,C25	10pF	RC0603	445-1269-1-ND	C1608COG1H100D	TDK
8	1	C26	0.22uF	RC0805	445-1350-1-ND	C2012X7R1H224K	TDK
9	1	C27	0.033uF	RC0603	PCC1769CT-ND	ECJ-1VB1E333K	Panasonic
10	1	C43	NC	RC1812			
11	1	C46	0.03uF	axial	75-125LS30	125LS30	Vishay
12	1	D1,D8	UCLAMP3301D	SOD-323	--	UCLAMP3301D.TCT	SEMTECH
13	1	D3	6.8V ZENER	D041	1N4736ADICT-ND	1N4736A-T	DIODES
14	1	D4	Switching Diode	D035	1N4148DICT-ND	1N4148-T	DIODES
15	1	D5,D6	LED	radial	67-1612-ND	SSL-LX5093SRC/E	LUMEX
16	1	D7	BAT54S/SOT	SOT23	BAT54SDICT-ND	BAT54S-7	DIODES
17	1	J1	5 VDC	RAPC712	SC1152-ND	RAPC712	Switchcraft
18	1	J2	HEADER 8X2	8X2PIN	S2011-36-ND	PZC36DAAN	Sullins
19	4	J3,J5,J7,J16	HEADER 2	2X1PIN	S1011-36-ND	PZC36SAAN	Sullins
20	4	J4,J6,J8,J9	Faston		A24747CT-ND	62395-1	AMP
21	1	J10	DUAL ROW 12X2 PIN MALE	12X2PIN	WM6824-ND	10-89-1241	Molex/Waldom
22	1	J11	DUAL ROW 12X2 PIN FEMALE	12X2PIN	S4312-ND	PPPC122LFBN	Sullins
23	2	J12,J17	HEADER 5	5X1PIN	S1011-36-ND	PZC36SAAN	Sullins
24	1	J13	HEADER 4	4X1PIN	S1011-36-ND	PZC36SAAN	Sullins
25	1	J14	10X2 CONNECTOR, 0.05"		A3210-ND	104068-1	AMP
26	4	JP1,JP13,JP14,JP15	HEADER 2	2X1PIN	S1011-36-ND	PZC36SAAN	Sullins
27	3	JP6,JP8,JP10	HEADER 3	3X1PIN	S1011-36-ND	PZC36SAAN	Sullins
28	1	JP12	HEADER 9	9X1PIN	S1011-36-ND	PZC36SAAN	Sullins
29	14	L1-L9,L11-L15	Ferrite bead, 600 Ohm	RC0805	445-1556-1-ND	MMZ2012S601A	TDK
30	1	RV1	VARISTOR	radial	581-VZD510XX	VE24M00511K	AVX
31	1	R2	8.06K, 1%	RC0805	311-8.06KCCT-ND	9C08052A8061FKHFT	Yageo
32	1	R4	25.5K, 1%	RC0805	311-25.5KCCT-ND	9C08052A2552FKHFT	Yageo
33	1	R6	100, 2W	axial	100W-2-ND	RSF200JB-100R	Yageo
34	1	R7	130, 1%	RC1206	311-130FCT-ND	9C12063A1300FGHFT	Yageo
35	1	R9	68, 1%	RC1206	311-68.0FCT-ND	9C12063A68R0FKHFT	Yageo
36	6	R10,R11,R12,R97,R98,R99	62	RC0805	P62ACT-ND	ERJ-6GEYJ620V	Panasonic
37	7	R14,R32,R34,R52,R53,R72,	750, 0.5%	RC0805	RR12P750DCT-ND	RR1220P-751-D	SUSUMU
		R135					
38	33	R15-R21,R26-R29,R39-R44,	220K, 0.1%	RC0805	RR12P220KBCT-ND	RR1220P-224-B-T5	SUSUMU
		R46-R49,R58,R59-R64,R66-R69					
39	8	R24,R25,R36,R37,R56,R57	3.4, 1%	RC1206	311-3.40FCT-ND	9C12063A3R40FGHFT	Yageo
		R136,R137					
40	3	R30,R50,R70	120K, 0.1%	RC0805	RR12P120KBCT-ND	RR1220P-124-B-T5	SUSUMU
41	3	R31,R51,R71	4.7K, 0.1%	RC0805	RR12P4.7KBCT-ND	RR1220P-472-B-T5	SUSUMU
42	6	R74,R76,R78,R87,R88,R94	10K	RC0805	P10KACT-ND	ERJ-6GEYJ103V	Panasonic
43	1	R77	10	RC0805	P10ACT-ND	ERJ-6GEYJ100V	Panasonic
44	1	R78	0	RC0805	P0.0ACT-ND	ERJ-6GEY0R00V	Panasonic
45	1	R79	100	RC0805	P100ACT-ND	ERJ-6GEYJ101J	Panasonic
46	1	R81	200	RC0805	P200ACT-ND	ERJ-6GEYJ201J	Panasonic
47	2	R82,R91	1K	RC0805	P1.0KACT-ND	ERJ-6GEYJ102V	Panasonic
48	1	R83	10.0K, 1%	RC0805	P10.0KCCT-ND	ERJ-6ENF1002V	Panasonic
49	1	R84	47K	RC0805	P47KACT-ND	ERJ-6GEYJ473V	Panasonic
50	1	R86	21.5K	RC0805	P21.5KCCT-ND	ERJ-6ENF2152V	Panasonic
51	10	R90,R92,R93,R95,R96,	NC	RC0805			
		R126-R130					
52	3	R100,R101,R102	100K	RC0805	P100KACT-ND	ERJ-6GEYJ104V	Panasonic
53	3	R89,R104,R105	3K	RC0805	P3.0KACT-ND	ERJ-6GEYJ302V	Panasonic
54	4	R131,R132,R133,R134	0	RC1206	P0.0ECT-ND	ERJ-8GEY0R00V	Panasonic
55	1	R139	1	RC1206	311-1.00FCT-ND	9C120631.00FGHFT	Yageo
56	1	R141	10, 2W	axial	10W-2-ND	RSF200JB-10R	Yageo
57	1	SW2	SWITCH		P8051SCT-ND	EVQ-PJX05M	Panasonic
58	12	TP1-TP7,TP9,TP17,TP18,TP20	TP	2X1PIN	S1011-36-ND	PZC36SAAN	Sullins
		TP21					
59	1	TP10	TP	3X1PIN	S1011-36-ND	PZC36SAAN	Sullins
60	2	TP13-TP14	Test Point		5011K-ND	5011	Keystone
61	1	TP15-TP16	Paper Clip GND				
62	1	TP19	HEADER 5X2	5X2PIN	S2011-36-ND	PZC36DAAN	Sullins
63	3	U1,U2,U3,U7	BAV99DW	SOT363	BAV99DWDICT-ND	BAV99DW-7	DIODES
64	1	U4	SER EEPROM		--	AT24C1024W-10SI-2.7	ATMEL
65	1	U5	71M6513 or 71M6513H	100TQFP	--	71M6513-IGT	TERIDIAN
66	1	at U5	100TQFP Socket	100TQFP	--	IC149-100-154S5	Yamaichi
67	1	U6	REGULATOR, 1%	SO8	296-1288-1-ND	TL431AIDR	Texas Instruments
68	1	Y1	32.768kHz		XC488CT-ND	ECS-.327-12.5-17-TR	ECS
69	1	LCD			153-1056-ND	VIM-808-DP-RC-S-HV	VARITRONIX

Table 4-1: D6513T3C1 Demo Board: Bill of Material

Item	Quantity	Reference	Part	Digi-Key P/N	P/N	Manufacturer
1	19	TP1,JP1,BT1,TP2,JP2,JP3,	HDR2X1	S1011-36-ND	PZC36SAAN	Sullins
		J3,TP4,J5,TP7,J7,TP8,TP9,				
		JP13,JP14,JP15,TP17,TP18,				
		TP11/12				
2	1	C1	2200uF, 16V	P5143-ND	ECA-1CM222	Panasonic
3	2	C14,C2	10uF, 10V	478-1672-1-ND	TAJB106K010R	AVX
4	1	C4	33uF, 10V	478-1667-1-ND	TAJB336K010R	AVX
5	7	C5,C17,C19-C22,C28	0.1uF	445-1349-1-ND	C2012X7R1H104K	TDK
6	1	C6	0.47uF, 1000Vdc	BC1918-ND	222 383 30474	BC Components
7	6	C8,C9,C10,C11,C12,C13	1000pF	PCC102BNCT-ND	ECJ-2VB1H102K	Panasonic
8	1	C15	NC	N/A	N/A	N/A
9	1	C16	NC	N/A	N/A	N/A
10	1	C18	0.1uF	PCC104BCT-ND	ECJ-3VB1H104K	Panasonic
11	1	C23	1nF	PCC102CGCT-ND	ECJ-2VC1H102J	Panasonic
12	2	C25,C24	10pF	PCC100CNCT-ND	ECJ-2VC1H100D	Panasonic
13	1	C26	0.22UF	445-1350-1-ND	C20212X7R1H224K	TDK
14	1	C27	33nF	PCC1834CT-ND	ECJ-2VB1H333K	Panasonic
15	1	D1	TL431	296-1288-1-ND	TL431AIDR	TI
16	1	D3	1N4736A	1N4736ADICT-ND	1N4736A-T	DIODES
17	1	D4	1N4148	1N4148DICT-ND	1N4148-T	DIODES
18	2	D5,D6	LED RED	67-1612-ND	SSL-LX5093SRC/E	Lumex
19	1	D7	BAT54S/SOT	BAT54SDICT-ND	BAT54S-7	DIODES
20	1	JP4	NC	N/A	N/A	N/A
21	4	JP8,JP9,TP10,JP10	HDR3X1	S1011-36-ND	PZC36SAAN	Sullins
22	1	JP11	NC	N/A	N/A	N/A
23	1	JP12	HDR9X1	S1011-36-ND	PZC36SAAN	Sullins
24	1	JP16	NC	N/A	N/A	N/A
25	1	J1	RAPC712	SC1152-ND	RAPC712	Switchcraft
26	1	J2	HEADER 8X2	S2011-36-ND	PZC36DAAN	Sullins
27	4	J4,J6,J8,J9	SPADE	A24747CT-ND	62395-1	
28	1	J10	HDR12X2	WM6824-ND	10-89-1241	Waldom
29	1	J11	FHDR12X2	S4312-ND	PPPC122LFBN	Sullins
30	1	J12	HDR4X1	S1011-36-ND	PZC36SAAN	Sullins
31	1	J13	HDR5X1	S1011-36-ND	PZC36SAAN	Sullins
32	1	J14	CONN10X2	A3210-ND	104068-1	AMP
33	1	J15	NC	N/A	N/A	N/A
34	1	NC	VARISTOR	N/A	N/A	N/A
35	1	R2	8.06K	311-8.06KCCT-ND	9C08052A8061FKHFT	Yageo
36	1	R4	25.5K	311-25.5KCCT-ND	9C08052A2552FKHFT	Yageo
37	1	R6	100, 2W	100W-2-ND	RSF200JB-100R	Yageo
38	1	R7	130	311-130FCT-ND	9C12063A1300FGHFT	Yageo
39	4	R8,R131,R132,R133	0	P0.0ECT-ND	ERJ-8GEY0R00V	Panasonic
40	1	R9	68	311-68.0FCT-ND	9C12063A68R0FKHFT	Yageo
41	15	R10,R11,R90,R92,R93,R95,	62	P62ACT-ND	ERJ-6GEYJ620V	Panasonic
		R96-R99,R126-R130				
42	4	R12,R22,R35,R54	0	P0.0ACT-ND	ERJ-6GEY0R00V	Panasonic
43	6	R14,R32,R34,R52,R53,R72	750	RR12P750DCT-ND	RR1220P-751-D	SUSUMU
44	33	R15-R21,R26-R29,R38-R44,	220K	RR08P220KBCT-ND	RR0816P-224-B-T5	SUSUMU
		R46-R49,R58-R64,R66-R69				
45	6	R24,R25,R36,R37,R56,R57	3.4	311-3.40FCT-ND	9C12063A3R4FGHFT	Yageo
46	3	R30,R50,R70	120K	RR12P120KBCT-ND	RR1220P-124-B-T5	SUSUMU
47	3	R31,R51,R71	4.7K	RR12P4.7KBCT-ND	RR1220P-472-B-T5	SUSUMU
48	8	R73-R78,R80,R81,R87,R88,R94	10K	P10KACT-ND	ERJ-GEYJ103V	Panasonic
49	1	R77	10	P10ACT-ND	ERJ-GEYJ100V	Panasonic
50	1	R79	100	P100ACT-ND	ERJ-6GEYJ101J	Panasonic
51	3	R82	1K	P1.0KACT-ND	ERJ-GEYJ102V	Panasonic
52	1	R83	18.7K	P18.7KCCT-ND	ERJ-6ENF1872V	Panasonic
53	1	R84	47K	P47KACT-ND	ERJ-6GEYJ473V	Panasonic
54	1	R85	470	P470ACT-ND	ERJ-6GEYJ471V	Panasonic
55	1	R86	21.5K	P21.5KCCT-ND	ERJ-6ENF2152V	Panasonic
56	4	R103	NC	N/A	N/A	N/A
57	3	R89,R104,R105	3K	P3.0KACT-ND	ERJ-GEYJ302V	Panasonic
58	1	R91	NC	N/A	N/A	N/A
59	3	R100,R101,R102	100k	P100KACT-ND	ERJ-6GEYJ104V	Panasonic
60	1	SW1	NC	N/A	N/A	N/A
61	1	SW2	PB-SW	P8051SCT-ND	EVQ-PJX05M	Panasonic
62	3	TP3,TP5,TP6	HDR2X1	S1011-36-ND	PNTEST	Sullins
63	4	TP13,TP14,TP15,TP16	Paperclip	N/A	N/A	TDK
64	1	TP19	HDR5X2	S2011-ND	PZC36DAAN	Sullins
65	3	U1,U2,U3	BAV99DW	BAV99DWDICT-ND	BAV99DW-7	DIODES
66	1	U4	AT24C1024W-10SI-2.7	AT24C1024W-10SI-2.7-ND	AT24C1024W-10SI-2.7	ATMEL
67	1	U5	SOCKET LQFP100	N/A	N/A	Yamaichi
68	1	Y1	32.768Khz	XC488CT-ND	ECS-.327-12.5-17-TR	ECS

Table 4-2: D6513T3B2 Demo Board: Bill of Material

Item	Q	Reference	Part	PCB Footprint	Digi-Key/Mouser Part Number	Part Number	Manufacturer
1	1	C1	2200uF	radial	P5143-ND	ECA-1CM222	Panasonic
2	3	C2,C39,C40	10uF	RC1812	478-1672-1-ND	TAJB106K010R	AVX
3	1	C4	33uF	RC1812	478-1688-1-ND	TAJB336K016R	AVX
4	10	C5,C17,C19,C20,C22,C28,C29,	0.1uF	RC0603	445-1314-1-ND	C1608X7R1H104K	TDK
		C37,C38,C41					
5	1	C6	0.47uF	axial	75-F1778410M2KCT0	222 383 30474	Vishay
6	6	C7,C18,C30,C36,C50,C51	NC	RC0603			
7	21	C8-C14,C23,C31,C33,C34,C35	1000pF	RC0603	445-1298-1-ND	C1608X7R2A102K	TDK
		C42-C49					
8	1	C15	1000pF	RC1206	399-3446-1-ND	C1812C102KDRACTU	
9	1	C16	1000pF	RC0805	445-1337-1-ND	C2012X7R2A102K	
10	2	C24,C25	22pF	RC0603	445-1273-1-ND	C1608C0G1H220J	TDK
11	1	C26	0.22uF	RC0603	445-1318-1-ND	C1608X7R1C224K	TDK
12	1	C27	0.033uF	RC0603	PCC1769CT-ND	ECJ-1VB1E333K	Panasonic
13	1	C32	0.03uF	axial	75-125LS30-R	125LS30-R	Vishay
14	1	C52	NC	RC1812			
15	2	D1,D8	UCLAMP3301D	SOD-323	--	UCLAMP3301D.TCT	SEMTECH
16	1	D3	6.8V ZENER	D041	1N4736ADICT-ND	1N4736A-T	DIODES
17	1	D4	Switching Diode	D035	1N4148DICT-ND	1N4148-T	DIODES
18	2	D5,D6	LED	radial	404-1104-ND	H-3000L	Stanley
19	1	D7	BAT54S/SOT	SOT23	BAT54S-FDICT-ND	BAT54S-F-7	DIODES
20	2	D8,D9	UCLAMP3301D	SOD-323	--	UCLAMP3301D.TCT	SEMTECH
21	1	J1	DC jack (2.5mm)	RAPC712	502-RAPC712X	RAPC712X	Switchcraft
22	1	J2	HEADER 8X2	8X2PIN	S2011E-36-ND	PZC36DAAN	Sullins
23	4	J3,J5,J7,J10	HEADER 2	2X1PIN	S1011E-36-ND	PZC36SAAN	Sullins
24	4	J6,J8,J9,J16	Spade Terminal		A24747CT-ND	62395-1	AMP
25	1	J14	10X2 CONNECTOR, 0.05"		571-5-104068-1	5-104068-1	AMP
26	1	J17	HEADER 5	5X1PIN	S1011E-36-ND	PZC36SAAN	Sullins
27	1	J18	HEADER 4	4X1PIN	S1011E-36-ND	PZC36SAAN	Sullins
28	2	JP8,JP10	HEADER 3	3X1PIN	S1011E-36-ND	PZC36SAAN	Sullins
29	1	JP12	HEADER 9	9X1PIN	S1011E-36-ND	PZC36SAAN	Sullins
30	4	JP13,JP14,JP15,JP16	HEADER 2	2X1PIN	S1011E-36-ND	PZC36SAAN	Sullins
31	14	L1,L3,L5,L7-L14,L16,L17,L18	Ferrite bead, 600 Ohm	RC0805	445-1556-1-ND	MMZ2012S601A	TDK
32	1	RV1	VARISTOR	radial	594-2381-594-55116	238159455116	Vishay
33	1	R2	8.06K, 1%	RC0603	P8.06KHCT-ND	ERJ-3EKF8061V	Panasonic
34	1	R4	25.5K, 1%	RC0603	P25.5KHCT-ND	ERJ-3EKF2552V	Panasonic
35	2	R6,R118	100, 2W	axial	100W-2-ND	RSF200JB-100R	Yageo
36	1	R7	130, 1%	RC1206	311-130FRCT-ND	RC1206FR-071300L	Yageo
37	1	R8	1.5	RC1206	P1.5ECT-ND	ERJ-8GEYJ1R5V	Panasonic
38	1	R9	68, 1%	RC1206	311-68.0FRCT-ND	RC1206FR-0768R0L	Yageo
39	10	R10,R11,R90,R92,R93,R95-R99	62	RC0603	P62GCT-ND	ERJ-3GEYJ620V	Panasonic
40	2	R12,R108	0	RC0603	P0.0GCT-ND	ERJ-3GEY0R00V	Panasonic
41	8	R13,R74,R76,R80,R87,R94,	10K	RC0603	P10KGCT-ND	ERJ-3GEYJ103V	Panasonic
		R104,R105,R106,R107					
42	7	R14,R32,R34,R52,R53,R72,	750, 1%	RC0805	P750CCT-ND	ERJ-6ENF7500V	Panasonic
		R135					
43	3	R15,R38,R58	2M, 1%	axial	71-RN65DF-2.0M	RN65D2004FB14	Dale
44	3	R16,R39,R59	274K, 1%	RC0805	P274KCCT-ND	ERJ-6ENF2743V	Panasonic
45	3	R17,R40,R60	270K, 1%	RC0805	RHM270KCCT-ND	MCR10EZHF2703	Rohm
46	3	R18,R41,R61	698, 1%	RC0805	P698CCT-ND	ERJ-6ENF6980V	Panasonic
47	8	R24,R25,R36,R37,R56,R57	3.4, 1%	RC1206	311-3.40FRCT-ND	RC1206FR-073R40L	Yageo
		R62,R63					
48	1	R75	200	RC0603	P200GCT-ND	ERJ-3GEYJ201V	
49	1	R77	10	RC0603	P10GCT-ND	ERJ-3GEYJ100V	Panasonic
50	1	R79	100	RC0603	P100GCT-ND	ERJ-3GEYJ101V	Panasonic
51	1	R82	1K	RC0603	P1.0KGCT-ND	ERJ-3GEYJ102V	Panasonic
52	1	R83	10.0K, 1%	RC0603	P10.0KHCT-ND	ERJ-3EKF1002V	Panasonic
53	1	R84	47K	RC0603	P47KGCT-ND	ERJ-3GEYJ473V	Panasonic
54	1	R86	21.5K	RC0603	P25.5KHCT-ND	ERJ-3EKF2552V	Panasonic
55		R91,R109-R112	NC	RC0603			
56	3	R100,R101,R102	100K	RC0603	P100KGCT-ND	ERJ-3GEYJ104V	Panasonic
57	1	R103	3K	RC0603	P3.0KGCT-ND	ERJ-3GEYJ302V	Panasonic
58	4	R131,R132,R133,R134	0	RC1206	P0.0ECT-ND	ERJ-8GEY0R00V	Panasonic
59	1	SW2	SWITCH		P8051SCT-ND	EVQ-PJX05M	Panasonic
60	8	TP1-TP8	TP	2X1PIN	S1011E-36-ND	PZC36SAAN	Sullins
61	4	TP10,TP11,TP20,TP21	TP	3X1PIN	S1011E-36-ND	PZC36SAAN	Sullins
62	2	TP13,TP14	Test Point		5011K-ND	5011	Keystone
63	3	U1,U2,U3,U8	BAV99DW	SOT363	BAV99DW-FDICT-ND	BAV99DW-7-F	DIODES
64	1	U4	SER EEPROM		AT24C1024W10SU2.7-ND	AT24C1024W-10SU-2.7	ATMEL
65	1	U5	71M6513 or 71M6513H	100TQFP	--	71M6513-IGT	TERIDIAN
66	1	U6	REGULATOR, 1%	SO8	296-1288-1-ND	TL431AIDR	Texas Instruments
67	1	U7	LCD		153-1056-ND	VIM-808-DP-RC-S-HV	VARITRONIX
68	1	Y1	32.768kHz		XC1195CT-ND	ECS-.327-12.5-17X-TR	ECS

Table 4-3: D6513T3D2 Demo Board: Bill of Material

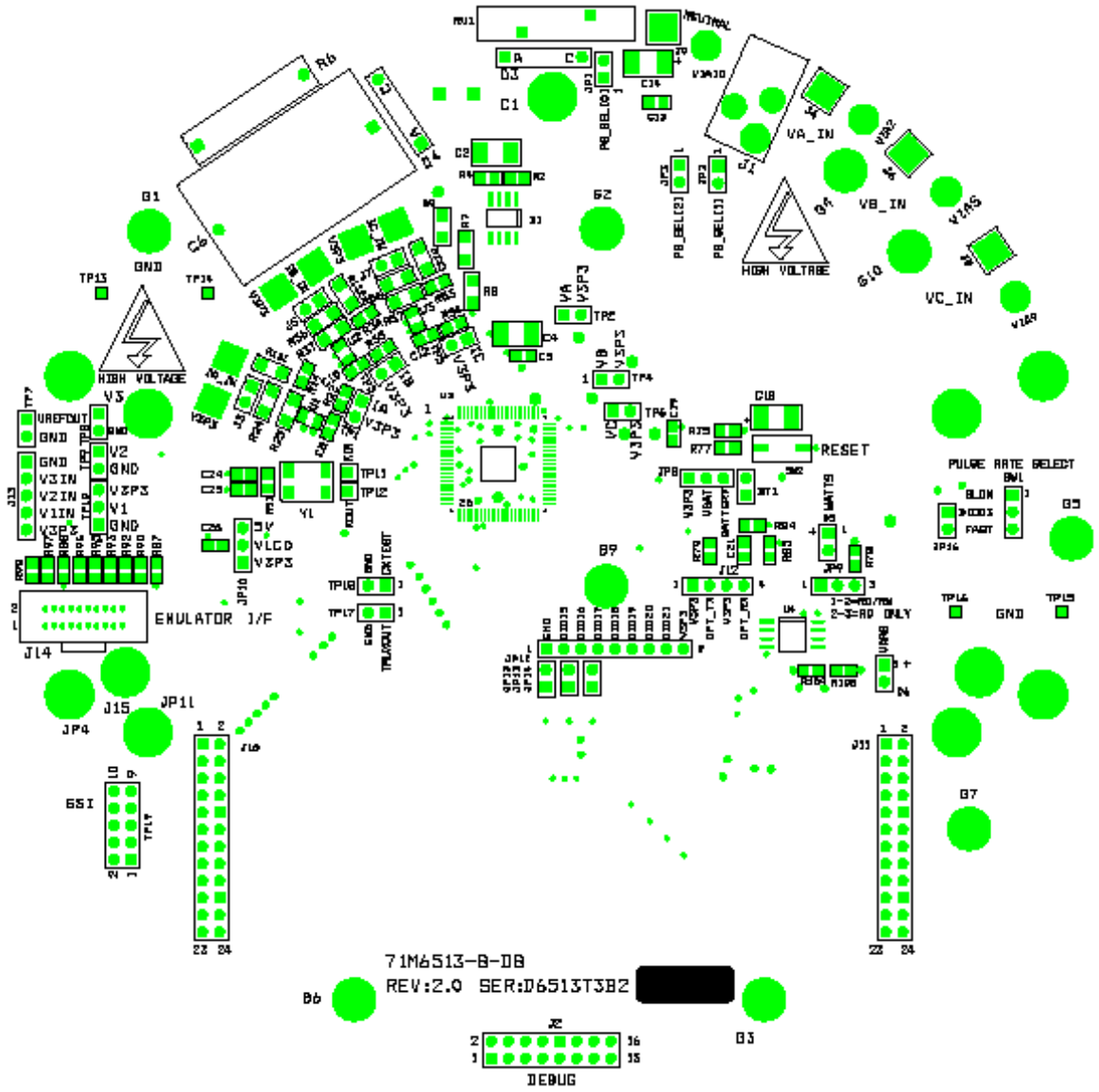


Figure 4-10: TERIDIAN D6513T3B2 Demo Board: Top View

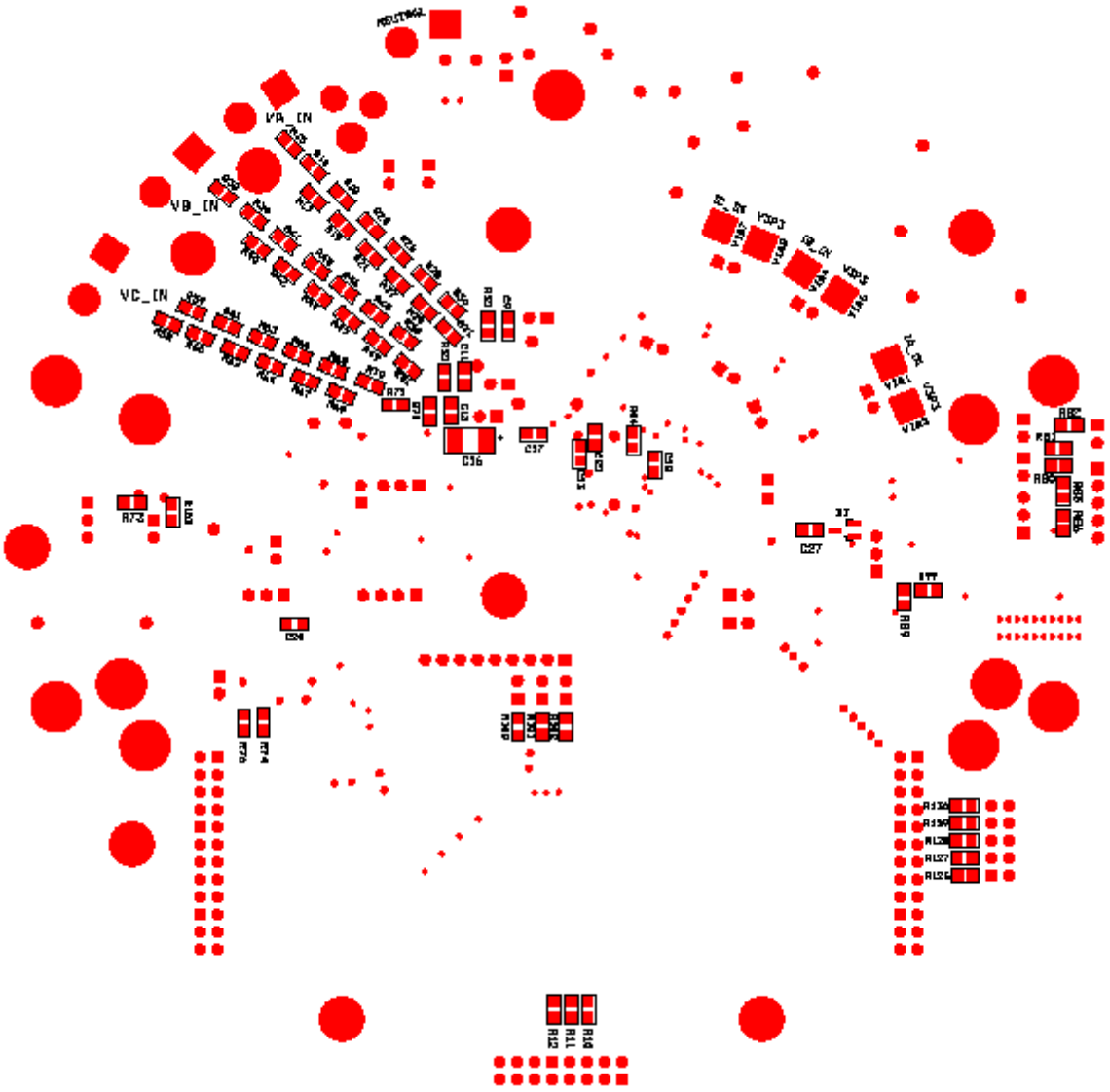


Figure 4-11: TERIDIAN D6513T3B2 Demo Board: Bottom View

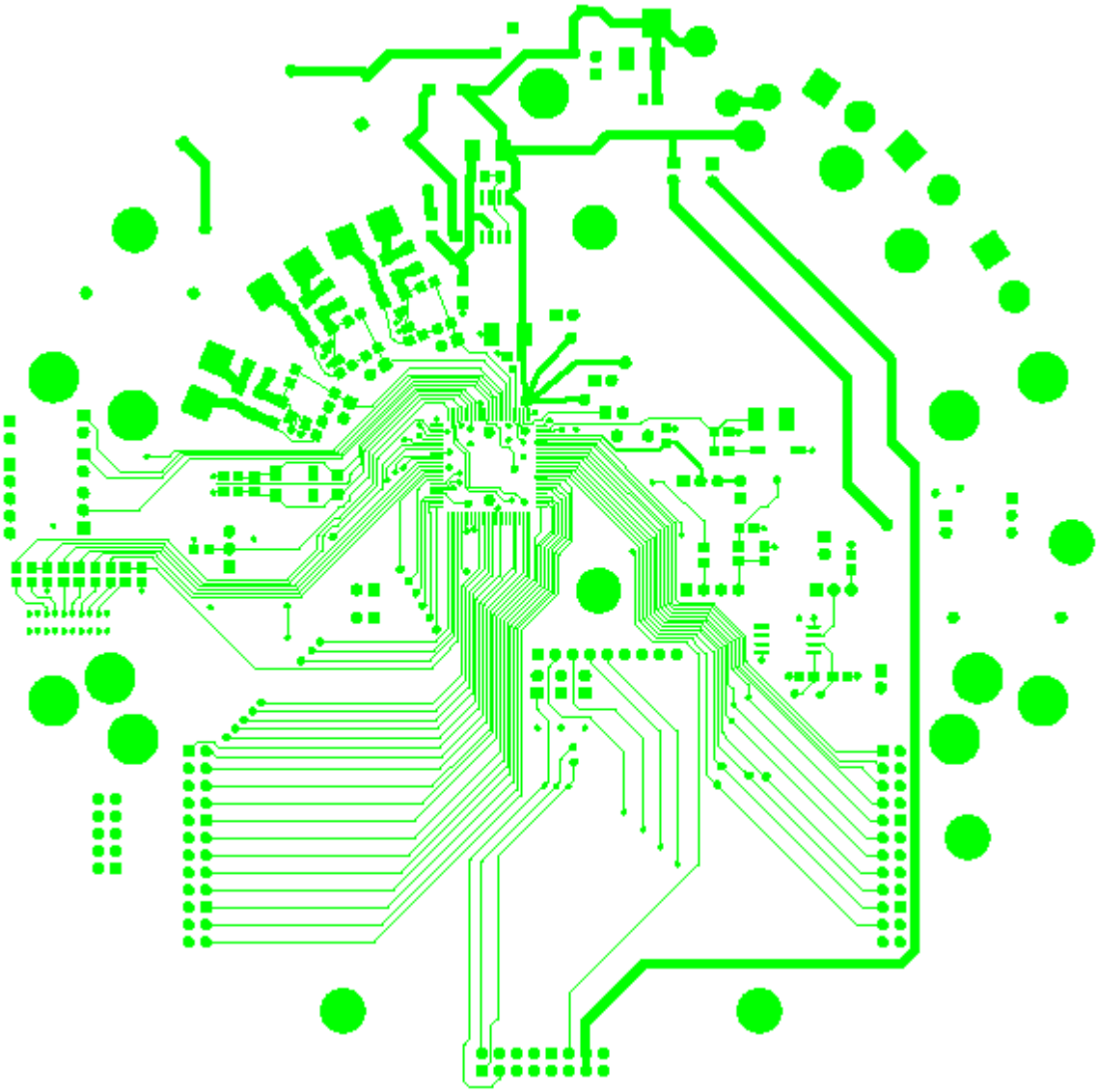


Figure 4-12: TERIDIAN D6513T3B2 Demo Board: Top Signal Layer

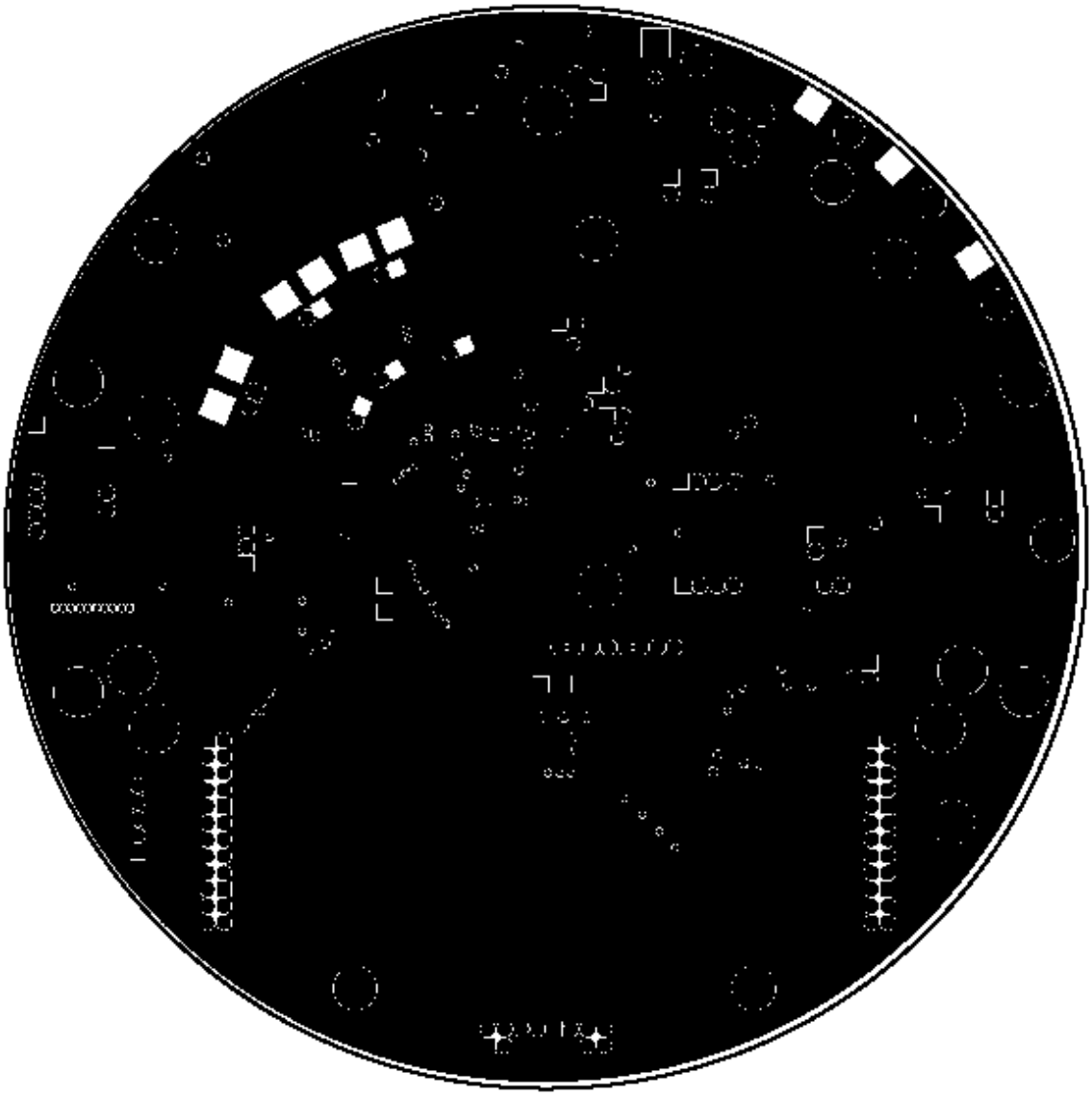


Figure 4-13: TERIDIAN D6513T3B2 Demo Board: Middle Layer 1 (Ground Plane)

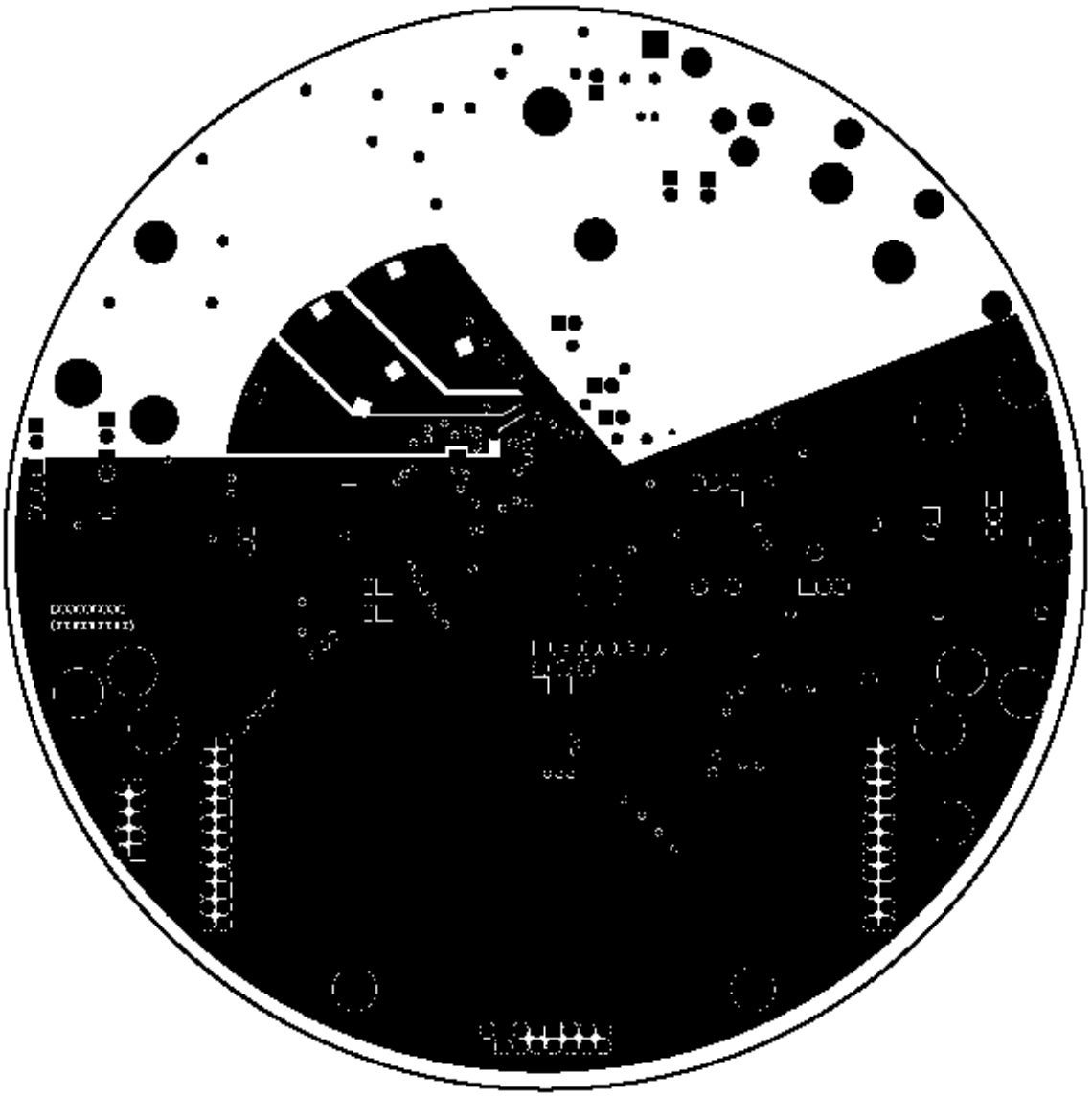


Figure 4-14: TERIDIAN D6513T3B2 Demo Board: Middle Layer 2 (Supply Plane)

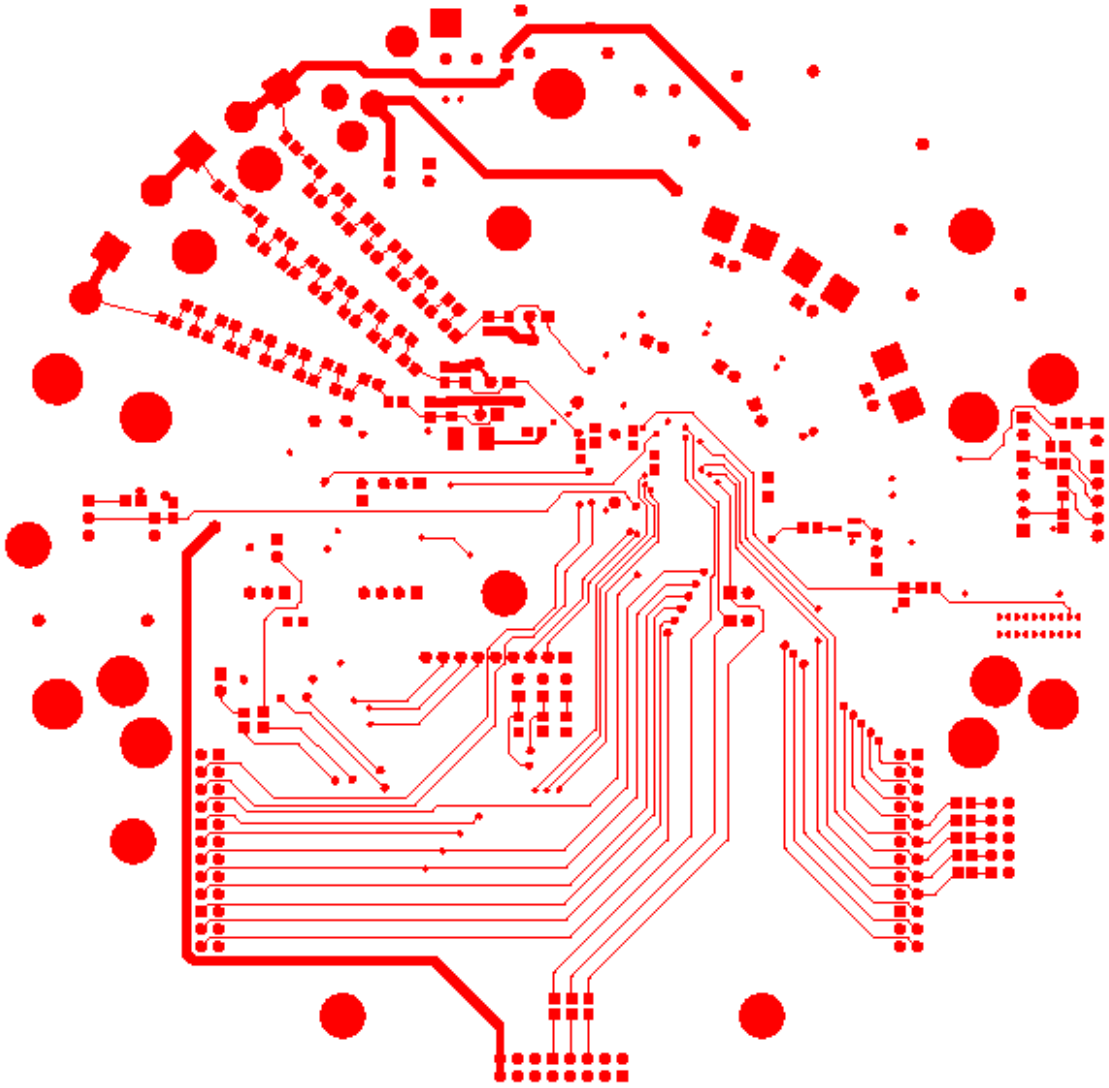


Figure 4-15: TERIDIAN D6513T3B2 Demo Board: Bottom Signal Layer

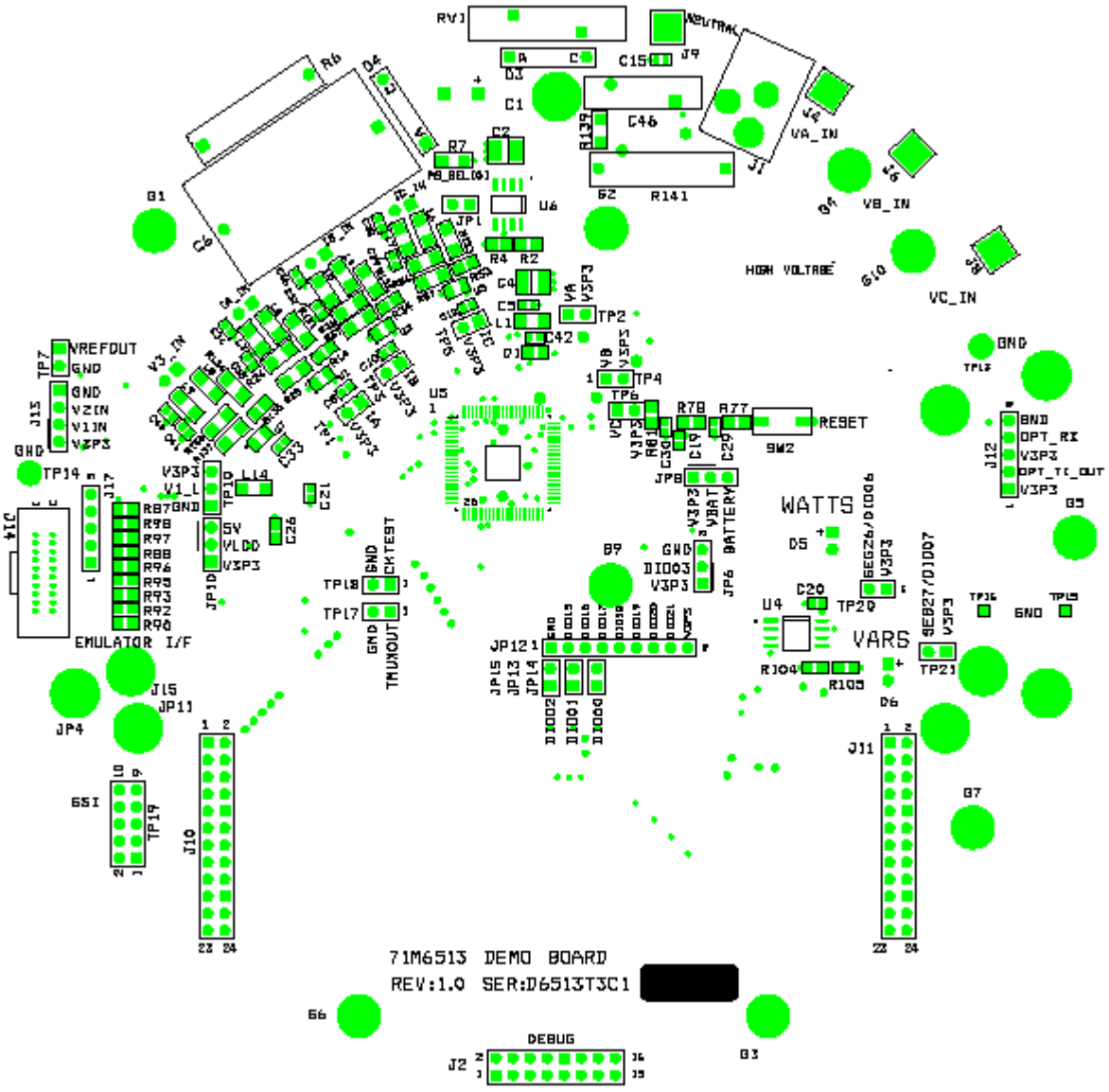


Figure 4-16: TERIDIAN D6513T3C1 Demo Board: Top View

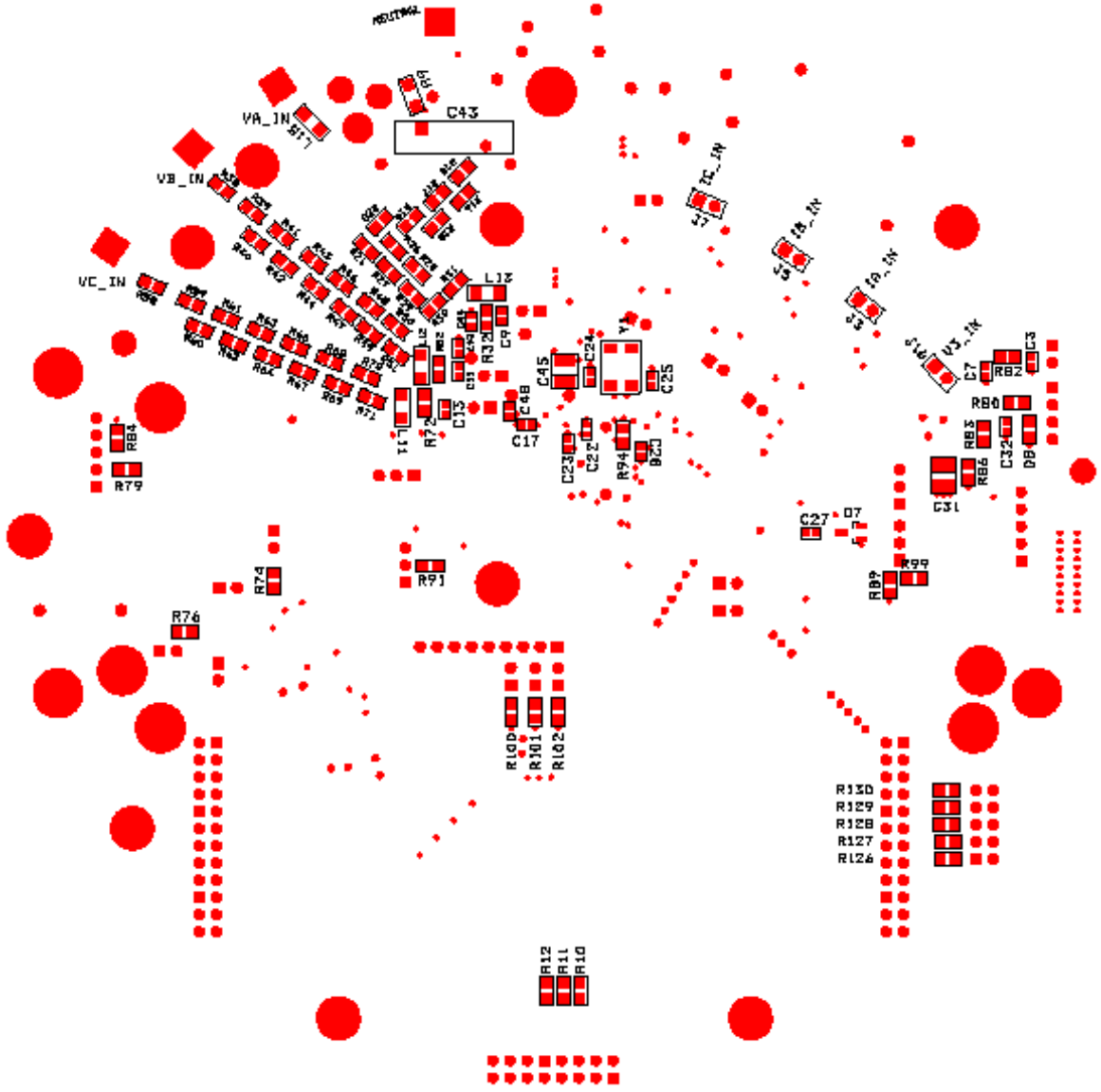


Figure 4-17: TERIDIAN D6513T3C1 Demo Board: Bottom View

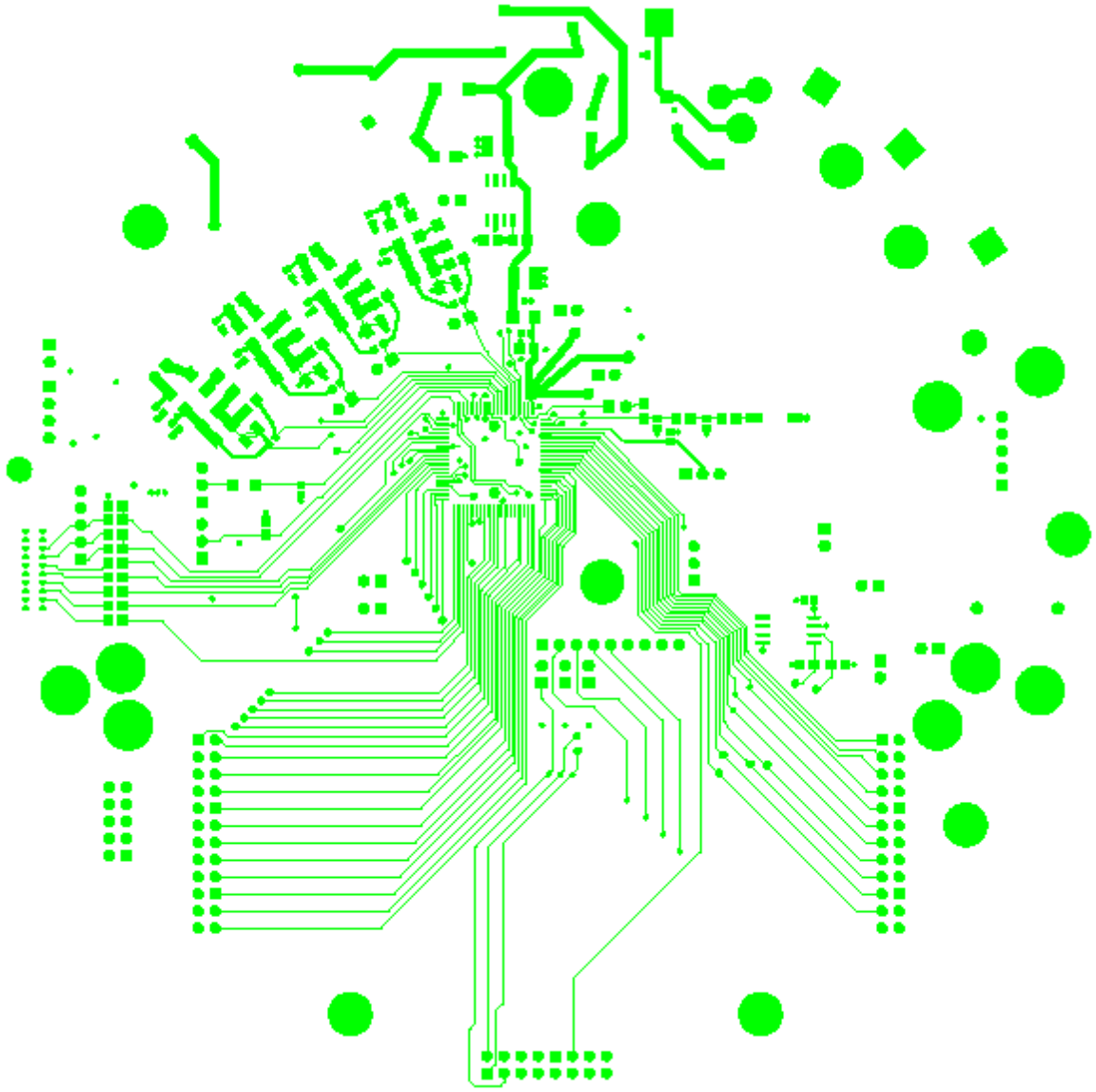


Figure 4-18: TERIDIAN D6513T3C1 Demo Board: Top Signal Layer

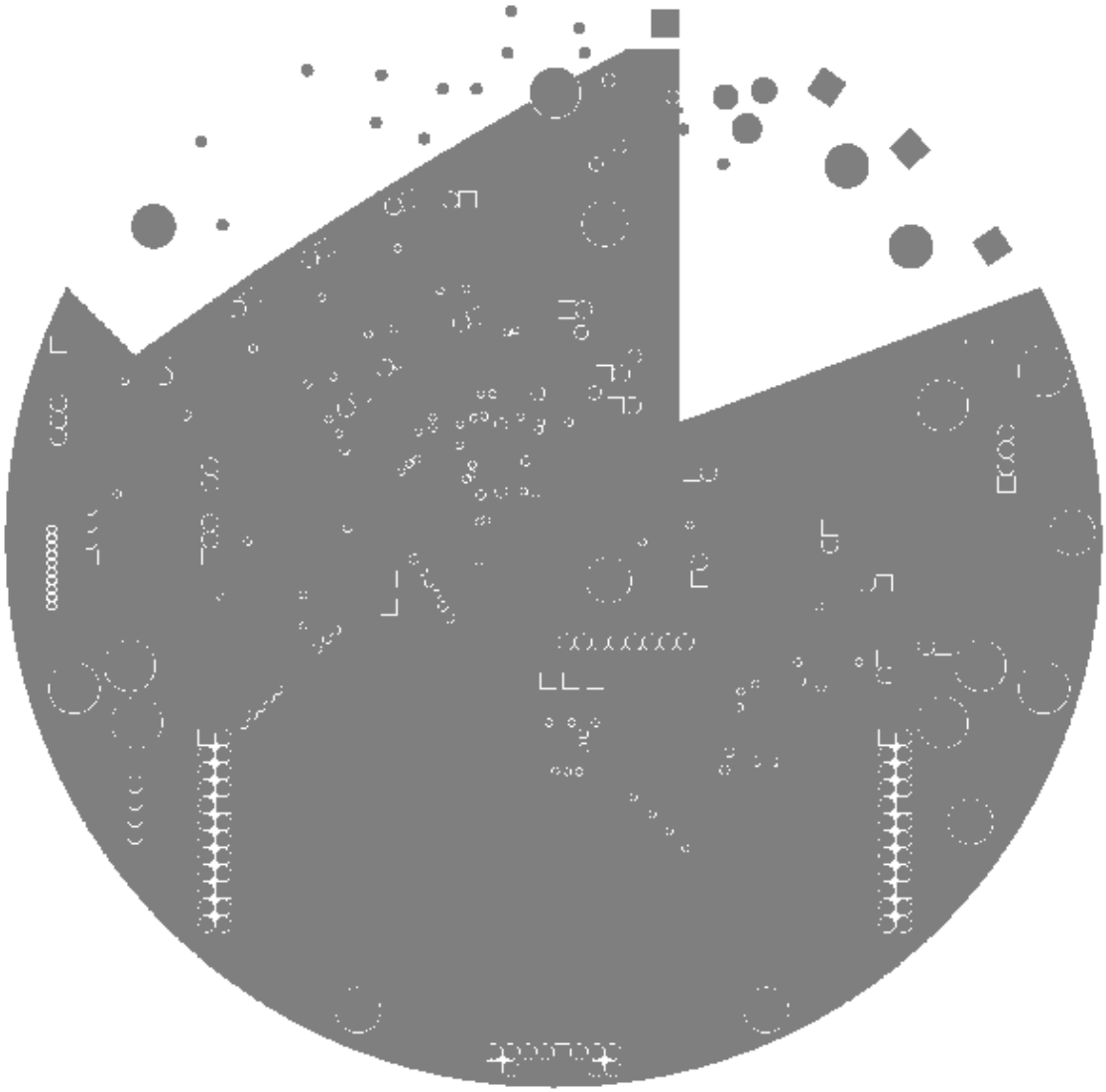


Figure 4-19: TERIDIAN D6513T3C1 Demo Board: Ground Plane Layer

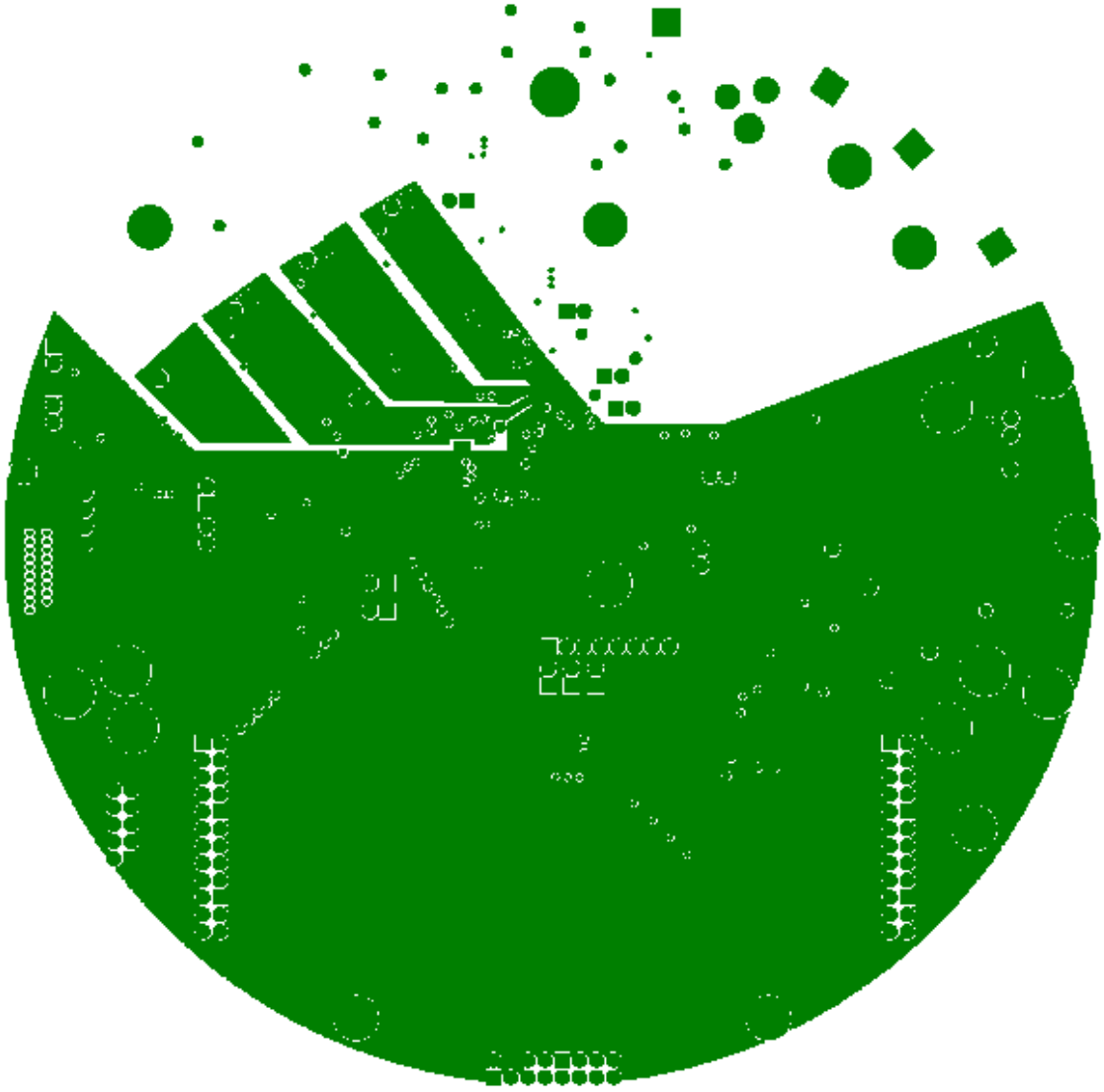


Figure 4-20: TERIDIAN D6513T3C1 Demo Board: Power Plane Layer

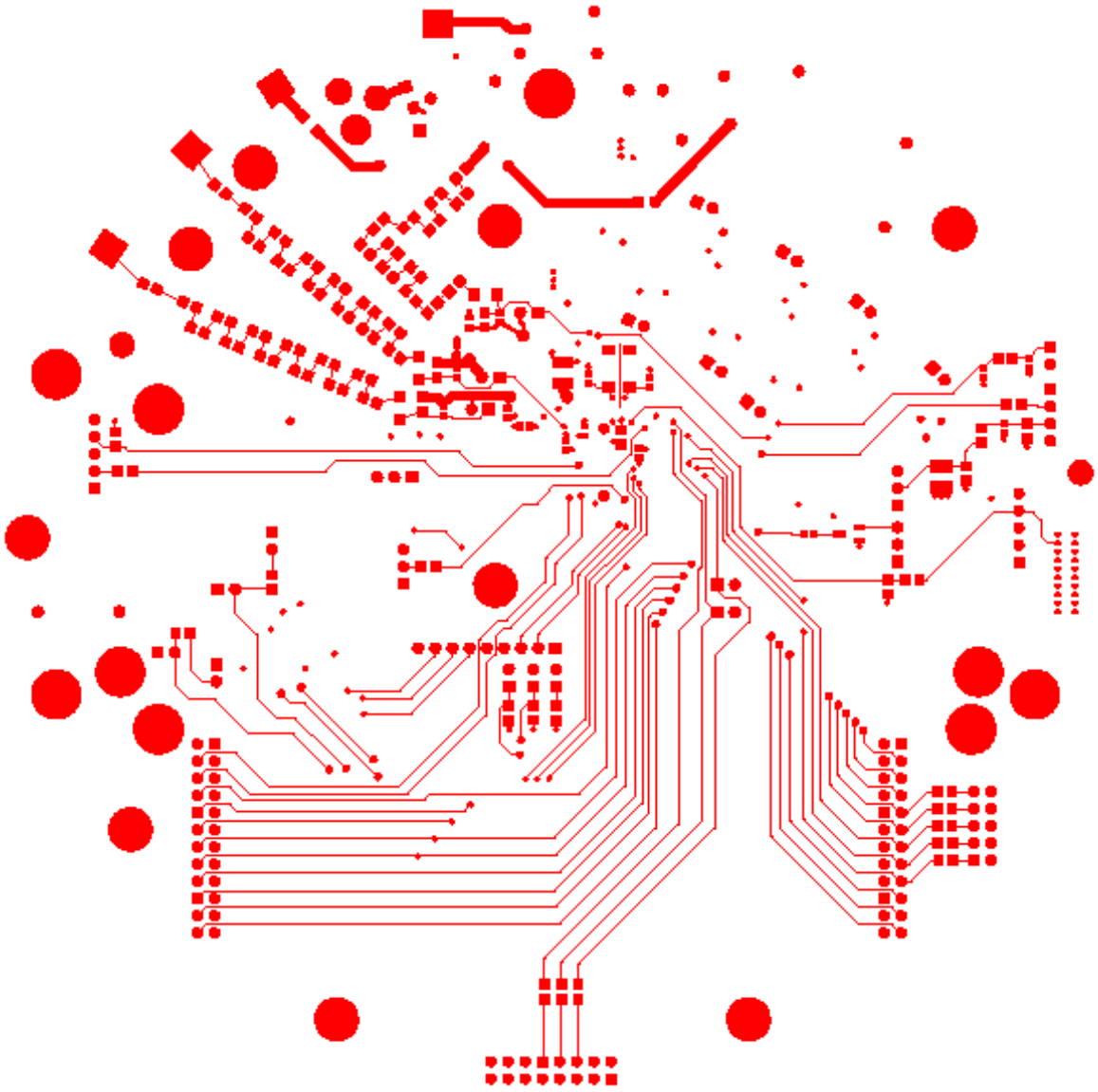


Figure 4-21: TERIDIAN D6513T3C1 Demo Board: Bottom Signal Layer

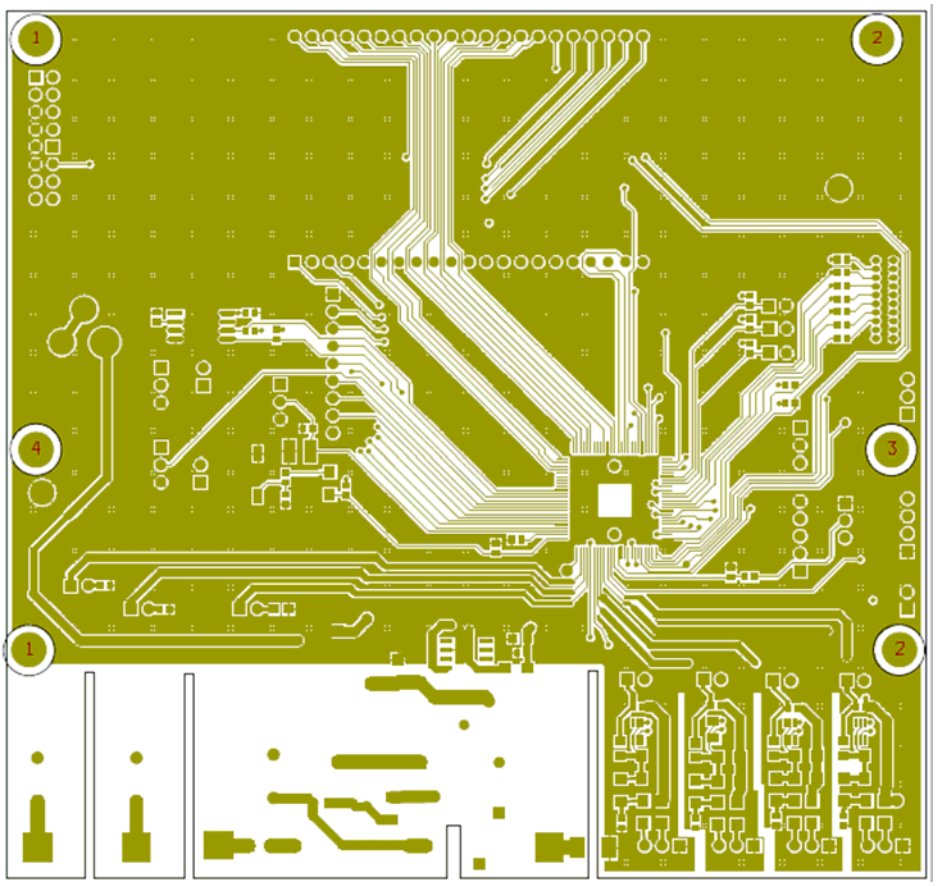


Figure 4-22: TERIDIAN D6513T3D2 Demo Board: Top Signal Layer

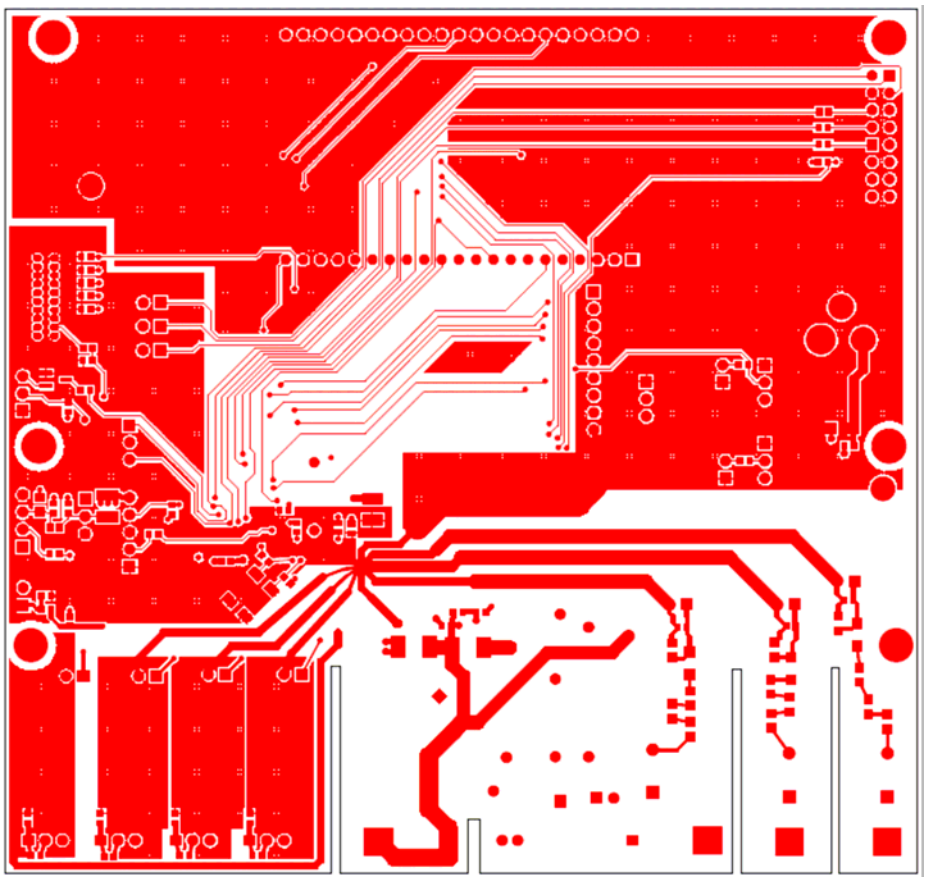


Figure 4-23: TERIDIAN D6513T3D2 Demo Board: Bottom Signal Layer

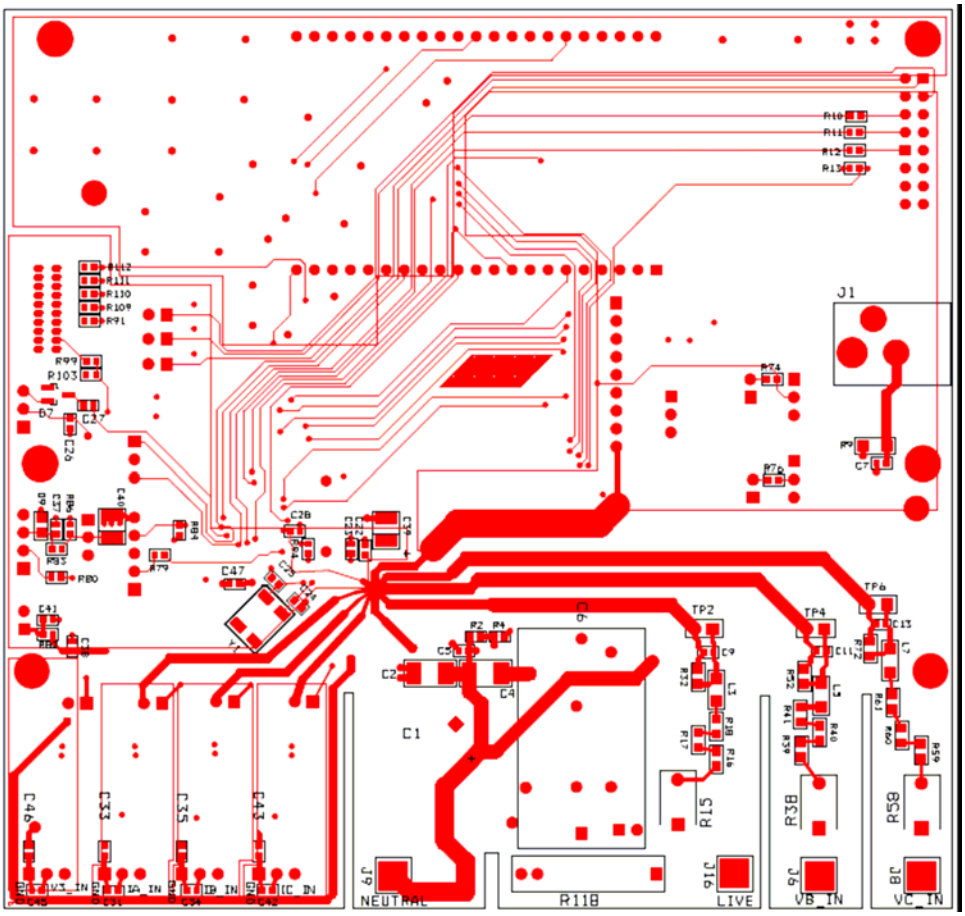


Figure 4-24: TERIDIAN D6513T3D2 Demo Board: Bottom View

Item	Q	Reference	Value	PCB Footprint	P/N	Manufacturer	Vendor	Vendor P/N
1	21	C1-C3,C5-C10,C12-C23	0.1uF	0805	C2012X7R1H104K	TDK	Digi-Key	445-1349-1-ND
2	1	C4	33uF/10V	1812	TAJB336K010R	AVX	Digi-Key	478-1687-1-ND
3	1	C11	10uF/16V, B Case	1812	TAJB106K016R	AVX	Digi-Key	478-1673-1-ND
4	2	D2,D3	LED	0805	LTST-C170KGKT	LITEON	Digi-Key	160-1414-1-ND
5	4	JP1,JP2,JP3,JP4	HDR2X1	2x1pin	PZC36SAAN	Sullins	Digi-Key	S1011-36-ND
6	1	J1	RAPC712		RAPC712	Switchcraft	Digi-Key	SC1152-ND
7	1	J2	DB9	DB9	A2100-ND	AMP	Digi-Key	A2100-ND
8	1	J3	HEADER 8X2	8x2pin	PPTC082LFBN	Sullins	Digi-Key	S4208-ND
9	4	R1,R5,R7,R8	10K	0805	ERJ-6GEYJ103V	Panasonic	Digi-Key	P10KACT-ND
10	2	R2,R3	1K	0805	ERJ-6GEYJ102V	Panasonic	Digi-Key	P1.0KACT-ND
11	1	R4	NC	0805	N/A	N/A	N/A	N/A
12	1	R6	0	0805	ERJ-6GEY0R00V	Panasonic	Digi-Key	P0.0ACT-ND
13	1	SW2	PB Switch	PB	EVQ-PJX05M	Panasonic	Digi-Key	P8051SCT-ND
14	2	TP5,TP6	test point	TP	5011	Keystone	Digi-Key	5011K-ND
15	5	U1,U2,U3,U5,U6	ADUM1100	SOIC8	ADUM1100AR	ADI	Digi-Key	ADUM1100AR-ND
16	1	U4	MAX3237CAI	SOG28	MAX3237CAI	MAXIM	Digi-Key	MAX3237CAI-ND
17	4		spacer		2202K-ND	Keystone	Digi-Key	2202K-ND
18	4		4-40, 1/4" screw		PMS4400-0025PH	Building Fasteners	Digi-Key	H342-ND
19	2		4-40, 5/16" screw		PMS4400-0031PH	Building Fasteners	Digi-Key	H343-ND
20	2		4-40 nut		HNZ440	Building Fasteners	Digi-Key	H216-ND

Table 4-4: Debug Board: Bill of Material

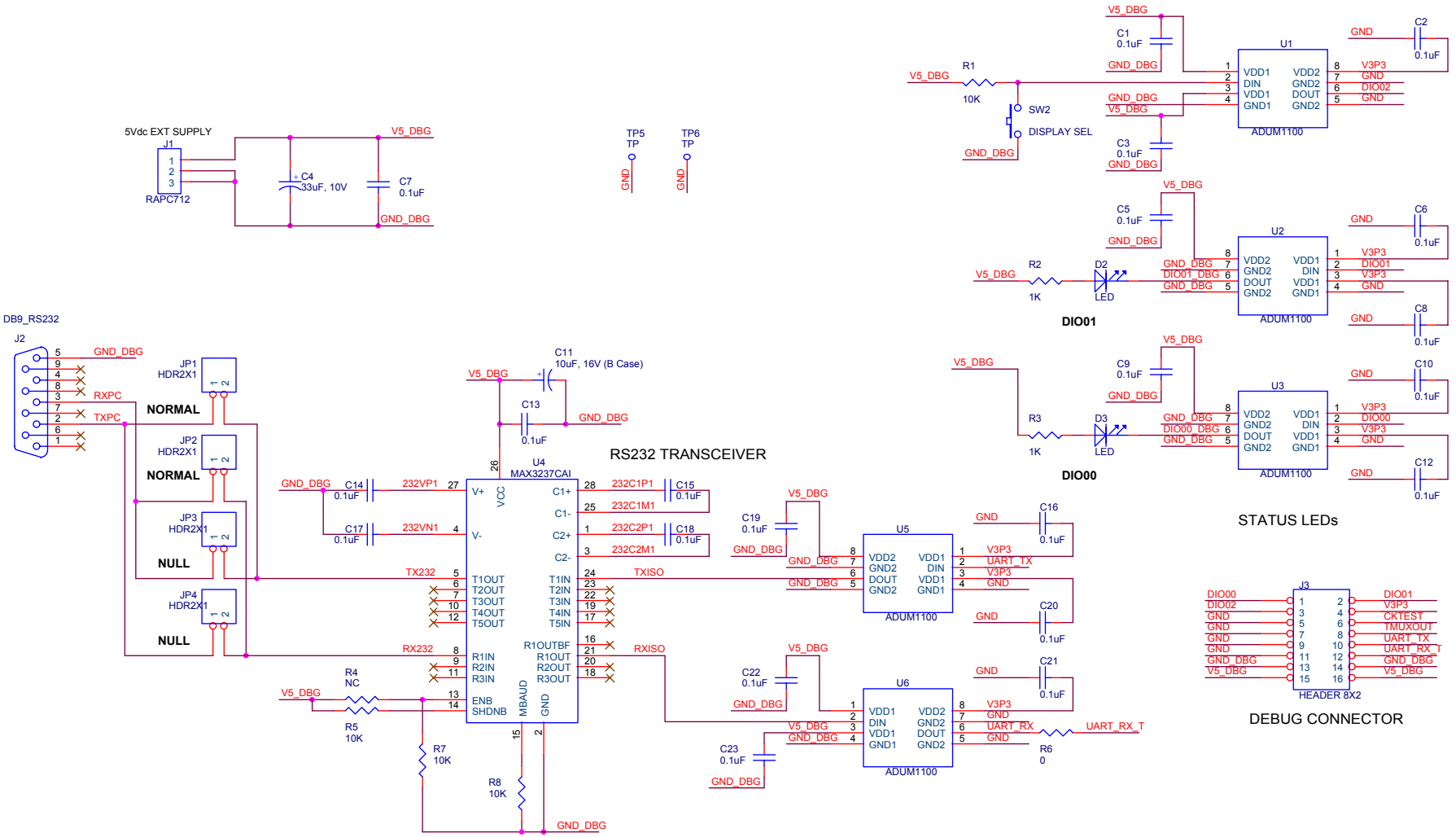


Figure 4-25: Debug Board: Electrical Schematic

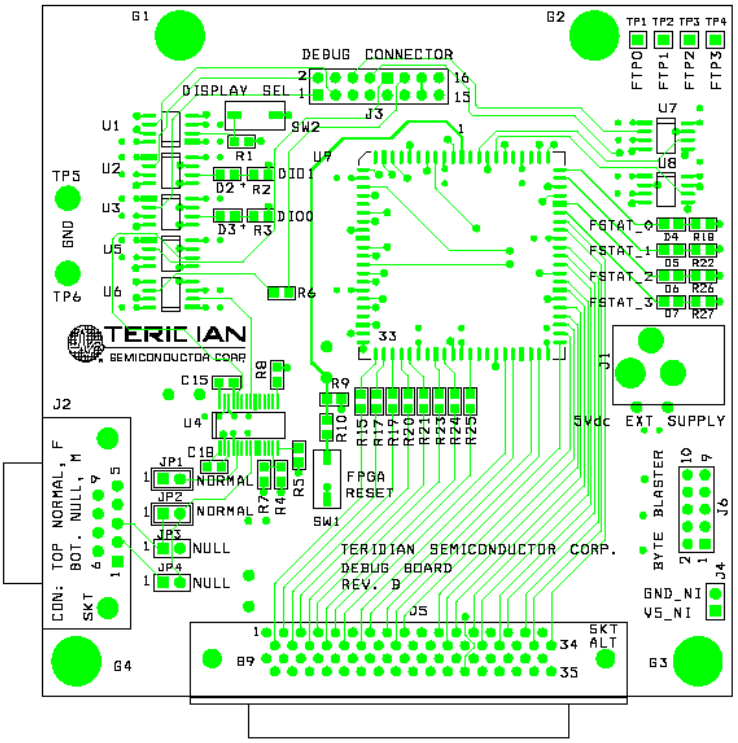


Figure 4-26: Debug Board: Top View

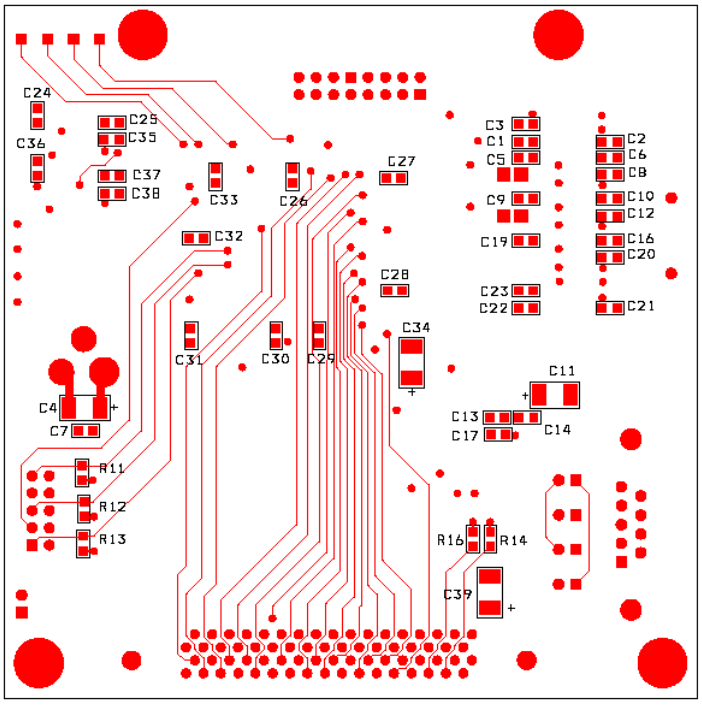


Figure 4-27: Debug Board: Bottom View

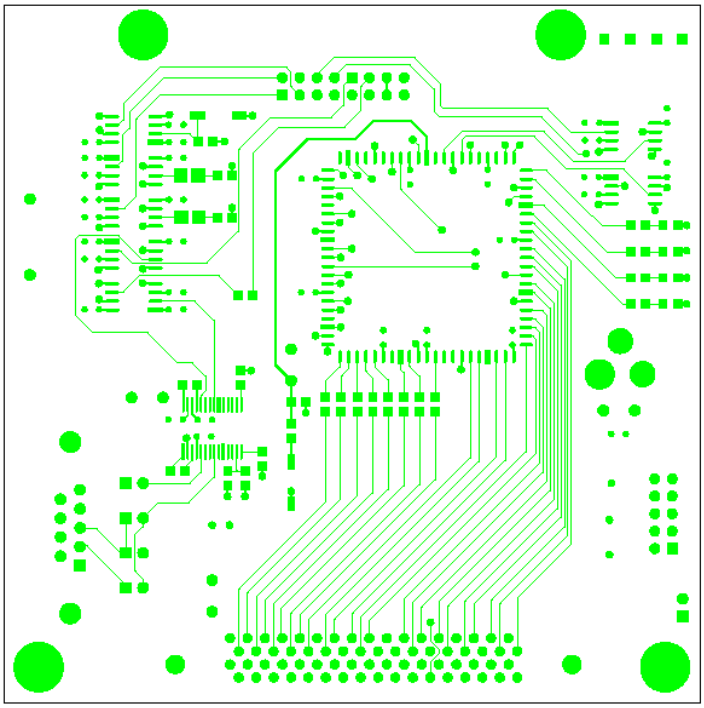


Figure 4-28: Debug Board: Top Signal Layer

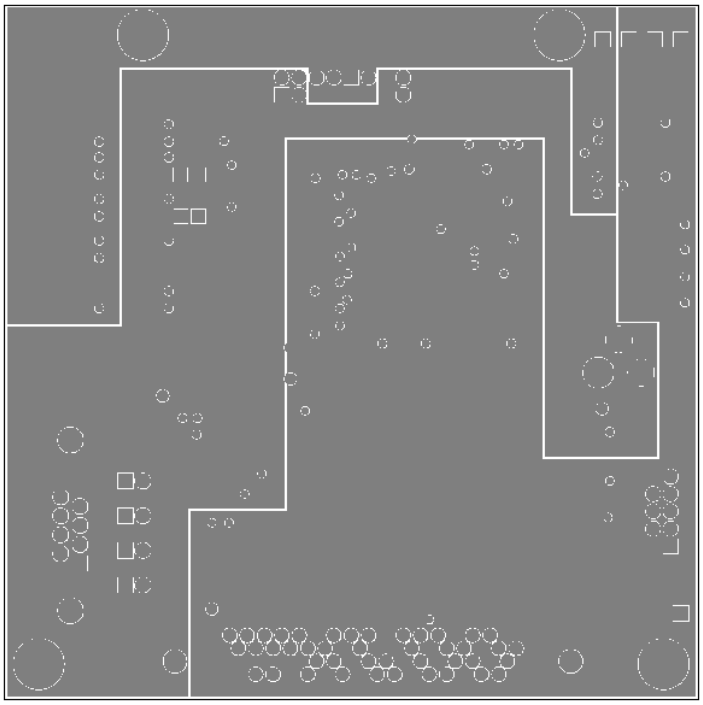


Figure 4-29: Debug Board: Middle Layer 1 (Ground Plane)

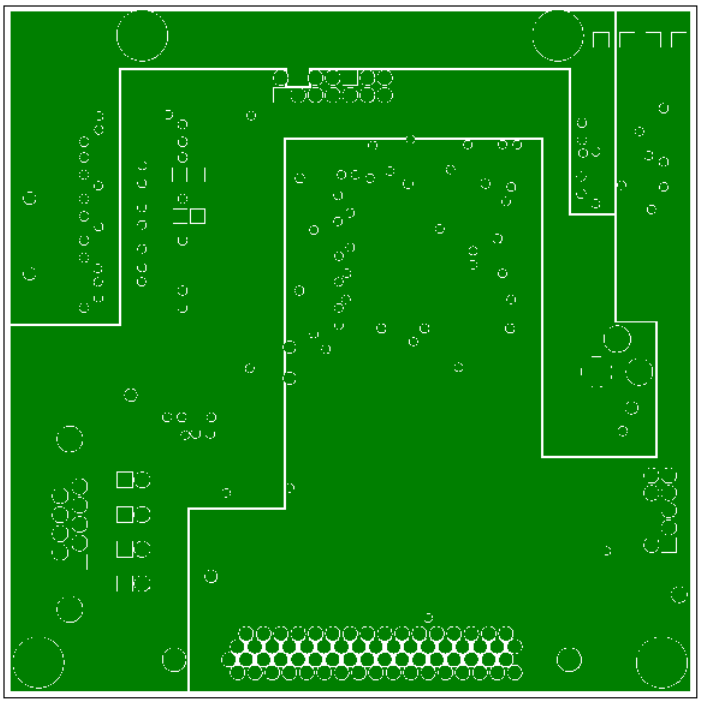


Figure 4-30: Debug Board: Middle Layer 2 (Supply Plane)

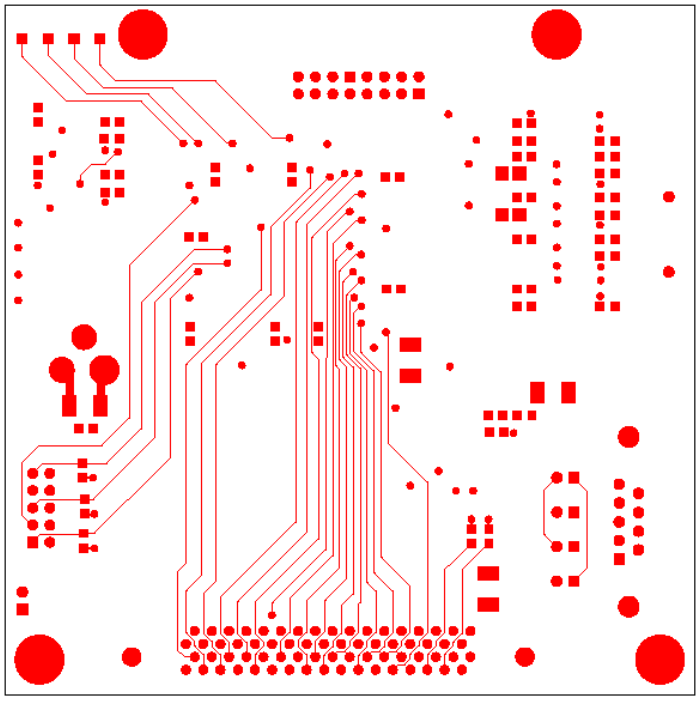


Figure 4-31: Debug Board: Bottom Trace Layer

Power/Ground/NC Pins:

Name	Pin #	Type	Description
GNDA	76,91	P	Analog ground: This pin should be connected directly to the analog ground plane.
GNDD	1, 40, 75	P	Digital ground: This pin should be connected directly to the digital ground plane.
V3P3A	77	P	Analog power supply: A 3.3V analog power supply should be connected to this pin.
V3P3D	9	P	Digital power supply: A 3.3V digital power supply should be connected to this pin.
VBAT	72	P	Battery backup power supply. A battery or super-capacitor is to be connected between VBAT and GNDD. If no battery is used, connect VBAT to V3P3D.
V2P5	73	O	Output of the 2.5V regulator. This pin should be terminated with a 0.1µF capacitor.
VLCD	96	P	LCD power supply.
NC	32,33,36, 42,43,44, 47,55,90,95	--	No Connect

Table 4-5: 71M6513/71M6513H Pin Description Table 1/3

Analog Pins:

Name	Pin #	Type	Description
IA IB IC	84 83 82	I	Line Current Sense Inputs: These pins are voltage inputs to the internal A/D converter. Typically, they are connected to the output of a current transformer.
VA VB VC	80 79 78	I	Line Voltage Sense Inputs: These pins are voltage inputs to the internal A/D converter. Typically, they are connected to the output of a resistor divider.
V1 V2 V3	88 87 86	I	Comparator Inputs: These pins are voltage inputs to the internal comparator. The voltages applied to these pins are compared to an internal reference voltage VBIAS (1.5V). If the input voltage is above the reference, the corresponding comparator output will be high (1). The outputs are maintained in the *COMP_STAT* register. A typical application is to sense the voltage on the DC supply. An external resistor divider is used to scale the power supply voltage to a level that triggers the comparator at the desired voltage drop. A 0.1µF capacitor to GNDA should be connected to the V1 pin.  If not used, the V3 pin should be left unconnected or connected to VREF.
VBIAS	81	O	Reference voltage used by the power fault detection circuit.
VREF	85	I/O	Voltage Reference for the ADC. A 0.1µF capacitor to GNDA should be connected to this pin.
XIN, XOUT	92 94	I	Crystal Inputs: A 32kHz style crystal should be connected across these pins. Typically, a 10pf capacitor is also connected from each pin to GNDA. See crystal manufacturer datasheet for details.
VDRV	7	O	Voltage boost output.

Table 4-6: 71M6513/71M6513H Pin Description Table 2/3

Digital Pins:

Name	Pin #	Type	Description
DIO_3, DIO_2, DIO_1, DIO_0	21 20 19 18	I/O	Input/output pins 0 through 3
COM3, COM2, COM1, COM0	25 24 23 22	O	LCD Common Outputs: These 4 pins provide the select signals for the LCD display.
SEG0…SEG2, SEG8…SEG23	See pinout	O	Dedicated LCD Segment Output.
SEG24/DIO4… SEG41/DIO21	See pinout	I/O	Multi-use pin, configurable as either LCD SEG driver or DIO.
SEG7/MUX_SYNC	37	O	Multi-use-pin LCD Segment Output/ MUX_SYNC is output for Synchronous serial interface
SEG6/SRDY	35	I/O	Multi-use-pin, LCD Segment Outputs/ SRDY input for Synchronous serial interface.
SEG5/SFR	11	O	Multi-use-pin, LCD Segment Output/ SFR output for Synchronous serial interface.
SEG4/SDATA	10	O	Multi-use-pin, LCD Segment Output/ SDATA output for Synchronous serial interface.
SEG3/SCLK	6	O	Multi-use-pin, LCD Segment Output/ SCLK output for Synchronous serial interface.
RESETZ	74	I	Chip reset: This input pin is used to reset the chip into a known state. For normal operation, this pin is set to 1. To reset the chip, this pin is driven to 0. This pin has an internal 30µA (nom.) current source pull-up. The minimum width of the pulse is 5µS. A 0.1µF capacitor to GNDD should be connected to this pin.
RX	71	I	UART input.
TX	5	O	UART output.
E_RXTX	2	I/O	Emulator serial data.
E_TBUS[3] E_TBUS[2] E_TBUS[1] E_TBUS[0]	12 13 14 15	O	Emulator trace bus. These pins have internal pull-up resistors.
E_ISYNC/BRKRQ	29	I/O	Emulator handshake. This pin has an internal pull-up resistor.
E_TCLK	100	O	Emulator clock. This pin has an internal pull-up resistor.
E_RST	97	I	Emulator reset. This pin has an internal pull-up resistor.

Table 4-7: 71M6513/71M6513H Pin Description Table 3/3

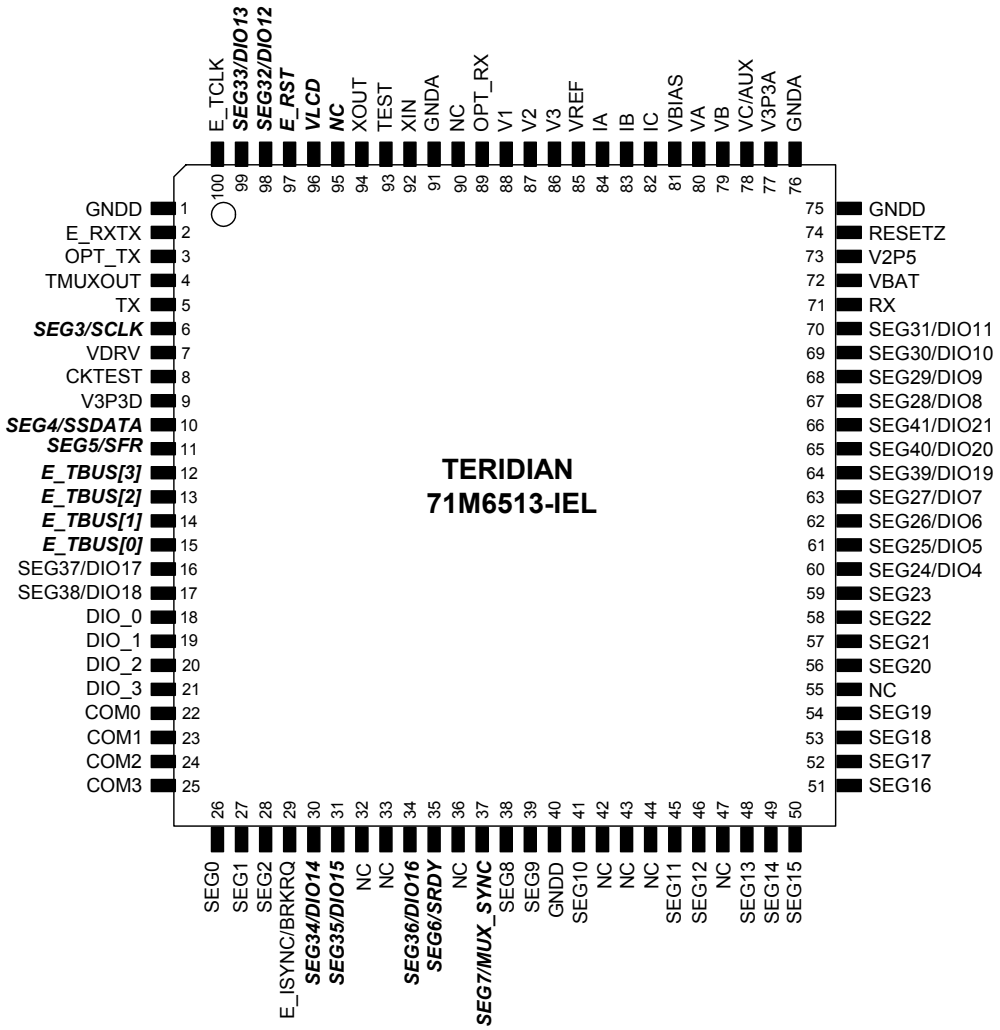


Figure 4-32: TERIDIAN 71M6513/71M6513H epLQFP100: Pinout (top view)

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