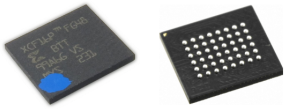


DLP® Configuration PROM for DLPC410

Check for Samples: DLPR410, DLPR4101

FEATURES

- **Pre-Programmed Xilinx(R) PROM Configures DLPC410**
- **Data Transfer up to 33 Mbps**
- **I/O Pins Compatible with 1.8 V to 3.3 V**
- **1.8 V Supply Voltage**
- **–40°C to 85°C Operating Temperature Range**
- **Load 4 Enhanced Functionality (DLPR4101 only)**

APPLICATIONS

- **Industrial:**
  - **Direct Imaging Lithography**
  - **Laser Marking and Repair Systems**
  - **Computer-to-Plate Printers**
  - **Rapid Prototyping Machines and 3D Printers**
  - **3D Scanners for Machine Vision and Quality Control**
- **Medical:**
  - **Phototherapy Devices**
  - **Ophthalmology**
  - **Vascular Imaging**
  - **Hyperspectral Imaging**
  - **3D Scanners for Limb and Skin Measurement**
  - **Confocal Microscopes**
- **Display:**
  - **3D Imaging Microscopes**
  - **Intelligent and Adaptive Lighting**
  - **Augmented Reality and Information Overlay**

DESCRIPTION

The DLP Discovery 4100 offers the highest speed pattern rates in the DLP catalog portfolio with the option for random row addressing. The DLPR410 and DLPR4101 are programmed PROMs used to properly configure the DLPC410, which supports both the 0.7 XGA chipset and 0.95 1080p chipset.

The DLPR410 and DLPR4101 is one of multiple components in the DLP Discovery 4100 chipsets (see TI Literature Number DLPU008). A dedicated chipset provides developers easier access to the DMD as well as high speed, independent micromirror control. See the list of required chipset component in Table 1)

Table 1. DLP Discovery 4100 Chipset Configurations

0.7 XGA Chipset			0.95 1080p Chipset		
Qty	**TI Part**	**Description**	**Qty**	**TI Part**	**Description**
1	DLP7000	0.7 XGA Type A DMD (digital micromirror device)	1	DLP9500	0.95 1080p Type A DMD (digital micromirror device)
1	DLPC410	DLP Discovery 4100 DMD Controller	1	DLPC410	DLP Discovery 4100 DMD Controller
1	DLPR410 and DLPR4101	DLP Discovery 4100 Configuration PROM	1	DLPR410 and DLPR4101	DLP Discovery 4100 Configuration PROM
1	DLPA200	DMD Micromirror Driver	2	DLPA200	DMD Micromirror Driver

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION CONTINUED

The DLPC410 configuration program is only available on the DLPR410 and DLPR4101. Reliable function and operation of the DLPR410 and DLPR4101 requires that it be used in conjunction with the other components of the chipset see Figure 1. For more information on the chipset components, see DLP Discovery 4100 chipset data sheet.

For complete electrical and mechanical specifications of the DLPR410 and DLPR4101, see the XCF16P product specification at www.xilinx.com.

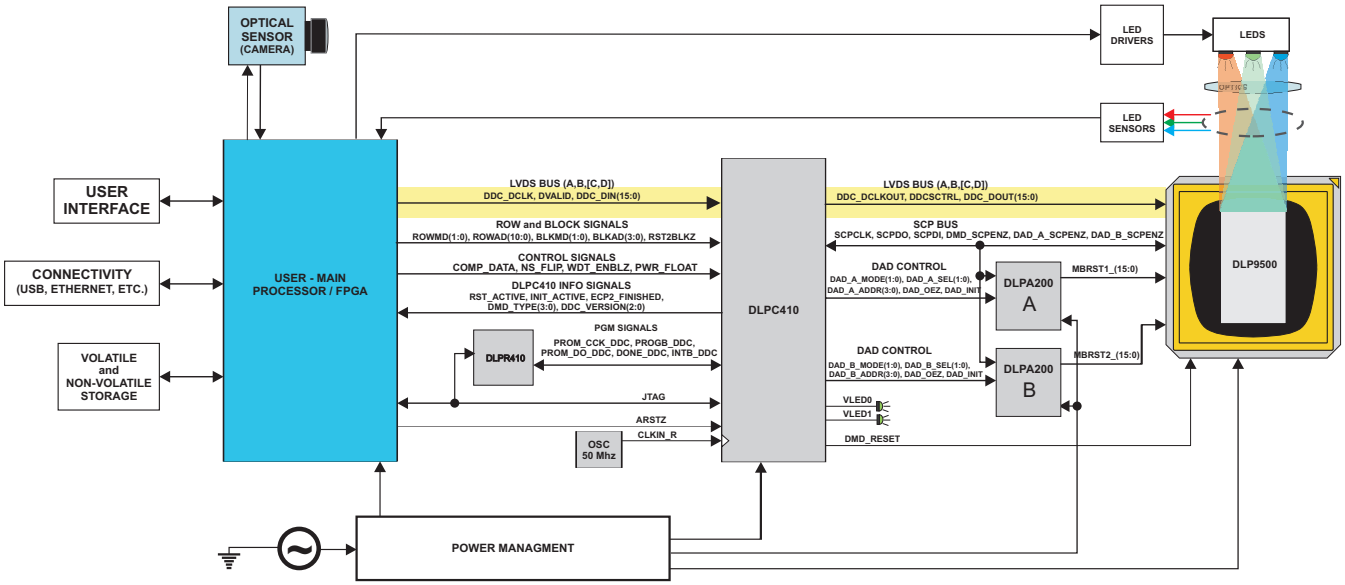


Figure 1. D4100 System Block Diagram

ORDERING INFORMATION

T_A	ORDERABLE PART NUMBER	Version	TOP-SIDE MARKING
–40°C to 85°C	DLPR410YVA	The DLPC410 will report version 5 when programed with this part	Silver Dot Located by Pin 1 (or white label with DDC4100-005) TI part number 2510442-0005
	DLPR4101YVA	The DLPC410 will report version 6 when programed with this part	Blue Dot Located by Pin 1, TI part number 2510442-0006

DEVICE PART NUMBER NOMENCLATURE

Figure 2 provides a legend of reading the complete device name for any DLP device. The DLPR410YVA is functionally equivalent to TI part number 2510442-0005. The DLPR4101YVA is an enhanced functionality part that adds "Load 4" functionality and is functionally equivalent to TI part number 2510442-0006 . For more information see the DLPC410 data sheet DLPS024 .

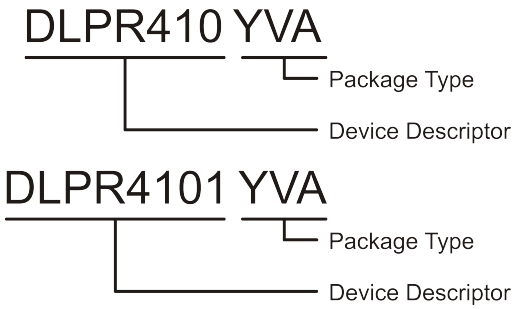


Figure 2. Device Nomenclature

DEVICE MARKING

Figure 3 is an image of the Xilinx XCF16P PROM used for the DLPR410 and DLPR4101 device (DLPR4101 shown as example).

Figure 3. Top and Bottom View of the Xilinx XCF16P TFBGA

PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NO.	NAME		
A1	GND	-	Ground
A2	GND	-	Ground
A3	OE/$\overline{\text{RESET}}$	I/O	Output Enable/Reset (Open-Drain I/O). When Low, this input holds the address counter reset and the DATA and CLKOUT outputs are placed in a high-impedance state. This is a bidirectional open-drain pin that is held Low while the PROM completes the internal power-on reset sequence. Polarity is not programmable.
A4	DNC	–	Do Not Connect. Leave unconnected.
A5	D6	O	DATA output pin to provide parallel data for configuring the DLPC410 in SelectMap (parallel) mode. Set to high-impedance state during ISPEN (when not clamped) and when serial mode is selected for configuration. Can be left unconnected when the PROM is used in serial mode.

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
A6	D7	O	DATA output pin to provide parallel data for configuring the DLPC410 in SelectMap (parallel) mode. Set to high-impedance state during ISPEN (when not clamped) and when serial mode is selected for configuration. Can be left unconnected when the PROM is used in serial mode.
B1	VCCINT	-	Positive 1.8 V supply voltage for internal logic.
B2	VCCO	-	Positive 3.3 V, 2.5 V or 1.8 V supply voltage connected to the output voltage drivers and internal buffers.
B3	CLK	I	Configuration clock input. An internal programmable control bit selects between the internal oscillator and the CLK input pin as the clock source to control the configuration sequence. Each rising edge on the CLK input increments the internal address counter if the CLK input is selected, $\overline{CE}$ is Low, OE/$\overline{RESET}$ is High, BUSY is Low (parallel mode only), and $\overline{CF}$ is High.
B4	$\overline{CE}$	I	Chip Enable Input. When $\overline{CE}$ is High, the device is put into low-power standby mode, the address couter is reset, and the DATA and CLKOUT outputs are placed in a high impedance state.
B5	D5	O	DATA output pin to provide parallel data for configuring the DLPC410 in SelectMap (parallel) mode. Set to high-impedance state during ISPEN (when not clamped) and when serial mode is selected for configuration. Can be left unconnected when the PROM is used in serial mode.
B6	GND	-	Ground
C1	BUSY	I	Busy Input. The BUSY input is enabled when parallel mode is selected for configuration. When BUSY is High, the internal address counter stops incrementing and the current data remains on the data pins. On the first rising edge of CLK after BUSY transitions from High to Low, the data for the next address is driven on the data pins. When serial mode or decompression is enabled during device programming, the BUSY input is disabled. BUSY has an internal 50 kΩ resistive pull-down to GND to provide a logic 0 to the device if the pin is not driven.
C2	CLKOUT	O	Configuration Clock Output. An internal programmable control bit enables the CLKOUT signal, which is sourced from either the internal oscillator or the CLK input pin. Each rising edge of the selected clock source increments the internal address counter if data is available, $\overline{CE}$ is Low, and OE/$\overline{RESET}$ is High. Output data is available on the rising edige of CLKOUT. CLKOUT is disabled if $\overline{CE}$ is High or OE/$\overline{RESET}$ is Low. If decompression is enabled, CLKOUT is parked High when decompressed data is not ready. When CLKOUT is disabled, the CLKOUT pin is put into a high-impedance state. If CLKOUT is used, then it must be pulled High externally using a 4.7 kΩ pull-up to to V_{CCO}.
C3	DNC	-	Do Not Connect. Leave unconnected.
C4	DNC	-	Do Not Connect. Leave unconnected.
C5	D4	O	DATA output pin to provide parallel data for configuring the DLPC410 in SelectMap (parallel) mode. Set to high-impedance state during ISPEN (when not clamped) and when serial mode is selected for configuration. Can be left unconnected when the PROM is used in serial mode.
C6	VCCO	-	Positive 3.3 V, 2.5 V or 1.8 V supply voltage connected to the output voltage drivers and internal buffers.
D1	$\overline{CF}$	I/O	Unused pin for JTAG instructions. If unused, the $\overline{CF}$ pin must be pulled High using an external 4.7 kΩ pull-up to V_{CCO}.
D2	$\overline{CEO}$	O	Chip Enable Output. Chip Enable Output is connected to the $\overline{CE}$ input of the next PROM in the chain. This output is Low when $\overline{CE}$ is Low and OE/$\overline{RESET}$ is High, AND the internal address counter has been incremented beyond its Terminal Count (TC) value or the PROM does not contain any blocks that correspond to the selected revision. $\overline{CEO}$ returns to High when OE/$\overline{RESET}$ goes Low or $\overline{CE}$ goes High.
D3	DNC	-	Do Not Connect. Leave unconnected.
D4	DNC	-	Do Not Connect. Leave unconnected.
D5	D3	O	DATA output pin to provide parallel data for configuring the DLPC410 in SelectMap (parallel) mode. Set to high-impedance state during ISPEN (when not clamped) and when serial mode is selected for configuration. Can be left unconnected when the PROM is used in serial mode.
D6	VCCO	-	Positive 3.3 V, 2.5 V or 1.8 V supply voltage connected to the output voltage drivers and internal buffers.
E1	VCCINT	-	Positive 1.8 V supply voltage for internal logic.

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
E2	TMS	I	Unused JTAG Mode Select Input. TMS has an internal 50 kΩ resistive pull-up to V_{CCJ} to provide a logic 1 to the device if the pin is not driven.
E3	DNC	-	Do Not Connect. Leave unconnected.
E4	DNC	-	Do Not Connect. Leave unconnected.
E5	D2	O	DATA output pin to provide parallel data for configuring the DLPC410 in SelectMap (parallel) mode. Set to high-impedance state during ISPEN (when not clamped) and when serial mode is selected for configuration. Can be left unconnected when the PROM is used in serial mode.
E6	TDO	O	Unused JTAG Serial Data Output. TDO has an internal 50 kΩ resistive pull-up to V_{CCJ} to provide a logic 1 to the system if the pin is not driven.
F1	GND	-	Ground
F2	DNC	-	Do Not Connect. Leave unconnected.
F3	DNC	-	Do Not Connect. Leave unconnected.
F4	DNC	-	Do Not Connect. Leave unconnected.
F5	GND	-	Ground
F6	GND	-	Ground
G1	TDI	I	Ununsed JTAG Serial Data Input. TDI has an internal 50 kΩ resistive pull-up to V_{CCJ} to provide a logic 1 to the device if the pin is not driven.
G2	DNC	-	Do Not Connect. Leave unconnected.
G3	REV_SEL0	I	Revision Select [1:0] Inputs. When the $\overline{\text{EN\_EXT\_SEL}}$ is Low, the Revision Select pins are used to select the design revision to be enabled, overriding the internal programmabled Revision Select control bits. The Revision Select [1:0] inputs have an internal 50 kΩ resistive pull-up to V_{CCO} to provide a logic 1 to the device if the pins are not driven.
G4	REV_SEL1	I	Revision Select [1:0] Inputs. When the $\overline{\text{EN\_EXT\_SEL}}$ is Low, the Revision Select pins are used to select the design revision to be enabled, overriding the internal programmabled Revision Select control bits. The Revision Select [1:0] inputs have an internal 50 kΩ resistive pull-up to V_{CCO} to provide a logic 1 to the device if the pins are not driven.
G5	VCCO	-	Positive 3.3 V, 2.5 V or 1.8 V supply voltage connected to the output voltage drivers and internal buffers.
G6	VCCINT	-	Positive 1.8 V supply voltage for internal logic.
H1	GND	-	Ground
H2	VCCJ	-	Positive 3.3 V or 2.5 V JTAG I/O supply voltage connected to the TDO output voltage driver and TCK, TMS and TDI input buffers.
H3	TCK	I	JTAG Clock Input. This pin is the JTAG test clock. It sequences the TAP controller and all the JTAG test and programming electronics.
H4	$\overline{\text{EN\_EXT\_SEL}}$	I	Unused Enable External Selection Input. $\overline{\text{EN\_EXT\_SEL}}$ has an internal 50 kΩ resisitive pull-up to V_{CCO} to provide a logic 1 to the device if the pin is not driven.
H5	D1	O	DATA output pin to provide parallel data for configuring the DLPC410 in SelectMap (parallel) mode. Set to high-impedance state during ISPEN (when not clamped) and when serial mode is selected for configuration. Can be left unconnected when the PROM is used in serial mode.
H6	D0	O	DATA output pin to provide data for configuring the DLPC410 in serial mode. Used with D1-D7 to provide data for configuring the DLPC410 in SelectMap (parallel) mode. Set to high-impedance state during ISPEN (when not clamped).

Related Documents

Table 2. Related Documentation

Document	TI Literature Number
DLP® Discovery™ 4100 Chipset Datasheet	DLPU008
DLP7000 0.7 XGA Type-A DMD data sheet	DLPS026
DLP9500 0.95 1080p Type-A DMD data sheet	DLPS025
DLPC410 Digital Controller data sheet	DLPS024
DLPA200 DMD Micromirror Driver data sheet	DLPS015

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	MAX	UNIT
V_{CCINT}	Internal supply voltage	Relative to ground	–0.5	2.7	V
V_{CCO}	I/O supply voltage	Relative to ground	–0.5	4.0	V
V_{IN}	Input voltage with respect to ground	V_{CCO} < 2.5 V	-0.5	3.6	V
		V_{CCO} ≥ 2.5 V	-0.5	3.6	V
V_{TS}	Voltage applied to high-impedance output	V_{CCO} < 2.5 V	-0.5	3.6	V
		V_{CCO} ≥ 2.5 V	-0.5	3.6	V
T_{stg}	Storage temperature	ambient	–65	150	°C
T_J	Junction temperature			125	°C
V_{ESD}	Electrostatic discharge voltage	Human Body Model(3)	2000		V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum DC undershoot below GND must be limited to either 0.5 V or 10 mA. During transitions, the device pins can undershoot to - 2 V or overshoot to 7 V, provided this overshoot or undershoot lasts less then 10 ns and with the forcing current being limited to 200 mA.
(3) JEDEC Std JESD22-A114A (C1 = 100 pF, R1 = 1500 Ω, R2 = 500 Ω).

Supply Voltage Requirements for Power-On Reset and Power-Down(1)

PARAMETER		MIN	MAX	UNIT
T_{VCC}	V_{CCINT} rise time from 0V to nominal voltage(2)	0.2	50	ms
V_{CCPOR}	POR threshold for V_{CCINT} supply	0.5	-	V
T_{OER}	OE/$\overline{\text{RESET}}$ release delay following POR(3)	0.5	30	ms
V_{CCPD}	Power-down threshold for V_{CCINT} supply	-	0.5	V
T_{RST}	Time required to trigger a device reset when the V_{CCINT} supply drops below the maximum V_{CCPD} threshold	10	-	ms

(1) V_{CCINT}, V_{CCO} and V_{CCJ} supplies can be applied in any order.
(2) At power up, the device requires the V_{CCINT} power supply to monotonically rise to the nominal operating voltage within the specified T_{VCC} rise time. If the power supply cannot meet this requirement, then the device might not perform power-on-reset properly. See Figure 6, page 11 in the Xilinx XCF16P (v2.18) Product Specification for more information.
(3) If the V_{CCINT} and V_{CCO} supplies do not reach their respective recommended operating conditions before the OE/$\overline{\text{RESET}}$ pin is released, then the configuration data from the PROM is not available at the recommended threshold levels. The configuration sequence must be delayed until both V_{CCINT} and V_{CCO} have reached their recommended operating conditions.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{CCINT} Internal voltage supply		1.65	1.8	2.0	V
V_{CCO} Supply voltage for output drivers	3.3 V Operation	3.0	3.3	3.6	V
	2.5 V Operation	2.3	2.5	2.7	V
	1.8 V Operation	1.7	1.8	1.9	V
V_{IL} Low-level input voltage	3.3 V Operation	0	-	0.8	V
	2.5 V Operation	0	-	0.7	V
	1.8 V Operation	-	-	20% V_{CCO}	V
V_{IH} High-level input voltage	3.3 V Operation	2.0	-	3.6	V
	2.5 V Operation	1.7	-	3.6	V
	1.8 V Operation	70% of V_{CCO}	-	3.6	V
T_{IN} Input signal transition time (measured between 10% V_{CCO} and 90% V_{CCO})		-	-	500	ns
V_O Output voltage		0	-	V_{CCO}	V
T_A Operating ambient temperature		-40	-	85	°C

REVISION HISTORY

Changes from Original (August 2012) to Revision A **Page**

- Changed the device From: Product Preview To: Production 1

Changes from Revision A (September 2012) to Revision B **Page**

- Changed the top-side marking in the "ORDERING INFORMATION table 2

Changes from Revision B (March 2013) to Revision C **Page**

- Added Top View of Device 1
- Added DLPR4101 "Load 4" enhanced functionality to Features 1
- Added DLPR410 and DLPR4101 (enhanced functionality PROM part number) to DLPR410 throughout document 1
- Added the Version column to the Ordering Inforamtion table 2
- Added DLPR4101 as TI part number 2510442-0006 2
- Added DLPR4101YVA as equivalent to TI part number 2510442-0006 3
- Added Reference to DLPC410 Data sheet 3
- Added DLPR410 to Figure 2 3
- Added Top View of Device to Figure 3 3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DLPR410YVA	ACTIVE	DSBGA	YVA	48	3	Pb-Free (RoHS)	Call TI	Level-3-260C-168 HR			Samples

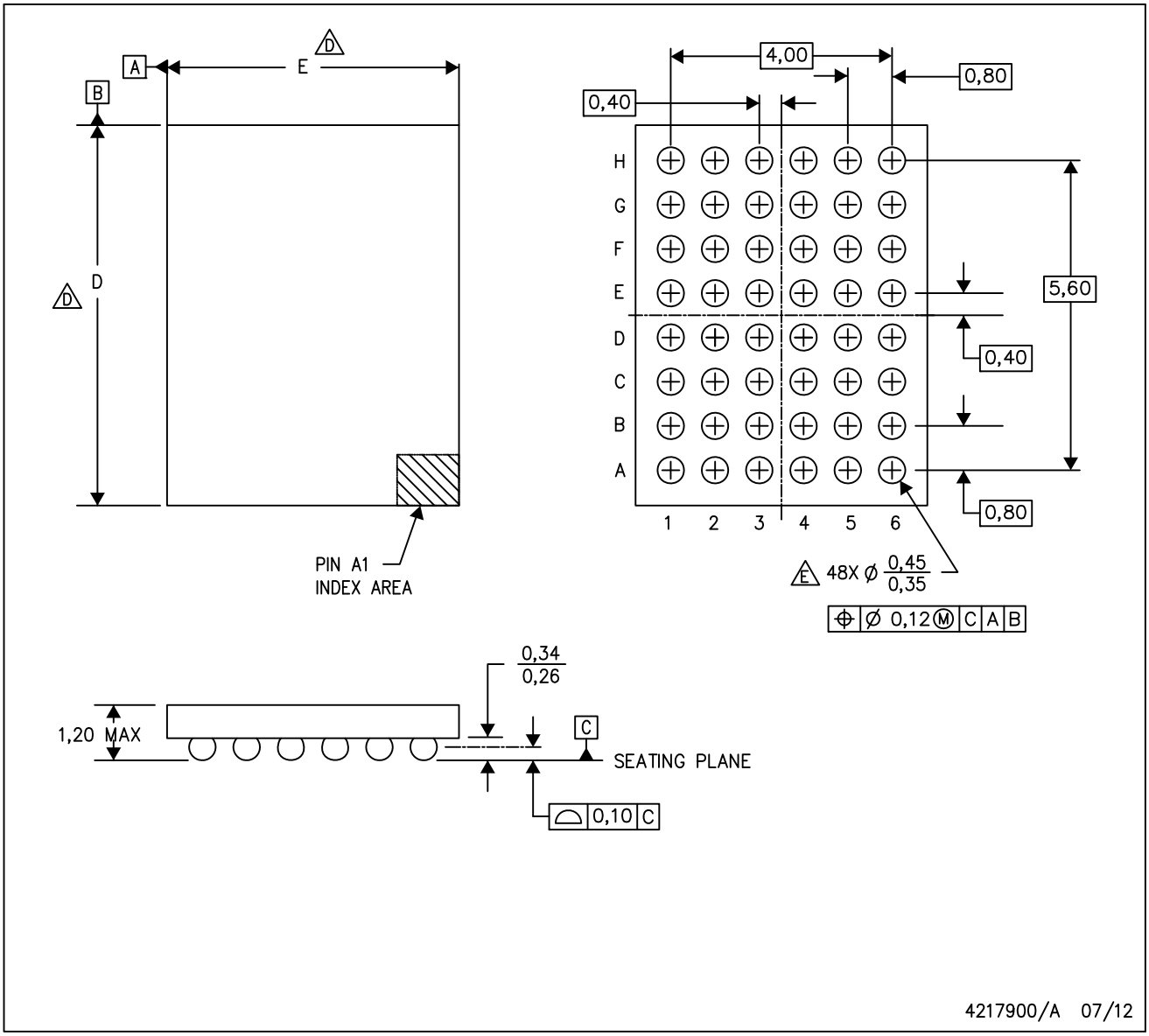
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

YVA (R–XBGA–N48) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
E. Reference Product Data Sheet for array population.
6 x 8 matrix pattern is shown for illustration only.
F. This package contains Pb–free balls.

NanoFree is a trademark of Texas Instruments.

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TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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