LM359 Dual, High Speed, Programmable, Current Mode (Norton) Amplifiers

Check for Samples: LM359

FEATURES

- **User Programmable Gain Bandwidth Product, Slew Rate, Input Bias Current, Output Stage Biasing Current and Total Device Power Dissipation**
- **High Gain Bandwidth Product (I_{SET} = 0.5 mA)**
  - **400 MHz for A_V = 10 to 100**
  - **30 MHz for A_V = 1**
- **High Slew Rate (I_{SET} = 0.5 mA)**
  - **60 V/µs for A_V = 10 to 100**
  - **30 V/µs for A_V = 1**
- **Current Differencing Inputs Allow High Common-Mode Input Voltages**
- **Operates from a Single 5V to 22V Supply**
- **Large Inverting Amplifier Output Swing, 2 mV to V_{CC} − 2V**
- **Low Spot Noise, 6 nV /√Hz, for f > 1 kHz**

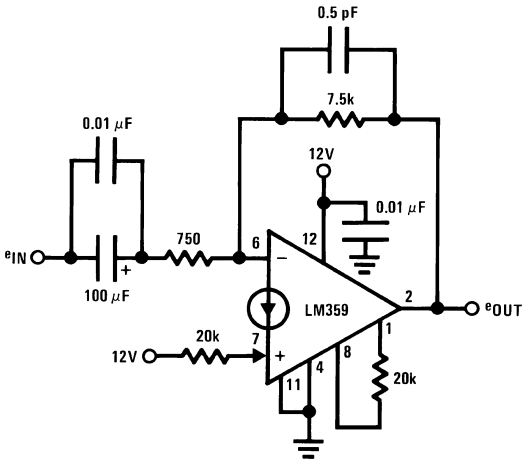
APPLICATIONS

- **General Purpose Video Amplifiers**
- **High Frequency, High Q Active Filters**
- **Photo-Diode Amplifiers**
- **Wide Frequency Range Waveform Generation Circuits**
- **All LM3900 AC Applications Work to Much Higher Frequencies**

DESCRIPTION

The LM359 consists of two current differencing (Norton) input amplifiers. Design emphasis has been placed on obtaining high frequency performance and providing user programmable amplifier operating characteristics. Each amplifier is broadbanded to provide a high gain bandwidth product, fast slew rate and stable operation for an inverting closed loop gain of 10 or greater. Pins for additional external frequency compensation are provided. The amplifiers are designed to operate from a single supply and can accommodate input common-mode voltages greater than the supply.

Typical Application



- A_V = 20 dB
- −3 dB bandwidth = 2.5 Hz to 25 MHz
- Differential phase error < 1° at 3.58 MHz
- Differential gain error < 0.5% at 3.58 MHz

Connection Diagram

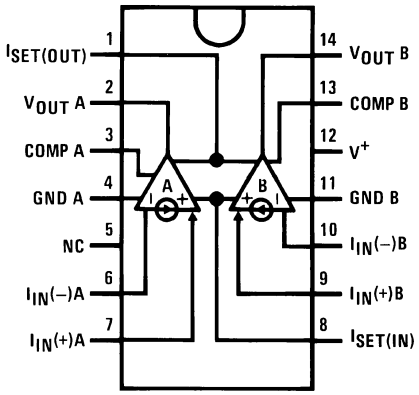


Figure 1. PDIP/SOIC Package Top View
See Package Number D0014A or NFF0014A

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage			22 V_{DC} or ±11 V_{DC}
Power Dissipation[3]		D Package	1W
		NFF Package	750 mW
Maximum T_J		D Package	+150°C
		NFF Package	+125°C
Thermal Resistance		D Package θ_{jA}	147°C/W still air
			110°C/W with 400 linear feet/min air flow
		NFF Package θ_{jA}	100°C/W still air
			75°C/W with 400 linear feet/min air flow
Input Currents, $I_{IN}(+)$ or $I_{IN}(-)$			10 mA_{DC}
Set Currents, $I_{SET(IN)}$ or $I_{SET(OUT)}$			2 mA_{DC}
Operating Temperature Range			0°C to +70°C
Storage Temperature Range			−65°C to +150°C
Lead Temperature		(Soldering, 10 sec.)	260°C
Soldering Information	PDIP Package	Soldering (10 sec.)	260°C
	SOIC Package	Vapor Phase (60 sec.)	215°C
		Infrared (15 sec.)	220°C

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) See Figure 22.

Electrical Characteristics

$I_{SET(IN)} = I_{SET(OUT)} = 0.5$ mA, $V_{supply} = 12$V, $T_A = 25$°C unless otherwise noted

Parameter	Conditions		Min	Typ	Max	Units
Open Loop Voltage	$V_{supply} = 12$V, $R_L = 1$k, f = 100 Hz		62	72		dB
Gain	$T_A = 125$°C			68		dB
Bandwidth Unity Gain	$R_{IN} = 1$ kΩ, $C_{comp} = 10$ pF		15	30		MHz
Gain Bandwidth Product, Gain of 10 to 100	$R_{IN} = 50$Ω to 200Ω		200	400		MHz
Slew Rate	Unity Gain	$R_{IN} = 1$ kΩ, $C_{comp} = 10$ pF		30		V/μs
	Gain of 10 to 100	$R_{IN} < 200$Ω		60		
Amplifier to Amplifier Coupling	f = 100 Hz to 100 kHz, $R_L = 1$k			−80		dB
Mirror Gain[1]	at 2 mA $I_{IN}(+)$, $I_{SET} = 5$ μA, $T_A = 25$°C		0.9	1.0	1.1	μA/μA
	at 0.2 mA $I_{IN}(+)$, $I_{SET} = 5$ μA Over Temp.		0.9	1.0	1.1	μA/μA
	at 20 μA $I_{IN}(+)$, $I_{SET} = 5$ μA Over Temp.		0.9	1.0	1.1	μA/μA
ΔMirror Gain[1]	at 20 μA to 0.2 mA $I_{IN}(+)$ Over Temp, $I_{SET} = 5$ μA			3	5	%
Input Bias Current	Inverting Input, $T_A = 25$°C			8	15	μA
	Over Temp.				30	μA
Input Resistance (βre)	Inverting Input			2.5		kΩ
Output Resistance	$I_{OUT} = 15$ mA rms, f = 1 MHz			3.5		Ω

(1) Mirror gain is the current gain of the current mirror which is used as the non-inverting input. $\left(A_I = \frac{I_{IN}(-)}{I_{IN}(+)}\right)$ ΔMirror Gain is the % change in A_I for two different mirror currents at any given temperature.

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Electrical Characteristics (continued)

$I_{SET(IN)} = I_{SET(OUT)} = 0.5$ mA, $V_{supply} = 12$V, $T_A = 25°C$ unless otherwise noted

Parameter	Conditions		Min	Typ	Max	Units
Output Voltage Swing (R_L = 600Ω)	V_{OUT} High	$I_{IN}(-)$ and $I_{IN}(+)$ Grounded	9.5	10.3		V
	V_{OUT} Low	$I_{IN}(-) = 100$ µA, $I_{IN}(+) = 0$		2	50	mV
Output Currents	Source	$I_{IN}(-)$ and $I_{IN}(+)$ Grounded, R_L = 100Ω	16	40		mA
	Sink (Linear Region)	V_{comp}−0.5V = V_{OUT} = 1V, $I_{IN}(+) = 0$		4.7		
	Sink (Overdriven)	$I_{IN}(-) = 100$ µA, $I_{IN}(+) = 0$, V_{OUT} Force = 1V	1.5	3		
Supply Current	Non-Inverting Input Grounded, $R_L = \infty$			18.5	22	mA
Power Supply Rejection(2)	f = 120 Hz, $I_{IN}(+)$ Grounded		40	50		dB

(2) See Figure 15 and Figure 16.

Typical Performance Characteristics

Open Loop Gain

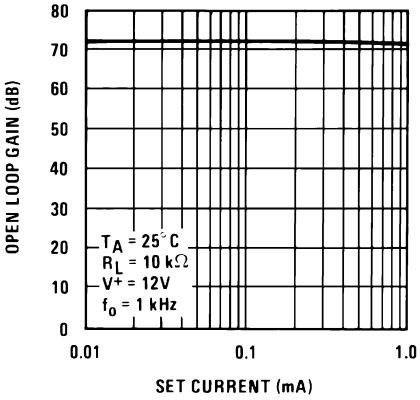
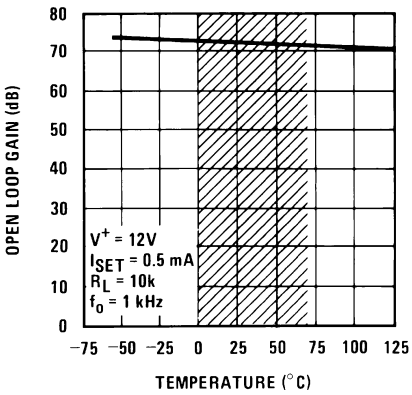


Figure 2.

Open Loop Gain



Note: Shaded area refers to LM359

Figure 3.

Open Loop Gain

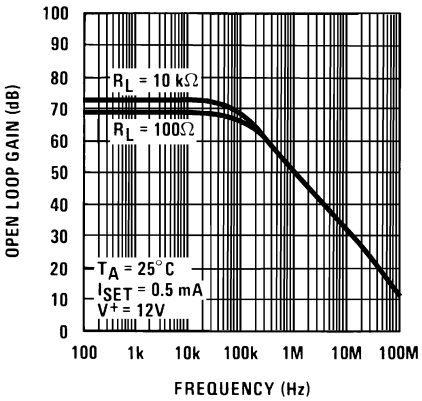


Figure 4.

Gain Bandwidth Product

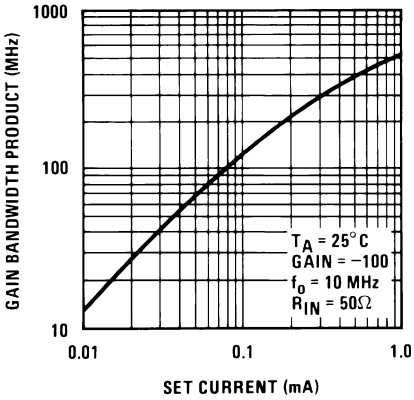


Figure 5.

Slew Rate

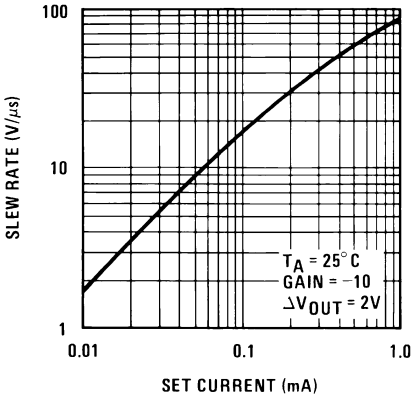


Figure 6.

Gain and Phase
Feedback Gain = − 100

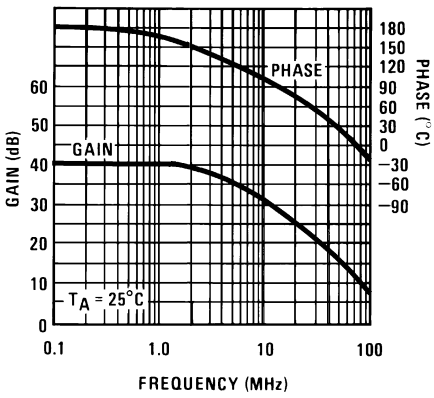


Figure 7.

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Typical Performance Characteristics (continued)

Inverting Input Bias Current

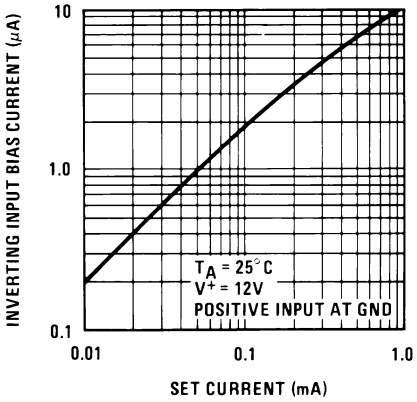
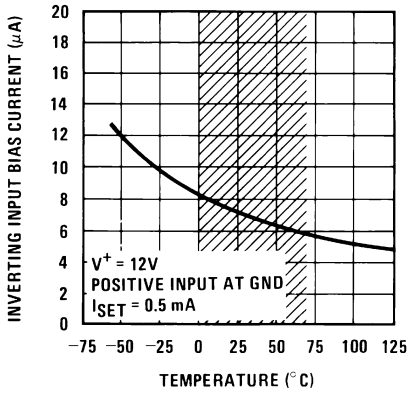


Figure 8.

Inverting Input Bias Current



Note: Shaded area refers to LM359

Figure 9.

Mirror Gain

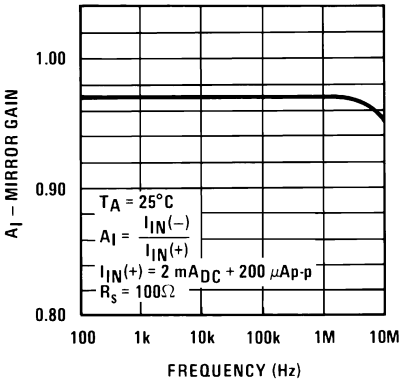
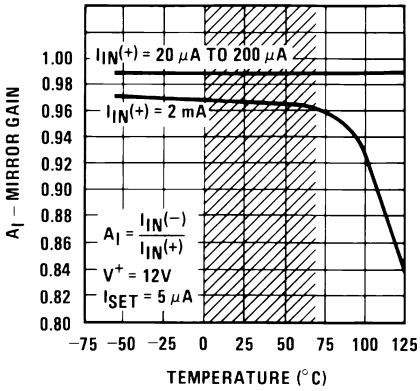


Figure 10.

Mirror Gain



Note: Shaded area refers to LM359

Figure 11.

Mirror Gain

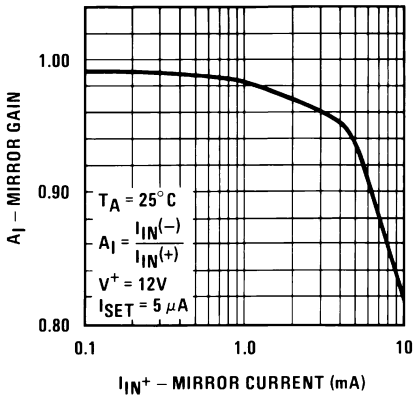
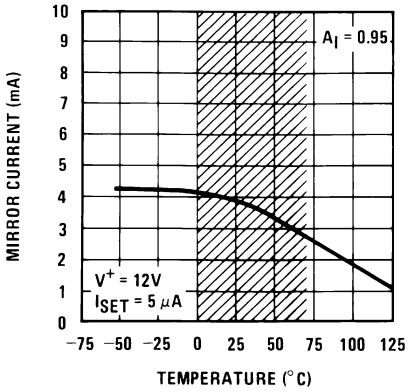


Figure 12.

Mirror Current



Note: Shaded area refers to LM359

Figure 13.

Typical Performance Characteristics (continued)

Supply Current

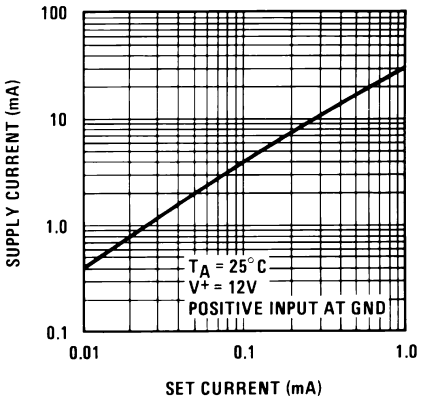


Figure 14.

Supply Rejection

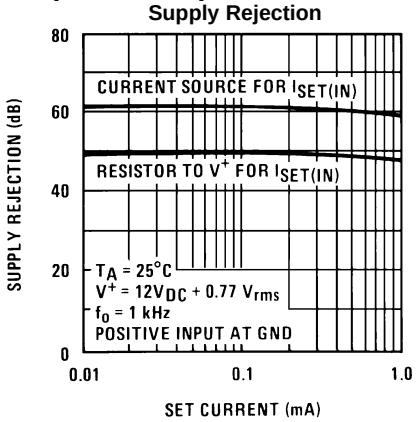


Figure 15.

Supply Rejection

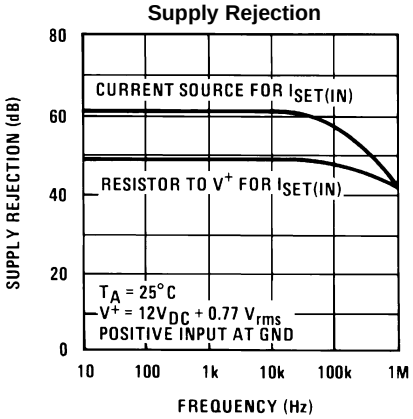


Figure 16.

Output Sink Current

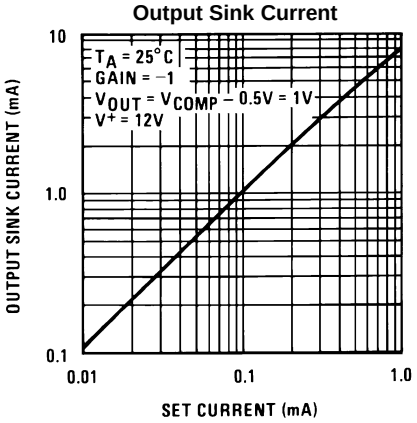


Figure 17.

Output Swing

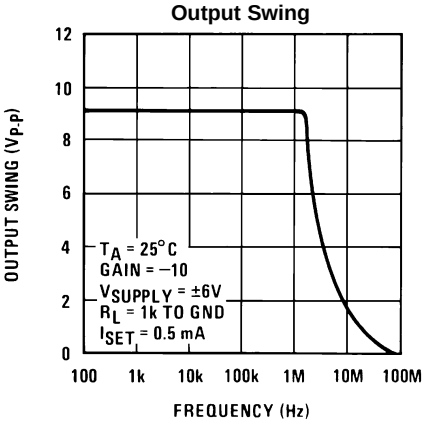


Figure 18.

Output Impedance

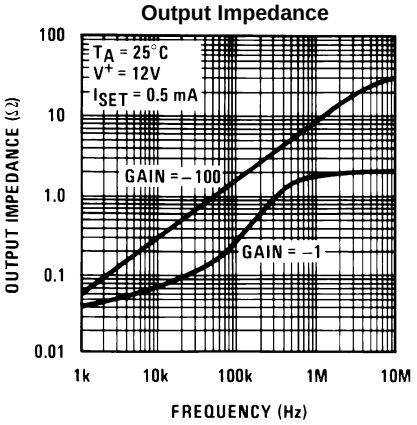


Figure 19.

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Typical Performance Characteristics (continued)

Amplifier to Amplifier Coupling (Input Referred)

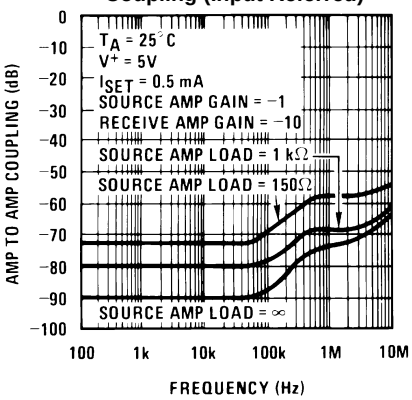


Figure 20.

Noise Voltage

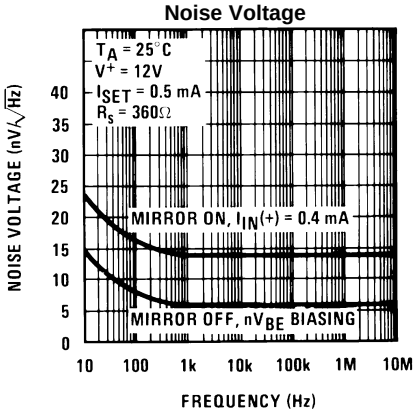
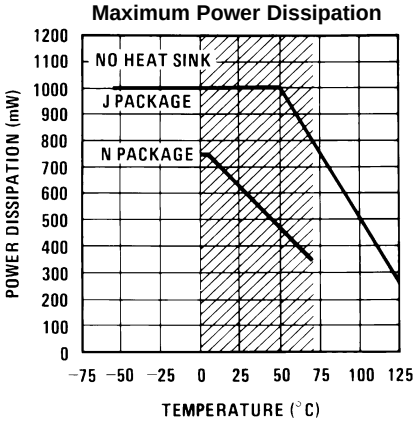


Figure 21.

Maximum Power Dissipation



Note: Shaded area refers to LM359J/LM359N

Figure 22.

APPLICATION HINTS

The LM359 consists of two wide bandwidth, decompensated current differencing (Norton) amplifiers. Although similar in operation to the original LM3900, design emphasis for these amplifiers has been placed on obtaining much higher frequency performance as illustrated in Figure 23.

This significant improvement in frequency response is the result of using a common-emitter/common-base (cascode) gain stage which is typical in many discrete and integrated video and RF circuit designs. Another versatile aspect of these amplifiers is the ability to externally program many internal amplifier parameters to suit the requirements of a wide variety of applications in which this type of amplifier can be used.

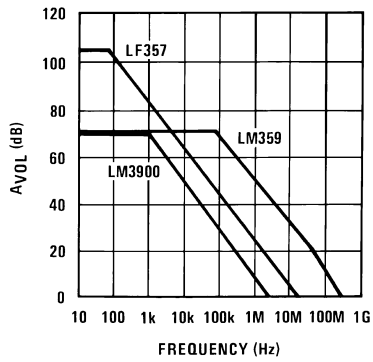


Figure 23.

DC BIASING

The LM359 is intended for single supply voltage operation which requires DC biasing of the output. The current mirror circuitry which provides the non-inverting input for the amplifier also facilitates DC biasing the output. The basic operation of this current mirror is that *the current (both DC and AC) flowing into the non-inverting input will force an equal amount of current to flow into the inverting input* . The mirror gain (A_I) specification is the measure of how closely these two currents match. For more details see TI Application Note AN-72 (Literature Number SNOA666).

DC biasing of the output is accomplished by establishing a reference DC current into the (+) input, $I_{IN}(+)$, and requiring the output to provide the (−) input current. This forces the output DC level to be whatever value necessary (within the output voltage swing of the amplifier) to provide this DC reference current, Figure 24.

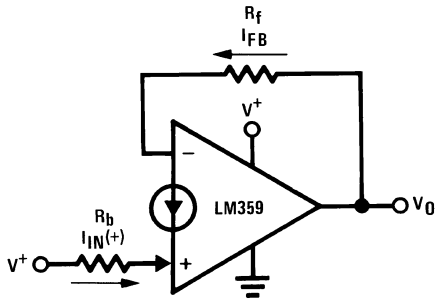


Figure 24.

$$V_{o(DC)} = V_{BE}(-) + I_{FB} R_f$$

$$I_{FB} = I_{IN}(+) A_I + I_b(-)$$

$$I_{IN}(+) = \frac{V^+ - V_{BE}(+)}{R_b}$$

$I_b(-)$ is the inverting input bias current

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The DC input voltage at each input is a transistor V_{BE}(≃ 0.6 V_{DC}) and must be considered for DC biasing. For most applications, the supply voltage, V^+, is suitable and convenient for establishing $I_{IN}(+)$. The inverting input bias current, $I_b(-)$, is a direct function of the programmable input stage current (see OPERATING CURRENT PROGRAMMABILITY (I_{SET})) and to obtain predictable output DC biasing set $I_{IN}(+) \geq 10 I_b(-)$.

The following figures illustrate typical biasing schemes for AC amplifiers using the LM359:

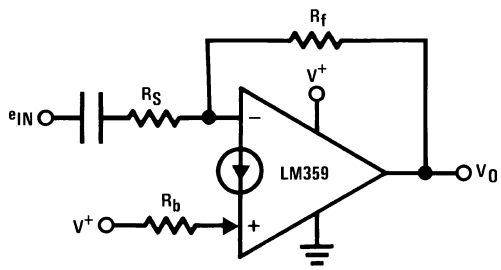

Figure 25. Biasing an Inverting AC Amplifier

$$A_{V(AC)} = -\frac{R_f}{R_s}$$

$$V_{o(DC)} = V_{BE}(-) + R_f\left[\frac{V^+ - V_{BE}(+)}{R_b} + I_b(-)\right]$$

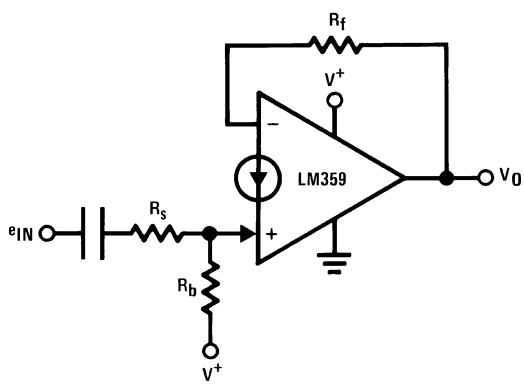

Figure 26. Biasing a Non-Inverting AC Amplifier

$$A_{V(AC)} = +\frac{R_f}{R_s + r_e}$$

$$V_{o(DC)} = V_{BE}(-) + R_f\left[\frac{V^+ - V_{BE}(+)}{R_b} + I_b(-)\right]$$

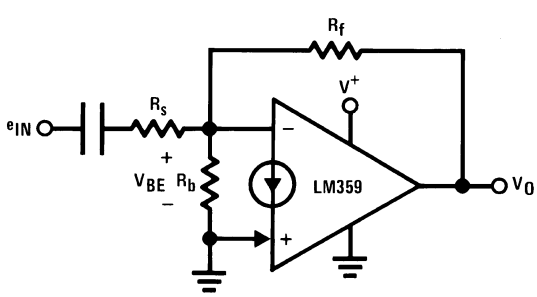

Figure 27. nV_{BE} Biasing

$$A_{V(AC)} = -\frac{R_f}{R_s}$$

$$V_{o(DC)} = V_{BE}(-)\left(1 + \frac{R_f}{R_B}\right) + I_b(-)R_f$$

The nV_{BE} biasing configuration is most useful for low noise applications where a reduced input impedance can be accommodated (see Typical Applications section).

OPERATING CURRENT PROGRAMMABILITY (I_{SET})

The input bias current, slew rate, gain bandwidth product, output drive capability and total device power consumption of both amplifiers can be simultaneously controlled and optimized via the two programming pins $I_{SET(OUT)}$ and $I_{SET(IN)}$.

$I_{SET(OUT)}$

The output set current ($I_{SET(OUT)}$) is equal to the amount of current sourced from pin 1 and establishes the class A biasing current for the Darlington emitter follower output stage. Using a single resistor from pin 1 to ground, as shown in Figure 28, this current is equal to:

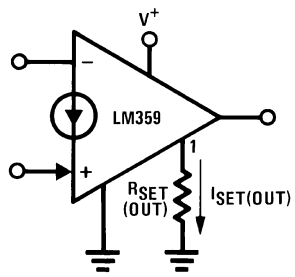

Figure 28. Establishing the Output Set Current

$$I_{SET(OUT)} = \frac{V^+ - V_{BE}}{R_{SET(OUT)} + 500\Omega}$$

The output set current can be adjusted to optimize the amount of current the output of the amplifier can sink to drive load capacitance and for loads connected to V^+. *The maximum output sinking current is approximately 10 times $I_{SET(OUT)}$.* This set current is best used to reduce the total device supply current if the amplifiers are not required to drive small load impedances.

$I_{SET(IN)}$

The input set current $I_{SET(IN)}$ is equal to the current flowing into pin 8. A resistor from pin 8 to V^+ sets this current to be:

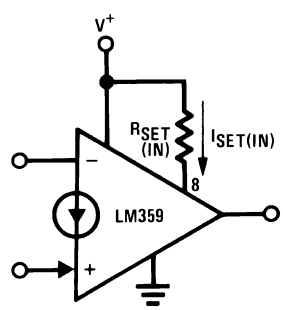

Figure 29. Establishing the Input Set Current

$$I_{SET(IN)} = \frac{V^+ - V_{BE}}{R_{SET(IN)} + 500\Omega}$$

$I_{SET(IN)}$ is most significant in controlling the AC characteristics of the LM359 as it directly sets the total input stage current of the amplifiers which determines the maximum slew rate, the frequency of the open loop dominant pole, the input resistance of the (−) input and the biasing current $I_b(-)$. All of these parameters are significant in wide band amplifier design. The input stage current is approximately 3 times $I_{SET(IN)}$ and by using this relationship the following first order approximations for these AC parameters are:

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$$S_{r(MAX)} = \text{max slew rate} \cong \frac{3\, I_{SET(IN)}\, (10^{-6})}{C_{comp}}\ (V/\mu s)$$

$$\text{frequency of dominant pole} \cong \frac{3\, I_{SET(IN)}}{2\pi\, C_{comp}\, A_{VOL}\, (0.026V)}\ (Hz)$$

$$\text{input resistance} = \beta re \cong \frac{150\ (0.026V)}{3 I_{SET(IN)}}\ (\Omega) \tag{1}$$

where C_{comp} is the total capacitance from the compensation pin (pin 3 or pin 13) to ground, A_{VOL} is the low frequency open loop voltage gain in V/V and an ambient temperature of 25°C is assumed (KT/q = 26 mV and β_{typ} = 150). $I_{SET(IN)}$ also controls the DC input bias current by the expression:

$$I_b(-) = \frac{3 I_{SET}}{\beta} \cong \frac{I_{SET}}{50} \text{ for NPN } \beta = 150 \tag{2}$$

which is important for DC biasing considerations.

The total device supply current (for both amplifiers) is also a direct function of the set currents and can be approximated by:

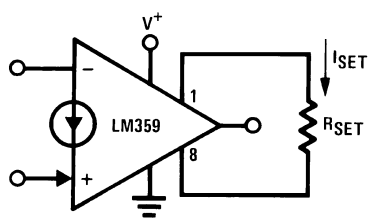
$$I_{supply} \simeq 27 \times I_{SET(OUT)} + 11 \times I_{SET(IN)} \tag{3}$$

with each set current programmed by individual resistors.

PROGRAMMING WITH A SINGLE RESISTOR

Operating current programming may also be accomplished using only one resistor by letting $I_{SET(IN)}$ equal $I_{SET(OUT)}$. The programming current is now referred to as I_{SET} and it is created by connecting a resistor from pin 1 to pin 8 (Figure 30).

$$I_{SET} = \frac{V^+ - 2\, V_{BE}}{R_{SET} + 1\ k\Omega} \text{ where } V_{BE} \cong 0.6V \tag{4}$$



$I_{SET(IN)} = I_{SET(OUT)} = I_{SET}$

Figure 30. Single Resistor Programming of I_{SET}

This configuration does not affect any of the internal set current dependent parameters differently than previously discussed except the total supply current which is now equal to:

$$I_{supply} \simeq 37 \times I_{SET} \tag{5}$$

Care must be taken when using resistors to program the set current to prevent significantly increasing the supply voltage above the value used to determine the set current. This would cause an increase in total supply current due to the resulting increase in set current and the maximum device power dissipation could be exceeded. The set resistor value(s) should be adjusted for the new supply voltage.

One method to avoid this is to use an adjustable current source which has voltage compliance to generate the set current as shown in Figure 31.

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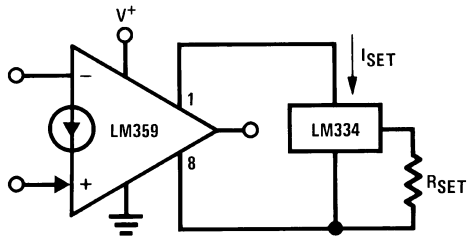

Figure 31. Current Source Programming of I_{SET}

$$I_{SET} = \frac{67.7\ mV}{R_{SET}}\ @25°C$$

This circuit allows I_{SET} to remain constant over the entire supply voltage range of the LM359 which also improves power supply ripple rejection as illustrated in the Typical Performance Characteristics. It should be noted, however, that the current through the LM334 as shown will change linearly with temperature but this can be compensated for (see LM334 data sheet).

Pin 1 must never be shorted to ground or pin 8 never shorted to V^+ without limiting the current to 2 mA or less to prevent catastrophic device failure.

CONSIDERATIONS FOR HIGH FREQUENCY OPERATION

The LM359 is intended for use in relatively high frequency applications and many factors external to the amplifier itself must be considered. Minimization of stray capacitances and their effect on circuit operation are the primary requirements. The following list contains some general guidelines to help accomplish this end:

1. Keep the leads of all external components as short as possible.
2. Place components conducting signal current from the output of an amplifier away from that amplifier's non-inverting input.
3. Use reasonably low value resistances for gain setting and biasing.
4. Use of a ground plane is helpful in providing a shielding effect between the inputs and from input to output. Avoid using vector boards.
5. Use a single-point ground and single-point supply distribution to minimize crosstalk. Always connect the two grounds (one from each amplifier) together.
6. Avoid use of long wires (> 2″) but if necessary, use shielded wire.
7. Bypass the supply close to the device with a low inductance, low value capacitor (typically a 0.01 μF ceramic) to create a good high frequency ground. If long supply leads are unavoidable, a small resistor (~10Ω) in series with the bypass capacitor may be needed and using shielded wire for the supply leads is also recommended.

COMPENSATION

The LM359 is internally compensated for stability with closed loop inverting gains of 10 or more. For an inverting gain of less than 10 and all non-inverting amplifiers (the amplifier always has 100% negative current feedback regardless of the gain in the non-inverting configuration) some external frequency compensation is required because the stray capacitance to ground from the (−) input and the feedback resistor add additional lagging phase within the feedback loop. The value of the input capacitance will typically be in the range of 6 pF to 10 pF for a reasonably constructed circuit board. When using a feedback resistance of 30 kΩ or less, the best method of compensation, without sacrificing slew rate, is to add a lead capacitor in parallel with the feedback resistor with a value on the order of 1 pF to 5 pF as shown in Figure 32.

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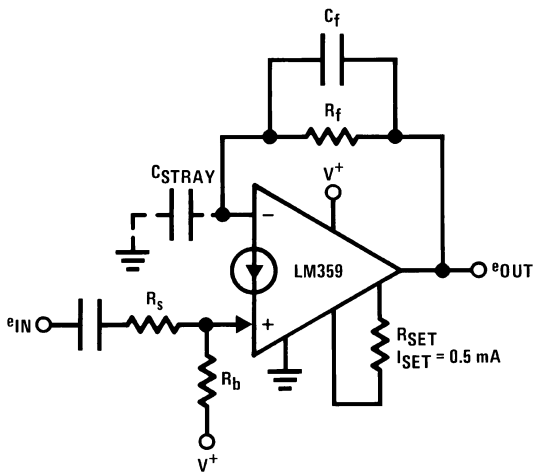

C_f = 1 pF to 5 pF for stability

Figure 32. Best Method of Compensation

Another method of compensation is to increase the effective value of the internal compensation capacitor by adding capacitance from the COMP pin of an amplifier to ground. An external 20 pF capacitor will generally compensate for all gain settings but will also reduce the gain bandwidth product and the slew rate. These same results can also be obtained by reducing $I_{SET(IN)}$ if the full capabilities of the amplifier are not required. This method is termed over-compensation.

Another area of concern from a stability standpoint is that of capacitive loading. The amplifier will generally drive capacitive loads up to 100 pF without oscillation problems. Any larger C loads can be isolated from the output as shown in Figure 33. Over-compensation of the amplifier can also be used if the corresponding reduction of the GBW product can be afforded.

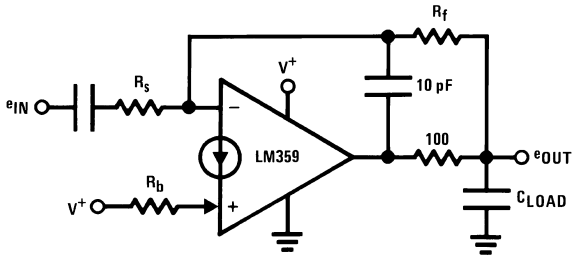

Figure 33. Isolating Large Capacitive Loads

In most applications using the LM359, the input signal will be AC coupled so as not to affect the DC biasing of the amplifier. This gives rise to another subtlety of high frequency circuits which is the effective series inductance (ESL) of the coupling capacitor which creates an increase in the impedance of the capacitor at high frequencies and can cause an unexpected gain reduction. Low ESL capacitors like solid tantalum for large values of C and ceramic for smaller values are recommended. A parallel combination of the two types is even better for gain accuracy over a wide frequency range.

AMPLIFIER DESIGN EXAMPLES

The ability of the LM359 to provide gain at frequencies higher than most monolithic amplifiers can provide makes it most useful as a basic broadband amplification stage. The design of standard inverting and non-inverting amplifiers, though different than standard op amp design due to the current differencing inputs, also entail subtle design differences between the two types of amplifiers. These differences will be best illustrated by design examples. For these examples a practical video amplifier with a passband of 8 Hz to 10 MHz and a gain of 20 dB will be used. It will be assumed that the input will come from a 75Ω source and proper signal termination will be considered. The supply voltage is 12 V_{DC} and single resistor programming of the operating current, I_{SET}, will be used for simplicity.

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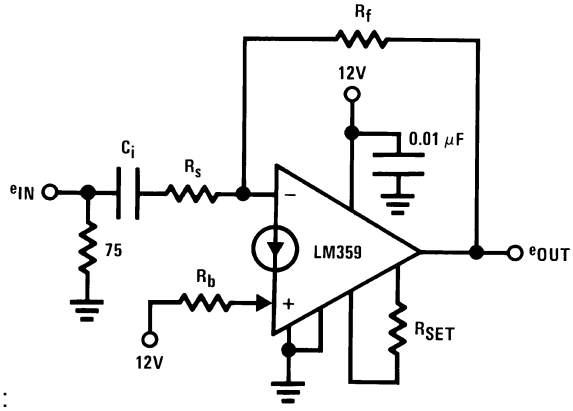
AN INVERTING VIDEO AMPLIFIER



1. Basic circuit configuration:
2. Determine the required I_{SET} from the characteristic curves for gain bandwidth product.GBW_{MIN}= 10 × 10 MHz = 100 MHzFor a flat response to 10 MHz a closed loop response to two octaves above 10 MHz (40 MHz) will be sufficient.

   Actual GBW = 10 × 40 MHz = 400 MHz I_{SET} required = 0.5 mA $R_{SET} = \frac{V^+ - 2\,V_{BE}}{I_{SET}} - 1\,k\Omega = \frac{10.8V}{0.5\,mA} - 1\,k\Omega = 20.6\,k\Omega$
3. Determine maximum value for R_f to provide stable DC biasing $I_{f(MIN)} \geq 10 \times \frac{3\,I_{SET}}{\beta} = 100\,\mu A$ minimum DC feedback current Optimum

   $$V_{oDC(opt)} = \frac{V_{o(MAX)} - V_{o(MIN)}}{2} + V_{o(MIN)} \approx \frac{(V^+ - 3\,V_{BE}) - 2\,mV}{2}$$

   output DC level for maximum symmetrical swing without clipping is: $V_{oDC(opt)} \cong \frac{12 - 1.8V}{2} = \frac{10.2V}{2} = 5.1\,V_{DC}$ $R_{f(MAX)}$ can now be found: $R_{f(MAX)} = \frac{V_{oDC(opt)} - V_{BE}(-)}{I_{f(MIN)}} = \frac{5.1V - 0.6V}{100\,\mu A} = 45\,k\Omega$ This value should not be exceeded for predictable DC biasing.
4. Select R_s to be large enough so as not to appreciably load the input termination resistance:$R_s \geq 750\Omega$; Let R_s = 750Ω
5. Select R_f for appropriate gain: $A_V = -\frac{R_f}{R_s}$ so; $R_f = 10\,R_s = 7.5\,k\Omega$ 7.5 kΩ is less than the calculated $R_{f(MAX)}$ so DC predictability is insured.
6. Since R_f = 7.5k, for the output to be biased to 5.1 V_{DC},

   the reference current $I_{IN}(+)$ must be: $I_{IN}(+) = \frac{5.1V - V_{BE}(-)}{R_f} = \frac{5.1V - 0.6V}{7.5\,k\Omega} = 600\,\mu A$

   Now R_b can be found by: $R_b = \frac{V^+ - V_{BE}(+)}{I_{IN}(+)} = \frac{12 - 0.6}{600\,\mu A} = 19\,k\Omega$
7. Select C_i to provide the proper gain for the 8 Hz minimum input frequency:

   $C_i \geq \frac{1}{2\pi\,R_s\,(f_{low})} = \frac{1}{2\pi\,(750\Omega)\,(8\,Hz)} = 26\,\mu F$ A larger value of C_i will allow a flat frequency response down to 8 Hz and a 0.01 μF ceramic capacitor in parallel with C_i will maintain high frequency gain accuracy.
8. Test for peaking of the frequency response and add a feedback “lead” capacitor to compensate if necessary.

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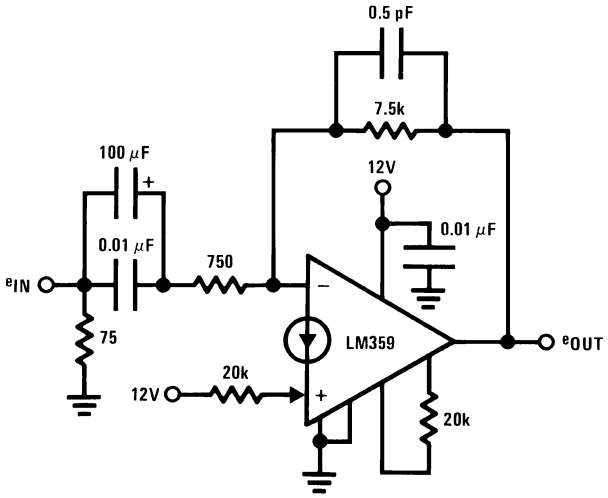
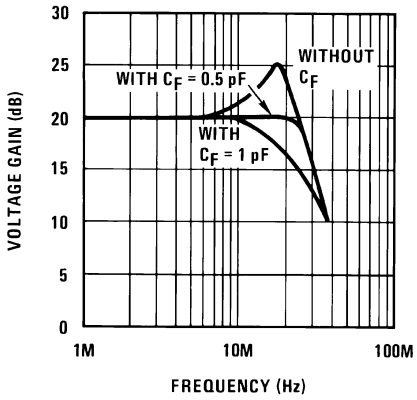


Figure 34. Final Circuit Using Standard 5% Tolerance Resistor Values



$V_{o(DC)}$ = 5.1V
Differential phase error < 1° for 3.58 MHz f_{IN}
Differential gain error < 0.5% for 3.58 MHz f_{IN}
$f_{-3\ dB}$ low = 2.5 Hz

Figure 35. Circuit Performance

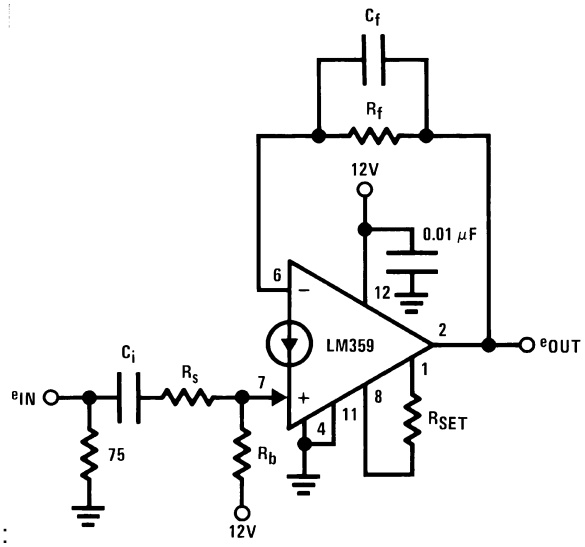
A NON-INVERTING VIDEO AMPLIFIER

For this case several design considerations must be dealt with.

- The output voltage (AC and DC) is strictly a function of the size of the feedback resistor and the sum of AC and DC “mirror current” flowing into the (+) input.
- The amplifier always has 100% current feedback so external compensation is required. Add a small (1 pF–5 pF) feedback capacitance to leave the amplifier's open loop response and slew rate unaffected.
- To prevent saturating the mirror stage the total AC and DC current flowing into the amplifier's (+) input should be less than 2 mA.
- The output's maximum negative swing is one diode above ground due to the V_{BE} diode clamp at the (−) input.

DESIGN EXAMPLE

e_{IN} = 50 mV (MAX), f_{IN} = 10 MHz (MAX), desired circuit BW = 20 MHz, A_V = 20 dB, driving source impedance = 75Ω, V^+ = 12V.



1. Basic circuit configuration:
2. Select I_{SET} to provide adequate amplifier bandwidth so that the closed loop bandwidth will be determined by R_f and C_f. To do this, the set current should program an amplifier open loop gain of at least 20 dB at the desired closed loop bandwidth of the circuit. For this example, an I_{SET} of 0.5 mA will provide 26 dB of open loop gain at 20 MHz which will be sufficient. Using single resistor programming for I_{SET}: $R_{SET} = \frac{V^+ - 2\,V_{BE}}{I_{SET}} - 1\,k\Omega = 20.6\,k\Omega$
3. Since the closed loop bandwidth will be determined by R_f and C_f $\left(f_{-3\,dB} = \frac{1}{2\pi\,R_f\,C_f}\right)$ to obtain a 20 MHz bandwidth, both R_f and C_f should be kept small. It can be assumed that C_f can be in the range of 1 pF to 5 pF for carefully constructed circuit boards to insure stability and allow a flat frequency response. This will limit the value of R_f to be within the range of: $\frac{1}{2\pi\,5\,pF\,20\,MHz} \le R_f \le \frac{1}{2\pi\,1\,pF\,20\,MHz}$ or $1.6\,k\Omega \le R_f \le 7.96\,k\Omega$ Also, for a closed loop gain of +10, R_f must be 10 times $R_s + r_e$ where r_e is the mirror diode resistance.
4. So as not to appreciably load the 75Ω input termination resistance the value of ($R_s + r_e$) is set to 750Ω.
5. For A_v = 10; R_f is set to 7.5 kΩ.
6. The optimum output DC level for symmetrical AC swing is: $V_{oDC(opt)} = \frac{V_{o(MAX)} - V_{o(MIN)}}{2} + V_{o(MIN)} = \frac{(12 - 1.8)V - 0.6V}{2} + 0.6V = 5.4\,V_{DC}$
7. The DC feedback current must be: $I_{FB} = \frac{V_{oDC(opt)} - V_{BE}(-)}{R_f} = \frac{5.4V - 0.6V}{7.5k} = 640\,\mu A = I_{IN}(+)$ DC biasing predictability will be insured because 640 µA is greater than the minimum of I_{SET}/5 or 100 µA.
8. For gain accuracy the total AC and DC mirror current should be less than 2 mA. For this example the maximum AC mirror current will be: $\frac{\pm e_{in\,peak}}{R_s + r_e} = \frac{\pm 50\,mV}{750\Omega} = \pm 66\,\mu A$ therefore the total mirror current range will be 574 µA to 706 µA which will insure gain accuracy.
9. R_b can now be found: $R_b = \frac{V^+ - V_{BE}(+)}{I_{IN}(+)} = \frac{12 - 0.6}{640\,\mu A} = 17.8\,k\Omega$
10. Since $R_s + r_e$ will be 750Ω and r_e is fixed by the DC mirror current to be: $r_e = \frac{KT}{q\,I_{IN}(+)} = \frac{26\,mV}{640\,\mu A} \cong 40\Omega$ at 25°C R_s must be 750Ω–40Ω or 710Ω which can be a 680Ω resistor in series with a 30Ω resistor which are standard 5% tolerance resistor values.

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11. As a final design step, C_i must be selected to pass the lower passband frequency corner of 8 Hz for this example. $C_i = \frac{1}{2\pi (R_s + r_e) f_{low}} = \frac{1}{2\pi (750\Omega) (8\ Hz)} = 26.5\ \mu F$ A larger value may be used and a 0.01 µF ceramic capacitor in parallel with C_i will maintain high frequency gain accuracy.

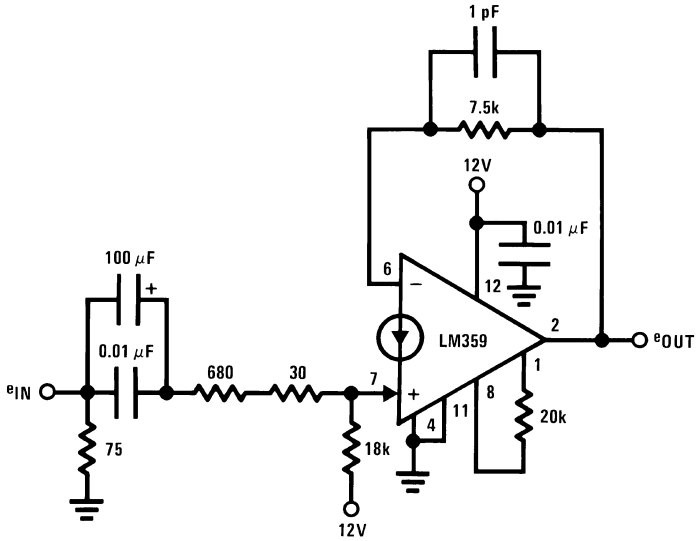
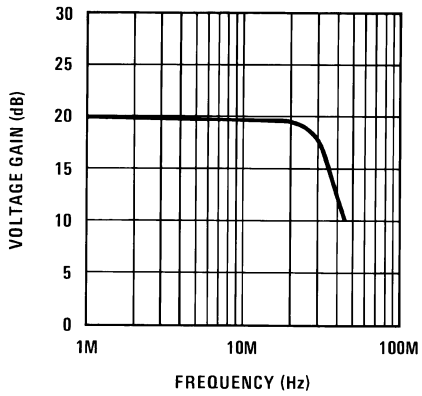


Figure 36. Final Circuit Using Standard 5% Tolerance Resistor Values



$V_{o(DC)}$ = 5.4V
Differential phase error < 0.5°
Differential gain error < 2%
$f_{-3\ dB}$ low = 2.5 Hz

Figure 37. Circuit Performance

GENERAL PRECAUTIONS

The LM359 is designed primarily for single supply operation but split supplies may be used if the negative supply voltage is well regulated as the amplifiers have no negative supply rejection.

The total device power dissipation must always be kept in mind when selecting an operating supply voltage, the programming current, I_{SET}, and the load resistance, particularly when DC coupling the output to a succeeding stage. To prevent damaging the current mirror input diode, the mirror current should always be limited to 10 mA, or less, which is important if the input is susceptible to high voltage transients. The voltage at any of the inputs must not be forced more negative than −0.7V without limiting the current to 10 mA.

The supply voltage must never be reversed to the device; however, plugging the device into a socket backwards would then connect the positive supply voltage to the pin that has no internal connection (pin 5) which may prevent inadvertent device failure.

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Typical Applications

DC Coupled Inputs

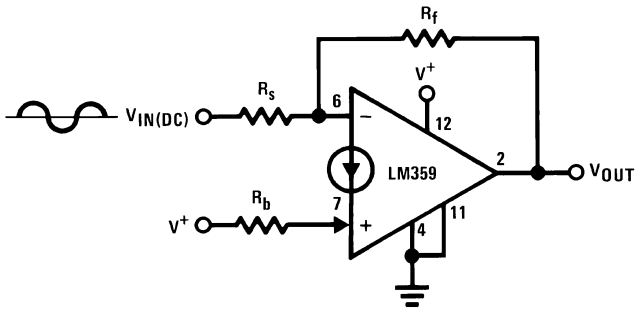

Figure 38. Inverting

$$V_{o(DC)} = \left[\frac{V^+ - V_{BE}(+)}{R_b} - \frac{V_{IN(DC)} - V_{BE}(-)}{R_s}\right] R_f + V_{BE}(-)$$

$$A_{V(AC)} = \frac{R_f}{R_s}$$

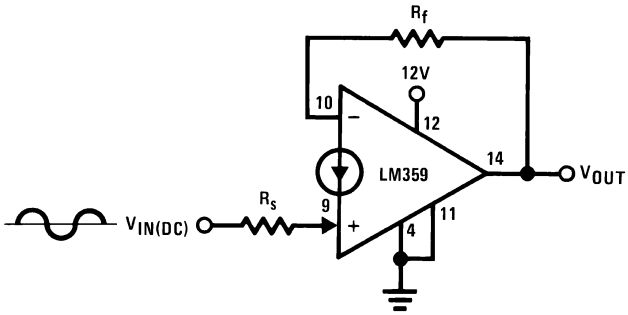

Figure 39. Non-Inverting

$$V_{o(DC)} = V_{BE}(-) + \frac{(V_{IN(DC)} - V_{BE}(+))\, R_f}{R_s}$$

$$A_{V(AC)} = +\frac{R_f}{R_s + r_e(+)}$$

- Eliminates the need for an input coupling capacitor
- Input DC level must be stable and can exceed the supply voltage of the LM359 provided that maximum input currents are not exceeded.

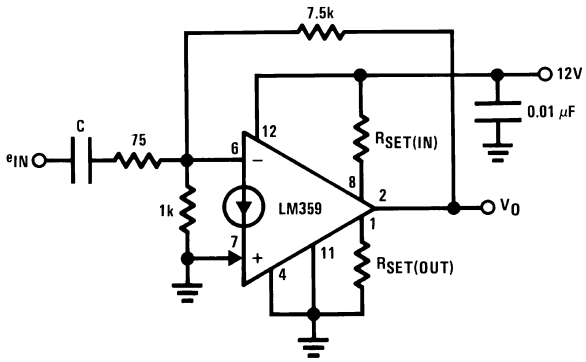

Figure 40. Noise Reduction using nV_{BE} Biasing

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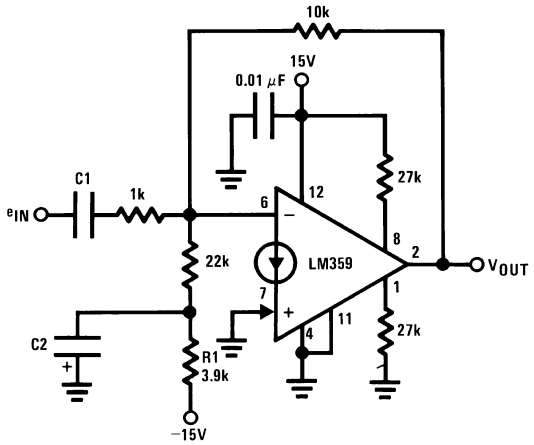


- R1 and C2 provide additional filtering of the negative biasing supply

Figure 41. nV_{BE} Biasing with a Negative Supply

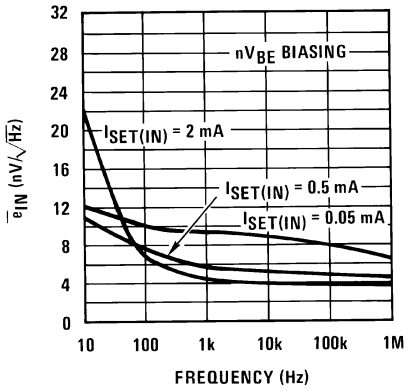
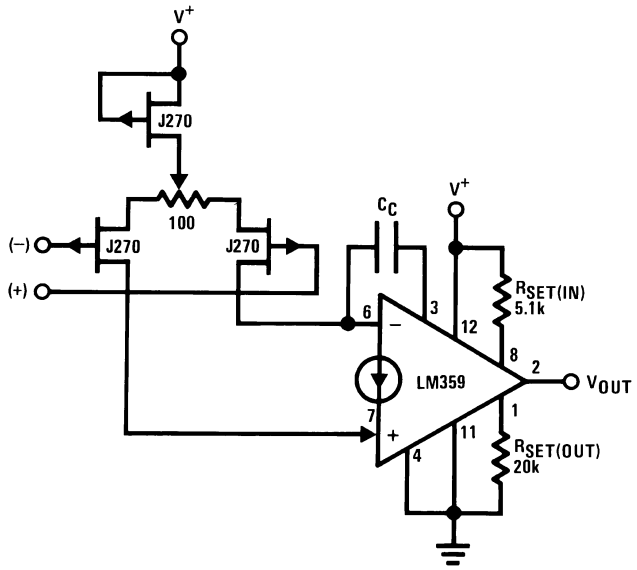
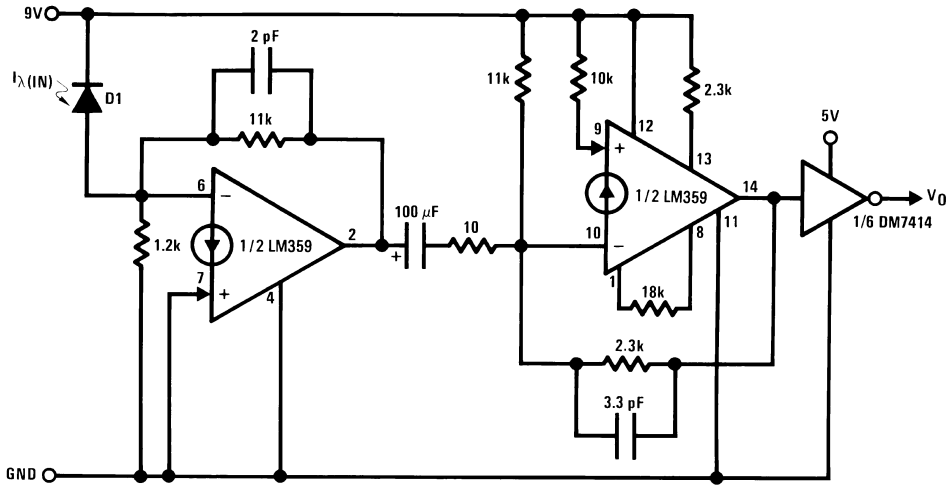


Figure 42. Typical Input Referred Noise Performance



- FET input voltage mode op amp
- For A_V = +1; BW = 40 MHz, S_r = 60 V/µs; C_C = 51 pF
- For A_V = +11; BW = 24 MHz, S_r = 130 V/µs; C_C = 5 pF
- For A_V = +100; BW = 4.5 MHz, S_r = 150 V/µs; C_C = 2 pF
- V_{OS} is typically <25 mV; 100Ω potentiometer allows a V_{OS} adjust range of ≈ ±200 mV
- Inputs must be DC biased for single supply operation

Figure 43. Adding a JFET Input Stage



D1 ~ RCA N-Type Silicon P-I-N Photodiode

- Frequency response of greater than 10 MHz
- If slow rise and fall times can be tolerated the gate on the output can be removed. In this case the rise and the fall time of the LM359 is 40 ns.
- T_{PDL} = 45 ns, T_{PDH} = 50 ns – T^2L output

Figure 44. Photo Diode Amplifier

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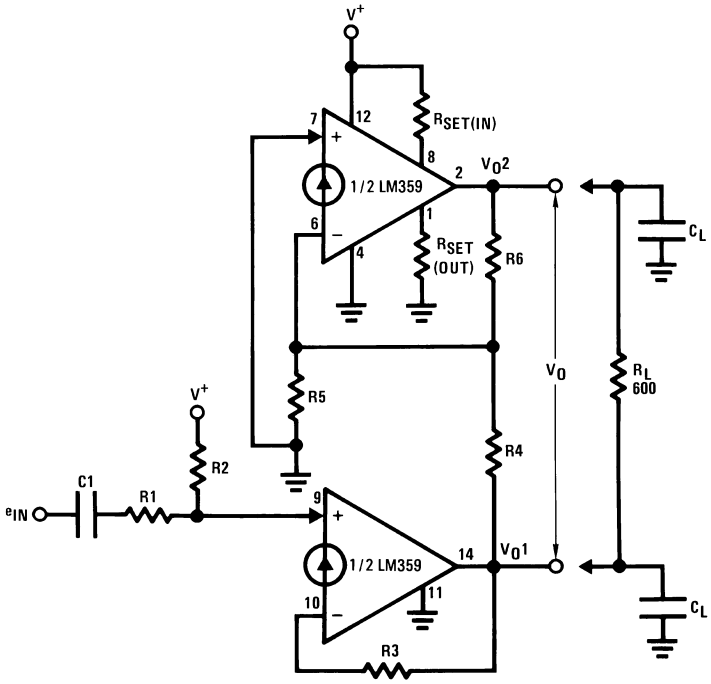
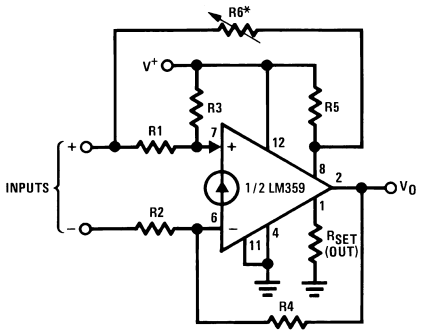


$$\text{For } V_o1 = V_o2 = \frac{V^+}{2}, \quad \frac{R3}{R2} = \frac{V^+ - 2\phi}{2\,(V^+ - \phi)}, \quad \frac{R6}{R5} = \frac{V^+ - 2\phi}{\phi} \text{ where } \phi \approx 0.6V$$

$$A_V = \frac{R3}{R1}\left(\frac{R6}{R4} + 1\right)$$

- 1 MHz−3 dB bandwidth with gain of 10 and 0 dbm into 600Ω
- 0.3% distortion at full bandwidth; reduced to 0.05% with bandwidth of 10 kHz
- Will drive C_L = 1500 pF with no additional compensation, ±0.01 μF with C_{comp} = 180 pF
- 70 dB signal to noise ratio at 0 dbm into 600Ω, 10 kHz bandwidth

Figure 45. Balanced Line Driver



$$V_{o(DC)} = \frac{R4}{R3}(V^{+} - \phi) \text{ where } \phi = 0.6V$$

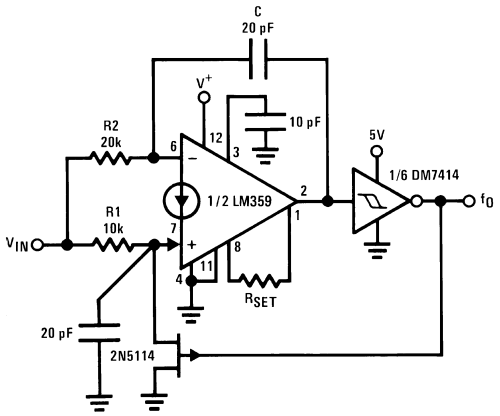
$$A_V = \frac{R4}{R1} \text{ for } R1 = R2$$

- CMRR is adjusted for max at expected CM input signal

$$R6 \approx \frac{R5}{5}, \text{ for } R5 = 100\ k\Omega$$

- Wide bandwidth
- 70 dB CMRR typ
- Wide CM input voltage range

Figure 46. Difference Amplifier



$$f_o = \frac{V_{IN} - \phi}{4\ C\Delta V\ R1}$$

where: $R2 = 2R1$

ϕ = amplifier input voltage = 0.6V

ΔV = DM7414 hysteresis, typ 1V

- 5 MHz operation
- T^2L output

Figure 47. Voltage Controlled Oscillator

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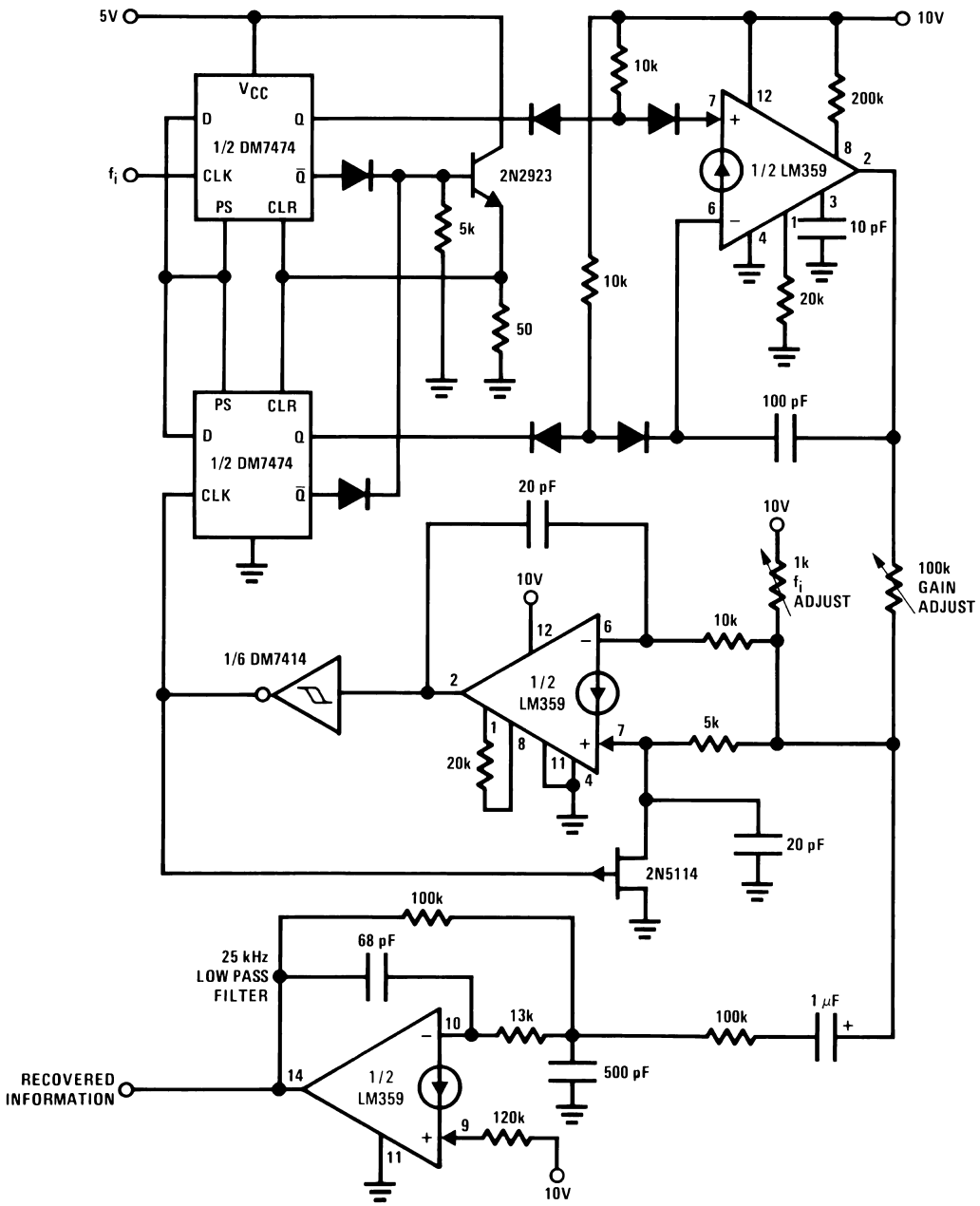
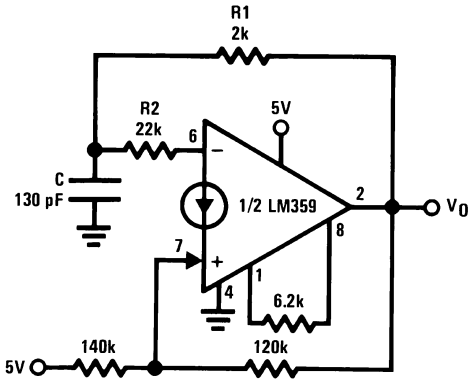


- Up to 5 MHz operation
- T^2L compatible input

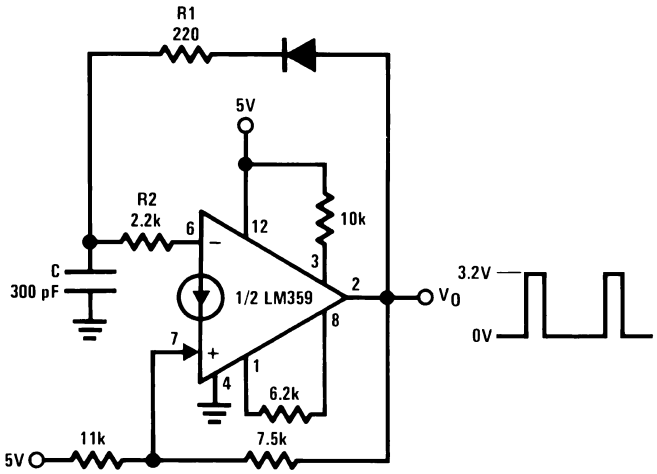
All diodes = 1N914

Figure 48. Phase Locked Loop



f = 1 MHz
Output is TTL compatible
Frequency is adjusted by R1 & C (R1 ≪ R2)

Figure 49. Squarewave Generator



Output is TTL compatible
Duty cycle is adjusted by R1
Frequency is adjusted by C
f = 1 MHz
Duty cycle = 20%

Figure 50. Pulse Generator

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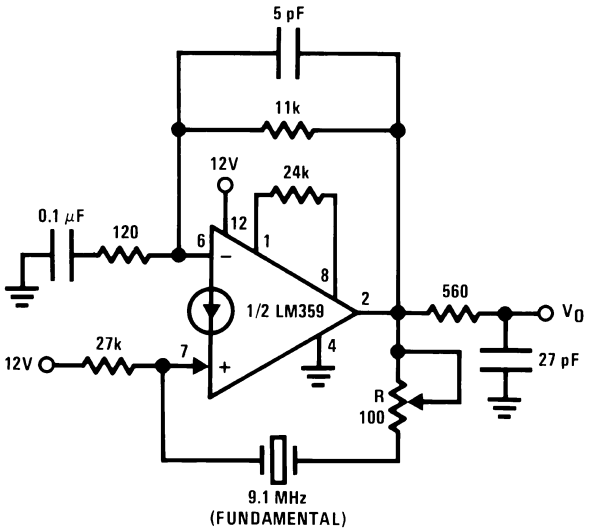
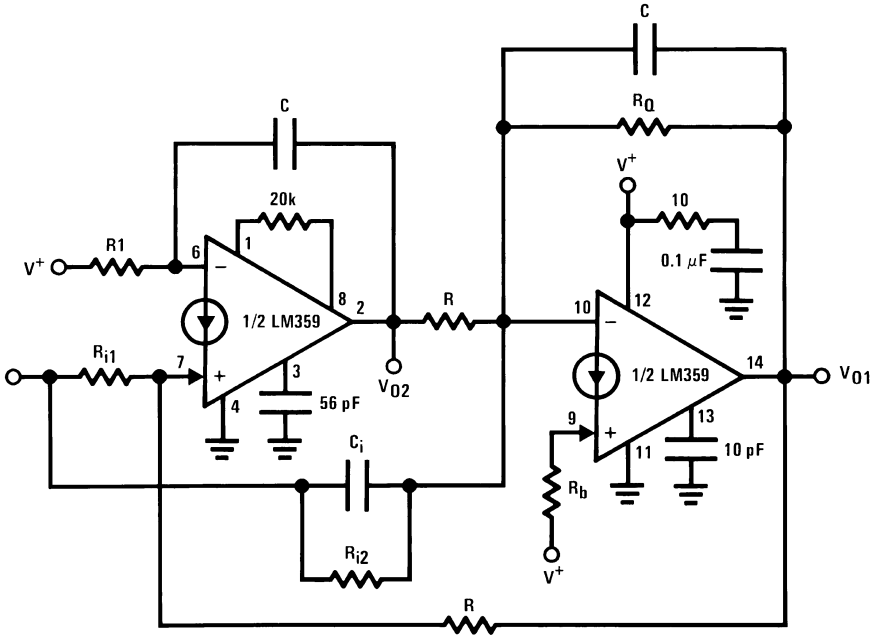


V_o = 500 mVp-p
f = 9.1 MHz
THD < 2.5%

Figure 51. Crystal Controlled Sinewave Oscillator



- The high speed of the LM359 allows the center frequency Q_o product of the filter to be: $f_o \times Q_o \leq 5$ MHz
- The above filter(s) maintain performance over wide temperature range
- One half of LM359 acts as a true non-inverting integrator so only 2 amplifiers (instead of 3 or 4) are needed for the biquad filter structure

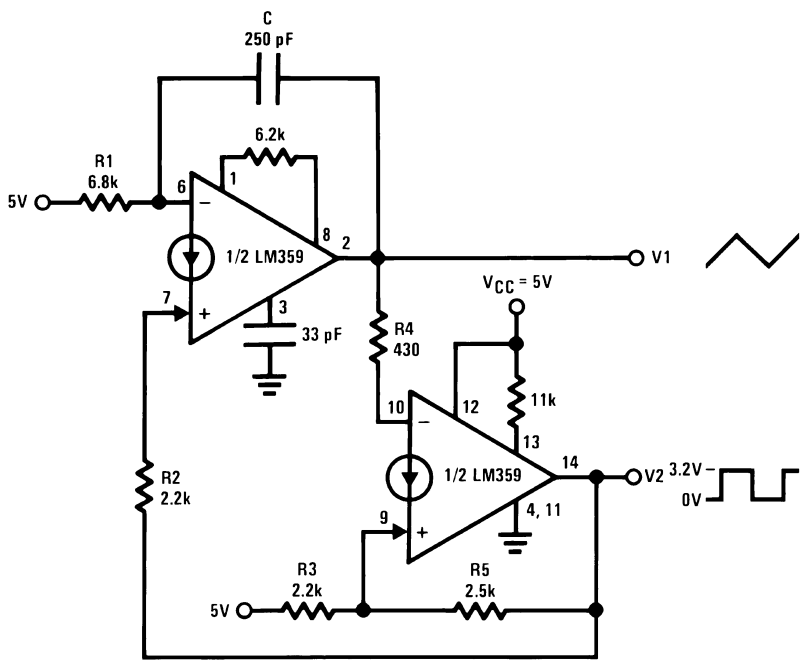
Figure 52. High Performance 2 Amplifier Biquad Filter(s)

Table 1. DC Biasing Equations for $V_{01(DC)} \simeq V_{02(DC)} \simeq V^+/2$

Type I	$\frac{2\,V_{IN(DC)}}{V^+\,(R_{i2})} + \frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}$; R1 = 2R
Type II	$\frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}$; R1 = 2R
Type III	$\frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}; \frac{1}{R1} = \frac{V_{IN(DC)}}{V^+\,(R_{i1})} + \frac{1}{2R}$

Table 2. Analysis and Design Equations

Type	V_{O1}	V_{O2}	C_i	R_{i2}	R_{i1}	f_o	Q_o	f_Z(notch)	$H_{o(LP)}$	$H_{o(BP)}$	$H_{o(HP)}$	$H_{o(BR)}$
I	BP	LP	O	R_{i2}	∞	1/2πRC	R_Q/R	—	R/R_{i2}	R_Q/R_{i2}	—	—
II	HP	BP	C_i	∞	∞	1/2πRC	R_Q/R	—	—	R_QC_i/RC	C_i/C	—
III	Notch/ BR	—	C_i	∞	R_{i1}	1/2πRC	R_Q/R	$1/2\pi\sqrt{RR_iCC_i}$	—	—	—	$H_o\big\vert_{f\to\infty} = C_i/C$ $H_o\big\vert_{f\to 0} = C/R_i$



V2 output is TTL compatible
R2 adjusts for symmetry of the triangle waveform
Frequency is adjusted with R5 and C

Figure 53. Triangle Waveform Generator

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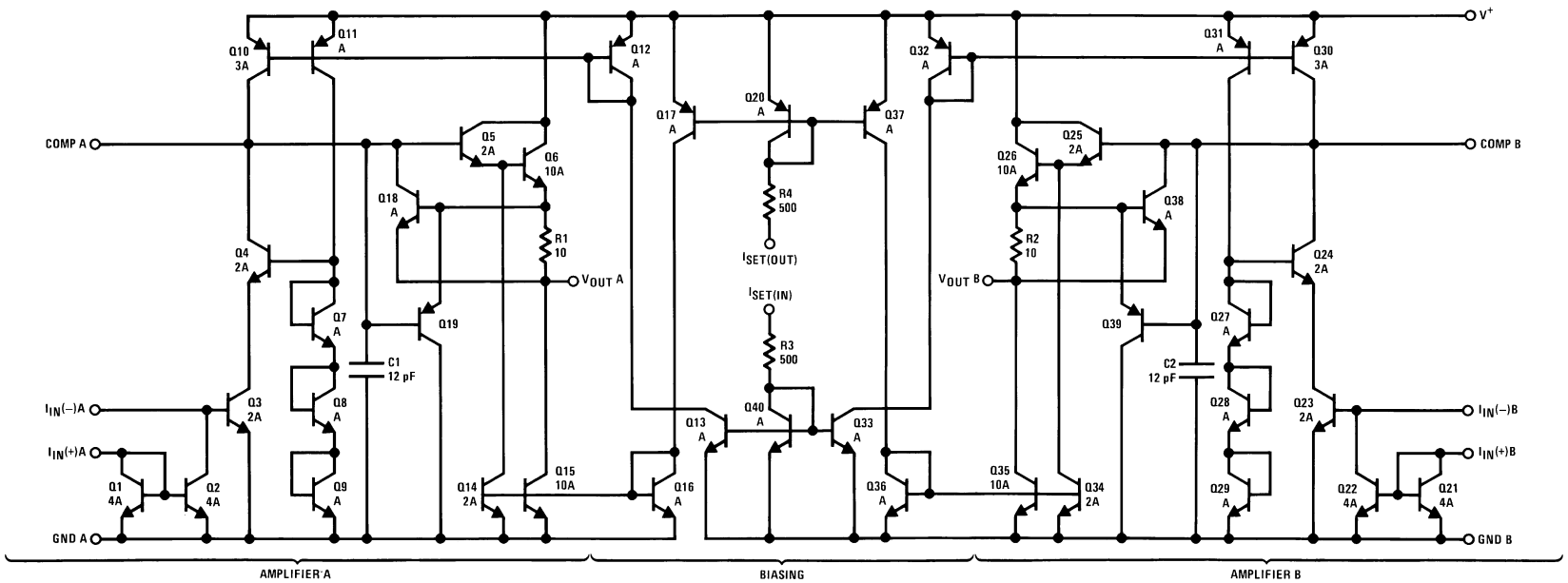
Schematic Diagram



REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	27

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM359M	NRND	SOIC	D	14	55	TBD	Call TI	Call TI	0 to 70	LM359M	
LM359M/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM359M	Samples
LM359MX	NRND	SOIC	D	14	2500	TBD	Call TI	Call TI	0 to 70	LM359M	
LM359MX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM359M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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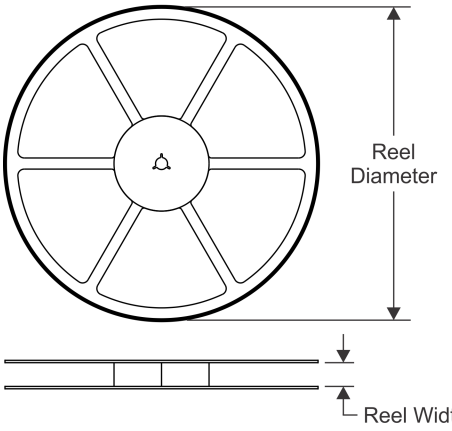
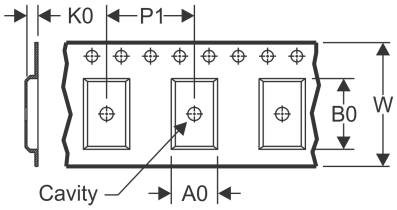
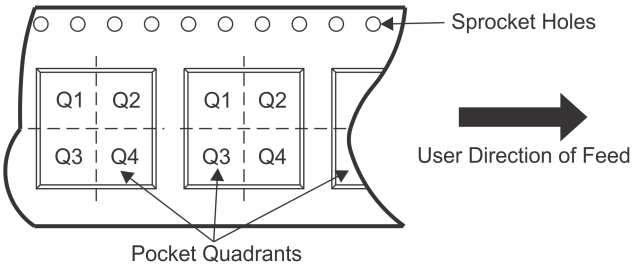


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

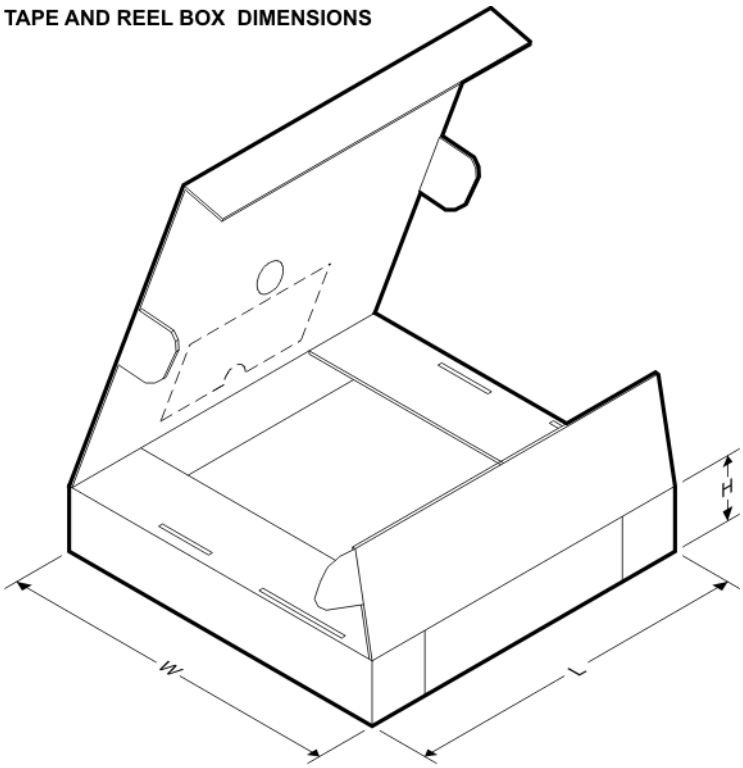
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM359MX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM359MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

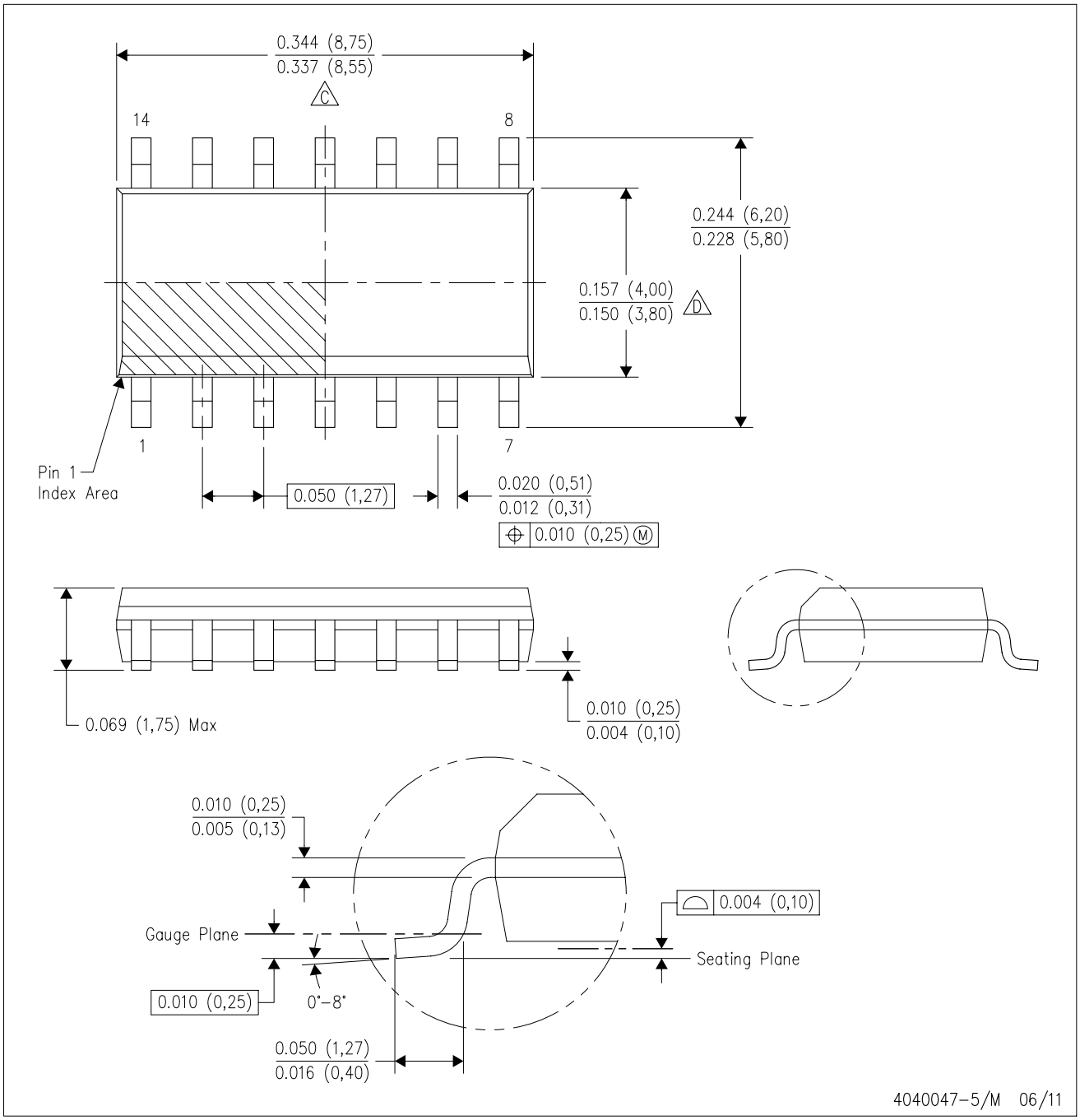
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM359MX	SOIC	D	14	2500	367.0	367.0	35.0
LM359MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

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