

MC74HCT245A

Octal 3-State Noninverting Bus Transceiver with LSTTL Compatible Inputs

High-Performance Silicon-Gate CMOS

The MC74HCT245A is identical in pinout to the LS245. This device may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

The MC74HCT245A is a 3-state noninverting transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

Features

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 V to 5.5 V
- Low Input Current: 1.0 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 304 FETs or 76 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant

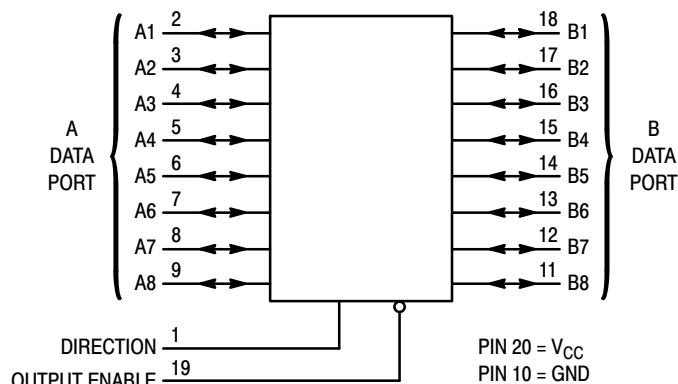


Figure 1. Logic Diagram

| Design Criteria | Value | Units |
|---------------------------------|-------|---------|
| Internal Gate Count* | 76 | ea |
| Internal Gate Propagation Delay | 1.0 | ns |
| Internal Gate Power Dissipation | 5.0 | μ W |
| Speed Power Product | 0.005 | pJ |

*Equivalent to a two-input NAND gate.

FUNCTION TABLE

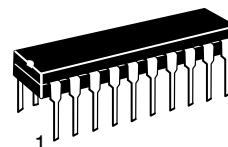
| Control Inputs | | Operation |
|----------------|-----------|---------------------------------------|
| Output Enable | Direction | |
| L | L | Data Transmitted from Bus B to Bus A |
| L | H | Data Transmitted from Bus A to Bus B |
| H | X | Buses Isolated (High-Impedance State) |

X = Don't Care

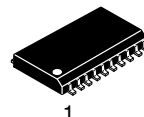


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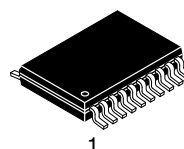
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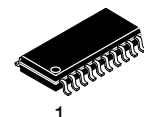
PDIP-20
N SUFFIX
CASE 738



SOIC-20W
DW SUFFIX
CASE 751D



TSSOP-20
DT SUFFIX
CASE 948E



SOEIAJ-20
F SUFFIX
CASE 967

PIN ASSIGNMENT

| | | | |
|-----------|----|----|-----------------|
| DIRECTION | 1 | 20 | V _{CC} |
| A1 | 2 | 19 | OUTPUT ENABLE |
| A2 | 3 | 18 | B1 |
| A3 | 4 | 17 | B2 |
| A4 | 5 | 16 | B3 |
| A5 | 6 | 15 | B4 |
| A6 | 7 | 14 | B5 |
| A7 | 8 | 13 | B6 |
| A8 | 9 | 12 | B7 |
| GND | 10 | 11 | B8 |

ORDERING INFORMATION

See detailed ordering, shipping information, and marking information in the package dimensions section on page 6 of this data sheet.

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MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------|---|-------------------------|------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | – 0.5 to + 7.0 | V |
| V_{in} | DC Input Voltage (Referenced to GND) | – 0.5 to $V_{CC} + 0.5$ | V |
| V_{out} | DC Output Voltage (Referenced to GND) | – 0.5 to $V_{CC} + 0.5$ | V |
| I_{in} | DC Input Current, per Pin | ± 20 | mA |
| I_{out} | DC Output Current, per Pin | ± 35 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ± 75 | mA |
| P_D | Power Dissipation in Still Air, PDIP† SOIC Package† TSSOP Package† | 750 500 450 | mW |
| T_{stg} | Storage Temperature | – 65 to + 150 | °C |
| T_L | Lead Temperature, 1 mm from Case for 10 Secs (PDIP, SOIC, SSOP or TSSOP Package) | 260 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|-------------------|--|------|----------|------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | 4.5 | 5.5 | V |
| V_{in}, V_{out} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V_{CC} | V |
| T_A | Operating Temperature, All Package Types | – 55 | + 125 | °C |
| t_r, t_f | Input Rise and Fall Time (Figure 1) | 0 | 500 | ns |

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limit | | | Unit |
|------------------|--|---|----------------------|------------------|-----------------|------------|------|
| | | | | – 55 to 25° C | ≤ 85° C | ≤ 125° C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{out} = 0.1 V or V _{CC} – 0.1 V I _{out} ≤ 20 μA | 4.5 5.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | V |
| V _{IL} | Maximum Low-Level Input Voltage | V _{out} = 0.1 V or V _{CC} – 0.1 V I _{out} ≤ 20 μA | 4.5 5.5 | 0.8 0.8 | 0.8 0.8 | 0.8 0.8 | V |
| V _{OH} | Minimum High-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA | 4.5 5.5 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | V |
| | | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0 mA | 4.5 | 3.98 | 3.84 | 3.7 | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA | 4.5 5.5 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | V |
| | | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0 mA | 4.5 | 0.26 | 0.33 | 0.4 | |
| I _{in} | Maximum Input Leakage Current | V _{in} = V _{CC} or GND, Pins 1 or 19 | 5.5 | ± 0.1 | ± 1.0 | ± 1.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{in} = V _{CC} or GND I _{out} = 0 μA | 5.5 | 4.0 | 40 | 160 | μA |
| I _{OZ} | Maximum Three-State Leakage Current | Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND, I/O Pins | 5.5 | ± 0.5 | ± 5.0 | ± 10 | μA |
| ΔI _{CC} | Additional Quiescent Supply Current | V _{in} = 2.4 V, Any One Input V _{in} = V _{CC} or GND, Other Inputs I _{out} = 0 μA | 5.5 | ≥ –55° C | 25° C to 125° C | | mA |
| | | | | 2.9 | 2.4 | | |

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, C_L = 50 pF, Input t_r = t_f = 6.0 ns)

| Symbol | Parameter | Guaranteed Limit | | | Unit |
|--|--|---|---------|----------|------|
| | | – 55 to 25° C | ≤ 85° C | ≤ 125° C | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, A to B or B to A (Figures 2 and 4) | 22 | 28 | 33 | ns |
| t _{PLZ} , t _{PHZ} | Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 3 and 5) | 30 | 36 | 42 | ns |
| t _{PZL} , t _{PZH} | Maximum Propagation Delay, Output Enable to A or 8 (Figures 3 and 5) | 30 | 36 | 42 | ns |
| t _{TLH} , t _{THL} | Maximum Output Transition Time. any Output (Figures 2 and 4) | 12 | 15 | 18 | ns |
| C _{in} | Maximum Input Capacitance (Pin 1 or 19) | 10 | 10 | 10 | pF |
| C _{out} | Maximum Three–State I/O Capacitance, (I/O in High–Impedance State) | 15 | 15 | 15 | pF |
| C _{PD} | Power Dissipation Capacitance (Per Enabled Output)* | Typical @ 25°C, V _{CC} = 5.0 V | | | pF |
| | | 97 | | | |

* Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}.

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SWITCHING WAVEFORMS

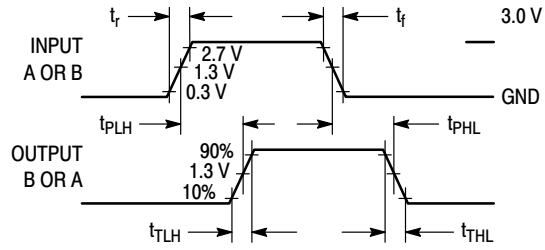


Figure 2.

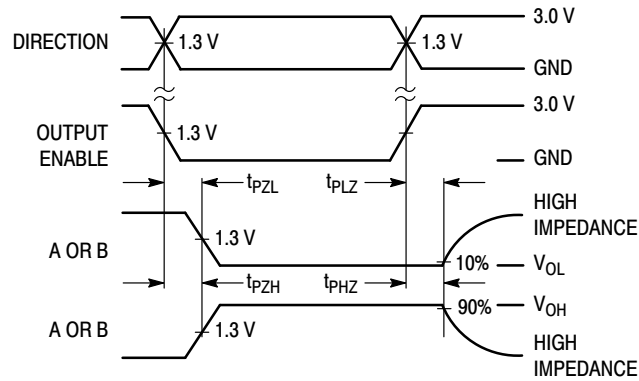
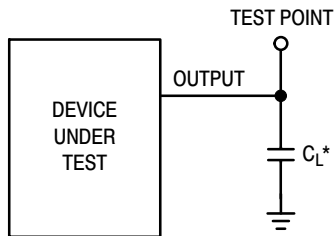
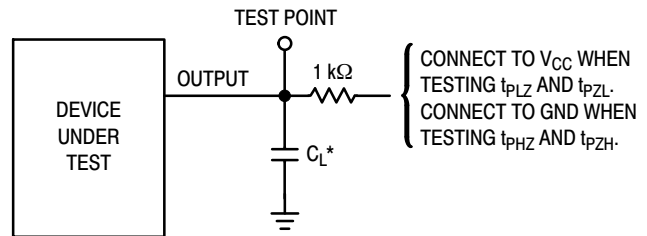


Figure 3.



*Includes all probe and jig capacitance

Figure 4.



*Includes all probe and jig capacitance

Figure 5. Test Circuit

MC74HCT245A

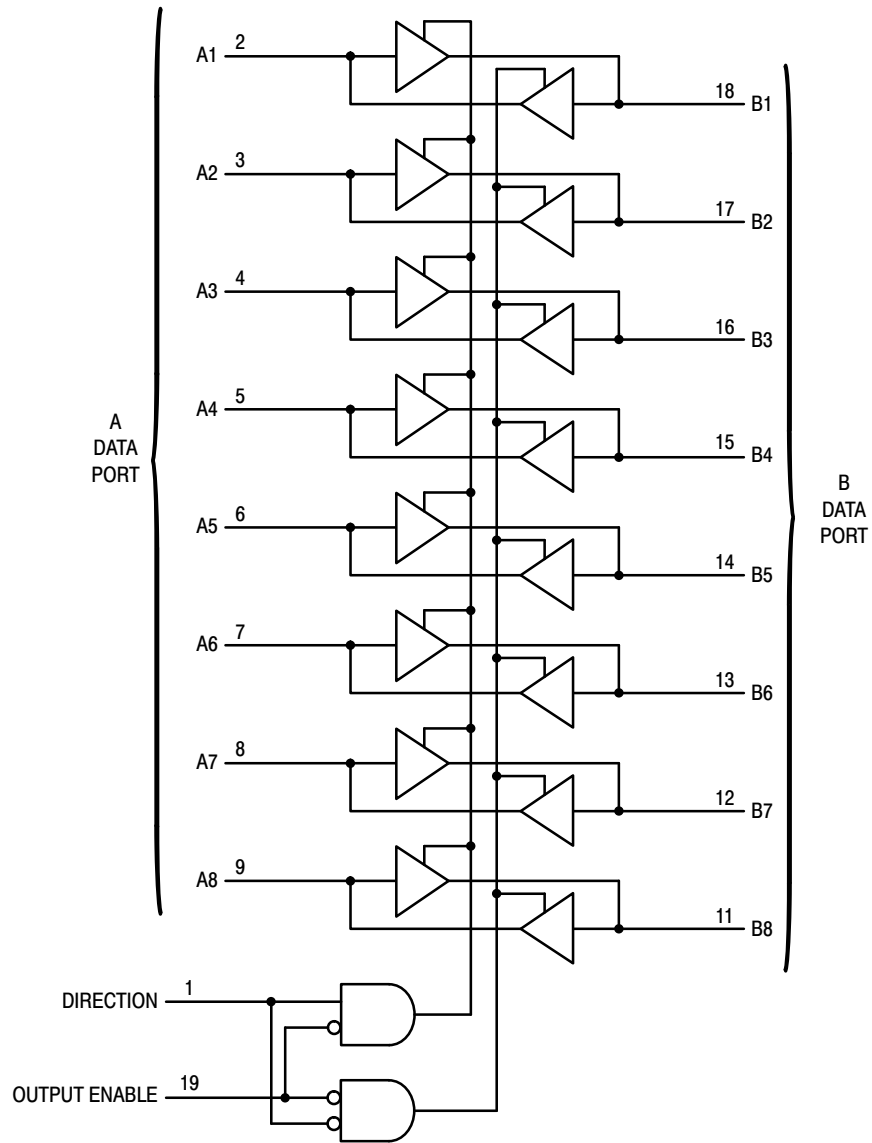


Figure 6. Expanded Logic Diagram

MC74HCT245A

ORDERING INFORMATION

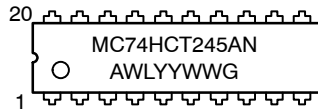
| Device | Package | Shipping [†] |
|------------------|------------------------|-----------------------|
| MC74HCT245ANG | PDIP-20 (Pb-Free) | 18 Units / Rail |
| MC74HCT245ADWG | SOIC-20 (Pb-Free) | 38 Units / Rail |
| MC74HCT245ADWR2G | SOIC-20 (Pb-Free) | 1000 / Tape & Reel |
| MC74HCT245ADTG | TSSOP-20* | 75 Units / Rail |
| MC74HCT245ADTR2G | TSSOP-20* | 2500 / Tape & Reel |
| MC74HCT245AFELG | SOEIAJ-20 (Pb-Free) | 2000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

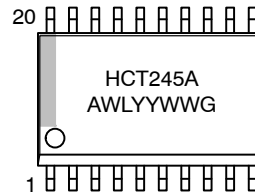
*These packages are inherently Pb-Free.

MARKING DIAGRAMS

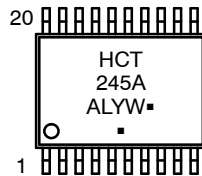
PDIP-20



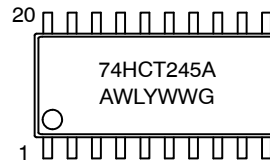
SOIC-20W



TSSOP-20



SOEIAJ-20

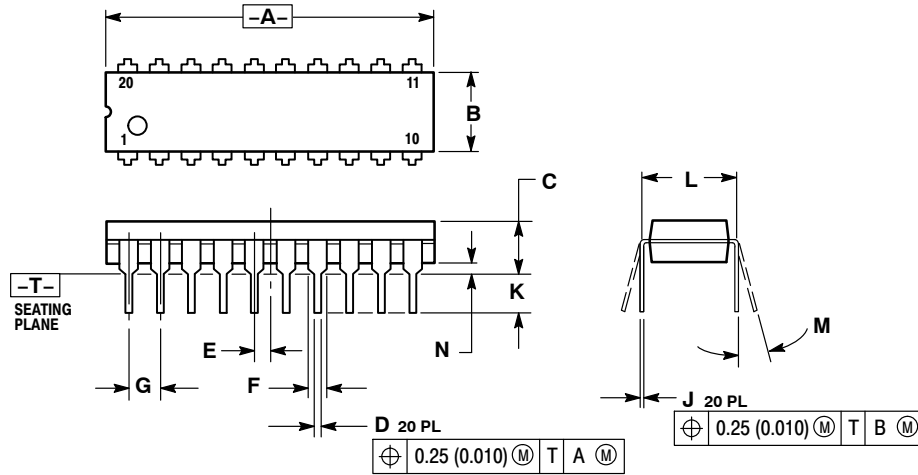


A = Assembly Location
 WL, L = Wafer Lot
 YY, Y = Year
 WW, W = Work Week
 G or ■ = Pb-Free Package
 (Note: Microdot may be in either location)

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PACKAGE DIMENSIONS

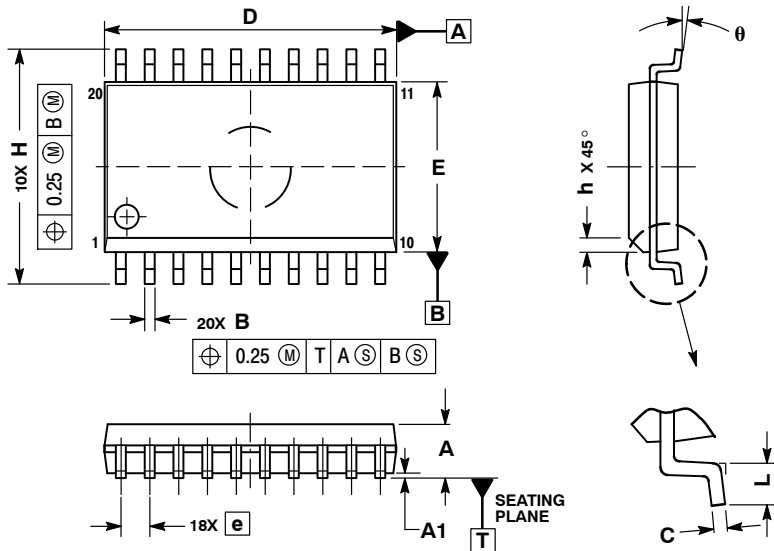
PDIP-20
N SUFFIX
 PLASTIC DIP PACKAGE
 CASE 738-03
 ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.010 | 1.070 | 25.66 | 27.17 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.150 | 0.180 | 3.81 | 4.57 |
| D | 0.015 | 0.022 | 0.39 | 0.55 |
| E | 0.050 BSC | | 1.27 BSC | |
| F | 0.050 | 0.070 | 1.27 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.140 | 2.80 | 3.55 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.020 | 0.040 | 0.51 | 1.01 |

SOIC-20W
DW SUFFIX
 CASE 751D-05
 ISSUE G



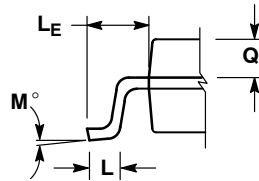
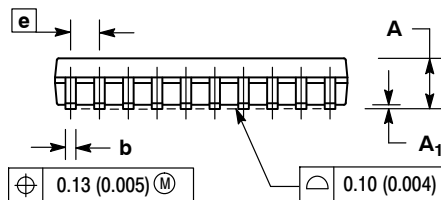
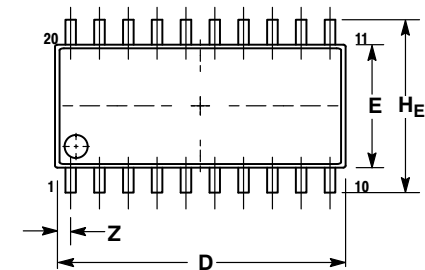
- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

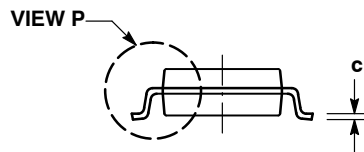
MC74HCT245A

PACKAGE DIMENSIONS

SOEIAJ-20
F SUFFIX
CASE 967-01
ISSUE A




DETAIL P



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| A ₁ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.15 | 0.25 | 0.006 | 0.010 |
| D | 12.35 | 12.80 | 0.486 | 0.504 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| H _E | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| L _E | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0° | 10° | 0° | 10° |
| Q ₁ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 0.81 | --- | 0.032 |

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Contact Us :

➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
Minhang District, Shanghai , China

➤ Sales :

Direct +86 (21) 6401-6692
Email amall@ameya360.com
QQ 800077892
Skype ameyasales1 ameyasales2

➤ Customer Service :

Email service@ameya360.com

➤ Partnership :

Tel +86 (21) 64016692-8333
Email mkt@ameya360.com