- **Meets or Exceeds the Requirements of TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendation V.11**
- **Bus Voltage Range . . . −7 V to 12 V**
- **Positive- and Negative-Current Limiting**
- **Driver Output Capability . . . 60 mA Max**
- **Driver Thermal-Shutdown Protection**
- **Receiver Input Impedance . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Input Hysteresis . . . 50 mV Typ**
- **Operates From Single 5-V Supply**
- **Low Power Requirements**

D OR P PACKAGE
(TOP VIEW)

V_{CC}	1		8	A
R	2		7	B
D	3		6	Z
GND	4		5	Y
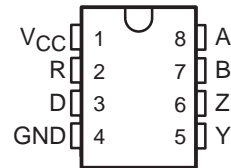
description

The SN75179B is a differential driver and receiver pair designed for balanced transmission-line applications and meets TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendation V.11. It is designed to improve the performance of full-duplex data communications over long bus lines.

The SN75179B driver output provides limiting for both positive and negative currents. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of −7 V to 12 V. The driver provides thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The SN75179B is designed to drive current loads of up to 60 mA maximum.

The SN75179B is characterized for operation from 0°C to 70°C.

Function Tables

DRIVER

INPUT D	OUTPUTS	
	Y	Z
H	H	L
L	L	H

RECEIVER

DIFFERENTIAL INPUTS A − B	OUTPUT R
$V_{ID} \geq 0.2$ V	H
-0.2 V $< V_{ID} < 0.2$ V	?
$V_{ID} \leq -0.2$ V	L
Open	?

H = high level, L = low level, ? = indeterminate

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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SN75179B
DIFFERENTIAL DRIVER AND RECEIVER PAIR
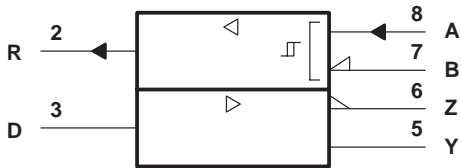
logic symbol[†]

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)
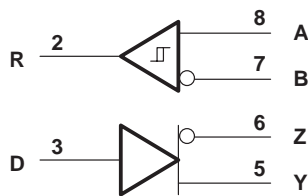
schematics of inputs and outputs

EQUIVALENT OF DRIVER INPUT

Driver input: $R_{(eq)}$ = 3 kΩ NOM
$R_{(eq)}$ = equivalent resistor

TYPICAL OF ALL DRIVER OUTPUTS

EQUIVALENT OF EACH RECEIVER INPUT

960 Ω NOM

16.8 kΩ NOM

960 Ω NOM

TYPICAL OF ALL RECEIVER OUTPUTS

85 Ω NOM

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INSTRUMENTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) .... 7 V
Voltage range at any bus terminal .... −10 V to 15 V
Differential input voltage, V_{ID} (see Note 2) .... ±25 V
Package thermal impedance, θ_{JA} (see Note 3): D package .... 197°C/W
P package .... 104°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	Driver	2			V
Low-level input voltage, V_{IL}	Driver			0.8	V
Common-mode input voltage, V_{IC}		−7‡		12	V
Differential input voltage, V_{ID}				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

‡ The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA			−1.5	V
V_O	Output voltage	$I_O = 0$	0		6	V
$|V_{OD1}|$	Differential output voltage	$I_O = 0$	1.5		6	V
$|V_{OD2}|$	Differential output voltage	$R_L = 100$ Ω, See Figure 1	$1/2V_{OD1}$ or 2‡			V
		$R_L = 54$ Ω, See Figure 1	1.5	2.5	5	V
$|V_{OD3}|$	Differential output voltage	See Note 4	1.5		5	V
$\Delta|V_{OD}|$	Change in magnitude of common-mode output voltage§				±0.2	V
V_{OC}	Common-mode output voltage	$R_L = 54$ Ω or 100 Ω, See Figure 1			3 −1	V
$\Delta|V_{OC}|$	Change in magnitude of common-mode output voltage§				±0.2	V
I_O	Output current	$V_{CC} = 0$, $V_O = -7$ V to 12 V			±100	µA
I_{IH}	High-level input current	$V_I = 2.4$ V			20	µA
I_{IL}	Low-level input current	$V_I = 0.4$ V			−200	µA
I_{OS}	Short-circuit output current	$V_O = -7$ V			−250	mA
		$V_O = V_{CC}$ or 12 V			250	
I_{CC}	Supply current (total package)	No load		57	70	mA

† All typical values are at $V_{CC} = 5$ V and $T_A = 25°$C.
‡ The minimum V_{OD2} with 100-Ω load is either $1/2 V_{OD2}$ or 2 V, whichever is greater.
§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input changes from a high level to a low level.
NOTE 4:   See TIA/EIA-485-A, Figure 3.5, Test Termination Measurement 2.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°$C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	$R_L = 54$ Ω, See Figure 3		15	22	ns
$t_{t(OD)}$	Differential output transition time			20	30	ns

Symbol Equivalents

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$|V_{OD1}|$	V_o	V_o
$|V_{OD2}|$	V_t ($R_L = 100$ Ω)	V_t ($R_L = 54$ Ω)
$|V_{OD3}|$		V_t (Test Termination Measurement 2)
$\Delta|V_{OD}|$	$||V_t|-|\overline{V}_t||$	$||V_t|-|\overline{V}_t||$
V_{OC}	$|V_{os}|$	$|V_{os}|$
$\Delta|V_{OC}|$	$|V_{os}-\overline{V}_{os}|$	$|V_{os}-\overline{V}_{os}|$
I_{OS}	$|I_{sa}|$, $|I_{sb}|$	
I_O	$|I_{xa}|$, $|I_{xb}|$	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	$V_O = 2.7$ V,	$I_O = -0.4$ mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	$V_O = 0.5$ V,	$I_O = 8$ mA		-0.2[‡]			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)					50		mV
V_{OH}	High-level output voltage	$V_{ID} = 200$ mV,	$I_{OH} = -400$ µA,	See Figure 2	2.7			V
V_{OL}	Low-level output voltage	$V_{ID} = -200$ mV,	$I_{OL} = 8$ mA,	See Figure 2			0.45	V
I_I	Line input current	Other input at 0 V,	See Note 5	$V_I = 12$ V			1	mA
				$V_I = -7$ V			-0.8	
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current				-15		-85	mA
I_{CC}	Supply current (total package)	No load				57	70	mA

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°$C.
‡ The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 5:   Refer to TIA/EIA-422-B for exact conditions.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°$C

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	$V_{ID} = -1.5$ V to 1.5 V,			19	35	ns
t_{PHL}	Propagation delay time, high- to low-level output	$C_L = 15$ pF,	See Figure 4		30	40	ns

PARAMETER MEASUREMENT INFORMATION
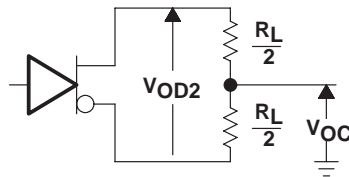
Figure 1. Driver V_{DD} and V_{OC}
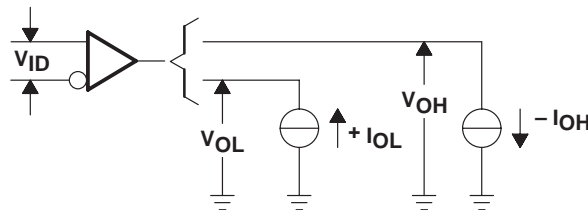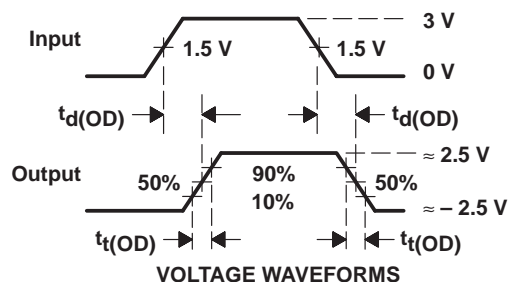

Figure 2. Receiver V_{OH} and V_{OL}

PARAMETER MEASUREMENT INFORMATION (CONTINUED)
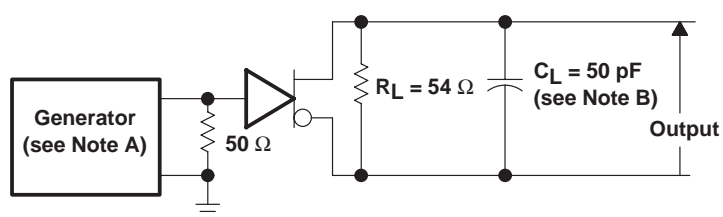
TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A.   The input pulse is supplied by a generator having the following characteristics: PRR $\leq$ 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, Z_O = 50 Ω.
   B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms
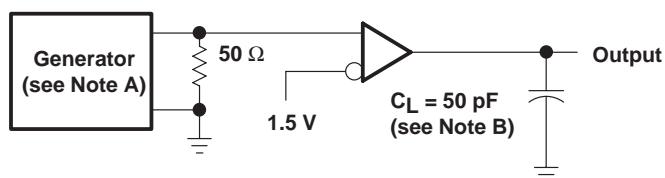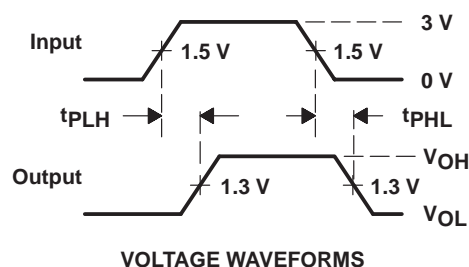

TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A.   The input pulse is supplied by a generator having the following characteristics: PRR $\leq$ 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, Z_O = 50 Ω.
   B. C_L includes probe and jig capacitance.

Figure 4. Receiver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS
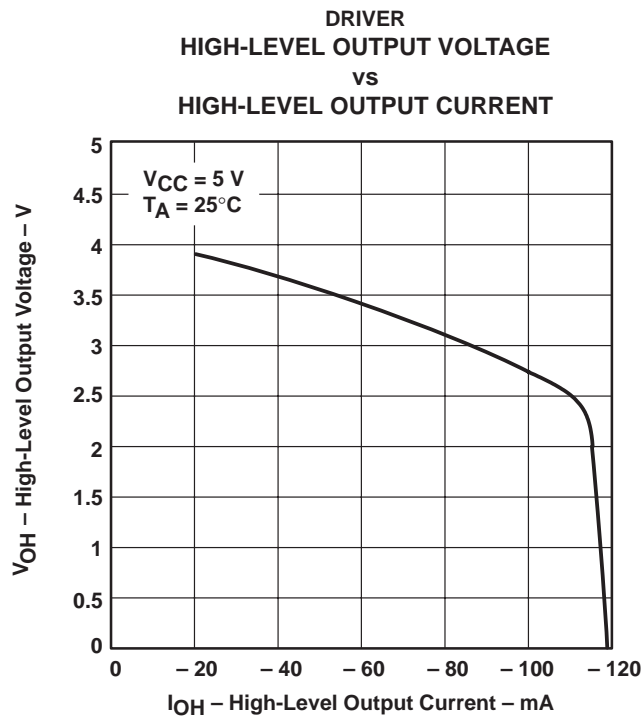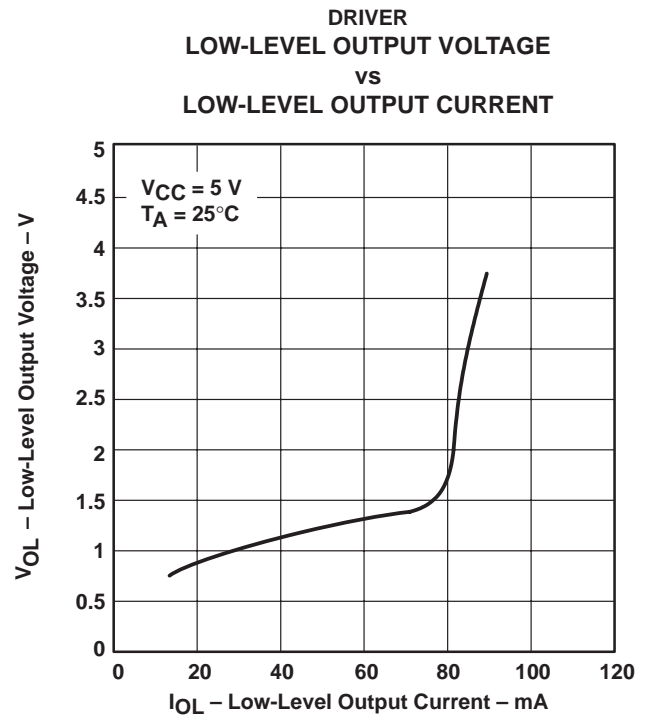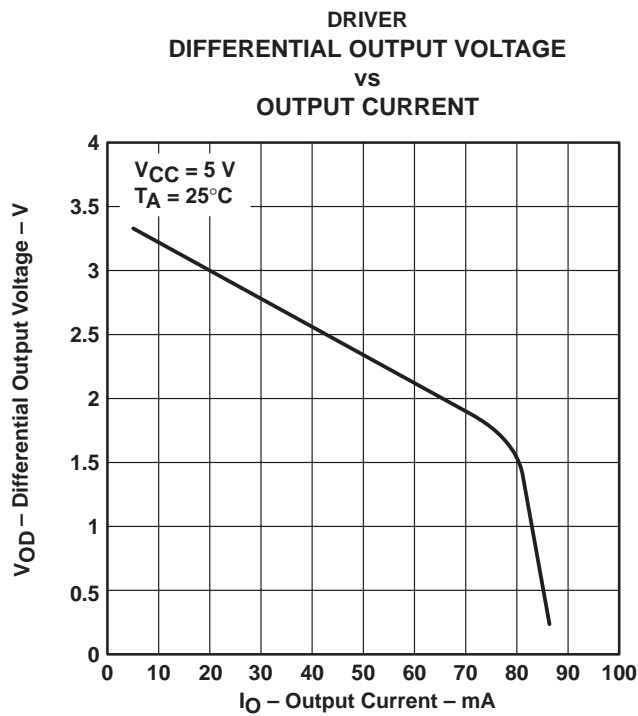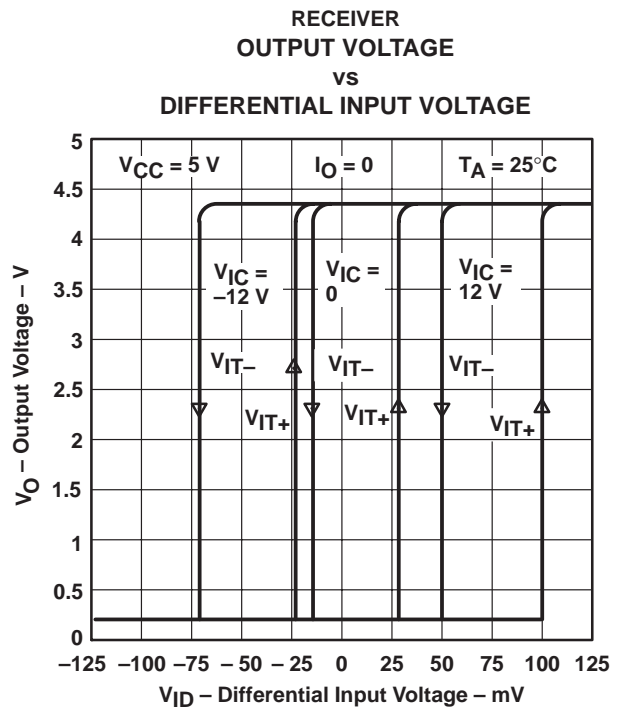
DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 5

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

Figure 6

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

Figure 7

RECEIVER
OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

Figure 8

7

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

V_{ID} = 0.2 V
T_A = 25°C

V_{CC} = 5.25 V
V_{CC} = 5 V
V_{CC} = 4.75 V

Figure 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

V_{CC} = 5 V
V_{ID} = 0.2 V
I_{OH} = −440 μA

Figure 10

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

V_{CC} = 5 V
T_A = 25°C

Figure 11

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

V_{CC} = 5 V
V_{ID} = −0.2 V
I_{OL} = 8 mA

Figure 12

TEXAS
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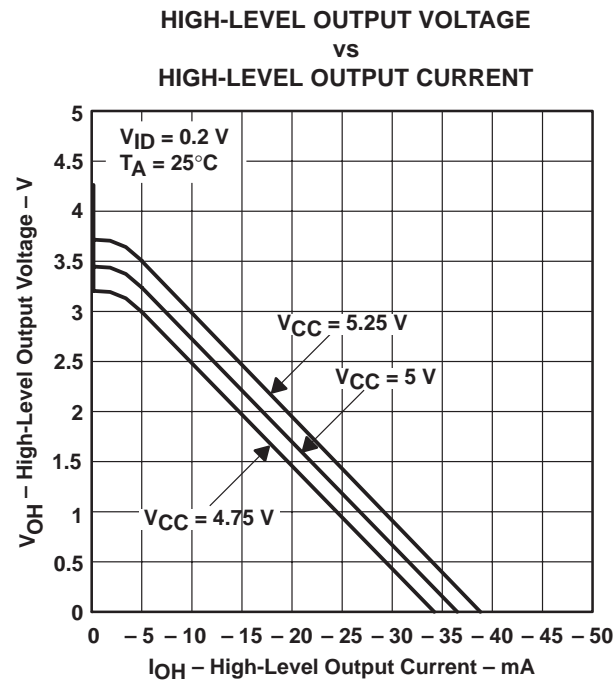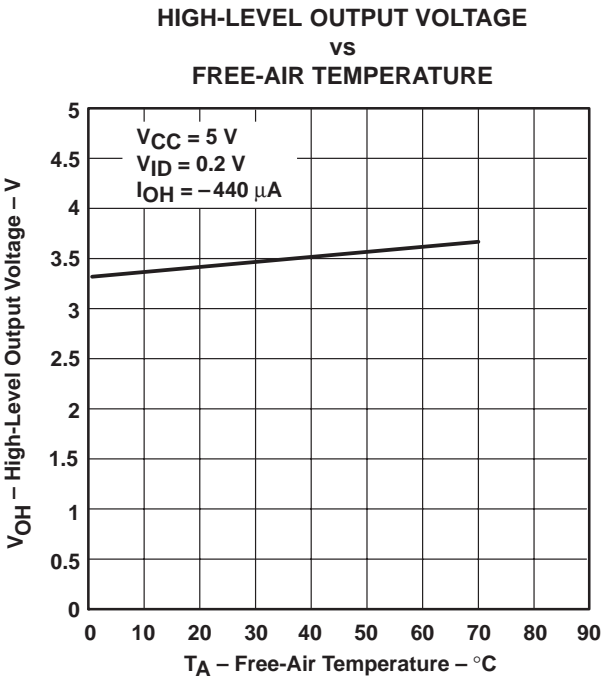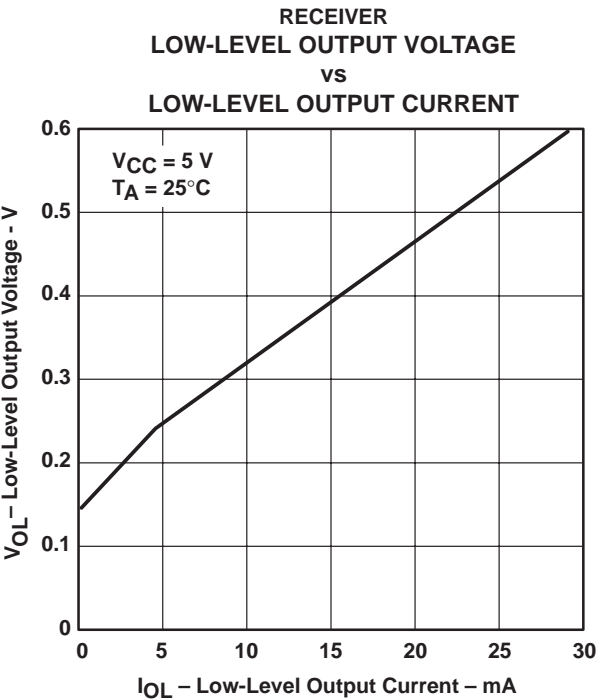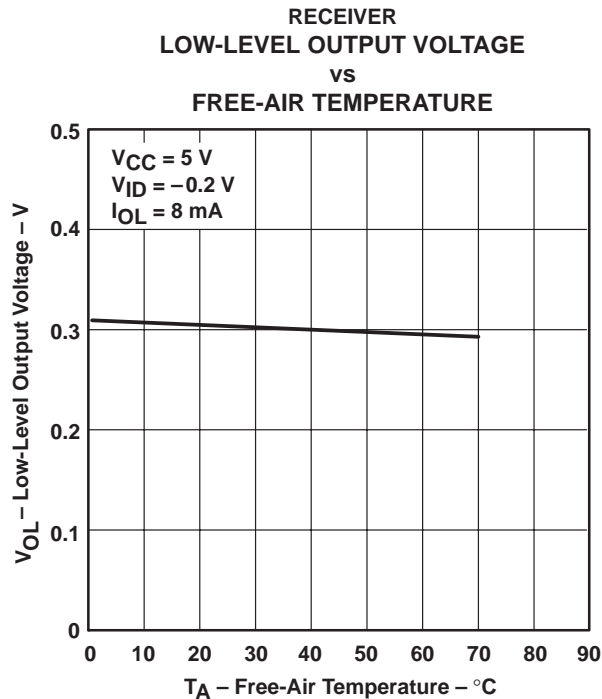
PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN75179BD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75179BDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75179BDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75179BDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75179BDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75179BDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75179BP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75179BPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75179BPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75179BPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75179BPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS
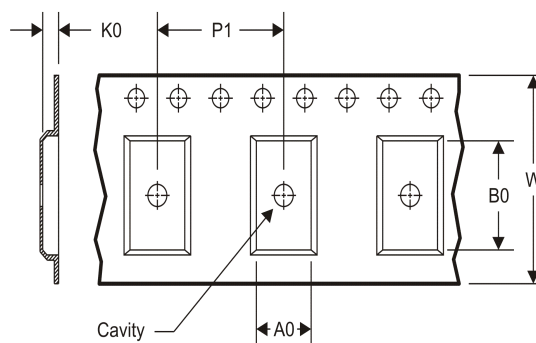
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75179BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75179BPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

TEXAS INSTRUMENTS

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75179BDR	SOIC	D	8	2500	340.5	338.1	20.6
SN75179BPSR	SO	PS	8	2000	367.0	367.0	38.0

P (R–PDIP–T8)   PLASTIC DUAL–IN–LINE PACKAGE

0.400 (10,16)
―――――――――
0.355 (9,02)

8   5

0.260 (6,60)
―――――――――
0.240 (6,10)

1   4

0.070 (1,78)
―――――――――
0.045 (1,14)

0.045 (1,14)
―――――――――
0.030 (0,76)

0.020 (0,51) MIN

0.325 (8,26)
―――――――――
0.300 (7,62)

0.015 (0,38)

0.200 (5,08) MAX

Gauge Plane

Seating Plane

0.125 (3,18) MIN

0.010 (0,25) NOM

0.100 (2,54)

0.021 (0,53)
―――――――――
0.015 (0,38)

⊕ | 0.010 (0,25) Ⓜ

0.430 (10,92)
MAX

4040082/E 04/2010

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MS–001 variation BA.

D (R−PDSO−G8)   PLASTIC SMALL OUTLINE

0.197 (5,00)
0.189 (4,80)
C

8   5

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)
D

Pin 1
Index Area

1   4

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) M

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/M   06/11

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
         D.   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E.   Reference JEDEC MS−012 variation AA.

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D (R−PDSO−G8)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

6x1,27

8x0,55

8x1,50

6x1,27

5,40

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0,07

All Around

4211283−2/E 08/12

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
        E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

4040063/C 03/03

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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