

## N-Channel NexFET™ Power MOSFETs

Check for Samples: [CSD16323Q3](#)

### FEATURES

- Optimized for 5V Gate Drive
- Ultra Low Q<sub>g</sub> and Q<sub>gd</sub>
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3mm x 3.3mm Plastic Package

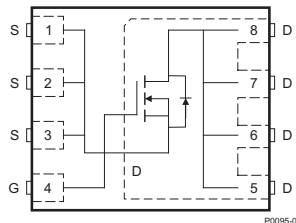
### APPLICATIONS

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems
- Optimized for Control or Synchronous FET Applications

### DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion and optimized for 5V gate drive applications.

Top View



P0085-01

### PRODUCT SUMMARY

V <sub>DS</sub>	Drain to Source Voltage	25	V
Q <sub>g</sub>	Gate Charge Total (4.5V)	6.2	nC
Q <sub>gd</sub>	Gate Charge Gate to Drain	1.1	nC
R <sub>DS(on)</sub>	Drain to Source On Resistance	V <sub>GS</sub> = 3V	5.4 mΩ
		V <sub>GS</sub> = 4.5V	4.4 mΩ
		V <sub>GS</sub> = 8V	3.8 mΩ
V <sub>th</sub>	Threshold Voltage	1.1	V

### ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD16323Q3	SON 3.3 × 3.3 Plastic Package	13-inch reel	2500	Tape and Reel

### ABSOLUTE MAXIMUM RATINGS

T <sub>A</sub> = 25°C unless otherwise stated		VALUE	UNIT
V <sub>DS</sub>	Drain to Source Voltage	25	V
V <sub>GS</sub>	Gate to Source Voltage	+10 / -8	V
I <sub>D</sub>	Continuous Drain Current, T <sub>C</sub> = 25°C	60	A
	Continuous Drain Current <sup>(1)</sup>	21	A
I <sub>DM</sub>	Pulsed Drain Current, T <sub>A</sub> = 25°C <sup>(2)</sup>	112	A
P <sub>D</sub>	Power Dissipation <sup>(1)</sup>	3	W
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 150	°C
E <sub>AS</sub>	Avalanche Energy, single pulse I <sub>D</sub> = 50A, L = 0.1mH, R <sub>G</sub> = 25Ω	125	mJ

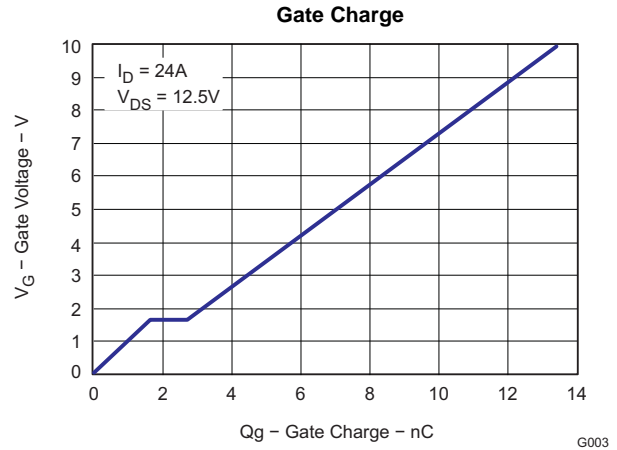
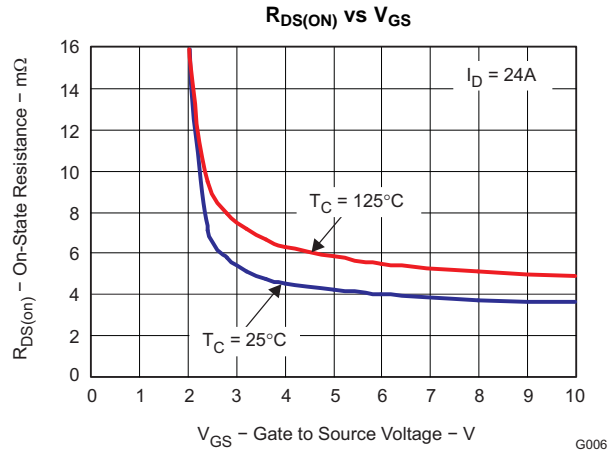
(1) R<sub>θJA</sub> = 43°C/W on 1in<sup>2</sup> Cu (2 oz.) on 0.060" thick FR4 PCB.

(2) Pulse width ≤300μs, duty cycle ≤2%



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ C$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>Static Characteristics</b>							
$BV_{DSS}$	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu A$	25			V	
$I_{DSS}$	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = 20V$			1	$\mu A$	
$I_{GSS}$	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = +10/-8V$			100	nA	
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.9	1.1	1.4	V	
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 3V, I_D = 24A$		5.4	7.2	m $\Omega$	
		$V_{GS} = 4.5V, I_D = 24A$		4.4	5.5	m $\Omega$	
		$V_{GS} = 8V, I_D = 24A$		3.8	4.5	m $\Omega$	
$g_{fs}$	Transconductance	$V_{DS} = 12.5V, I_D = 24A$		108		S	
<b>Dynamic Characteristics</b>							
$C_{ISS}$	Input Capacitance	$V_{GS} = 0V, V_{DS} = 12.5V, f = 1MHz$		1020	1300	pF	
$C_{OSS}$	Output Capacitance			740	960	pF	
$C_{RSS}$	Reverse Transfer Capacitance			50	65	pF	
$R_g$	Series Gate Resistance	$V_{DS} = 12.5V, I_D = 24A$		1.4	2.8	$\Omega$	
$Q_g$	Gate Charge Total (4.5V)			6.2	8.4	nC	
$Q_{gd}$	Gate Charge Gate to Drain			1.1		nC	
$Q_{gs}$	Gate Charge Gate to Source			1.8		nC	
$Q_{g(th)}$	Gate Charge at $V_{th}$			1		nC	
$Q_{OSS}$	Output Charge		$V_{DS} = 12.5V, V_{GS} = 0V$		14		nC
$t_{d(on)}$	Turn On Delay Time		$V_{DS} = 12.5V, V_{GS} = 4.5V, I_D = 24A$ $R_G = 2\Omega$		5.3		ns
$t_r$	Rise Time			15		ns	
$t_{d(off)}$	Turn Off Delay Time			13		ns	
$t_f$	Fall Time			6.3		ns	
<b>Diode Characteristics</b>							
$V_{SD}$	Diode Forward Voltage	$I_S = 24A, V_{GS} = 0V$		0.85	1	V	
$Q_{rr}$	Reverse Recovery Charge	$V_{DD} = 12.5V, I_F = 24A, di/dt = 300A/\mu s$		21		nC	
$t_{rr}$	Reverse Recovery Time	$V_{DD} = 12.5V, I_F = 24A, di/dt = 300A/\mu s$		16		ns	

**THERMAL INFORMATION**

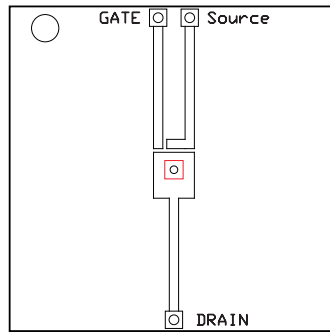
THERMAL METRIC <sup>(1)(2)</sup>		CSD16323Q3	UNITS
		8 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance	42.0	°C/W
$\theta_{JcTop}$	Junction-to-case (top) thermal resistance	20.6	
$\theta_{JB}$	Junction-to-board thermal resistance	8.8	
$\psi_{JT}$	Junction-to-top characterization parameter	0.3	
$\psi_{JB}$	Junction-to-board characterization parameter	8.7	
$\theta_{JcBot}$	Junction-to-case (bottom) thermal resistance	0.1	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).  
 (2) For thermal estimates of this device based on PCB copper area, see the [TI PCB Thermal Calculator](#).



M0161-01

Max  $R_{\theta JA} = 58^{\circ}\text{C/W}$   
when mounted on 1  
 $\text{inch}^2$  of 2 oz. Cu.

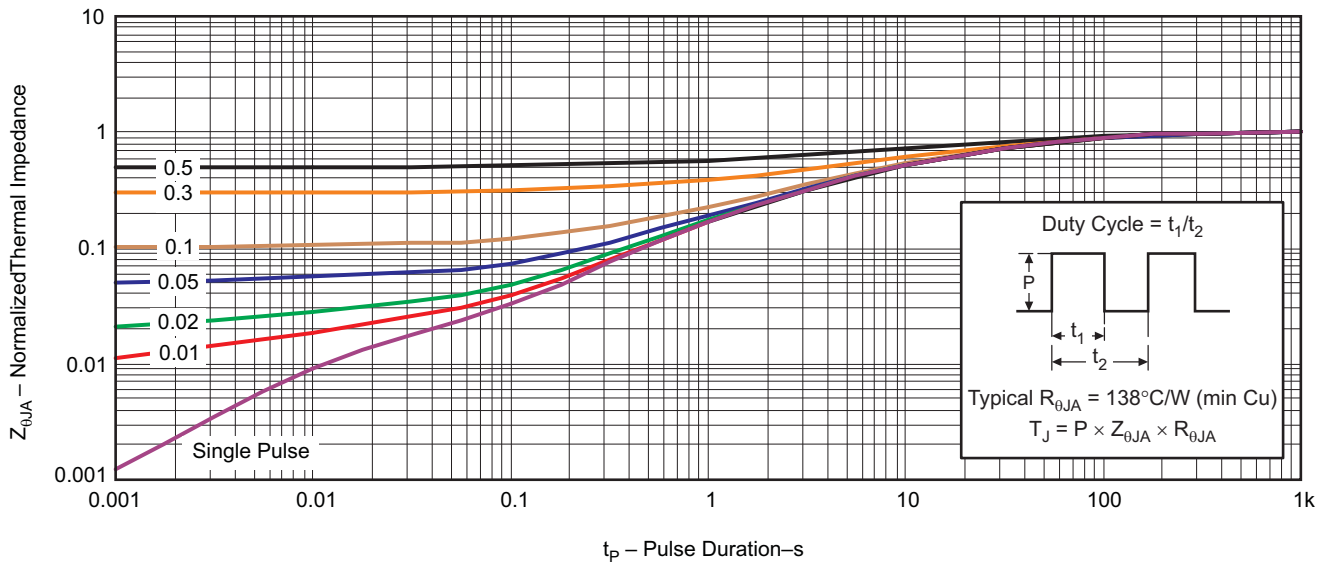


M0161-02

Max  $R_{\theta JA} = 162^{\circ}\text{C/W}$   
when mounted on  
minimum pad area of 2  
oz. Cu.

### TYPICAL MOSFET CHARACTERISTICS

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)



G012

Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

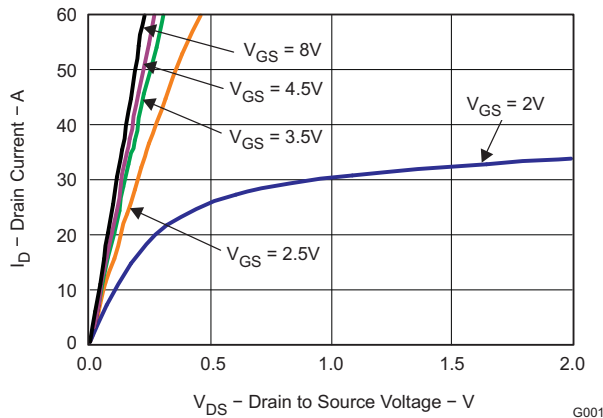


Figure 2. Saturation Characteristics

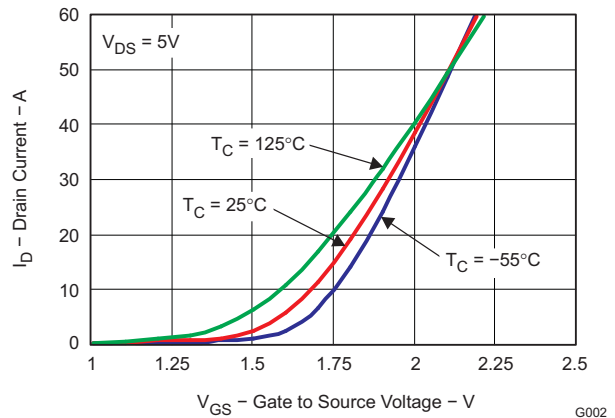


Figure 3. Transfer Characteristics

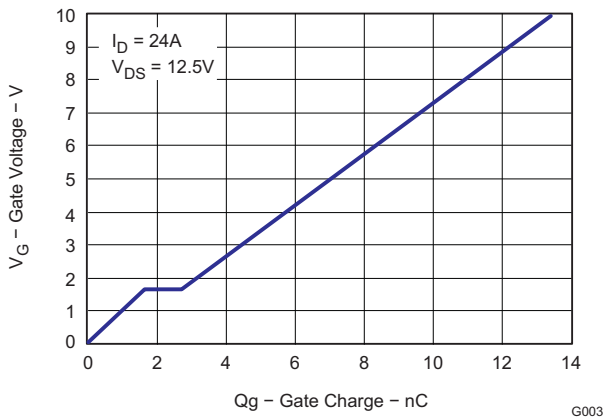


Figure 4. Gate Charge

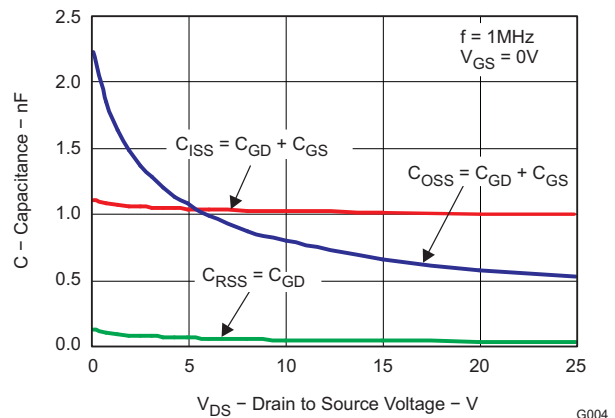


Figure 5. Capacitance

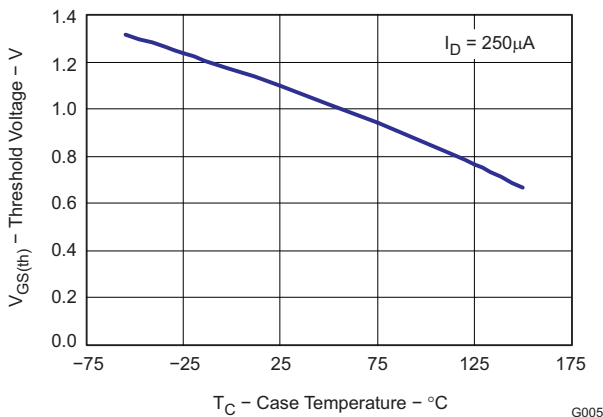


Figure 6. Threshold Voltage vs. Temperature

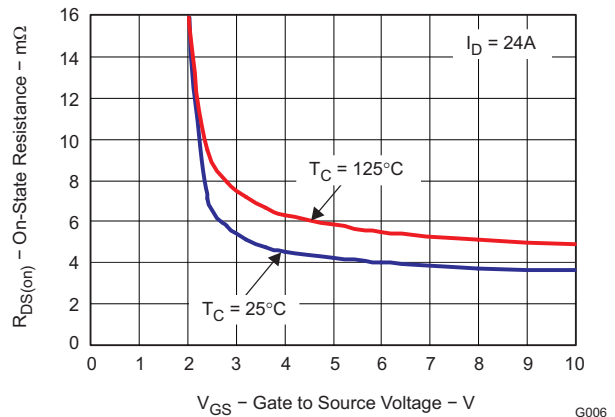


Figure 7. On Resistance vs. Gate Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

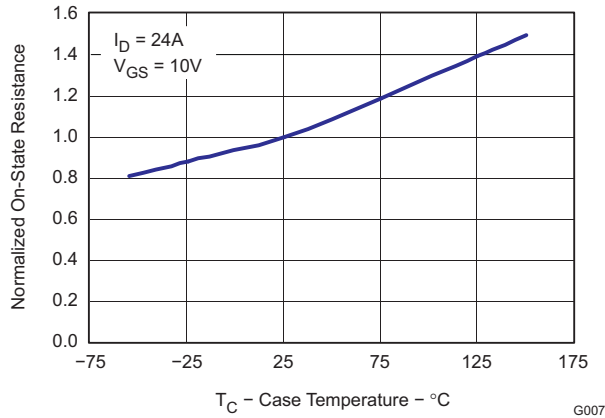


Figure 8. Normalized On Resistance vs. Temperature

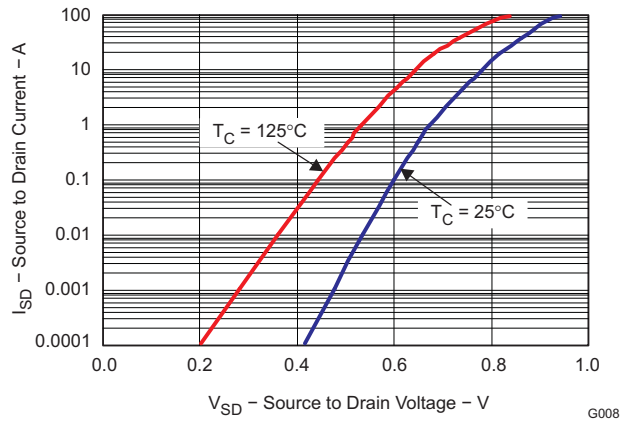


Figure 9. Typical Diode Forward Voltage

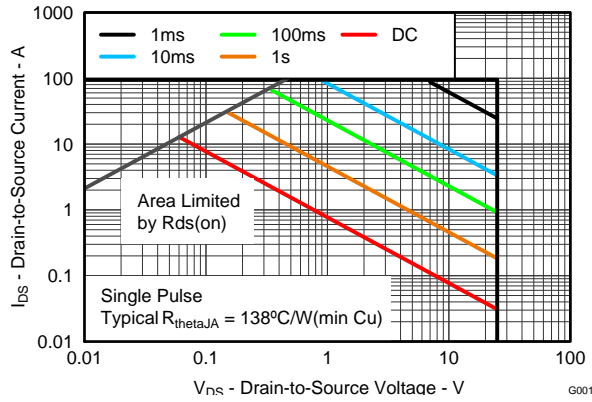


Figure 10. Maximum Safe Operating Area

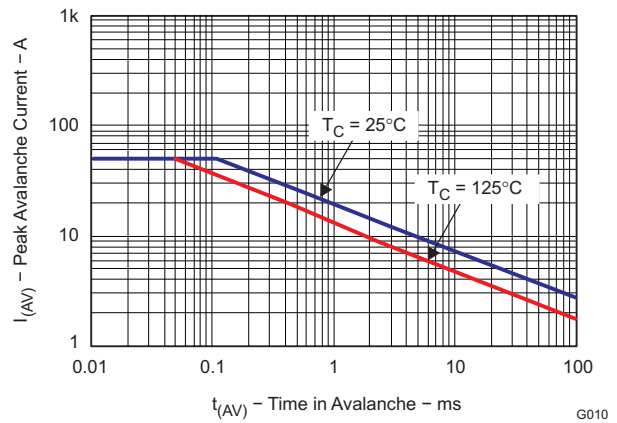


Figure 11. Single Pulse Unclamped Inductive Switching

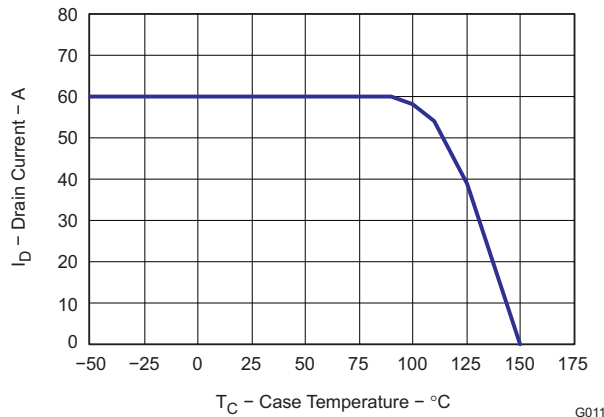
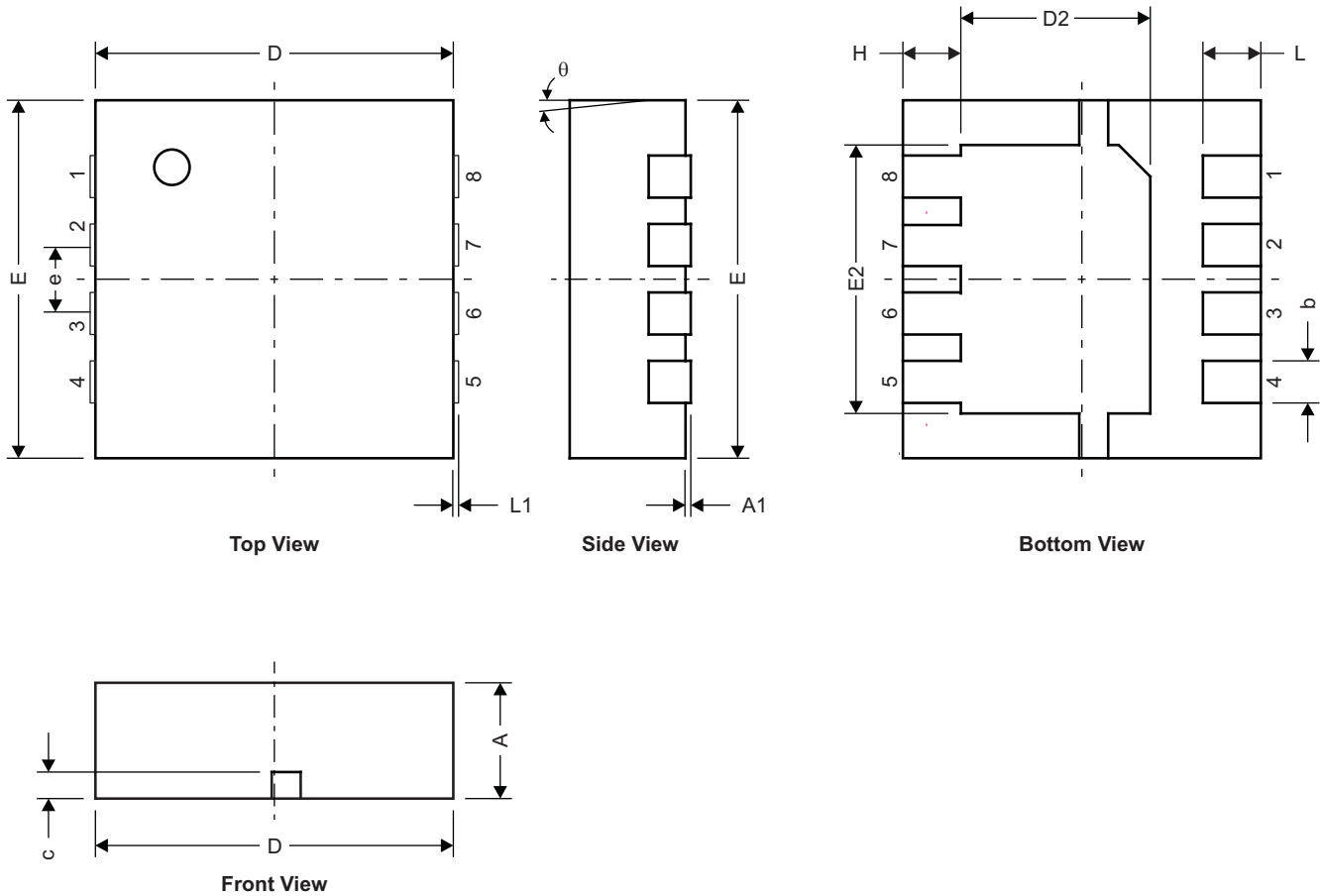


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

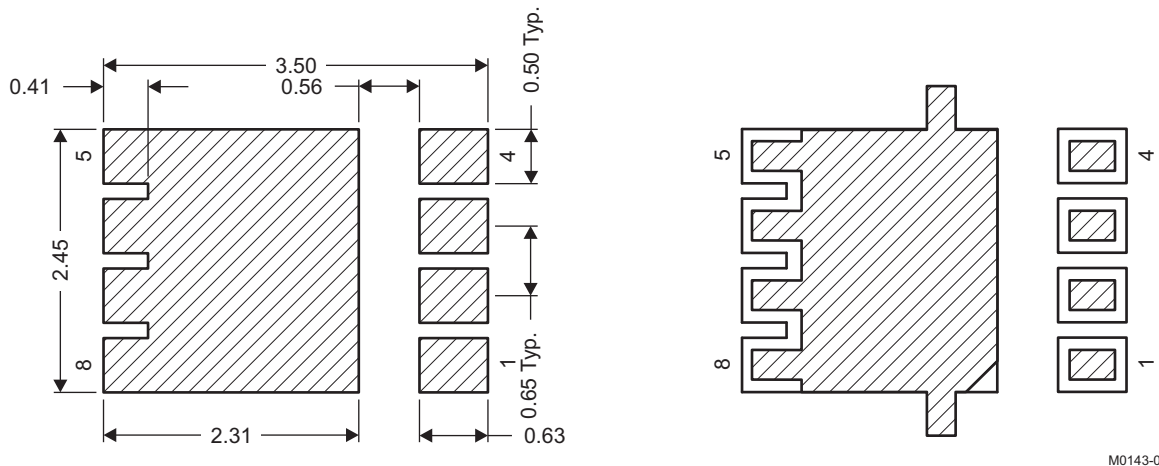
Q3 Package Dimensions



M0142-01

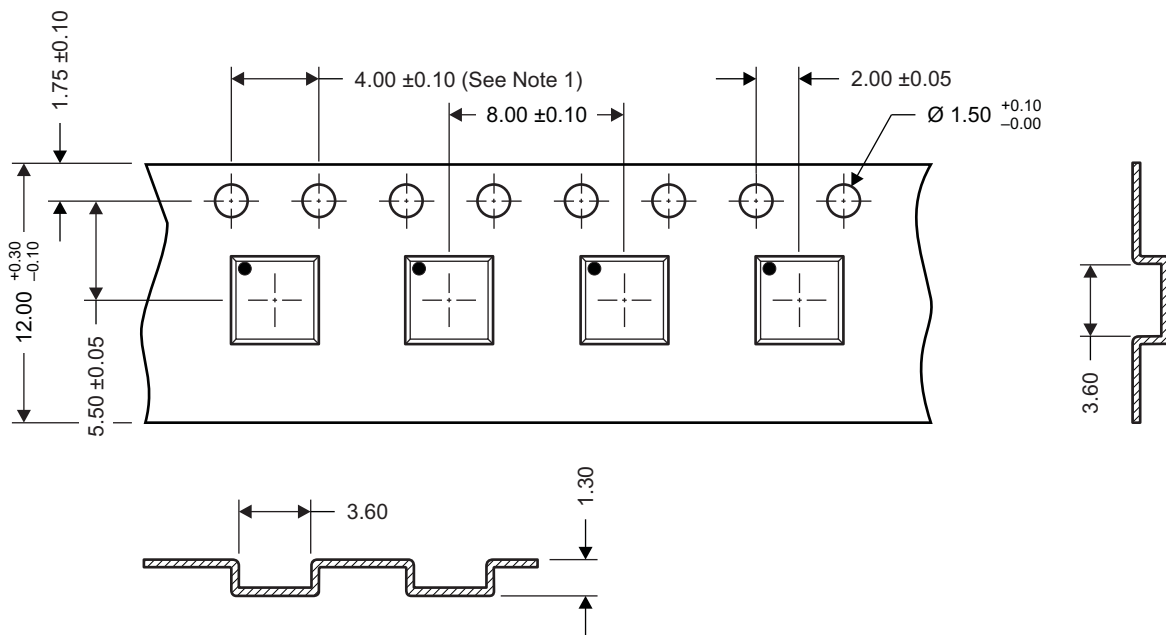
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D1	-	-	-	-	-	-
D2	1.650	1.750	1.800	0.065	0.069	0.071
E	3.200	3.300	3.400	0.126	0.130	0.134
E1	-	-	-	-	-	-
E2	2.350	2.450	2.550	0.093	0.096	0.100
e	0.650 TYP			0.026		
H	0.35	0.450	0.550	0.014	0.018	0.022
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	-	-	-	-	-	-
theta	-	-	-	-	-	-

**Recommended PCB Pattern**



For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

**Q3 Tape and Reel Information**



**Notes:**

1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.2$
2. Camber not to exceed 1mm IN 100mm, noncumulative over 250mm
3. Material: black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. Thickness:  $0.30 \pm 0.05$ mm
6. MSL1 260°C (IR and Convection) PbF Reflow Compatible



## REVISION HISTORY

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**Changes from Original (August 2009) to Revision A** **Page**

- Changed  $R_{DS(on)}$  -  $V_{GS} = 3V$ ,  $I_D = 24A$  MAX value From: 6.5 To: 7.2 ..... **2**
  - Deleted the Package Marking Information section ..... **8**
- 

**Changes from Revision A (April 2010) to Revision B** **Page**

- Replaced the THERMAL CHARACTERISTICS table with the new Thermal Information Table ..... **3**
  - Replaced [Figure 10](#) - Maximum Safe Operating Area ..... **6**
-

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD16323Q3	VSON-CLIP	DQG	8	2500	330.0	12.4	3.6	3.6	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD16323Q3	VSON-CLIP	DQG	8	2500	336.6	336.6	41.3

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