

# NCP103

## 150 mA CMOS Low Dropout Regulator

The NCP103 is 150 mA LDO that provides the engineer with a very stable, accurate voltage with low noise suitable for space constrained, noise sensitive applications. In order to optimize performance for battery operated portable applications, the NCP103 employs the dynamic quiescent current adjustment for very low  $I_Q$  consumption at no-load.

### Features

- Operating Input Voltage Range: 1.7 V to 5.5 V
- Available in Fixed Voltage Options: 0.9 V to 3.5 V  
Contact Factory for Other Voltage Options
- Very Low Quiescent Current of Typ. 50  $\mu\text{A}$
- Standby Current Consumption: Typ. 0.1  $\mu\text{A}$
- Low Dropout: 75 mV Typical at 150 mA
- $\pm 1\%$  Accuracy at Room Temperature
- High Power Supply Ripple Rejection: 75 dB at 1 kHz
- Thermal Shutdown and Current Limit Protections
- Stable with a 1  $\mu\text{F}$  Ceramic Output Capacitor
- Available in uDFN 1.0 x 1.0 mm Package
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- PDAs, Mobile phones, GPS, Smartphones
- Wireless Handsets, Wireless LAN, Bluetooth<sup>®</sup>, Zigbee<sup>®</sup>
- Portable Medical Equipment
- Other Battery Powered Applications

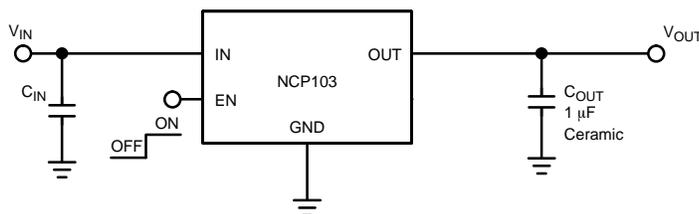


Figure 1. Typical Application Schematic



ON Semiconductor<sup>®</sup>

[www.onsemi.com](http://www.onsemi.com)



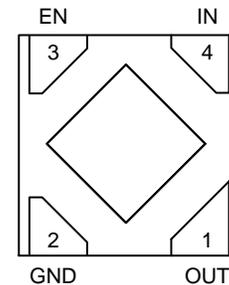
UDFN4  
MX SUFFIX  
CASE 517CU

### MARKING DIAGRAM



XX = Specific Device Code  
M = Date Code

### PIN CONNECTION

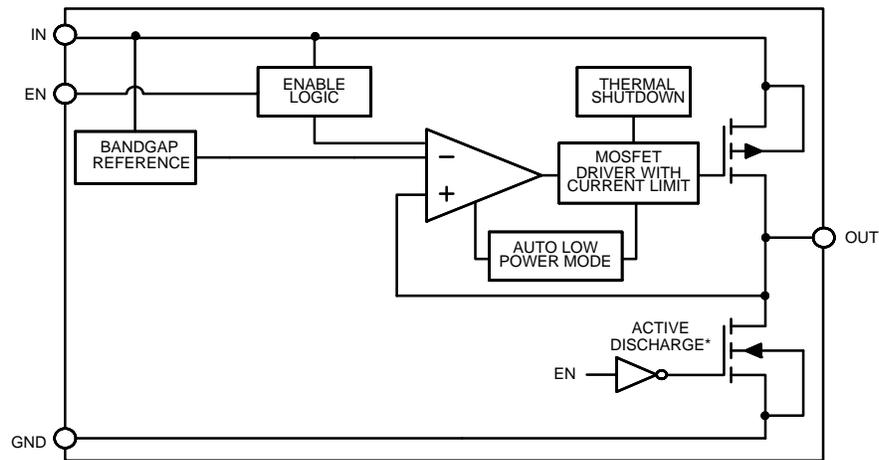


(Bottom View)

### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 14 of this data sheet.

# NCP103



\*Active output discharge function is present only in NCP103AMXyyyTCG devices.  
yyy denotes the particular  $V_{OUT}$  option.

**Figure 2. Simplified Schematic Block Diagram**

## PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	OUT	Regulated output voltage pin. A small ceramic capacitor with minimum value of 1 $\mu\text{F}$ is needed from this pin to ground to assure stability.
2	GND	Power supply ground.
3	EN	Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.
4	IN	Input pin. A small capacitor is needed from this pin to ground to assure stability.
–	EPAD	Exposed pad should be connected directly to the GND pin. Soldered to a large ground copper plane allows for effective heat removal.

## ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	$V_{IN}$	–0.3 V to 6 V	V
Output Voltage	$V_{OUT}$	–0.3 V to $V_{IN} + 0.3$ V or 6 V	V
Enable Input	$V_{EN}$	–0.3 V to $V_{IN} + 0.3$ V or 6 V	V
Output Short Circuit Duration	$t_{SC}$	$\infty$	s
Maximum Junction Temperature	$T_{J(MAX)}$	150	$^{\circ}\text{C}$
Storage Temperature	$T_{STG}$	–55 to 150	$^{\circ}\text{C}$
ESD Capability, Human Body Model (Note 2)	$ESD_{HBM}$	2000	V
ESD Capability, Machine Model (Note 2)	$ESD_{MM}$	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:  
ESD Human Body Model tested per EIA/JESD22–A114,  
ESD Machine Model tested per EIA/JESD22–A115,  
Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

## THERMAL CHARACTERISTICS (Note 3)

Rating	Symbol	Value	Unit
Thermal Characteristics, uDFN4 1x1 mm Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	170	$^{\circ}\text{C}/\text{W}$

3. Single component mounted on 1 oz, FR 4 PCB with 645  $\text{mm}^2$  Cu area.

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## ELECTRICAL CHARACTERISTICS

$-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$ ;  $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$  for  $V_{OUT}$  options greater than 1.5 V. Otherwise  $V_{IN} = 2.5\text{ V}$ , whichever is greater;  $I_{OUT} = 1\text{ mA}$ ,  $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$ , unless otherwise noted.  $V_{EN} = 0.9\text{ V}$ . Typical values are at  $T_J = +25^{\circ}\text{C}$ . Min./Max. are for  $T_J = -40^{\circ}\text{C}$  and  $T_J = +85^{\circ}\text{C}$  respectively (Note 4).

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit	
Operating Input Voltage		$V_{IN}$	1.7		5.5	V	
Output Voltage Accuracy	$-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$	$V_{OUT} \leq 2.0\text{ V}$	$V_{OUT}$	-40	+40	mV	
		$V_{OUT} > 2.0\text{ V}$		-2	+2	%	
Line Regulation	$V_{OUT} + 0.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ ( $V_{IN} \geq 1.7\text{ V}$ )	Reg <sub>LINE</sub>		0.01	0.1	%/V	
Load Regulation	$I_{OUT} = 1\text{ mA}$ to 150 mA	Reg <sub>LOAD</sub>		10	30	mV	
Load Transient	$I_{OUT} = 1\text{ mA}$ to 150 mA or 150 mA to 1 mA in 1 $\mu\text{s}$ , $C_{OUT} = 1\text{ }\mu\text{F}$	Tran <sub>LOAD</sub>		-30/ +20		mV	
Dropout Voltage (Note 5)	$I_{OUT} = 150\text{ mA}$	$V_{OUT} = 1.5\text{ V}$	$V_{DO}$		180	235	mV
		$V_{OUT} = 1.85\text{ V}$			120	165	
		$V_{OUT} = 2.8\text{ V}$			75	125	
		$V_{OUT} = 3.0\text{ V}$			72	120	
		$V_{OUT} = 3.1\text{ V}$			70	120	
		$V_{OUT} = 3.3\text{ V}$			65	110	
Output Current Limit	$V_{OUT} = 90\% V_{OUT(nom)}$	$I_{CL}$	150	550		mA	
Ground Current	$I_{OUT} = 0\text{ mA}$	$I_Q$		50	95	$\mu\text{A}$	
Shutdown Current	$V_{EN} \leq 0.4\text{ V}$ , $V_{IN} = 5.5\text{ V}$	$I_{DIS}$		0.01	1	$\mu\text{A}$	
EN Pin Threshold Voltage High Threshold Low Threshold	$V_{EN}$ Voltage increasing $V_{EN}$ Voltage decreasing	$V_{EN\_HI}$ $V_{EN\_LO}$	0.9		0.4	V	
EN Pin Input Current	$V_{EN} = 5.5\text{ V}$	$I_{EN}$		0.3	1.0	$\mu\text{A}$	
Power Supply Rejection Ratio	$V_{IN} = 3.6\text{ V}$ , $V_{OUT} = 3.1\text{ V}$ $I_{OUT} = 150\text{ mA}$	$f = 1\text{ kHz}$	PSRR		75	dB	
Output Noise Voltage	$V_{IN} = 2.5\text{ V}$ , $V_{OUT} = 1.8\text{ V}$ , $I_{OUT} = 150\text{ mA}$ $f = 10\text{ Hz}$ to 100 kHz	$V_N$		60		$\mu\text{V}_{rms}$	
Thermal Shutdown Temperature	Temperature increasing from $T_J = +25^{\circ}\text{C}$	$T_{SD}$		160		$^{\circ}\text{C}$	
Thermal Shutdown Hysteresis	Temperature falling from $T_{SD}$	$T_{SDH}$		20		$^{\circ}\text{C}$	
Active Output Discharge Resistance	$V_{EN} < 0.4\text{ V}$ , Version A only	$R_{DIS}$		100		$\Omega$	

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at  $T_J = T_A = 25^{\circ}\text{C}$ . Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
5. Characterized when  $V_{OUT}$  falls 100 mV below the regulated voltage at  $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$ .

TYPICAL CHARACTERISTICS

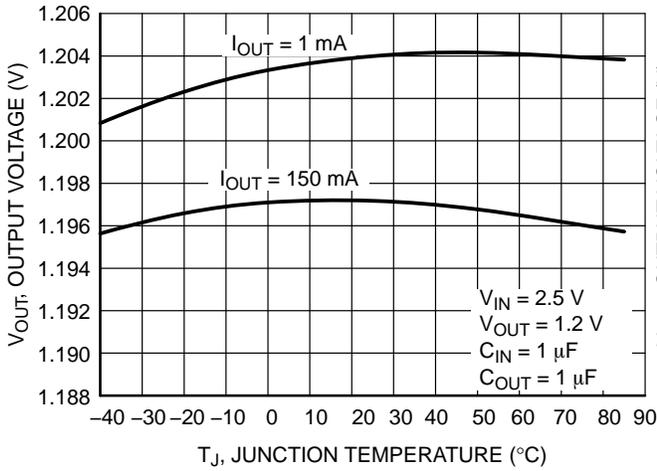


Figure 3. Output Voltage vs. Temperature  
V<sub>OUT</sub> = 1.2 V

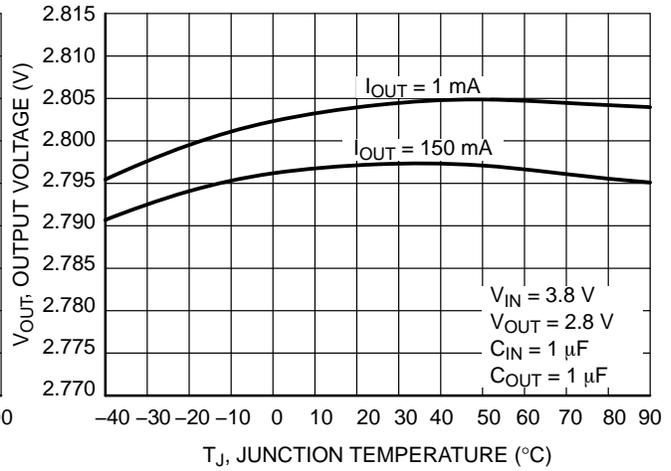


Figure 4. Output Voltage vs. Temperature  
V<sub>OUT</sub> = 2.8 V

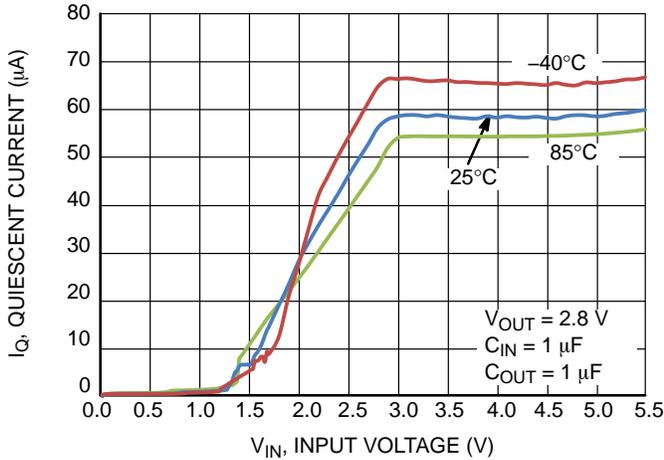


Figure 5. Quiescent Current vs. Input Voltage

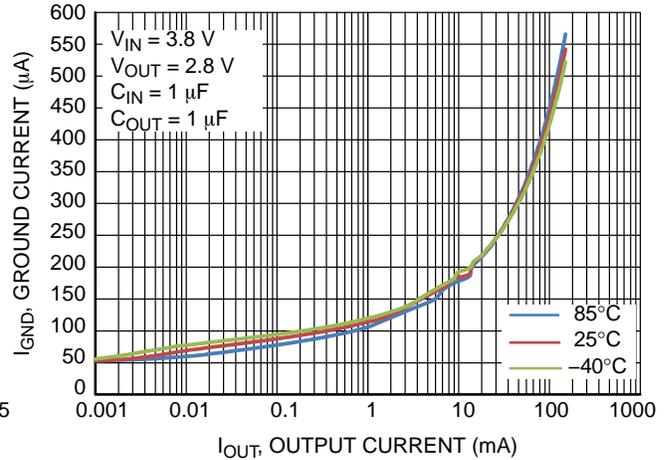


Figure 6. Ground Current vs. Output Current

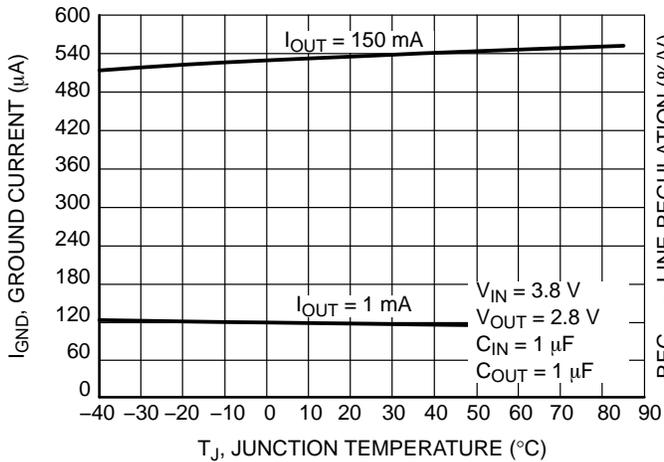


Figure 7. Ground Current vs. Temperature

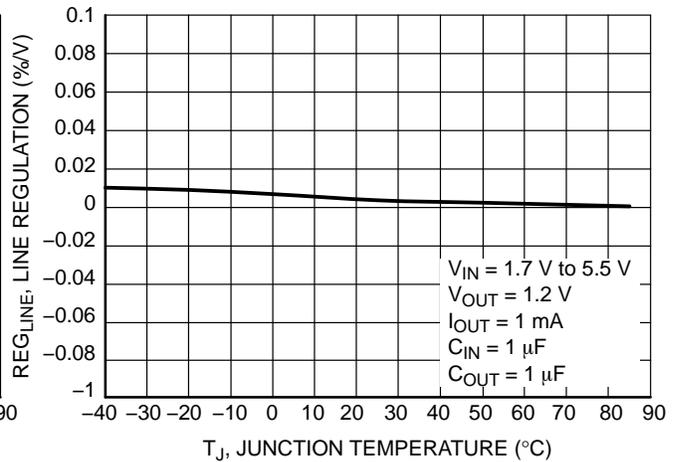


Figure 8. Line Regulation vs. Output Current  
V<sub>OUT</sub> = 1.2 V

TYPICAL CHARACTERISTICS

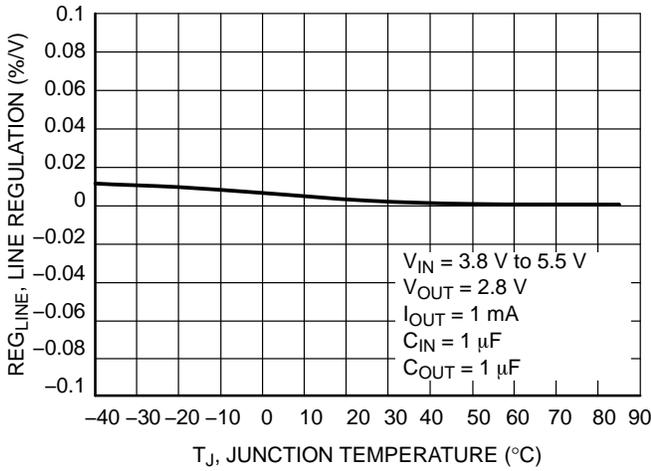


Figure 9. Line Regulation vs. Temperature  
V<sub>OUT</sub> = 2.8 V

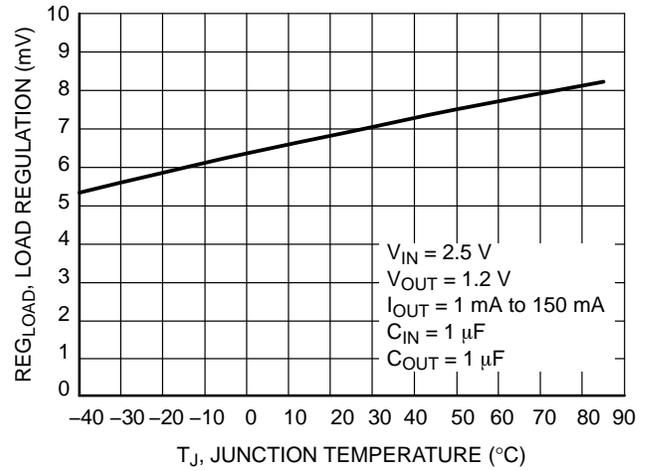


Figure 10. Load Regulation vs. Temperature  
V<sub>OUT</sub> = 1.2 V

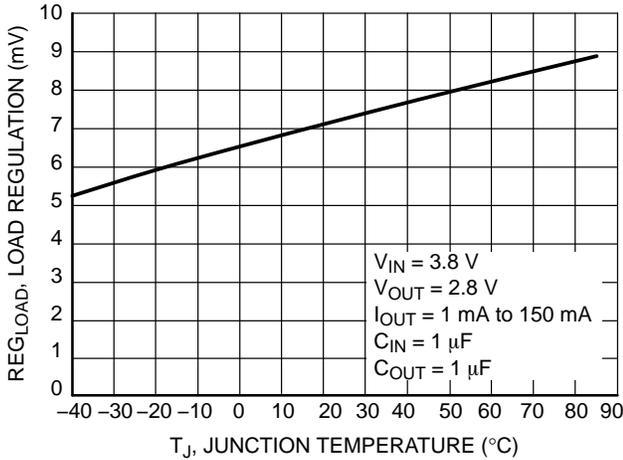


Figure 11. Load Regulation vs. Temperature  
V<sub>OUT</sub> = 2.8 V

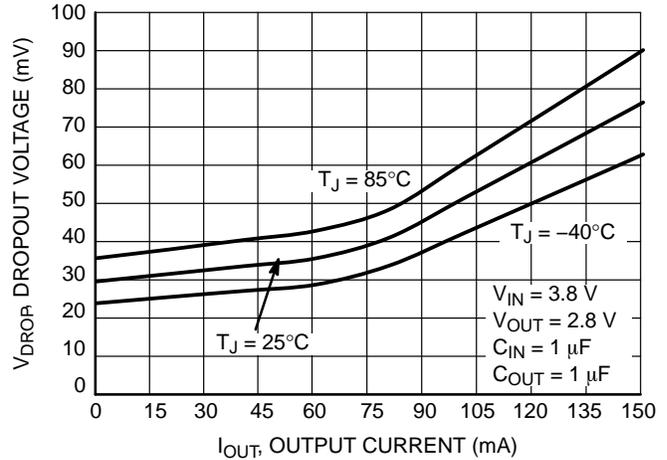


Figure 12. Dropout Voltage vs. Output Current  
V<sub>OUT</sub> = 2.8 V

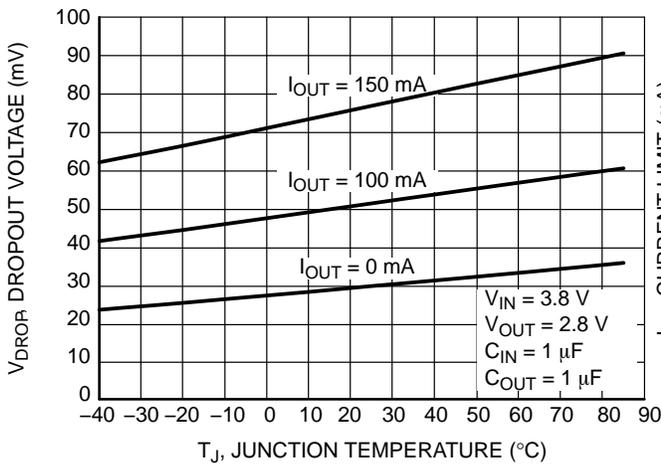


Figure 13. Dropout Voltage vs. Temperature

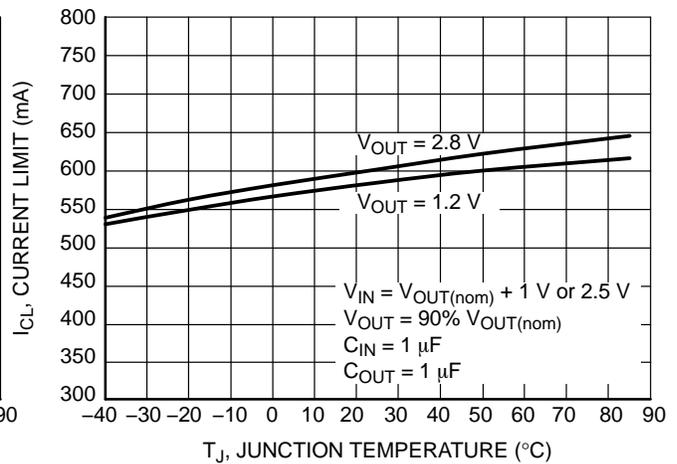


Figure 14. Current Limit vs. Temperature

TYPICAL CHARACTERISTICS

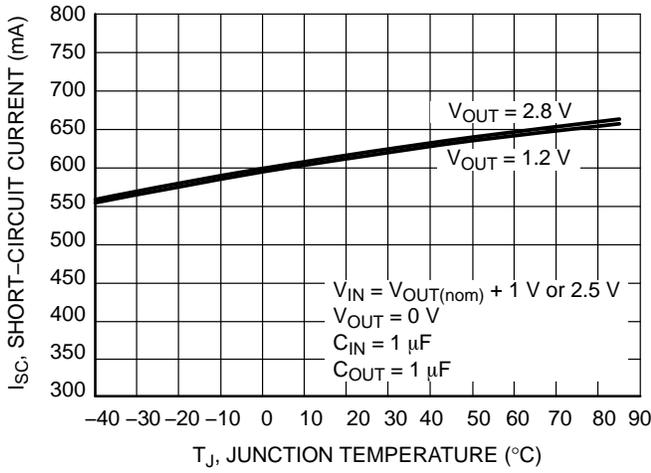


Figure 15. Short-Circuit Current vs. Temperature

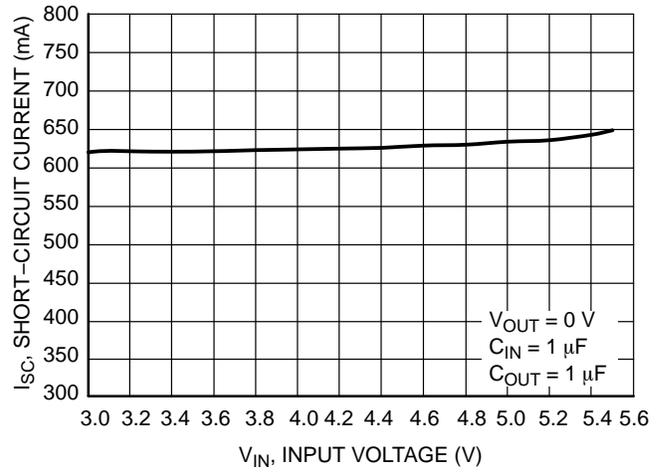


Figure 16. Short-Circuit Current vs. Input Voltage

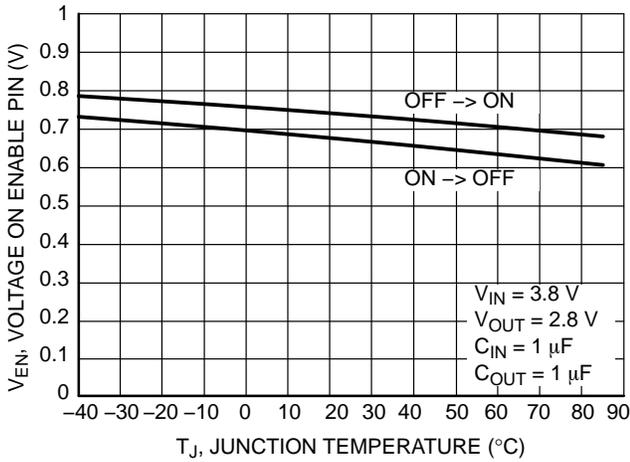


Figure 17. Enable Voltage Threshold vs. Temperature

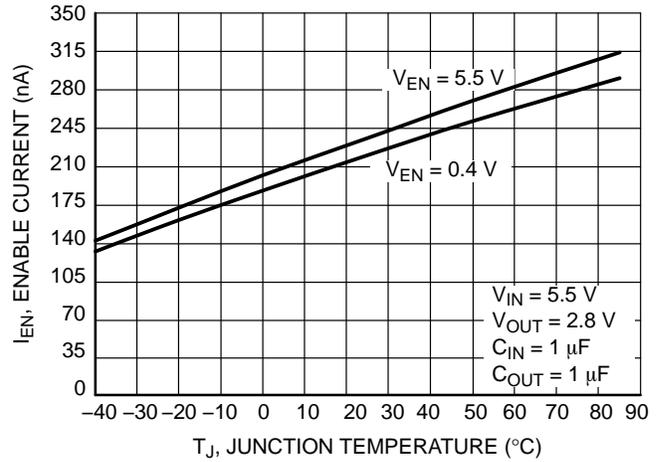


Figure 18. Current to Enable Pin vs. Temperature

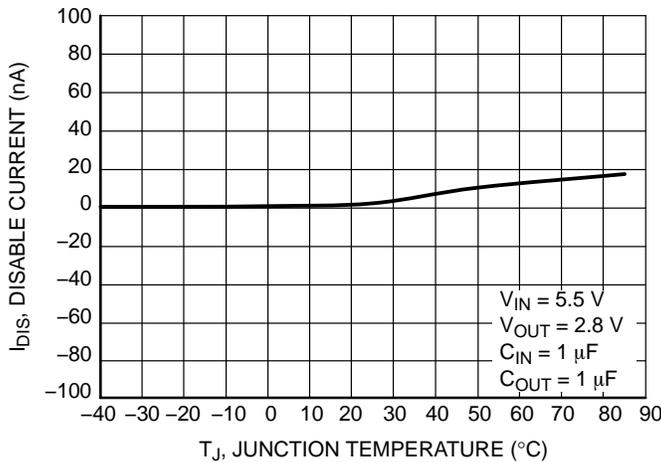
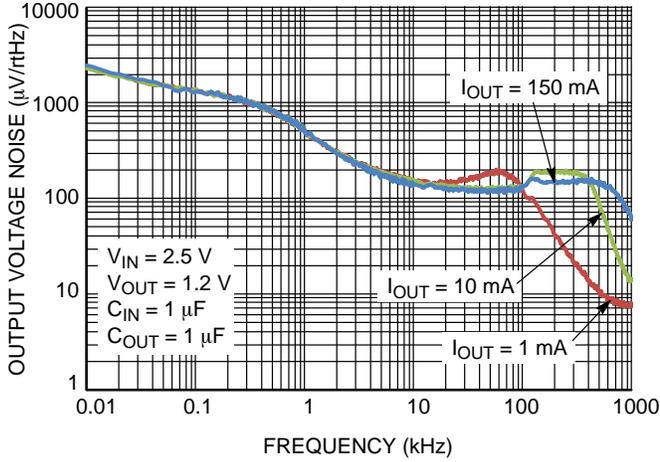


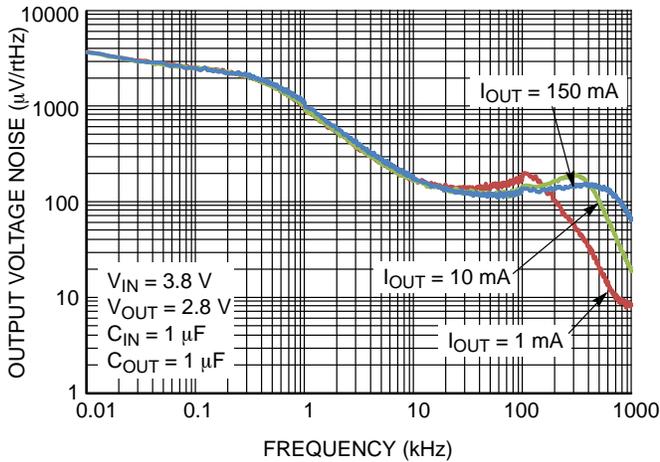
Figure 19. Disable Current vs. Temperature

TYPICAL CHARACTERISTICS



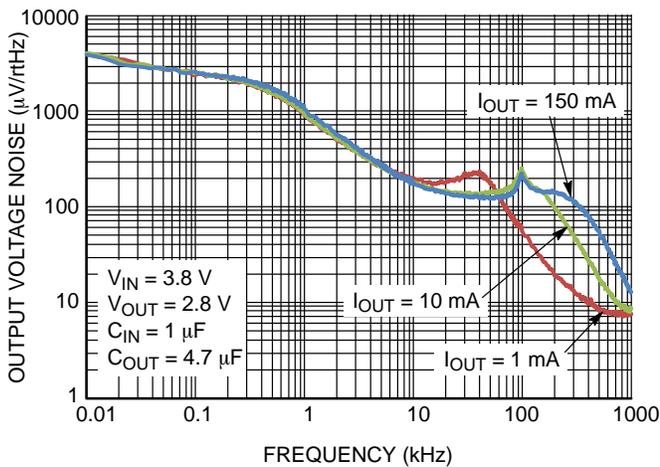
$I_{OUT}$	RMS Output Noise ( $\mu\text{V}$ )	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	60.93	59.11
10 mA	52.73	50.63
150 mA	51.20	48.96

Figure 20. Output Voltage Noise Spectral Density for  $V_{OUT} = 1.2\text{ V}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$



$I_{OUT}$	RMS Output Noise ( $\mu\text{V}$ )	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	79.23	74.66
10 mA	75.03	70.37
150 mA	77.28	72.66

Figure 21. Output Voltage Noise Spectral Density for  $V_{OUT} = 2.8\text{ V}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$



$I_{OUT}$	RMS Output Noise ( $\mu\text{V}$ )	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	80.17	75.29
10 mA	81.28	76.46
150 mA	81.31	76.77

Figure 22. Output Voltage Noise Spectral Density for  $V_{OUT} = 2.8\text{ V}$ ,  $C_{OUT} = 4.7\text{ }\mu\text{F}$

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## TYPICAL CHARACTERISTICS

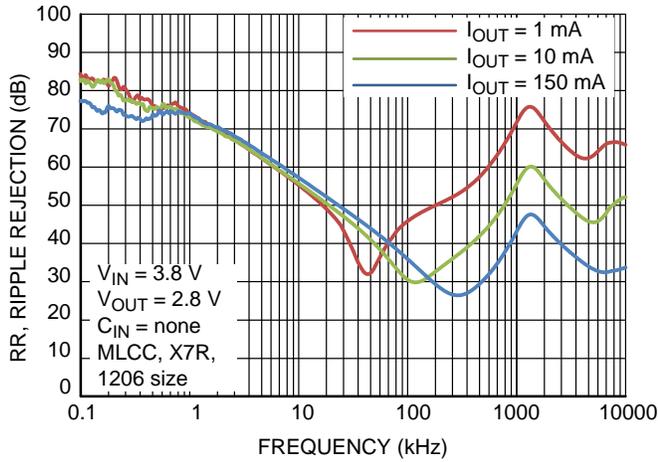


Figure 23. Power Supply Rejection Ratio,  
 $V_{OUT} = 1.2\text{ V}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$

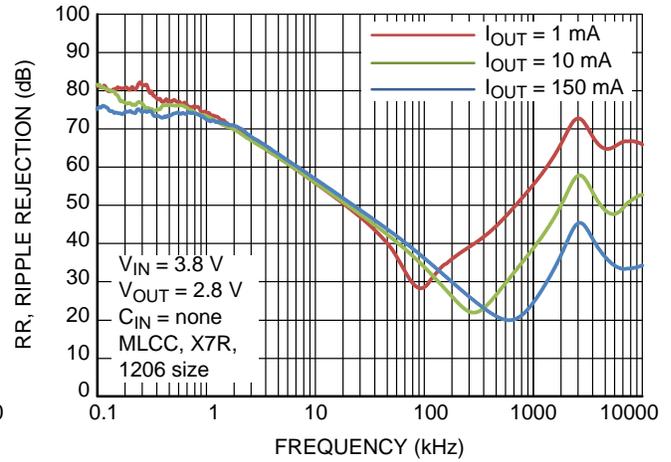


Figure 24. Power Supply Rejection Ratio,  
 $V_{OUT} = 2.8\text{ V}$ ,  $C_{OUT} = 4.7\text{ }\mu\text{F}$

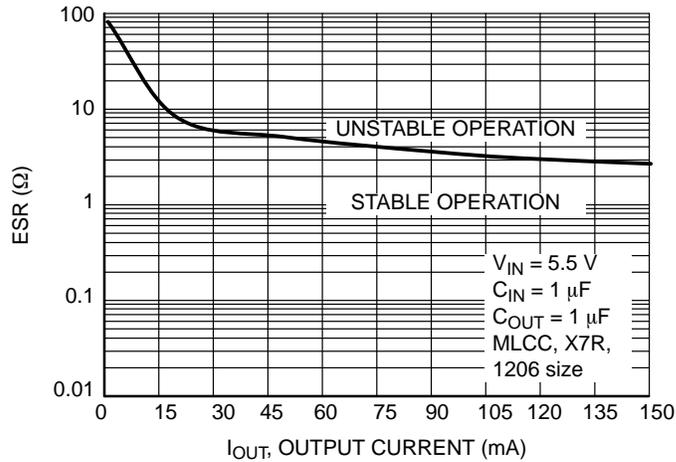


Figure 25. Output Capacitor ESR vs. Output Current

TYPICAL CHARACTERISTICS

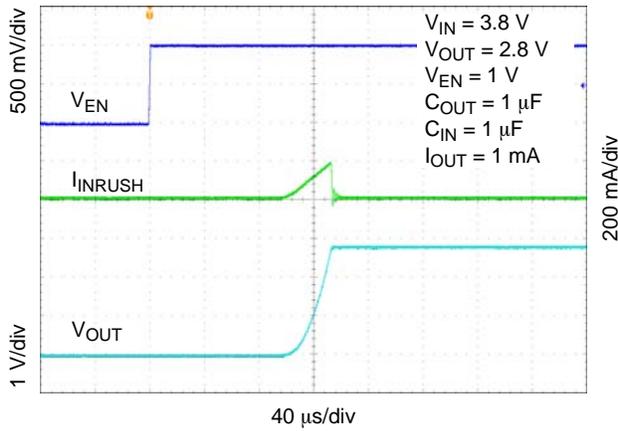


Figure 26. Enable Turn-on Response,  $C_{OUT} = 1 \mu F$ ,  $I_{OUT} = 1 \text{ mA}$

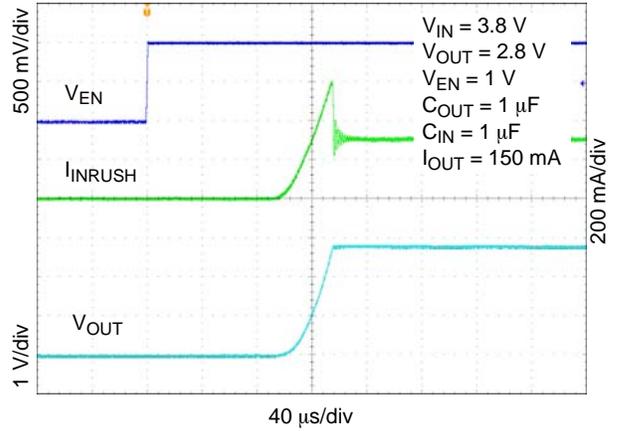


Figure 27. Enable Turn-on Response,  $C_{OUT} = 1 \mu F$ ,  $I_{OUT} = 150 \text{ mA}$

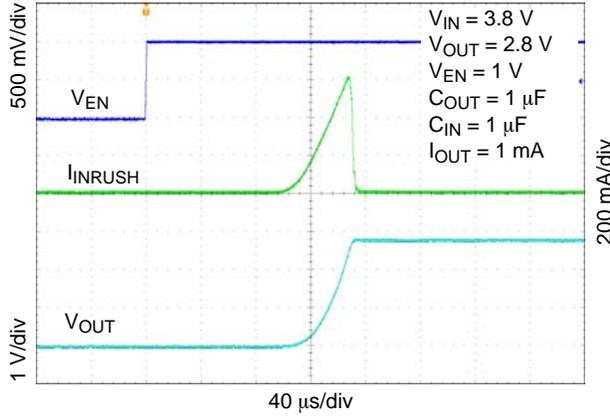


Figure 28. Enable Turn-on Response,  $C_{OUT} = 4.7 \mu F$ ,  $I_{OUT} = 1 \text{ mA}$

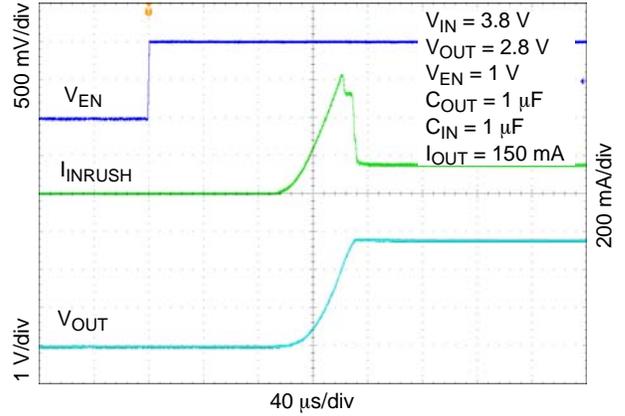


Figure 29. Enable Turn-on Response,  $C_{OUT} = 4.7 \mu F$ ,  $I_{OUT} = 150 \text{ mA}$

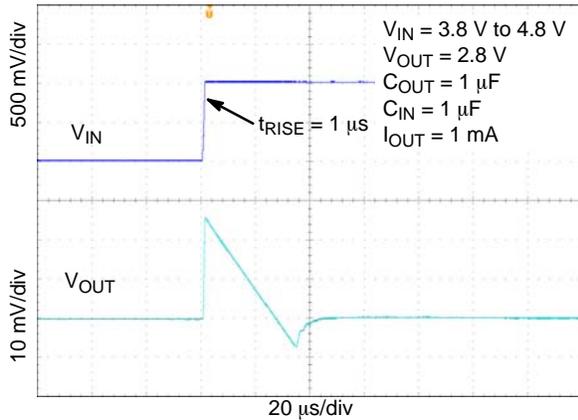


Figure 30. Line Transient Response – Rising Edge,  $V_{OUT} = 2.8 \text{ V}$ ,  $I_{OUT} = 1 \text{ mA}$

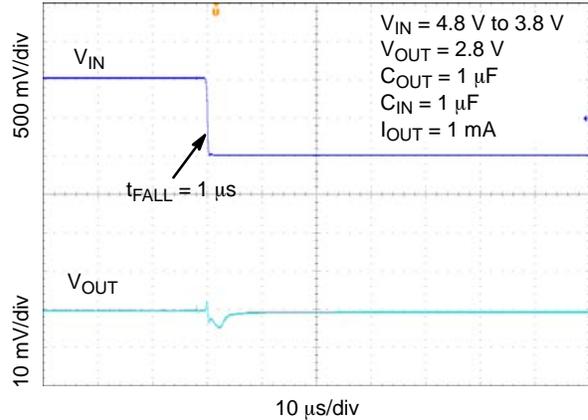


Figure 31. Line Transient Response – Falling Edge,  $V_{OUT} = 2.8 \text{ V}$ ,  $I_{OUT} = 1 \text{ mA}$

TYPICAL CHARACTERISTICS

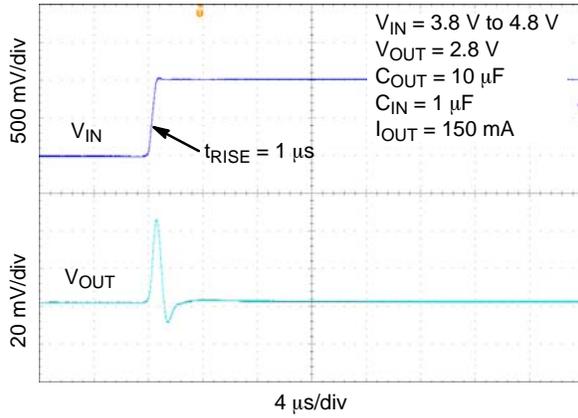


Figure 32. Line Transient Response – Rising Edge,  $V_{OUT} = 2.8\text{ V}$ ,  $I_{OUT} = 150\text{ mA}$

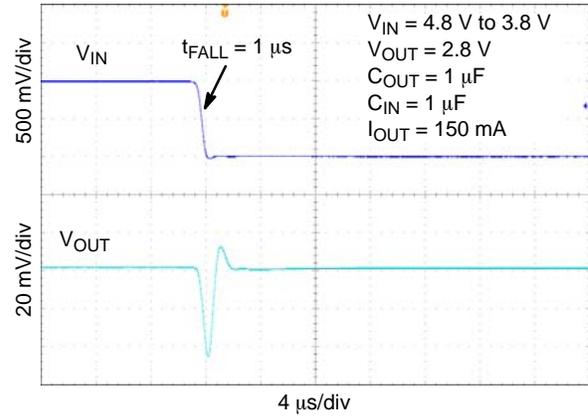


Figure 33. Line Transient Response – Falling Edge,  $V_{OUT} = 2.8\text{ V}$ ,  $I_{OUT} = 150\text{ mA}$

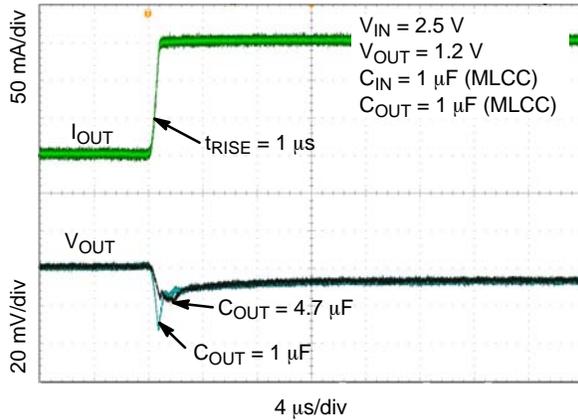


Figure 34. Load Transient Response – Rising Edge,  $V_{OUT} = 1.2\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$  to  $150\text{ mA}$ ,  $C_{OUT} = 1\text{ μF}$ ,  $4.7\text{ μF}$

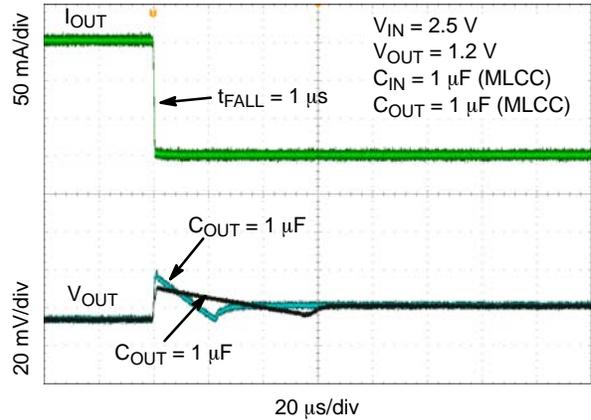


Figure 35. Load Transient Response – Falling Edge,  $V_{OUT} = 1.2\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$  to  $150\text{ mA}$ ,  $C_{OUT} = 1\text{ μF}$ ,  $4.7\text{ μF}$

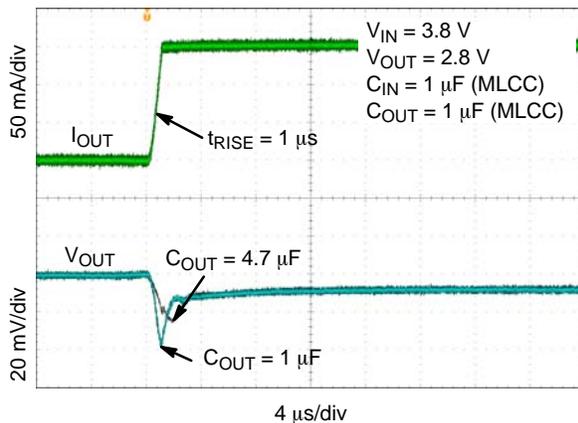


Figure 36. Load Transient Response – Rising Edge,  $V_{OUT} = 2.8\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$  to  $150\text{ mA}$ ,  $C_{OUT} = 1\text{ μF}$ ,  $4.7\text{ μF}$

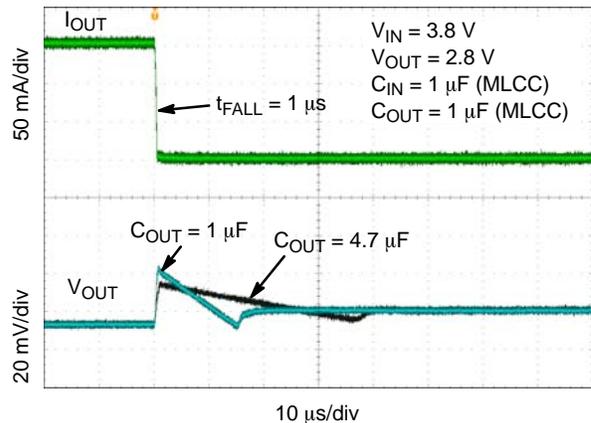
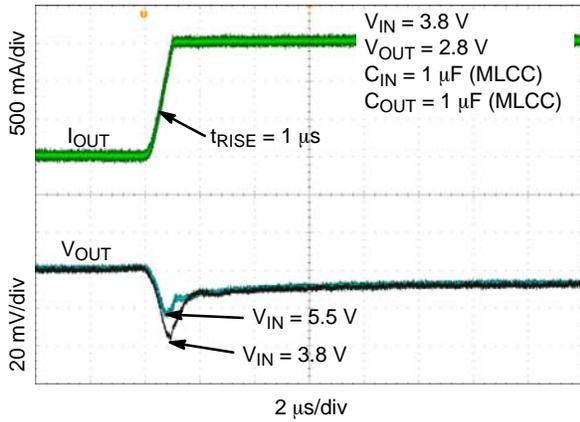
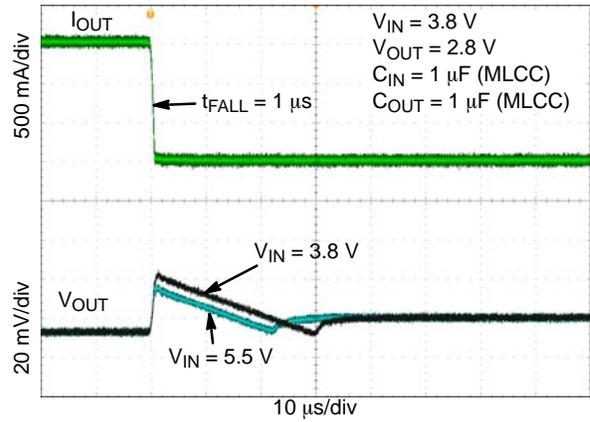


Figure 37. Load Transient Response – Falling Edge,  $V_{OUT} = 2.8\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$  to  $150\text{ mA}$ ,  $C_{OUT} = 1\text{ μF}$ ,  $4.7\text{ μF}$

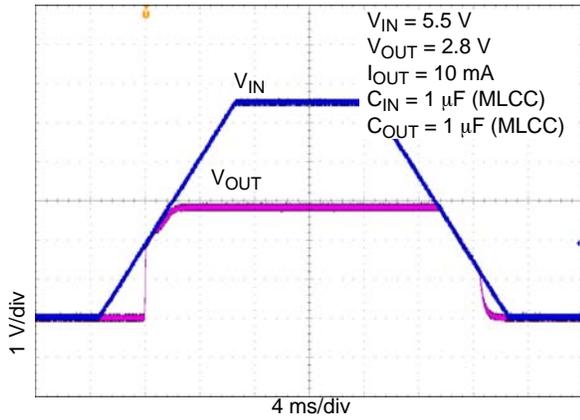
TYPICAL CHARACTERISTICS



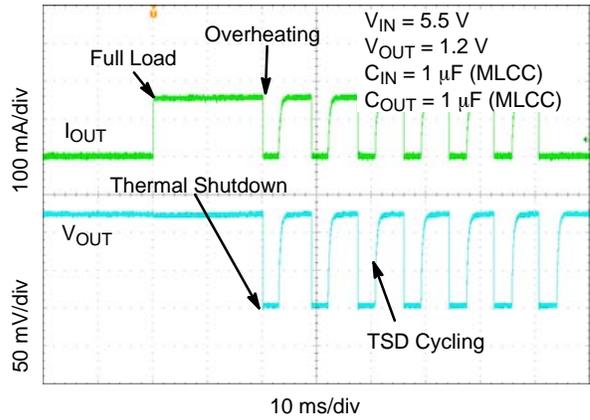
**Figure 38. Load Transient Response – Rising Edge,  $V_{OUT} = 2.8\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$  to  $150\text{ mA}$ ,  $V_{IN} = 3.8\text{ V}$ ,  $5.5\text{ V}$**



**Figure 39. Load Transient Response – Falling Edge,  $V_{OUT} = 2.8\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$  to  $150\text{ mA}$ ,  $V_{IN} = 3.8\text{ V}$ ,  $5.5\text{ V}$**



**Figure 40. Turn-on/off – Slow Rising  $V_{IN}$**



**Figure 41. Short-Circuit and Thermal Shutdown**

## APPLICATIONS INFORMATION

### General

The NCP103 is a high performance 150 mA Low Dropout Linear Regulator. This device delivers very high PSRR (over 75 dB at 1 kHz) and excellent dynamic performance as load/line transients. In connection with very low quiescent current this device is very suitable for various battery powered applications such as tablets, cellular phones, wireless and many others. The device is fully protected in case of output overload, output short circuit condition and overheating, assuring a very robust design.

### Input Capacitor Selection ( $C_{IN}$ )

It is recommended to connect at least a 1 $\mu$ F Ceramic X5R or X7R capacitor as close as possible to the IN pin of the device. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage. There is no requirement for the min. /max. ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes. Larger input capacitor may be necessary if fast and large load transients are encountered in the application.

### Output Decoupling ( $C_{OUT}$ )

The NCP103 requires an output capacitor connected as close as possible to the output pin of the regulator. The recommended capacitor value is 1  $\mu$ F and X7R or X5R dielectric due to its low capacitance variations over the specified temperature range. The NCP103 is designed to remain stable with minimum effective capacitance of 0.22  $\mu$ F to account for changes with temperature, DC bias and package size. Especially for small package size capacitors such as 0402 the effective capacitance drops rapidly with the applied DC bias.

There is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the  $C_{OUT}$  but the maximum value of ESR should be less than 3  $\Omega$ . Larger output capacitors and lower ESR could improve the load transient response or high frequency PSRR. It is not recommended to use tantalum capacitors on the output due to their large ESR. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperature.

### Enable Operation

The NCP103 uses the EN pin to enable/disable its device and to deactivate/activate the active discharge function.

If the EN pin voltage is <0.4 V the device is guaranteed to be disabled. The pass transistor is turned-off so that there is virtually no current flow between the IN and OUT. The active discharge transistor is active so that the output voltage  $V_{OUT}$  is pulled to GND through a 100  $\Omega$  resistor. In the

disable state the device consumes as low as typ. 10 nA from the  $V_{IN}$ .

If the EN pin voltage >0.9 V the device is guaranteed to be enabled. The NCP103 regulates the output voltage and the active discharge transistor is turned-off.

The EN pin has internal pull-down current source with typ. value of 300 nA which assures that the device is turned-off when the EN pin is not connected. In the case where the EN function isn't required the EN should be tied directly to IN.

### Output Current Limit

Output Current is internally limited within the IC to a typical 550 mA. The NCP103 will source this amount of current measured with a voltage drops on the 90% of the nominal  $V_{OUT}$ . If the Output Voltage is directly shorted to ground ( $V_{OUT} = 0$  V), the short circuit protection will limit the output current to 580 mA (typ). The current limit and short circuit protection will work properly over whole temperature range and also input voltage range. There is no limitation for the short circuit duration.

### Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold ( $T_{SD} - 160^{\circ}\text{C}$  typical), Thermal Shutdown event is detected and the device is disabled. The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold ( $T_{SDU} - 140^{\circ}\text{C}$  typical). Once the IC temperature falls below the  $140^{\circ}\text{C}$  the LDO is enabled again. The thermal shutdown feature provides the protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

### Power Dissipation

As power dissipated in the NCP103 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part.

The maximum power dissipation the NCP103 can handle is given by:

$$P_{D(MAX)} = \frac{[125^{\circ}\text{C} - T_A]}{\theta_{JA}} \quad (\text{eq. 1})$$

The power dissipated by the NCP103 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN}(I_{GND}@I_{OUT}) + I_{OUT}(V_{IN} - V_{OUT}) \quad (\text{eq. 2})$$

## NCP103

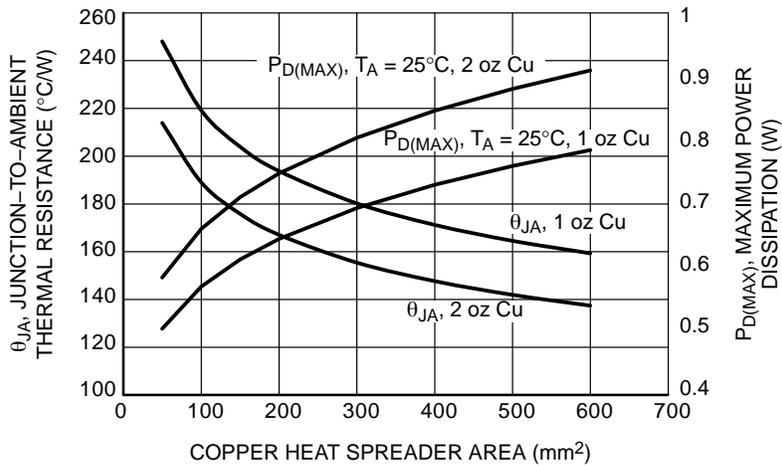


Figure 42.  $\theta_{JA}$  vs. Copper Area (uDFN4)

### Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case that  $V_{OUT} > V_{IN}$ . Due to this fact in cases, where the extended reverse current condition can be anticipated the device may require additional external protection.

### Power Supply Rejection Ratio

The NCP103 features very good Power Supply Rejection ratio. If desired the PSRR at higher frequencies in the range 100 kHz – 10 MHz can be tuned by the selection of  $C_{OUT}$  capacitor and proper PCB layout.

### Turn-On Time

The turn-on time is defined as the time period from EN assertion to the point in which  $V_{OUT}$  will reach 98% of its

nominal value. This time is dependent on various application conditions such as  $V_{OUT(NOM)}$ ,  $C_{OUT}$  and  $T_A$ . For example typical value for  $V_{OUT} = 1.2\text{ V}$ ,  $C_{OUT} = 1\ \mu\text{F}$ ,  $I_{OUT} = 1\ \text{mA}$  and  $T_A = 25^\circ\text{C}$  is 90  $\mu\text{s}$ .

### PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics place  $C_{IN}$  and  $C_{OUT}$  capacitors close to the device pins and make the PCB traces wide. In order to minimize the solution size, use 0402 capacitors. Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated from the equation above (Equation 2). Expose pad should be tied the shortest path to the GND pin.

# NCP103

## ORDERING INFORMATION

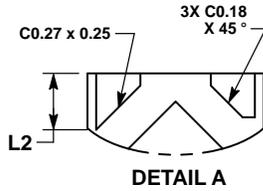
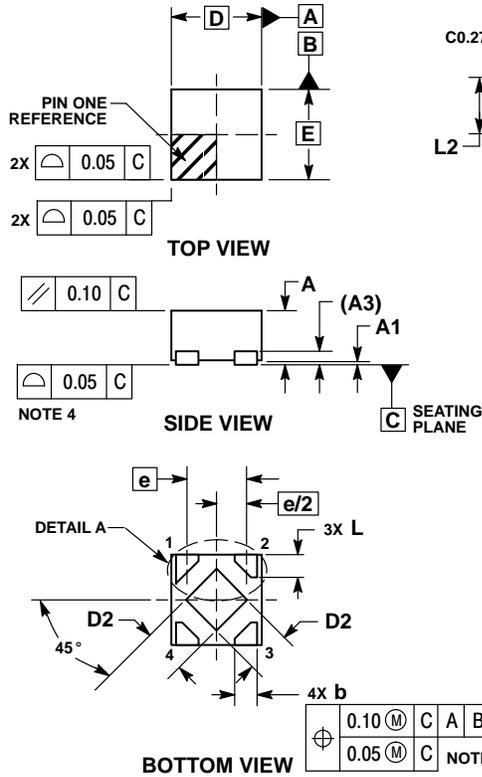
Device	Voltage Option	Marking	Marking Rotation	Option	Package	Shipping <sup>†</sup>		
NCP103AMX090TCG	0.9 V	AQ	0°	With active output discharge function	uDFN4 (Pb-Free)	3000 / Tape & Reel		
NCP103AMX100TCG	1.0 V	5	180°					
NCP103AMX105TCG	1.05 V	A	0°					
NCP103AMX110TCG	1.1 V	E	180°					
NCP103AMX120TCG	1.2 V	D	0°					
NCP103AMX125TCG	1.25 V	D	180°					
NCP103AMX130TCG	1.3 V	AD	0°					
NCP103AMX150TCG	1.5 V	E	0°					
NCP103AMX160TCG	1.6 V	Y	180°					
NCP103AMX180TCG	1.8 V	K	180°					
NCP103AMX185TCG	1.85 V	F	0°					
NCP103AMX210TCG	2.1 V	P	180°					
NCP103AMX220TCG	2.2 V	R	180°					
NCP103AMX240TCG	2.4 V	AL	0°					
NCP103AMX260TCG	2.6 V	V	180°					
NCP103AMX270TCG	2.7 V	AK	0°					
NCP103AMX280TCG	2.8 V	J	0°					
NCP103AMX285TCG	2.85 V	K	0°					
NCP103AMX300TCG	3.0 V	L	0°					
NCP103AMX310TCG	3.1 V	P	0°					
NCP103AMX330TCG	3.3 V	Q	0°					
NCP103AMX345TCG	3.45 V	AE	0°					
NCP103AMX350TCG	3.5 V	3	180°					
NCP103BMX100TCG	1.0 V	5	270°	Without active output discharge function			uDFN4 (Pb-Free)	3000 / Tape & Reel
NCP103BMX105TCG	1.05 V	A	90°					
NCP103BMX110TCG	1.1 V	E	270°					
NCP103BMX120TCG	1.2 V	D	90°					
NCP103BMX125TCG	1.25 V	D	270°					
NCP103BMX130TCG	1.3 V	CD	0°					
NCP103BMX150TCG	1.5 V	E	90°					
NCP103BMX160TCG	1.6 V	Y	270°					
NCP103BMX180TCG	1.8 V	K	270°					
NCP103BMX185TCG	1.85 V	F	90°					
NCP103BMX210TCG	2.1 V	P	270°					
NCP103BMX220TCG	2.2 V	R	270°					
NCP103BMX250TCG	2.5 V	CH	0°					
NCP103BMX260TCG	2.6 V	V	270°					
NCP103BMX280TCG	2.8 V	J	90°					
NCP103BMX285TCG	2.85 V	K	90°					
NCP103BMX300TCG	3.0 V	L	90°					
NCP103BMX310TCG	3.1 V	P	90°					
NCP103BMX330TCG	3.3 V	Q	90°					
NCP103BMX345TCG	3.45 V	CE	0°					
NCP103BMX350TCG	3.5 V	3	270°					

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NCP103

## PACKAGE DIMENSIONS

### UDFN4 1.0x1.0, 0.65P CASE 517CU ISSUE O

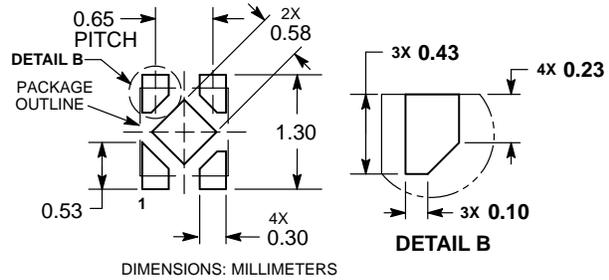


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.03 AND 0.07 FROM THE TERMINAL TIPS.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	---	0.60
A1	0.00	0.05
A3	0.15	REF
b	0.20	0.30
D	1.00	BSC
D2	0.38	0.58
E	1.00	BSC
e	0.65	BSC
L	0.20	0.30
L2	0.27	0.37

### RECOMMENDED MOUNTING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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