

# FDB15N50

## N-Channel UniFET™ MOSFET

500 V, 15 A, 380 mΩ

### Features

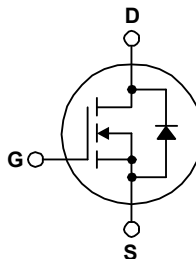
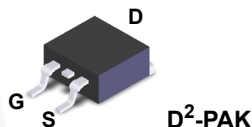
- Low gate charge  $Q_g$  results in simple drive requirement (Typ. 33 nC)
- Improved Gate, avalanche and high reappplied dv/dt ruggedness
- Reduced  $R_{DS(on)}$  ( 330mΩ ( Typ.) @  $V_{GS} = 10\text{ V}$ ,  $I_D = 7.5\text{ A}$ )
- Reduced Miller capacitance and low Input capacitance (Typ.  $C_{rss} = 16\text{ pF}$ )
- Improved switching speed with low EMI
- 175°C rated junction temperature

### Description

UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

### Applications

- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDB15N50	Unit
$V_{DSS}$	Drain to Source Voltage	500	V
$V_{GS}$	Gate to Source Voltage	$\pm 30$	V
$I_D$	Drain Current Continuous ( $T_C = 25^\circ\text{C}$ , $V_{GS} = 10\text{V}$ )	15	A
	Continuous ( $T_C = 100^\circ\text{C}$ , $V_{GS} = 10\text{V}$ )	11	A
	Pulsed (Note 1)	60	A
$P_D$	Power dissipation	300	W
	Derate above $25^\circ\text{C}$	2	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$
	Soldering Temperature for 10 seconds	300 (1.6mm from case)	$^\circ\text{C}$

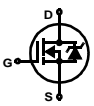
### Thermal Characteristics

Symbol	Parameter	FDB15N50	Unit
$R_{\theta JC}$	Thermal Resistance Junction to Case, Max.	0.50	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient, Max.	62	$^\circ\text{C}/\text{W}$

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB15N50	FDB15N50	D <sup>2</sup> -PAK	330 mm	24 mm	800 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	
<b>Statics</b>							
$B_{VDSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$	500	-	-	V	
$\Delta B_{VDSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	Reference to $25^\circ\text{C}$ , $I_D = 1\text{mA}$	-	0.58	-	$\text{V}/^\circ\text{C}$	
$R_{DS(ON)}$	Drain to Source On-Resistance	$V_{GS} = 10\text{V}$ , $I_D = 7.5\text{A}$	-	0.33	0.38	$\Omega$	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250\mu\text{A}$	2.0	3.4	4.0	V	
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{V}$	$T_C = 25^\circ\text{C}$	-	-	25	$\mu\text{A}$
		$V_{GS} = 0\text{V}$	$T_C = 150^\circ\text{C}$	-	-	250	
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 30\text{V}$	-	-	$\pm 100$	nA	
<b>Dynamics</b>							
$g_{fs}$	Forward Transconductance	$V_{DD} = 10\text{V}$ , $I_D = 7.5\text{A}$	10	-	-	S	
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 10\text{V}$ , $V_{DS} = 400\text{V}$ , $I_D = 15\text{A}$	-	33	41	nC	
$Q_{gs}$	Gate to Source Gate Charge		-	7.2	10	nC	
$Q_{gd}$	Gate to Drain "Miller" Charge		-	12	16	nC	
$t_{d(ON)}$	Turn-On Delay Time		$V_{DD} = 250\text{V}$ , $I_D = 15\text{A}$	-	9	-	ns
$t_r$	Rise Time	$R_G = 6.2\Omega$ , $R_D = 17\Omega$	-	5.4	-	ns	
$t_{d(OFF)}$	Turn-Off Delay Time		-	26	-	ns	
$t_f$	Fall Time		-	5	-	ns	
$C_{ISS}$	Input Capacitance	$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$	-	1850	-	pF	
$C_{OSS}$	Output Capacitance		-	230	-	pF	
$C_{RSS}$	Reverse Transfer Capacitance		-	16	-	pF	
<b>Avalanche Characteristics</b>							
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)		760	-	-	mJ	
$I_{AR}$	Avalanche Current		-	-	15	A	
<b>Drain-Source Diode Characteristics</b>							
$I_S$	Continuous Source Current (Body Diode)	MOSFET symbol showing the integral reverse p-n junction diode. 	-	-	15	A	
$I_{SM}$	Pulsed Source Current (Body Diode) (Note 1)		-	-	60	A	
$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 15\text{A}$	-	0.86	1.2	V	
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 15\text{A}$ , $di_{SD}/dt = 100\text{A}/\mu\text{s}$	-	470	730	ns	
$Q_{RR}$	Reverse Recovered Charge	$I_{SD} = 15\text{A}$ , $di_{SD}/dt = 100\text{A}/\mu\text{s}$	-	5	6.6	$\mu\text{C}$	

### Notes:

- 1: Repetitive rating; pulse width limited by maximum junction temperature.
- 2: Starting  $T_J = 25^\circ\text{C}$ ,  $L = 7.0\text{mH}$ ,  $I_{AS} = 15\text{A}$ .

## Typical Characteristics

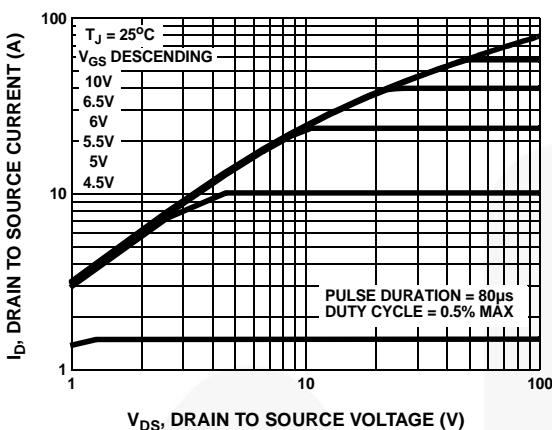


Figure 1. Output Characteristics

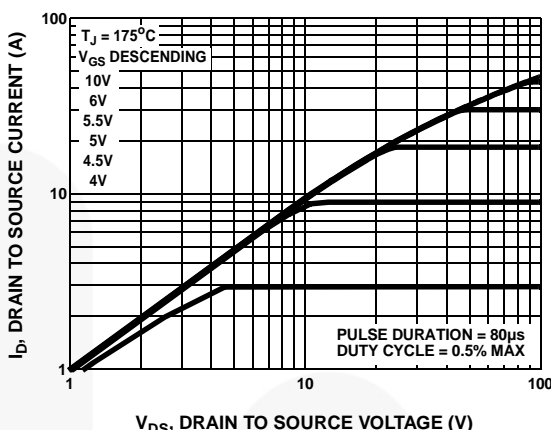


Figure 2. Output Characteristics

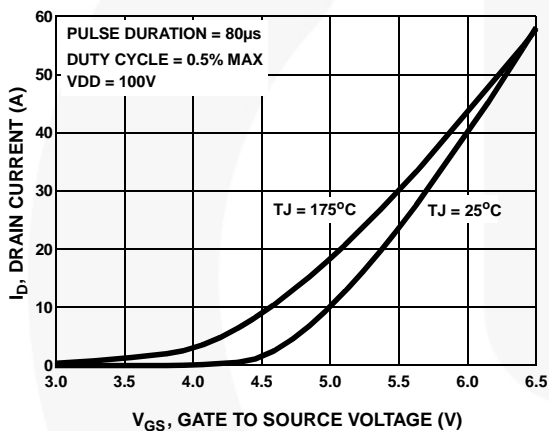


Figure 3. Transfer Characteristics

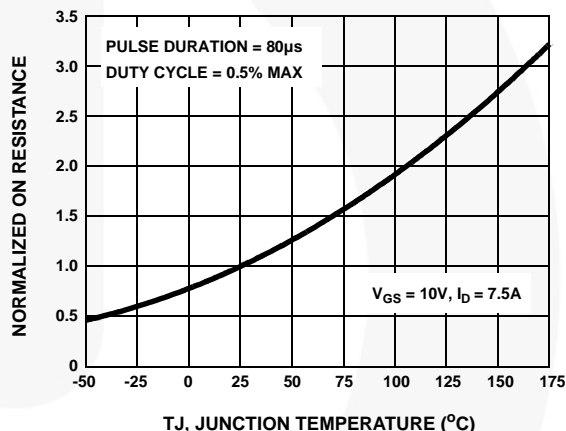


Figure 4. Normalized Drain To Source On Resistance vs Junction Temperature

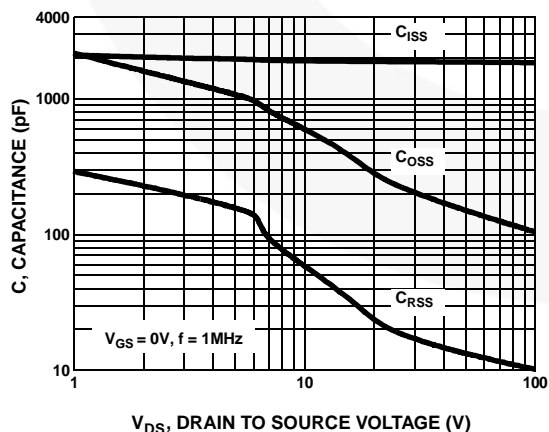


Figure 5. Capacitance vs Drain To Source Voltage

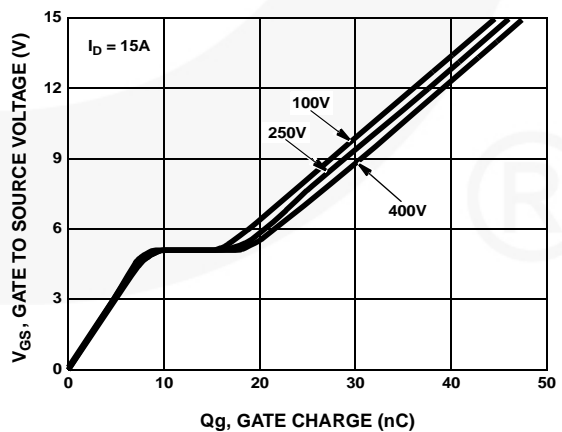
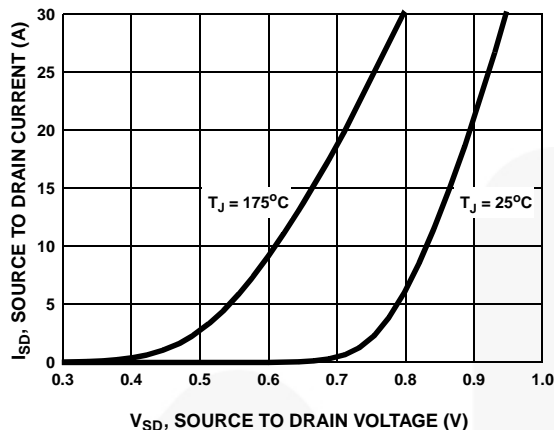
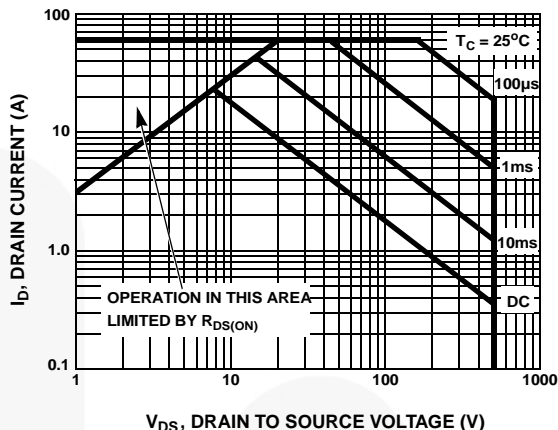


Figure 6. Gate Charge Waveforms For Constant Gate Current

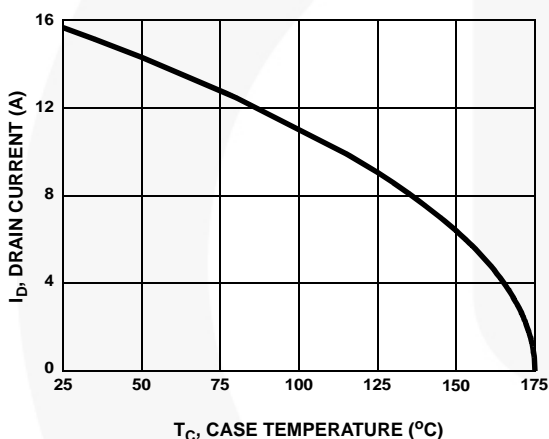
## Typical Characteristics



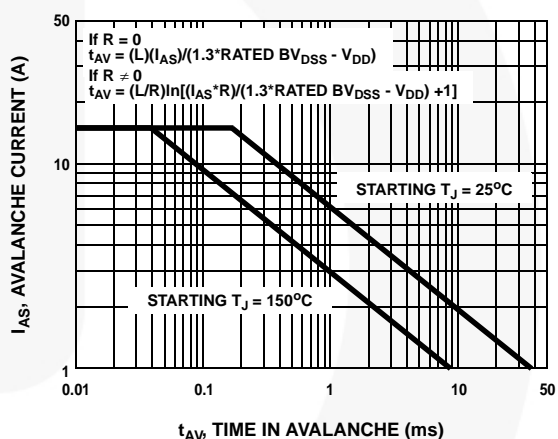
**Figure 7. Body Diode Forward Voltage vs Body Diode Current**



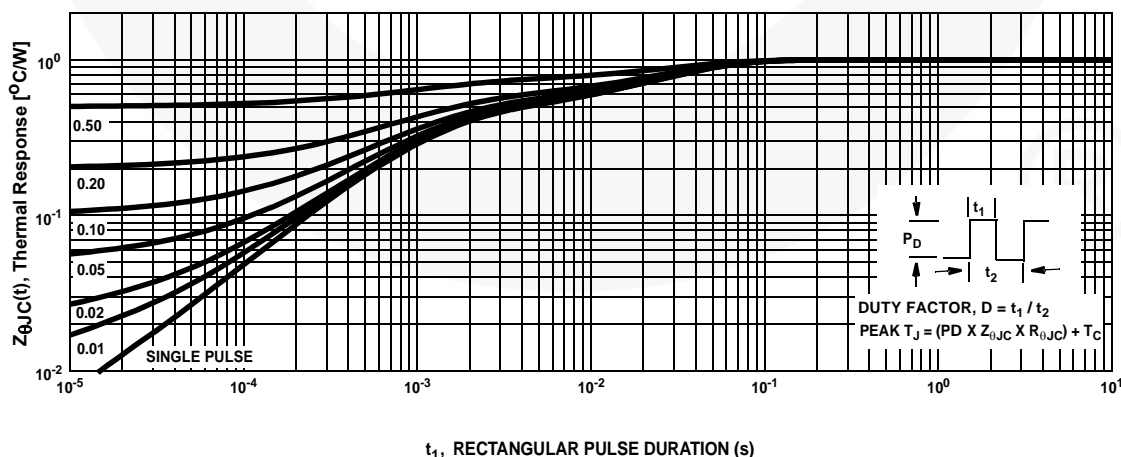
**Figure 8. Maximum Safe Operating Area**



**Figure 9. Maximum Drain Current vs Case Temperature**



**Figure 10. Unclamped Inductive Switching Capability**



**Figure 11. Normalized Transient Thermal Impedance, Junction to Case**

### Test Circuits and Waveforms

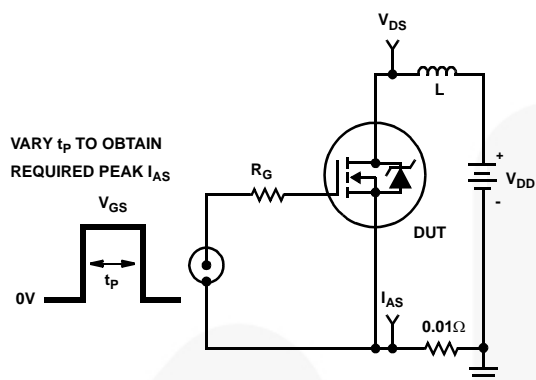


Figure 12. Unclamped Energy Test Circuit

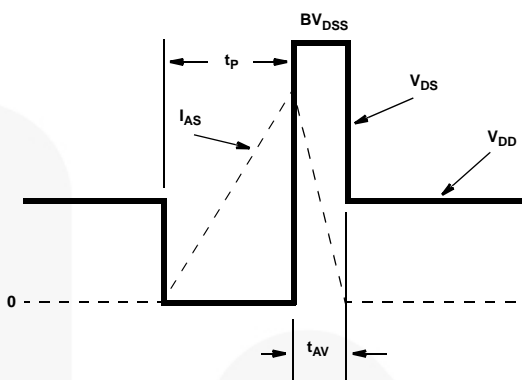


Figure 13. Unclamped Energy Waveforms

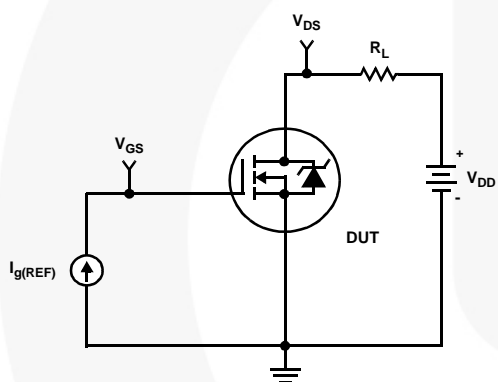


Figure 14. Gate Charge Test Circuit

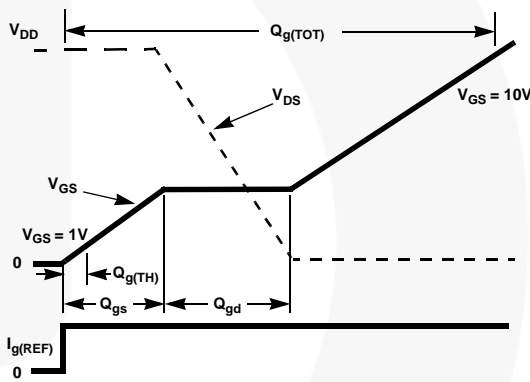


Figure 15. Gate Charge Waveforms

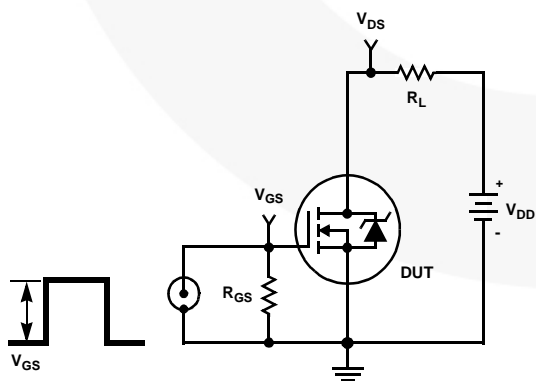


Figure 16. Switching Time Test Circuit

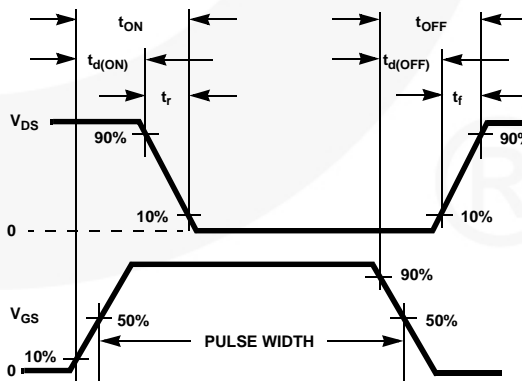
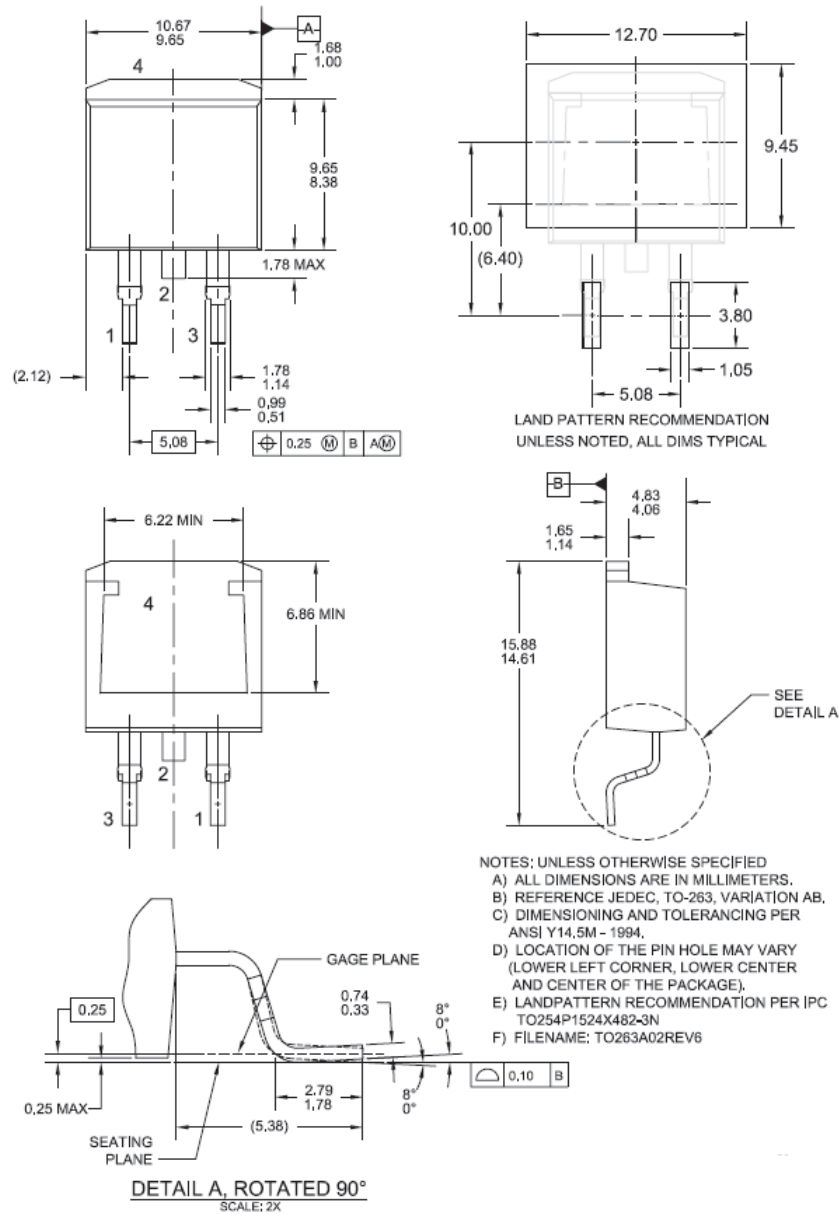


Figure 17. Switching Time Waveform

## Mechanical Dimensions



**Figure 18. TO263 (D<sup>2</sup>PAK), Molded, 2-Lead, Surface Mount**

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Rev. 166

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