Power MOSFET

30 V, 4.2 m Ω , 71 A, Single N–Channel, u8FL

Features

- Low R_{DS(on)} to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- NVTFS4C06NWF Wettable Flanks Product
- NVT Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	30	V
Gate-to-Source Voltage			V_{GS}	±20	V
Continuous Drain		T _A = 25°C	I _D	21	Α
Current $R_{\theta JA}$ (Notes 1, 2, 4)		T _A = 100°C		15	
Power Dissipation R _{θJA}		T _A = 25°C	P _D	3.1	W
(Note 1, 2, 4)	Steady	T _A = 100°C		1.6	
Continuous Drain Current R _{0.IC} (Note 1,	State	T _A = 25°C	I _D	71	
3, 4)		T _A = 100°C		50	Α
Power Dissipation		T _A = 25°C	P_{D}	37	W
$R_{\theta JC}$ (Note 1, 3, 4)		T _A = 100°C		18	
Pulsed Drain Current	$T_A = 25^{\circ}$	$C, t_p = 10 \mu s$	I _{DM}	367	Α
Operating Junction and Storage Temperature			T _J , T _{stg}	–55 to +175	°C
Source Current (Body Diode)			IS	33	Α
Single Pulse Drain–to–Source Avalanche Energy $(T_J = 25$ °C, $I_L = 26$ A_{pk} , $L = 0.1$ mH)			E _{AS}	34	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Drain) (Notes 1 and 4)	$R_{\theta JC}$	4.1	°C/W
Junction-to-Ambient - Steady State (Notes 1 and 2)	$R_{\theta JA}$	48	C/ V V

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Surface–mounted on FR4 board using a 650 mm^2 2 oz. Cu pad.
- Assumes heat-sink sufficiently large to maintain constant case temperature independent of device power.
- 4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

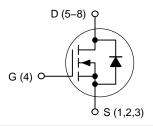


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V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX
30 V	4.2 mΩ @ 10 V	71 A
30 V	6.1 mΩ @ 4.5 V	717

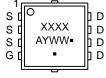
N-Channel MOSFET





MARKING DIAGRAM





4C06 = Specific Device Code for

NVMTS4C06N

06WF = Specific Device Code of NVTFS4C06NWF

A = Assembly Location

Y = Year WW = Work Week ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit	
OFF CHARACTERISTICS	•			•			•	
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		30			V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /				14.4		mV/°C	
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 24 V	$T_J = 25^{\circ}C$ $T_J = 125^{\circ}C$			1.0	μΑ	
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS}$	_			±100	nA	
ON CHARACTERISTICS (Note 5)				<u>I</u>				
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$		1.3		2.2	V	
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				3.8		mV/°C	
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 30 A		3.4	4.2		
		V _{GS} = 4.5 V	I _D = 30 A		4.9	6.1	mΩ	
Forward Transconductance	9FS	V _{DS} = 1.5 V, I _I	o = 15 A		58		S	
Gate Resistance	R _G	T _A = 25°	С		1.0		Ω	
CHARGES AND CAPACITANCES								
Input Capacitance	C _{ISS}				1683		pF	
Output Capacitance	Coss	V _{GS} = 0 V, f = 1 MH	z, V _{DS} = 15 V		841			
Reverse Transfer Capacitance	C _{RSS}				40			
Capacitance Ratio	C _{RSS} /C _{ISS}	V _{GS} = 0 V, V _{DS} = 15 V, f = 1 MHz			0.023			
Total Gate Charge	Q _{G(TOT)}				11.6		nC	
Threshold Gate Charge	Q _{G(TH)}				2.6			
Gate-to-Source Charge	Q _{GS}	$V_{GS} = 4.5 \text{ V}, V_{DS} = 7$	15 V; I _D = 30 A		4.7			
Gate-to-Drain Charge	Q_{GD}				4.0			
Gate Plateau Voltage	V_{GP}				3.1		V	
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 1	5 V; I _D = 30 A		26		nC	
SWITCHING CHARACTERISTICS (Note 6)	. , ,							
Turn-On Delay Time	t _{d(ON)}				10			
Rise Time	t _r	Vcs = 4.5 V. Vn	e = 15 V.		32		ns	
Turn-Off Delay Time	t _{d(OFF)}	$V_{GS} = 4.5 \text{ V}, V_{D}$ $I_{D} = 15 \text{ A}, R_{G}$	$= 3.0 \Omega$		18			
Fall Time	t _f				5.0			
Turn-On Delay Time	t _{d(ON)}	$V_{GS} = 10 \text{ V}, V_{DS} = 15 \text{ V},$ $I_{D} = 15 \text{ A}, R_{G} = 3.0 \Omega$			8.0			
Rise Time	t _r				28		ns	
Turn-Off Delay Time	t _{d(OFF)}				24			
Fall Time	t _f				3.0			
DRAIN-SOURCE DIODE CHARACTERISTIC	s	1						
Forward Diode Voltage	V_{SD}	V _{GS} = 0 V,	T _J = 25°C		0.8	1.1	V	
		I _S = 10 A	T _J = 125°C		0.63			
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dIS/dt = 100 A/μs, I _S = 30 A			34			
Charge Time	t _a				17		ns	
Discharge Time	t _b				17		1	
Reverse Recovery Charge	Q _{RR}				22		nC	
• • •		1						

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width $\leq 300 \,\mu\text{s}$, duty cycle $\leq 2\%$.

^{6.} Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

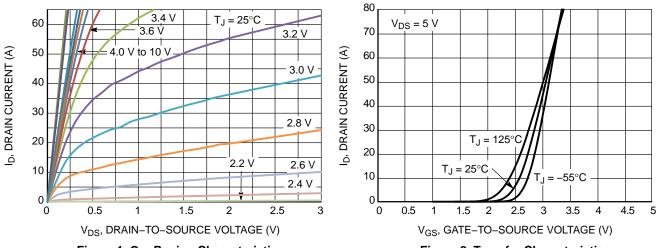


Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics

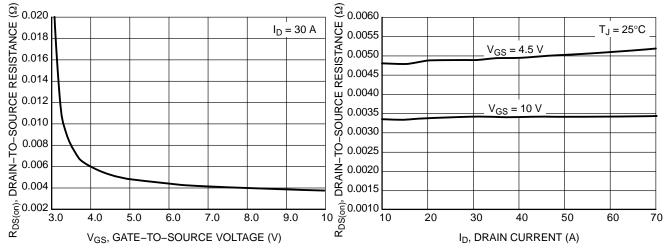


Figure 3. On-Resistance vs. V_{GS}

Figure 4. On-Resistance vs. Drain Current and Gate Voltage

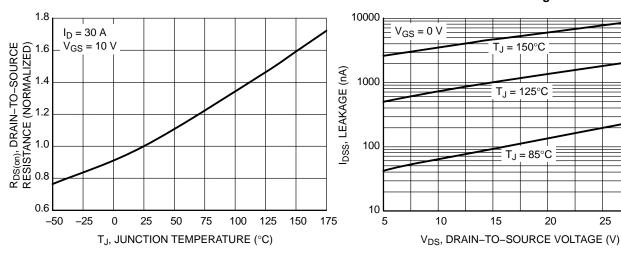


Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current vs. Voltage

30

TYPICAL CHARACTERISTICS

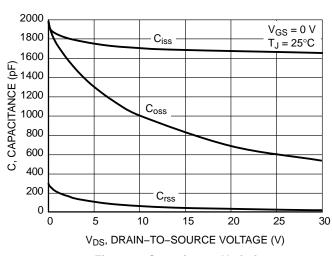


Figure 7. Capacitance Variation

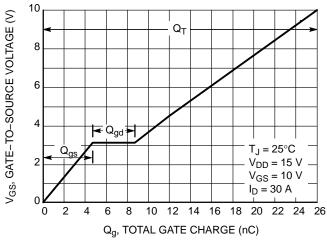


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

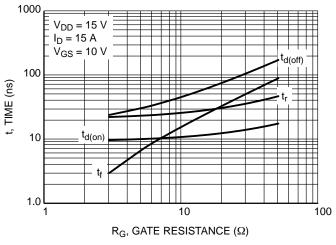


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

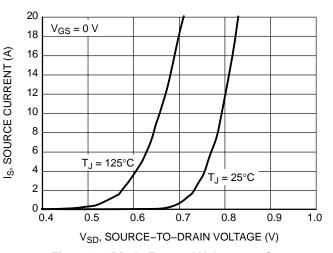


Figure 10. Diode Forward Voltage vs. Current

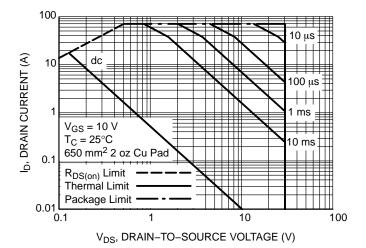


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS

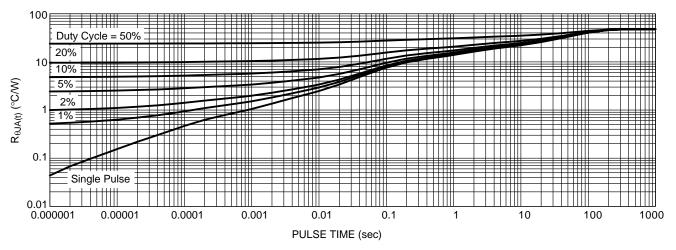


Figure 12. Thermal Response

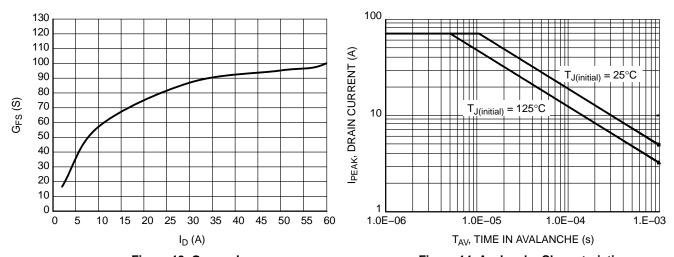


Figure 13. G_{FS} vs. I_D

Figure 14. Avalanche Characteristics

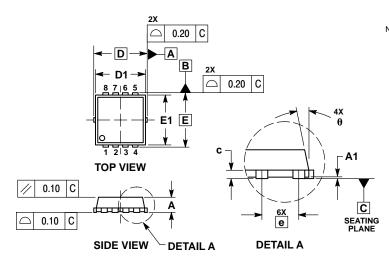
ORDERING INFORMATION

Device	Package	Shipping [†]		
NVTFS4C06NTAG	WDFN8 (Pb-Free)	1500 / Tape & Reel		
NVTFS4C06NWFTAG	WDFN8 (Pb-Free)	1500 / Tape & Reel		
NVTFS4C06NTWG	WDFN8 (Pb-Free)	5000 / Tape & Reel		
NVTFS4C06NWFTWG	WDFN8 (Pb-Free)	5000 / Tape & Reel		

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

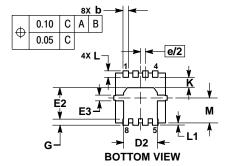
WDFN8 3.3x3.3, 0.65P CASE 511AB ISSUE D



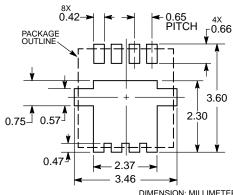
NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES			
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
Α	0.70	0.75	0.80	0.028	0.030	0.031	
A1	0.00		0.05	0.000		0.002	
b	0.23	0.30	0.40	0.009	0.012	0.016	
С	0.15	0.20	0.25	0.006	0.008	0.010	
D	3.30 BSC			0.130 BSC			
D1	2.95	3.05	3.15	0.116	0.120	0.124	
D2	1.98	2.11	2.24	0.078	0.083	0.088	
E		3.30 BSC		0.130 BSC			
E1	2.95	3.05	3.15	0.116	0.120	0.124	
E2	1.47	1.60	1.73	0.058	0.063	0.068	
E3	0.23	0.30	0.40	0.009	0.012	0.016	
е	0.65 BSC			0.026 BSC			
G	0.30	0.41	0.51	0.012	0.016	0.020	
K	0.65	0.80	0.95	0.026	0.032	0.037	
L	0.30	0.43	0.56	0.012	0.017	0.022	
L1	0.06	0.13	0.20	0.002	0.005	0.008	
M	1.40	1.50	1.60	0.055	0.059	0.063	
θ	0 °		12 °	0 °		12 °	



SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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