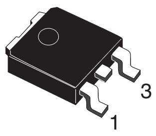
STGD6NC60HD

N-channel 600V - 7A - DPAK
Very fast PowerMESH™ IGBT

General features

Type	V_{CES}	$V_{CE(sat)}$Max @25°C	I_C @100°C
STGD6NC60HD	600V	<2.5V	7A

- Low on voltage drop (V_{cesat})
- Low C_{RES} / C_{IES} ratio (no cross-conduction susceptibility)
- Very soft ultra fast recovery antiparallel diode
- High frequency operation

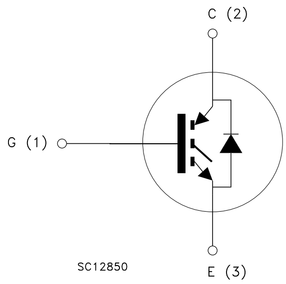


DPAK

Description

Using the latest high voltage technology based on a patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, the PowerMESH™ IGBTs, with outstanding performances. The suffix “H” identifies a family optimized for high frequency application in order to achieve very high switching performances (reduced tfall) maintaining a low voltage drop.

Internal schematic diagram



Applications

- High frequency inverters
- SMPS and PFC in both hard switch and resonant topologies
- Motor drivers

Order codes

Part number	Marking	Package	Packaging
STGD6NC60HDT4	GD6NC60HD	DPAK	Tape & reel

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage (V_{GS} = 0)	600	V
I_C (1)	Collector current (continuous) at T_C = 25°C	15	A
I_C (1)	Collector current (continuous) at T_C = 100°C	7	A
I_{CM} (2)	Collector current (pulsed)	21	A
V_{GE}	Gate-emitter voltage	±20	V
I_F	Diode RMS forward current at Tc=25°C	10	A
P_{TOT}	Total dissipation at T_C = 25°C	56	W
T_{stg}	Storage temperature	– 55 to 150	°C
T_j	Operating junction temperature		
T_l	Maximum lead temperature for soldering purpose (for 10sec. 1.6 mm from case)	300	°C

1. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{JMAX} - T_C}{R_{THJ-C} \times V_{CESAT(MAX)}(T_C, I_C)}$$

2. Pulse width limited by max junction temperature

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	2	°C/W
Rthj-amb	Thermal resistance junction-ambient max	62.5	°C/W

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	I_C= 1mA, V_{GE}= 0	600			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE}= 15V, I_C= 3A V_{GE}= 15V, I_C= 3A, Tc= 125°C		1.9 1.7	2.5	V V
$V_{GE(th)}$	Gate threshold voltage	V_{CE}= V_{GE}, I_C= 250 µA	3.75		5.75	V
I_{CES}	Collector cut-off current (V_{GE} = 0)	V_{CE}= Max rating,T_C= 25°C V_{CE}=Max rating,T_C= 125°C			10 1	µA mA
I_{GES}	Gate-emitter leakage current (V_{CE} = 0)	V_{GE}= ±20V, V_{CE}= 0			±100	nA
g_{fs}	Forward transconductance	V_{CE} = 15V, I_C= 3A		3		S

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies} C_{oes} C_{res}	Input capacitance Output capacitance Reverse transfer capacitance	V_{CE} = 25V, f = 1MHz, V_{GE} = 0		205 32 5.5		pF pF pF
Q_g Q_{ge} Q_{gc}	Total gate charge Gate-emitter charge Gate-collector charge	V_{CE} = 390V, I_C = 3A, V_{GE} = 15V, *(see Figure 17)*		13.6 3.4 5.1		nC nC nC
I_{CL}	Turn-off SOA minimum current	V_{clamp}=390V, Tj=150°C, R_G=10Ω, V_{GE}=15V		19		A

Table 5. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	V_{CC} = 390V, I_C = 3A R_G= 10Ω, V_{GE}= 15V, Tj= 25°C *(see Figure 18)*		12 5 612		ns ns A/µs
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	V_{CC} = 390V, I_C = 3A R_G= 10Ω, V_{GE}= 15V, Tj=125°C *(see Figure 18)*		13 4.3 560		ns ns A/µs
$t_r(V_{off})$ $t_d(_{off})$ t_f	Off voltage rise time Turn-off delay time Current fall time	V_{CC} = 390V, I_C = 3A, R_{GE} = 10Ω, V_{GE} = 15V,T_J=25°C *(see Figure 18)*		40 76 100		ns ns ns
$t_r(V_{off})$ $t_d(_{off})$ t_f	Off voltage rise time Turn-off delay time Current fall time	V_{CC} = 390V, I_C = 3A, R_{GE}=10Ω, V_{GE} =15V, Tj=125°C *(see Figure 18)*		60 98 124		ns ns ns

Table 6. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E_{on}(1) E_{off}(2) E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	V_{CC} = 390V, I_C = 3A R_G= 10Ω, V_{GE}=15V, Tj=25°C *(see Figure 18)*		20 68 88		µJ µJ µJ
E_{on}(1) E_{off}(2) E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	V_{CC} = 390V, I_C = 3A R_G= 10Ω, V_{GE}= 15V, Tj= 125°C *(see Figure 18)*		37 93 130		µJ µJ µJ

1. Eon is the tun-on losses when a typical diode is used in the test circuit in figure 2. If the IGBT is offered in a package with a co-pak diode, the co-pack diode is used as external diode. IGBTs & Diode are at the same temperature (25°C and 125°C)
2. Turn-off losses include also the tail of the collector current

Table 7. Collector-emitter diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_f	Forward on-voltage	I_f = 1.5A I_f = 1.5A, Tj = 125°C		1.6 1.3	2.1	V V
t_{rr} Q_{rr} I_{rrm}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_f = 3A,V_R = 40V, Tj = 25°C, di/dt = 100 A/µs *(see Figure 19)*		21 14 1.36		ns nC A
t_{rr} Q_{rr} I_{rrm}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_f = 3A,V_R = 40V, Tj =125°C, di/dt = 100A/µs *(see Figure 19)*		34 32 1.88		ns nC A

2.1 Electrical characteristics (curves)

Figure 1. Output characteristics

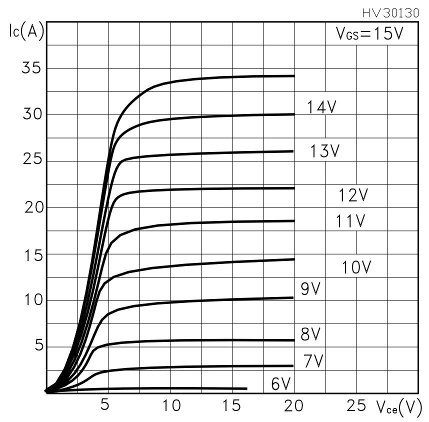


Figure 2. Transfer characteristics

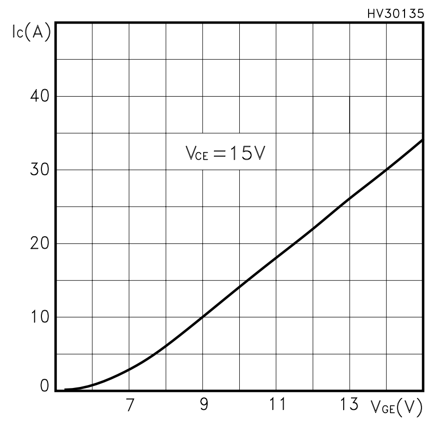


Figure 3. Transconductance

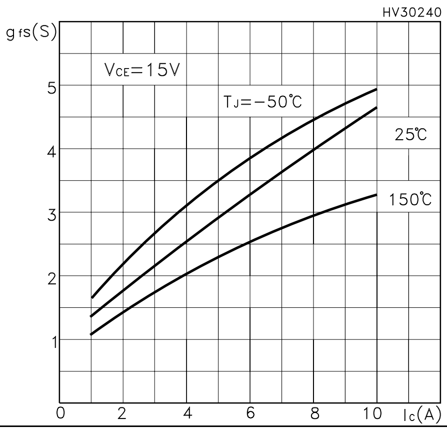


Figure 4. Collector-emitter on voltage vs temperature

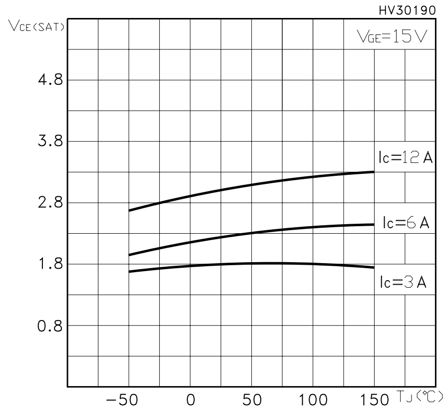


Figure 5. Gate charge vs gate-source voltage

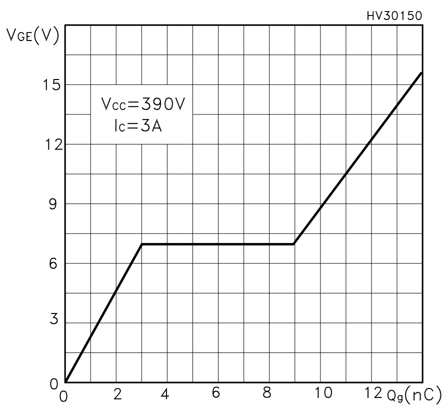


Figure 6. Capacitance variations

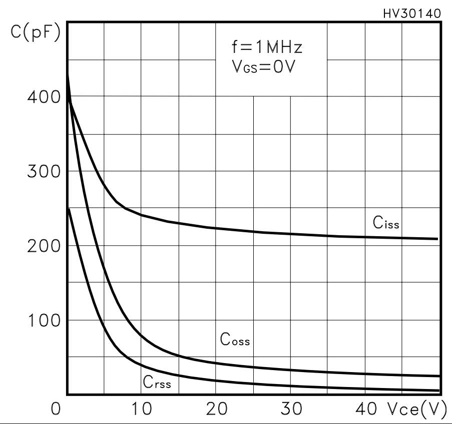


Figure 7. Normalized gate threshold voltage vs temperature

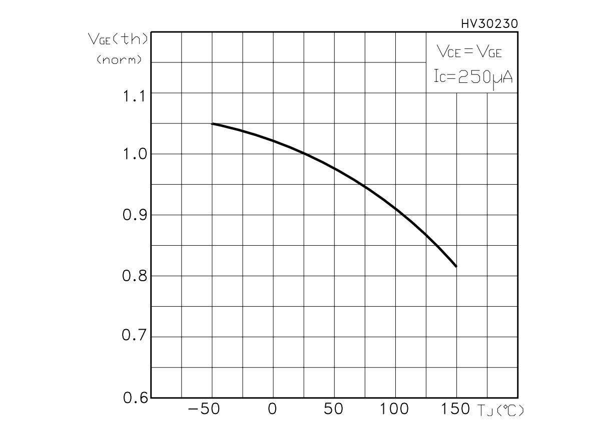


Figure 8. Collector-emitter on voltage vs collector current

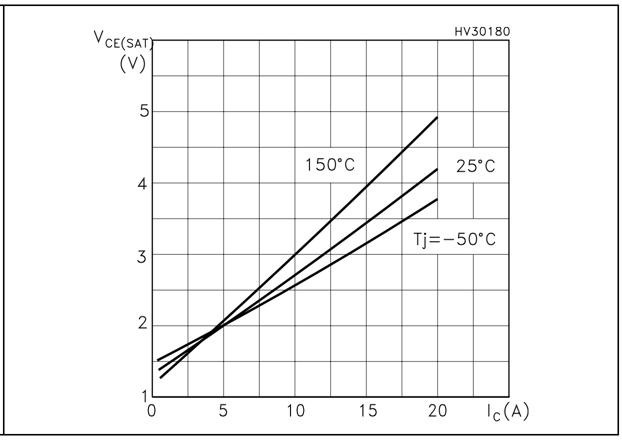


Figure 9. Normalized breakdown voltage vs temperature

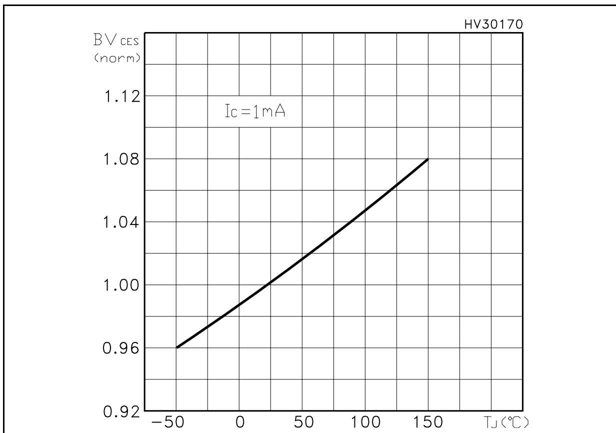


Figure 10. Switching losses vs temperature

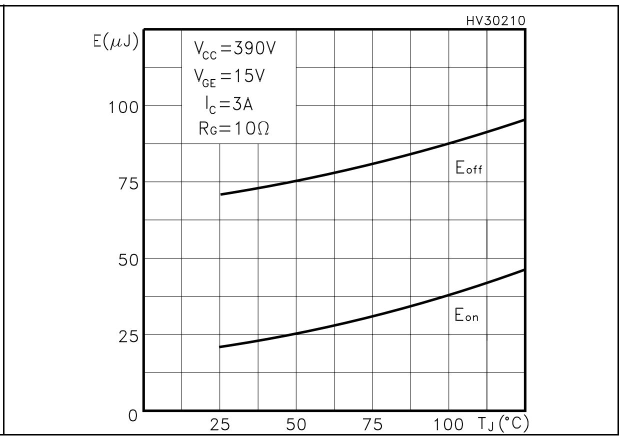


Figure 11. Switching losses vs gate resistance

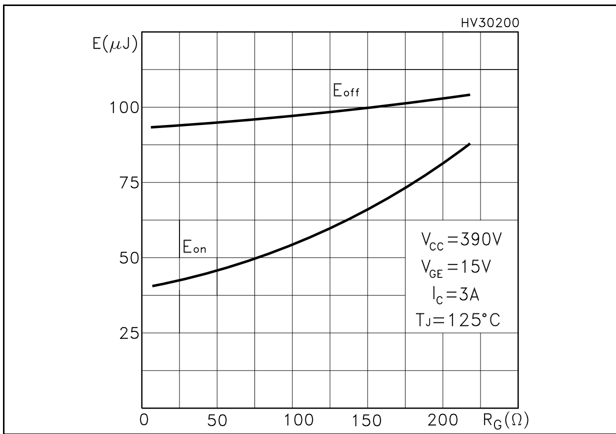


Figure 12. Switching losses vs collector current

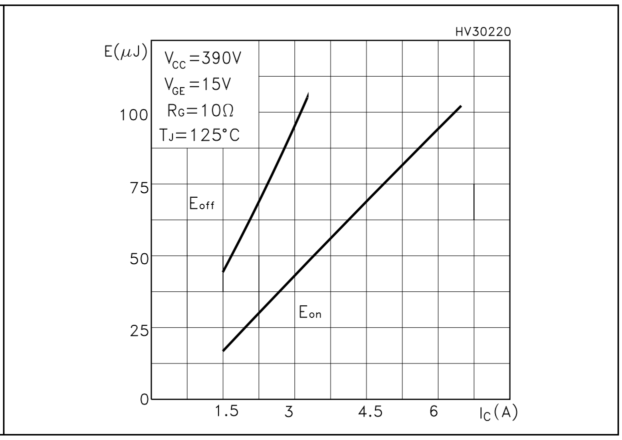


Figure 13. Thermal Impedance

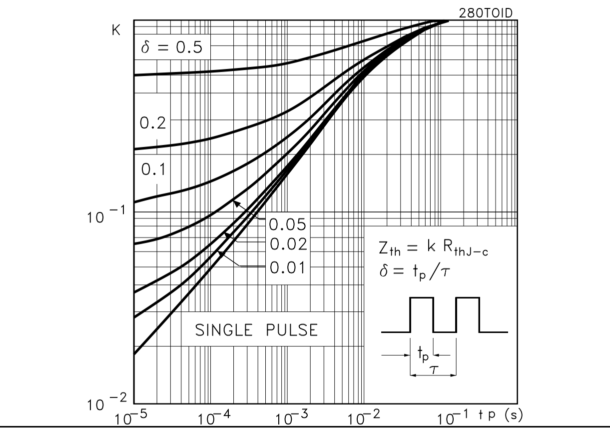


Figure 14. Turn-off SOA

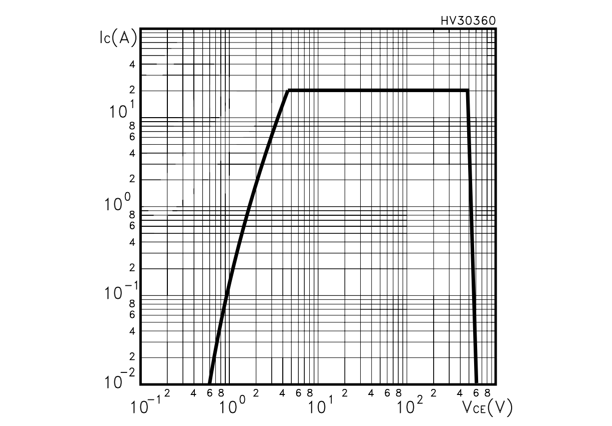
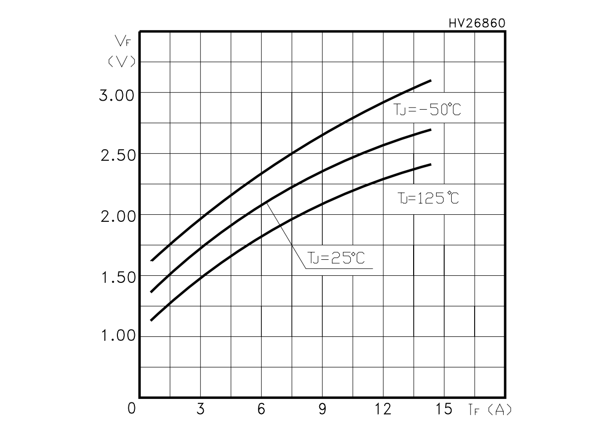


Figure 15. Emitter-collector diode characteristics



3 Test circuit

Figure 16. Test circuit for inductive load switching

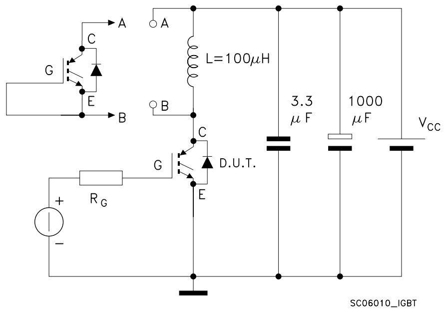


Figure 17. Gate charge test circuit

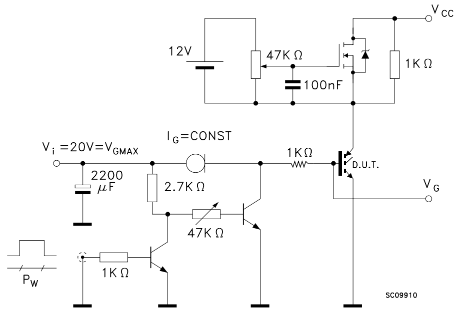


Figure 18. Switching waveform

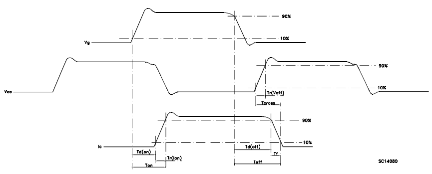
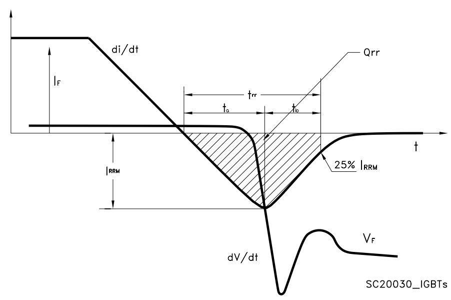


Figure 19. Diode recovery time waveform

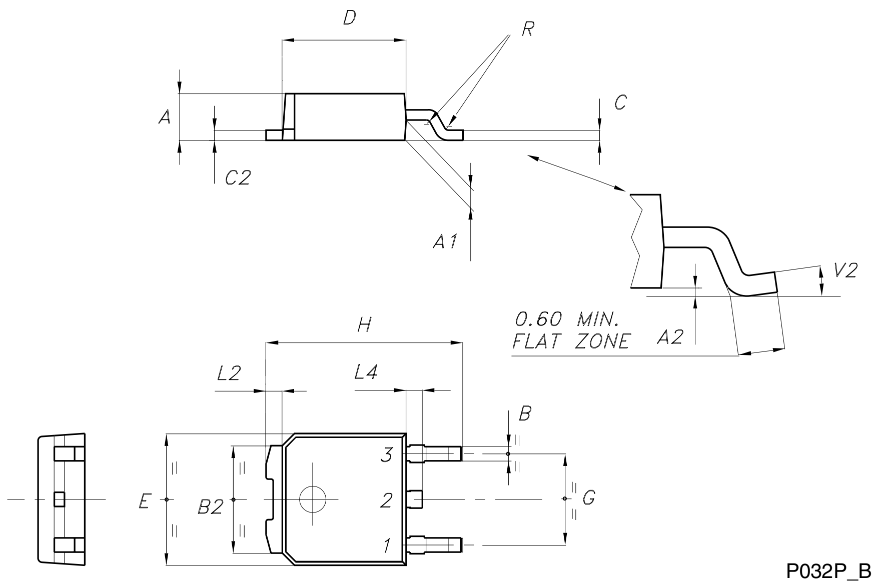


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

TO-252 (DPAK) MECHANICAL DATA

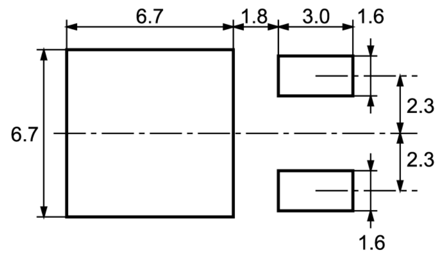
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



P032P_B

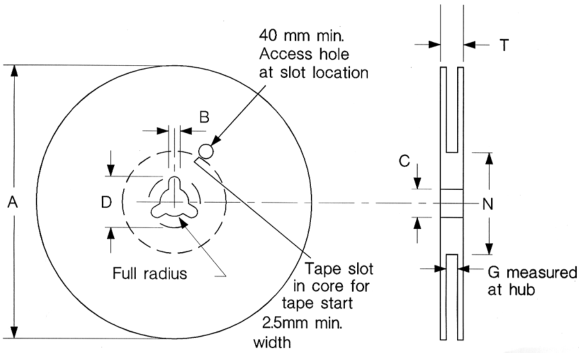
5 Packaging mechanical data

DPAK FOOTPRINT



All dimensions are in millimeters

TAPE AND REEL SHIPMENT



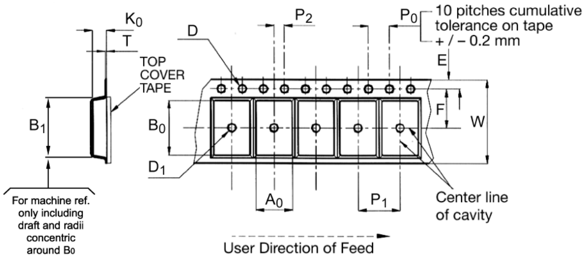
REEL MECHANICAL DATA

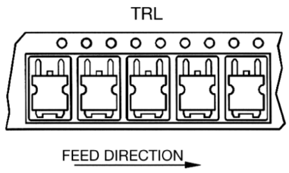
DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

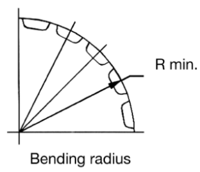
BASE QTY	BULK QTY
2500	2500

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641







6 Revision history

Table 8. Revision history

Date	Revision	Changes
04-Aug-2005	1	First release
07-Mar-2006	2	Complete version
07-Feb-2007	3	The document has been reformatted

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