



# **P-Channel NexFET™ Power MOSFET**

Check for Samples: CSD25213W10

### **FEATURES**

- Ultra Low Qg and Qgd
- Small Footprint 1mm x 1mm
- Low Profile 0.62mm Height
- Pb Free
- Gate-Source Voltage Clamp
- Gate ESD Protection
- RoHS Compliant
- Halogen Free

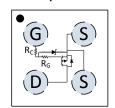
### **APPLICATIONS**

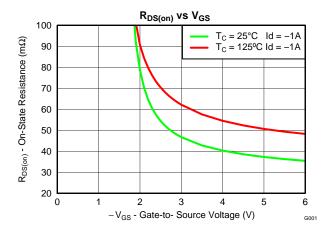
- Battery Management
- Load Switch
- Battery Protection

### **DESCRIPTION**

The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra low profile.

**Top View** 





### **PRODUCT SUMMARY**

V <sub>DS</sub>	Drain to Source Voltage	-20	V	
$Q_g$	Gate Charge Total (4.5V)	2.2	nC	
$Q_{gd}$	Gate Charge Gate to Drain	0.14	nC	
R <sub>DS(on)</sub>	Drain to Source On	$V_{GS} = -2.5V$	54	mΩ
	Resistance	V <sub>GS</sub> = -4.5V	39	mΩ
V <sub>GS(th)</sub>	Threshold Voltage	-0.85	;	V

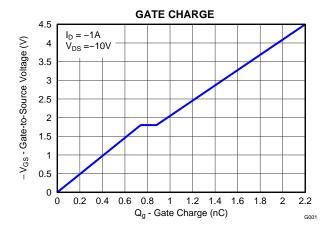
### **ORDERING INFORMATION**

Device	Package	Package Media		Ship	
CSD25213W10	1 x 1 Wafer Level Package	7-inch reel	3000	Tape and Reel	

### **ABSOLUTE MAXIMUM RATINGS**

T <sub>A</sub> = 25°C	unless otherwise stated	VALUE	UNIT
V <sub>DS</sub>	Drain to Source Voltage	-20	٧
V <sub>GS</sub>	Gate to Source Voltage	-6.0	V
I <sub>D</sub>	Continuous Drain Current, $T_A = 25^{\circ}C^{(1)}$	-1.6	Α
I <sub>DM</sub>	Pulsed Drain Current, T <sub>A</sub> = 25°C <sup>(2)</sup>	-16	Α
I <sub>G</sub>	Continuous Gate Clamp Current <sup>(3)</sup>	-5	mA
P <sub>D</sub>	Power Dissipation <sup>(1)</sup>	1	W
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 150	°C

- (1)  $R_{\theta JA} = 75^{\circ}\text{C/W}$  on  $1\text{in}^2$  Cu (2 oz.) on 0.060" thick FR4 PCB.
- (2) Pulse width ≤300µs, duty cycle ≤2%
- (3) Limited by gate resistance.





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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### **ELECTRICAL CHARACTERISTICS**

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$ 

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Static Ch	aracteristics						
BV <sub>DSS</sub>	Drain to Source Voltage	$V_{GS} = 0V, I_{D} = -250\mu A$	-20			V	
BV <sub>GSS</sub>	Gate to Source Voltage;	$V_{DS} = 0V, I_{G} = -250\mu A$	-6.0			V	
I <sub>DSS</sub>	Drain to Source Leakage Current	V <sub>GS</sub> = 0V, V <sub>DS</sub> = -10V			-1	μΑ	
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{DS} = 0V$ , $V_{GS} = -6V$			-100	nA	
V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-0.60	-0.85	-1.10	V	
D	Dunin to Course On Besistance	$V_{GS} = -2.5V, I_D = -1A$		54	67	mΩ	
R <sub>DS(on)</sub>	Drain to Source On Resistance	$V_{GS} = -4.5V, I_D = -1A$		39	47	mΩ	
9 <sub>fs</sub>	Transconductance	$V_{DS} = -10V, I_{D} = -1A$		6.2		S	
Dynamic	Characteristics						
C <sub>ISS</sub>	Input Capacitance			368	478	pF	
Coss	Output Capacitance	$V_{GS} = 0V, V_{DS} = -10V, f = 10kHz$		148	192	pF	
C <sub>RSS</sub>	Reverse Transfer Capacitance			7.8	10.1	pF	
R <sub>G</sub>	Series Gate Resistance			20		Ω	
R <sub>C</sub>	Series Clamp Resistance			5000		Ω	
Qg	Gate Charge Total (-4.5V)			2.2	2.9	nC	
Q <sub>gd</sub>	Gate Charge Gate to Drain	10)/ 1 11		0.14		nC	
Q <sub>gs</sub>	Gate Charge Gate to Source	$V_{DS} = -10V, I_{D} = -1A$		0.74		nC	
Q <sub>g(th)</sub>	Gate Charge at Vth			0.43		nC	
Q <sub>OSS</sub>	Output Charge	$V_{DS} = -10V, V_{GS} = 0V$		2.5		nC	
t <sub>d(on)</sub>	Turn On Delay Time			510		ns	
t <sub>r</sub>	Rise Time	$V_{DS} = -10V, V_{GS} = -2.5V, I_D = -1A$		520		ns	
t <sub>d(off)</sub>	Turn Off Delay Time	$R_G = 10\Omega$		1000		ns	
t <sub>f</sub>	Fall Time			970		ns	
Diode Ch	naracteristics						
V <sub>SD</sub>	Diode Forward Voltage	$I_S = -1A$ , $V_{GS} = 0V$		-0.77	-1	V	
Q <sub>rr</sub>	Reverse Recovery Charge	$V_{DS} = -10V, I_F = -1A,$ di/dt = 200A/ $\mu$ s		4.0		nC	
t <sub>rr</sub>	Reverse Recovery Time	$V_{DS} = -10V, I_F = -1A,$ di/dt = 200A/ $\mu$ s		11		ns	

### THERMAL CHARACTERISTICS

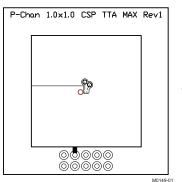
 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$ 

	PARAMETER	MIN	TYP	MAX	UNIT
D	Junction to Ambient Thermal Resistance <sup>(1)</sup>		75		°C/W
$R_{\theta JA}$	Junction to Ambient Thermal Resistance <sup>(2)</sup>		265		°C/W

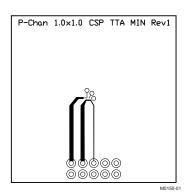
- (1) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.
   (2) Device mounted on FR4 material with minimum Cu mounting area.

Product Folder Links: CSD25213W10





Max  $R_{\theta JA} = 90^{\circ} C/W$ when mounted on 1inch<sup>2</sup> of 2 oz. Cu.



Max  $R_{\theta JA} = 333^{\circ} C/W$  when mounted on minimum pad area of 2 oz. Cu.

### TYPICAL MOSFET CHARACTERISTICS

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$ 

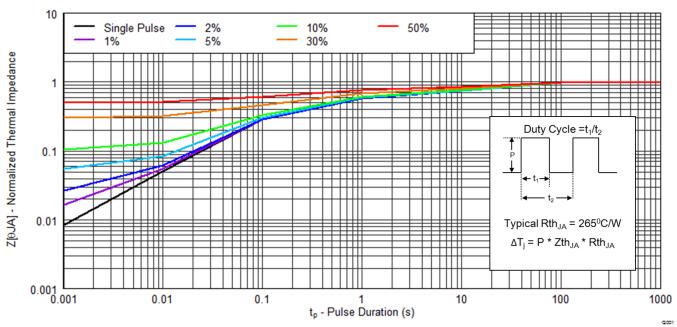


Figure 1. Transient Thermal Impedance

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1.1

-V<sub>GS(th)</sub> - Threshold Voltage (V)



# **TYPICAL MOSFET CHARACTERISTICS (continued)**

### (T<sub>A</sub> = 25°C unless otherwise stated)

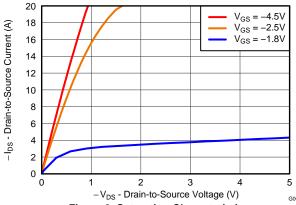
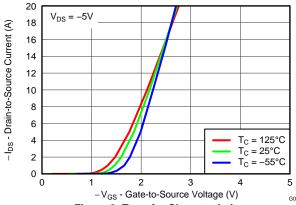
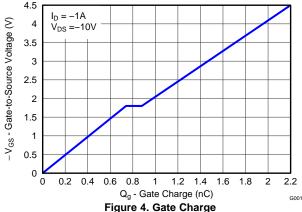


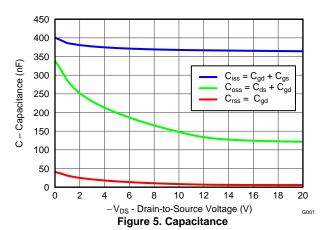
Figure 2. Saturation Characteristics



**NSTRUMENTS** 

Figure 3. Transfer Characteristics





100  $T_C = 25^{\circ}C$  Id = -1A $R_{DS(on)}$  - On-State Resistance  $(m\Omega)$ 90  $T_C = 125^{\circ}C \text{ Id} = -1A$ 80 70 60 50 40 30 20 3 -V<sub>GS</sub> - Gate-to- Source Voltage (V)

Figure 7. On-State Resistance vs. Gate-to-Source Voltage

Figure 6. Threshold Voltage vs. Temperature



### TYPICAL MOSFET CHARACTERISTICS (continued)

(T<sub>A</sub> = 25°C unless otherwise stated)

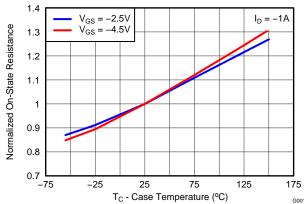


Figure 8. Normalized On-State Resistance vs. Temperature

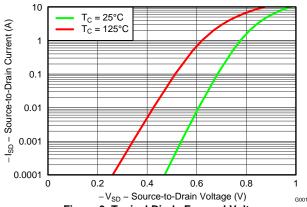


Figure 9. Typical Diode Forward Voltage

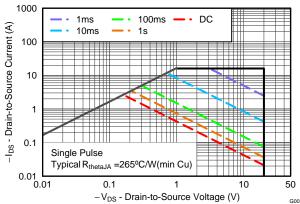


Figure 10. Maximum Safe Operating Area

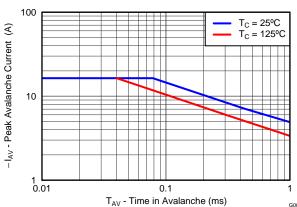


Figure 11. Single Pulse Unclamped Inductive Switching

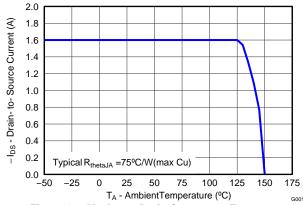


Figure 12. Maximum Drain Current vs. Temperature

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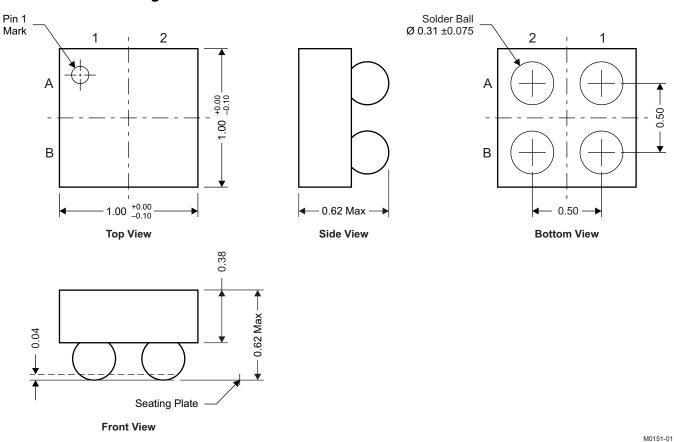
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# TEXAS INSTRUMENTS

### **MECHANICAL DATA**

# CSD25213W10 Package Dimensions

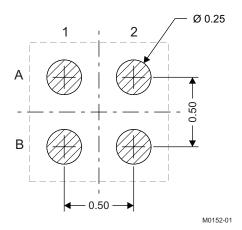


NOTE: All dimensions are in mm (unless otherwise specified)

### **Pin Configuration Table**

POSITION	DESIGNATION						
A1	Gate						
B1	Drain						
A2, B2	Source						

### **Land Pattern Recommendation**

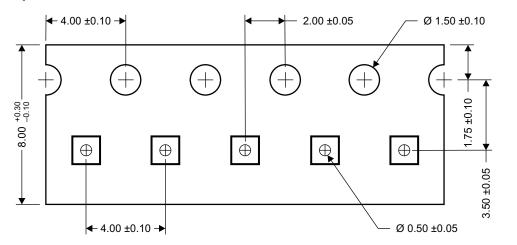


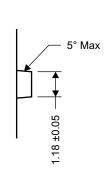
NOTE: All dimensions are in mm (unless otherwise specified)

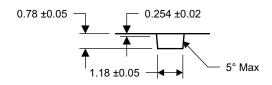
Product Folder Links: CSD25213W10



### **Tape and Reel Information**







M0153-01

- (1) All dimensions are in mm (unless otherwise specified)
- (2) Pin 1 will be oriented in the top left quadrant of the tape enclosure (closest to the carrier tape sprocket holes).



### PACKAGE OPTION ADDENDUM

17-Jul-2013

### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	_			Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples	
	(1)		Drawing		Qty	(2)		(3)		(4/5)	
CSD25213W10	ACTIVE	DSBGA	YZB	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-55 to 150	213	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

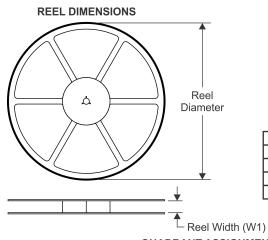
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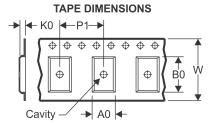
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# PACKAGE MATERIALS INFORMATION

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### TAPE AND REEL INFORMATION





A0	
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

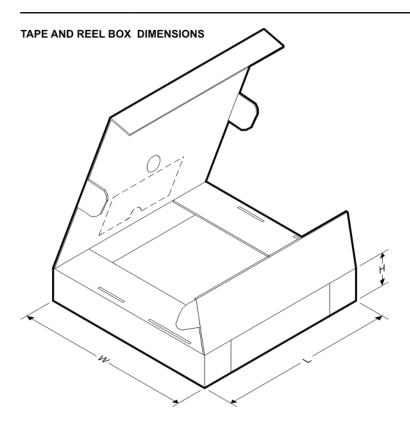
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



### \*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25213W10	DSBGA	YZB	4	3000	180.0	8.4	1.06	1.06	0.69	4.0	8.0	Q1

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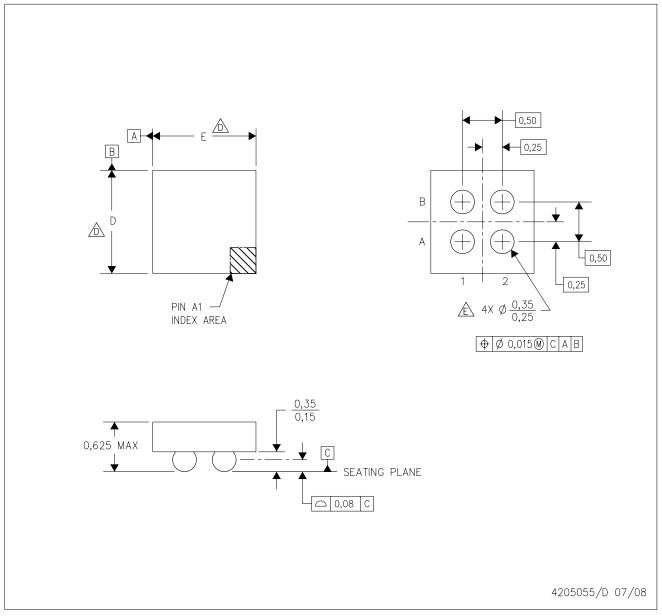


### \*All dimensions are nominal

ĺ	Device	Device Package Type		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
	CSD25213W10	DSBGA	YZB	4	3000	210.0	185.0	35.0	

# YZB (S-XBGA-N4)

### DIE-SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- Devices in YZB package can have dimension D ranging from 0.94 to 1.65 mm and dimension E ranging from 0.94 to 1.65 mm.

  To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
- E. Reference Product Data Sheet for array population. 2 x 2 matrix pattern is shown for illustration only.
- F. This package contains lead—free balls. Refer to YEB (Drawing #4204178) for tin—lead (SnPb) balls.



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