Using the HI5714 Evaluation Board

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Description

The HI5714 evaluation board was designed to easily allow a user to evaluate the performance of the HI5714 8-bit 75 MSPS Analog-to-Digital converter (ADC). The board includes clock driver circuitry, reference voltage generators, two input options and a reconstruct DAC. A block diagram of the evaluation board is shown in Figure 3.

HI5714 Theory of Operation

The HI5714 design utilizes a folding and interpolating architecture. This architecture reduces the number of comparators, reference taps, and latches in comparison to a full parallel flash converter, and as a result reduces power requirements, die size and cost. A full parallel 8-bit flash converter requires 255 comparators, 255 references and 255 latches, while the HI5714 utilizes only 16 comparators, 16 references and 16 latches.

A folding A/D converter operates basically like a 2 step subranging converter by using 2 lower resolution converters to do a course and subranged fine conversion. The major difference in the folding technique is that the folding amplifiers are used to do the fine conversion in parallel with the course conversion, where the fine and course conversions are done in a sequential mode for a conventional subranging converter. The folding architecture uses only the folding amplifiers, voltage comparators, flip-flops and decoding circuits. Sample and hold and DAC circuits are not required.

A folding amplifier is a number of parallel differential pairs with interconnected outputs as shown in Figure 1. The folding ratio is the number of differential pairs used in the amplifier, which is 16 for the HI5714. When compared to a traditional straight flash architecture, one folding amplifier with a folding ratio of 16 replaces 16 input comparators.

Assuming no interpolation were to be performed, the number of folding amplifiers necessary to implement an 8-bit conversion (using a folding ratio of 16) would be DC at 16.

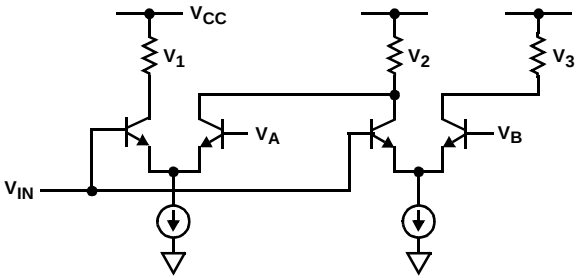

FIGURE 1. FOLDING AMPLIFIER WITH A FOLDING RATIO OF 2

Features

- HI5714 Analog to Digital Converter
- External Reference
- Two Analog Inputs: One AC Coupled, One DC Coupled
- Reconstruct DAC: HI5721
- Buffered Digital Outputs

The interpolation technique further reduces the number of necessary amplifiers by using passive elements to derive the remaining signals. Interpolation (as seen in Figure 2) takes advantage of the overlap between two adjacent amplifiers

and uses resistor taps to fill in the gaps (thereby replacing three out of every four amplifiers with resistors). Signal distortion introduced by interpolation can be ignored as only the zero crossing is of importance.

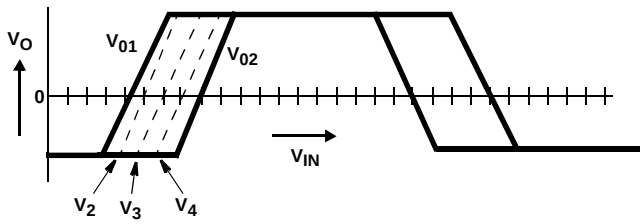

FIGURE 2. INTERPOLATED AMPLIFIER OUTPUTS

As stated earlier in this section, the HI5714 uses a folding ratio of 16 (16 latched comparators) with an interpolation ratio of 4 (4 folding amplifiers). These 16 latched comparators in turn are decoded into 32 ROM enables to provide the 5 LSBs of the converter. There are 8 subranging sections of the input voltage range which perform the coarse conversion and provide the 3 MSBs of the device.

The bias current generator is based on a simple band gap reference which provides a typical variation of 1% over the full temperature range.

The operation of the part is depicted in the timing diagram in Figure 4. There is a 1 cycle clock delay from the analog input sampling point to the corresponding digital output data.

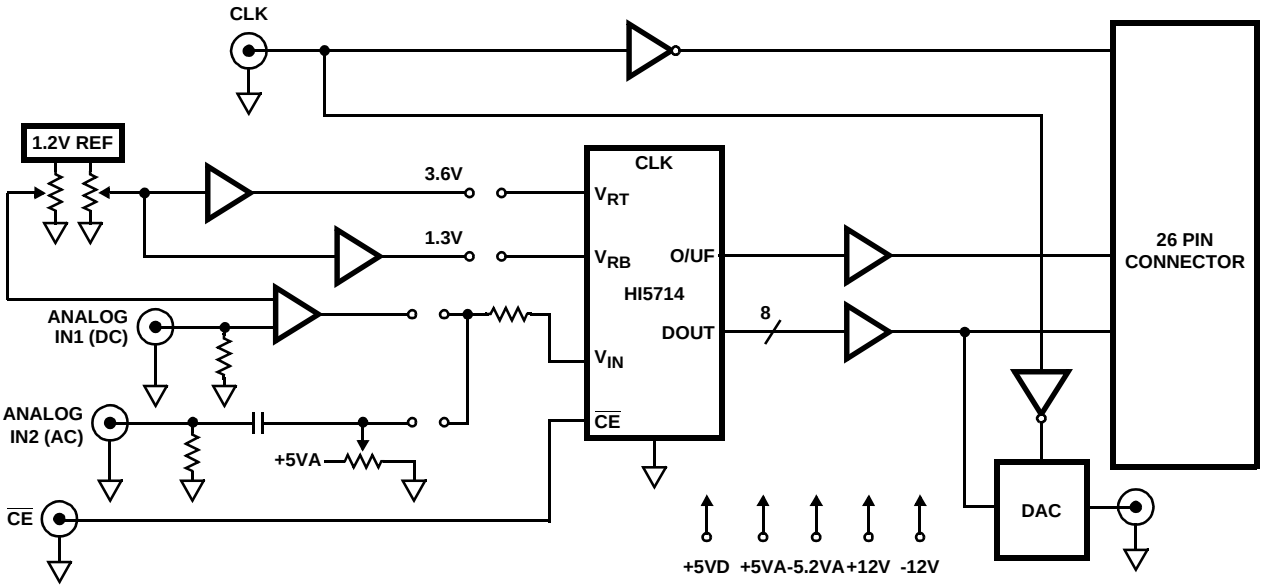

FIGURE 3. EVALUATION BOARD BLOCK DIAGRAM

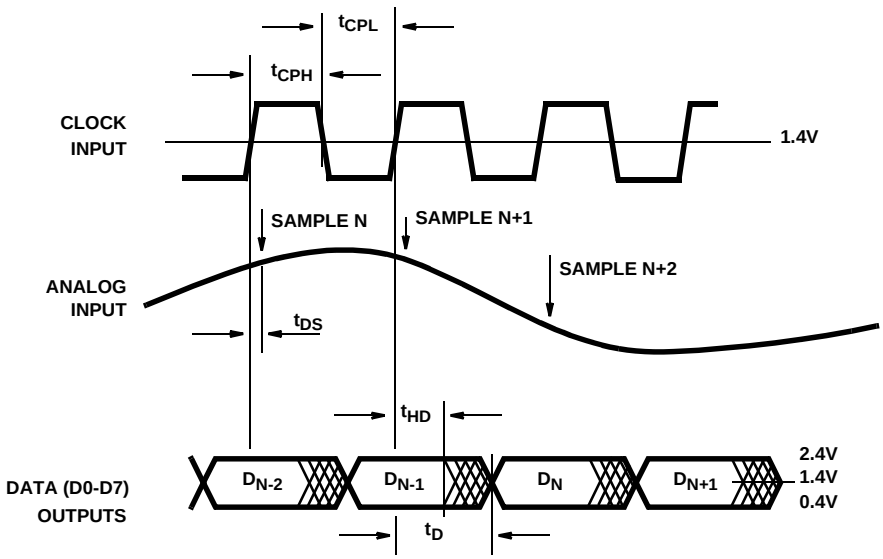

FIGURE 4. HI5714 TIMING

Power Supplies and Layout

The HI5714 Evaluation Board is a four layer board with a layout optimized for the best performance for the ADC. Figures 11 through 16 include a schematic of the board, a board layout, and the various board layers. The user should feel free to copy the layout in their application.

In order optimize the performance of the HI5714 at power up, it is necessary that AV_{DD} and DV_{DD} be driven from separate supplies. The supplies to the board should be driven by clean linear regulated supplies. AGND and DGND are tied together under the HI5714. Do not tie the supply grounds together back at the supplies as this will create a ground loop and generate additional noise.

Decoupling capacitors should be placed as close to the HI5714 as possible. A 0.1µF and a 0.001µF leaded capacitor will provide good decoupling but chip capacitors will provide better decoupling at higher clock frequencies. Do not forget a large value cap (1µF to 10µF) for low frequency decoupling somewhere on your PC board.

Table 1 lists the operating conditions for the power supplies.

TABLE 1. POWER SUPPLIES

POWER SUPPLY	MIN	TYP	MAX	CURRENT TYP
+5VA	+4.75V	+5.0V	+5.25V	25mA
-5.2VA	-5.3V	-5.2V	-5.0V	-120mA
+5VD	+4.75V	+5.0V	+5.25V	136mA
+12V	+10V	+12V	+15V	25mA
-12V	-10V	-12V	-15V	-20mA

Reference Circuit

For the following discussion, refer to the board schematic and the board layout drawing.

The HI5714 requires two reference voltages: V_{RT} and V_{RB}. The external voltage reference generator on the evaluation board is used to generate a V_{RT} of about 3.6V and a V_{RB} of about 1.3V. The ICL8069 reference diode generates a 1.2V voltage that is gained up by two op amps to the reference voltages V_{RT} and V_{RT} for the ADC. V_{RT} should be kept in the range of 3.5V to 3.9V. P1 is adjusted at the factory for a V_{RB} of 1.3V ±2mV.

Analog Input

The analog input to the HI5174 can be configured in various ways depending on the input signal and the required level of performance. A signal voltage with a maximum span of V_{RT} to V_{RB} can be AC coupled to the HI5714 through the V_{IN2} BNC and applied to the ADC by installing jumper JP2. P4 would be adjusted to center the signal in the range of the HI5714. This may or may not be adequate depending on the type of input signal.

An HA5020 buffer (as shown in Figure 5) is also provided that can be used to drive the part by inserting JP1. The gain of the circuit can be calculated from:

$$V_{OUT} = -\left(\frac{R_9}{R_7}\right)V_{IN} + \left(1 + \frac{R_9}{R_7}\right)\left(\frac{R_1}{R_1 + R_2}\right)V_{OFFSET}$$

The combination of the buffer and the external reference will give the best performance for the HI5714 and allow the most flexibility when dealing with various types of input signals. If an application is extremely cost sensitive then the internal bias generators along with the AC coupled version of the input circuit can be used.

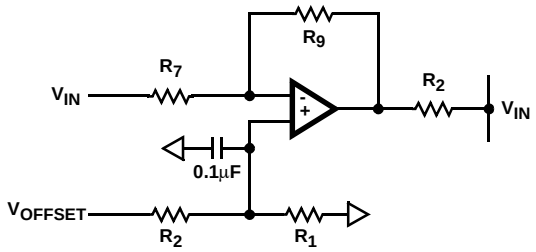

FIGURE 5. MODIFIED BUFFER

Input Clock Driver and Timing

The clock input to the HI5174 evaluation board should be driven with a standard TTL level signal. U4 (75F04) will buffer the clock input and drive the HI5714 as well as the 26 pin connector. For optimum performance of the HI5714 the duty cycle of the clock should be kept at 50% ±10%. U5 and U6 (74F541) will buffer the output bits and keep the power transients caused by charging a large bus capacitance off the supplies to the ADC.

As with any high speed ADC, clock jitter (in this case external) must be accounted for. Clock jitter will cause the converter to sample at a nonuniform rate, thus having the effect of distorting the digital representation and raise the noise floor. For this reason, users should take care to provide as uniform a clock signal as possible to assure optimal performance.

TABLE 2. TIMING SPECIFICATIONS

PARAMETER	DESCRIPTION	MIN	TYP	MAX
t_{OD}	HI5714 Data Delay	-	10ns	13ns
t_{PD1}	74F04 Prop Delay	2.4ns	-	8.5ns
t_{PD2}	74F04 Prop Delay	2.4ns	-	8.5ns
t_{PD3}	74F541 Prop Delay	2.1ns	-	7.5ns

Figure 6 shows the timing for the evaluation board. The data corresponding to a particular sample will be available at the output of the HI5714 after the required data latency (1 cycle) plus an output delay. Table 2 lists the values that can be expected for the various timing delays. Refer to the datasheet for additional timing information.

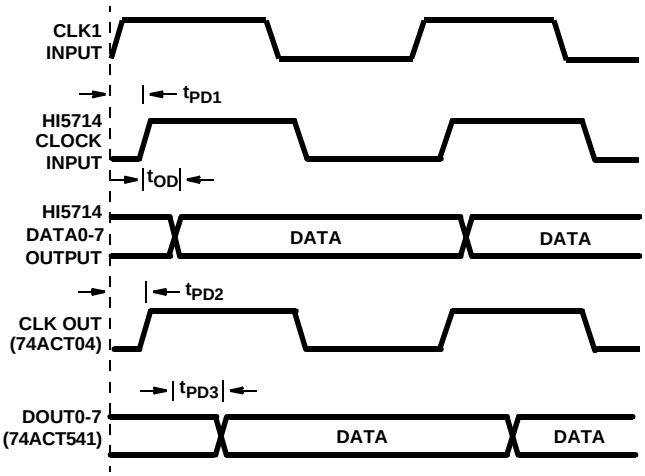

FIGURE 6. INPUT-TO-OUTPUT TIMING

DAC Setup

The HI5721 is used as a reconstruct DAC to allow the user to easily view the performance of the HI5714. The HI5721 is a TTL, 10-bit, 125MHz DAC.

The internal reference in the HI5721 is a -1.25V (typical) bandgap voltage reference with a 100µV/^{o}C temperature drift. The internal reference should be buffered by the

Control Amplifier to provide adequate drive for the segmented current cells and the R2/R resistor ladder. Reference Out (REF OUT) should be connected to the Control Amplifier Input (CTRL AMP IN). The Control Amplifier Output (CTRL AMP OUT) should be used to drive the Reference Input (REF IN) and a 0.1µF capacitor to analog V-(-AV_{EE}). This improves settling time by decoupling switching noise from the analog output of the HI5721.

The Full Scale Output Current is controlled by the CTRL AMP IN pin and the set resistor (R_{SET}). The ratio is:

I_{OUT} (Full Scale) = (CTRL AMP IN/R_{SET}) x 32

The outputs I_{OUT} and $I_{\overline{OUT}}$ are complementary current outputs. Current is steered to either I_{OUT} or $I_{\overline{OUT}}$ in proportion to the digital input code. The sum of the two currents is always equal to the full scale current minus one LSB. The current output can be converted to a voltage by using a resistor load. Both current outputs should have the same load (50Ω typically). The output voltage is:

$V_{OUT} = I_{OUT} \times R_{OUT}$

The compliance range of the outputs is from -1.5V to +3.0V.

HI5714 Characterization

Various tests can be used to characterize the performance of the HI5714. The integral nonlinearity (INL) and differential nonlinearity (DNL) specs are considered a measure of the low frequency characteristics of the ADC. These parameters are evaluated at the factory using a histogram approach with a low frequency ramp input.

A three bit reconstruction DAC, as shown in Figure 7, can be constructed to do a rough evaluation of HI5714 for DNL, missing codes, and transition noise.

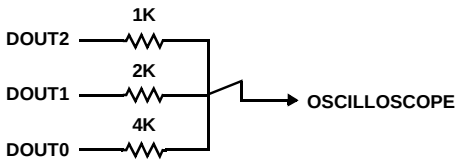

FIGURE 7. THREE BIT RECONSTRUCTION DAC

The input frequency is set so that the input will changes by 1 LSB for every k conversions of the ADC. The p-to-p voltage of the staircase is then determined by the number of LSB steps within one period of the input ramp. The following equations can be used:

$$V_{P-P} = \frac{m \times FSR}{2^n}$$

$$T = \frac{m \times k}{F_S}$$

Where:

F_S = sampling frequency of the ADC.

FSR = full scale range of the ADC.

k = desired test resolution (number of conversions per LSB).

m = desired number of steps (LSBs) per ramp period.

n = number of bits of the ADC.

For example, if k = 10, n = 8, m = 16, F_S = 20 MSPS, and FSR = 1V then the input ramp would have a V_{P-P} of 62.5mV and a period (T) of 8µs. To view the reconstructed output, connect the X axis of an oscilloscope to the ramp input and the Y axis would be connected to the reconstruction DAC output. Another oscilloscope could be used to probe the bits to verify the codes that are being tested. The analog input should be low pass filtered to remove as much noise as possible. Notice that the input ramp is only covering m steps out a possible 2^n possible for the ADC. Therefore, the generator used for this test will have to be able to offset the input through the range of the converter so all the codes for the ADC can be inspected.

Figure 8 shows what an ideal reconstructed output would look like with and without various errors. For an ideal ADC and an ideal ramp input, the digital output code will change state by 1 LSB every kth conversion for an 1 LSB change on the input. ADC errors will make the codes change before or after the kth conversion and will translate to a larger or smaller step width. The actual step width size would be compared with the ideal LSB size to determine errors. Since this is a visual comparison it will tend not to be very precise.

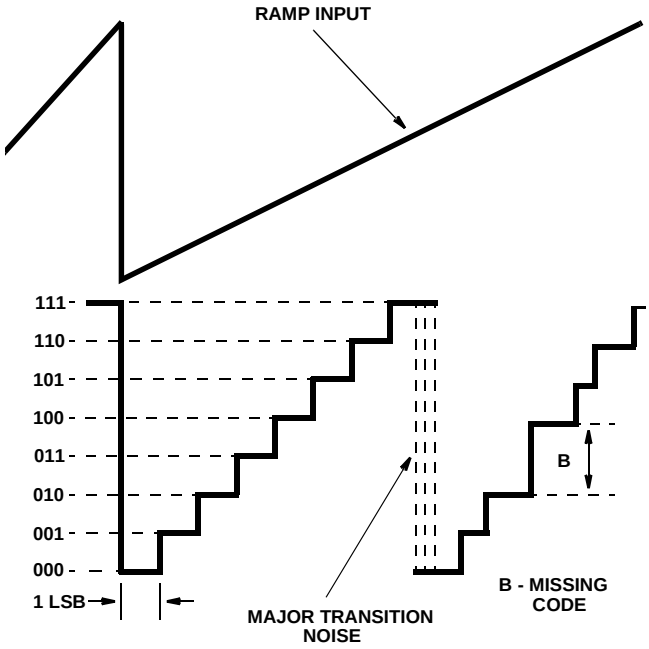

FIGURE 8. THREE BIT DAC WAVEFORMS

Further dynamic testing is used to evaluate the HI5714 performance as the input starts to approach Nyquist (F_S/2). Among these tests are Signal-to-Noise Ratio (SNR), Signal-to-Noise And Distortion (SINAD), and Total Harmonic Distortion (THD).

Coherent testing is recommended in order to avoid the inaccuracies due to windowing. Coherent sampling is governed by the following relationship: F_T/F_S = M/N. Where F_T is the frequency of the input tone, F_S is the sampling frequency, N is the number of samples, and M is the number of cycles over which the samples are taken. By making M an integer and prime (1, 3, 5. . .) the samples are assured of

being non-repetitive.

Figure 9 shows the test system used to do dynamic testing on the HI5714. The clock (CLK) and analog input (AIN) signal sources are derived from low phase noise HP8662A generators that are phase locked to each other to ensure coherence. The output of the generator that drives the analog input to the evaluation board is first passed through a bandpass filter to improve the spectral purity of the signal. The ADC data is captured by a logic analyzer and then transferred over the GPIB bus to the PC. The PC has all the software to perform the Fast Fourier (FFT) and do the required data analysis.

A 10-bit accurate DAC is used to do the bandwidth testing. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The CLK and analog input frequencies are set up so a 1kHz beat frequency is generated on the output of the DAC. Full power bandwidth is the frequency at which the amplitude of the digitally reconstructed output is 3dB down from the low frequency value.

Refer to the HI5714 datasheet for a complete list of test definitions and the results that can be expected using the evaluation board.

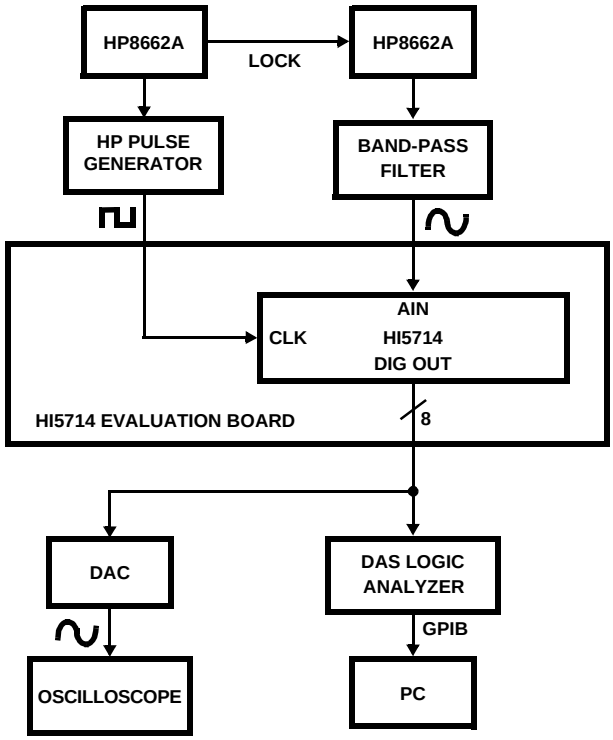

FIGURE 9. COHERENT TEST SYSTEM

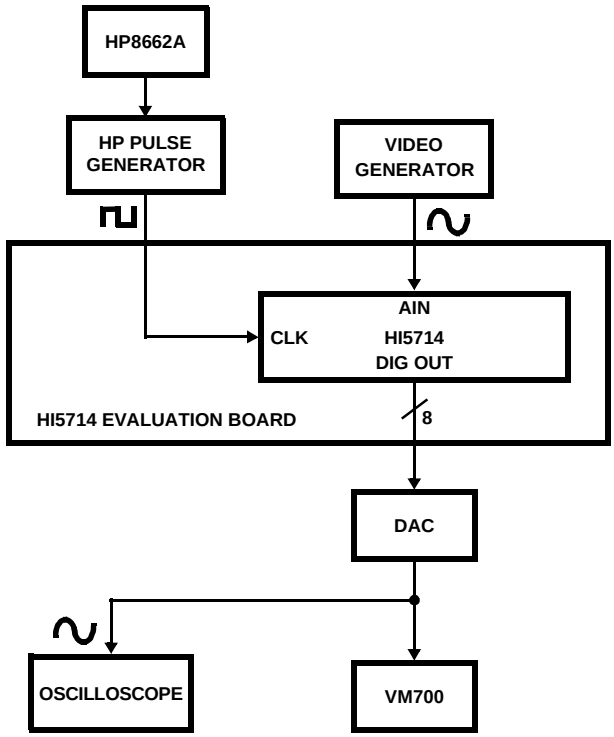

FIGURE 10. VIDEO TEST SYSTEM

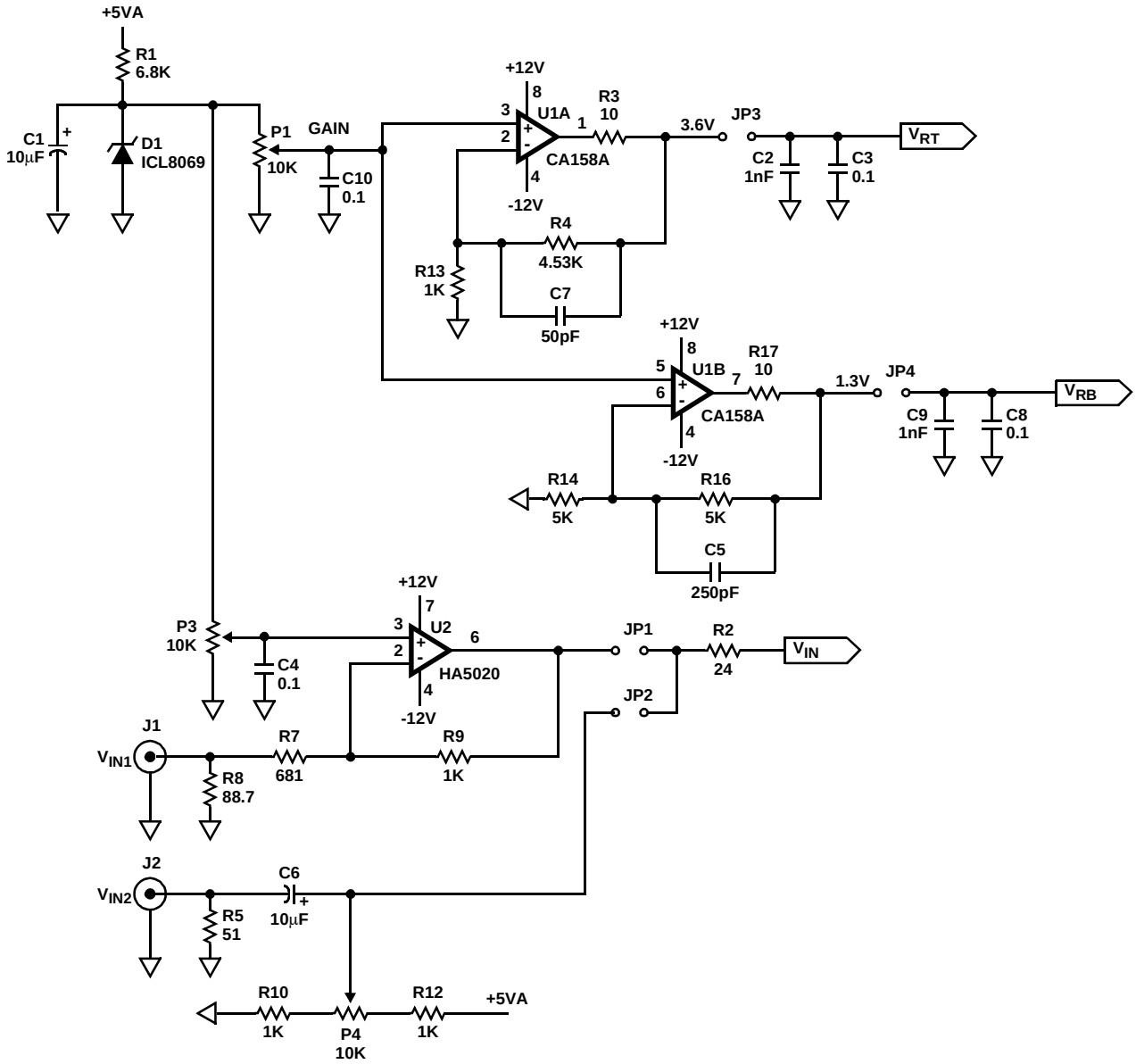

FIGURE 11A. SCHEMATIC

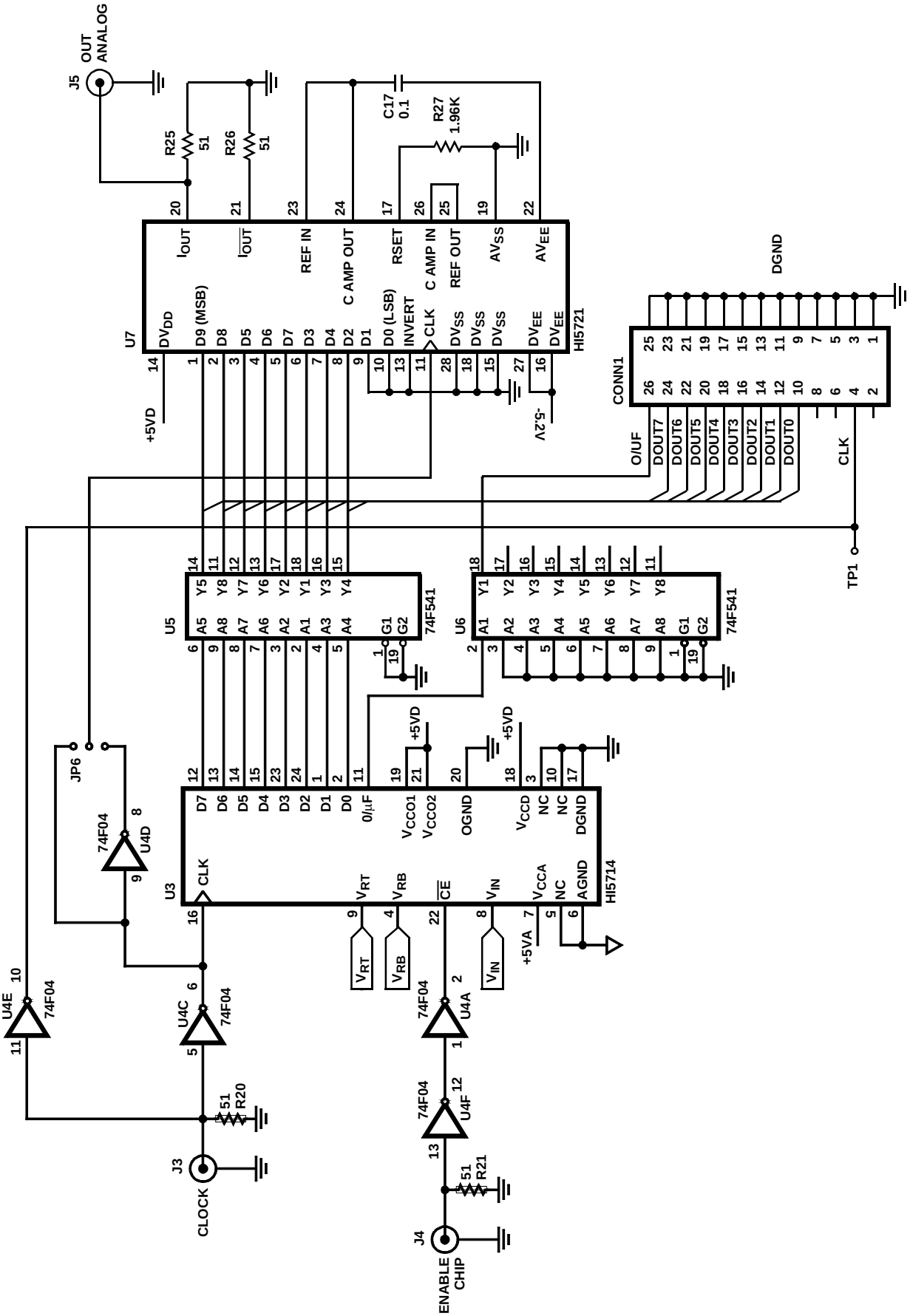

FIGURE 11B. SCHEMATIC

TABLE 3. PARTS LIST

ITEM	QUANTITY	REFERENCE DESIGNATOR	PART
1	1	CONN1	26 Pin
2	7	C1, C6, C11, C12, C13, C14, C15	10µF, Tantalum
3	4	C2, C9, C30, C31	1nF, Chip Cap
4	7	C3, C8, C17, C22, C26, C28, C29	0.1µF, Chip Cap
4a	8	C4, C10, C20, C21, C23-C25, C27	0.1µF
5	1	C5	250pF
6	1	C7	50pF
7	4	C19, C32, C33, C34	0.01F
8	1	D1	ICL8069
9	3	FB1, FB2, FB3	Ferrite Bead
10	5	JP1, JP2, JP3, JP4, JP5	2 Pin
11	1	JP6	3 Pin
12	5	J1, J2, J3, J4, J5	BNC
13	3	P1, P3, P4	10K
14	1	R1	6.8K
15	1	R2	24
16	2	R3, R17	10
17	1	R4	4.53K
18	5	R5, R20, R21, R25, R26	51
19	1	R7	681
20	1	R8	88.7
21	4	R9, R10, R12, R13	1K
22	2	R14, R16	5K
23	1	R27	1.96K
24	1	U1	CA158A
25	1	U2	HA5020
26	1	U3	HI5714
27	1	U4	74F04
28	2	U6, U5	74F541
29	1	U7	HI5721, Not Installed

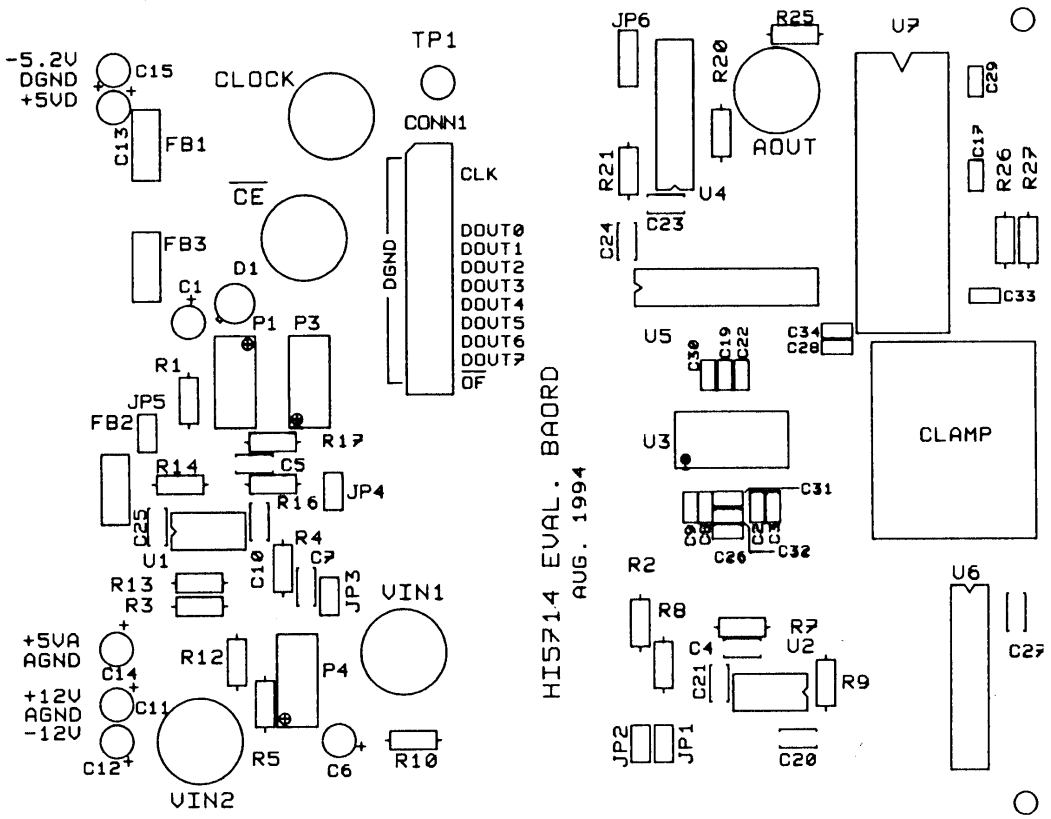

FIGURE 12. SILKSCREEN

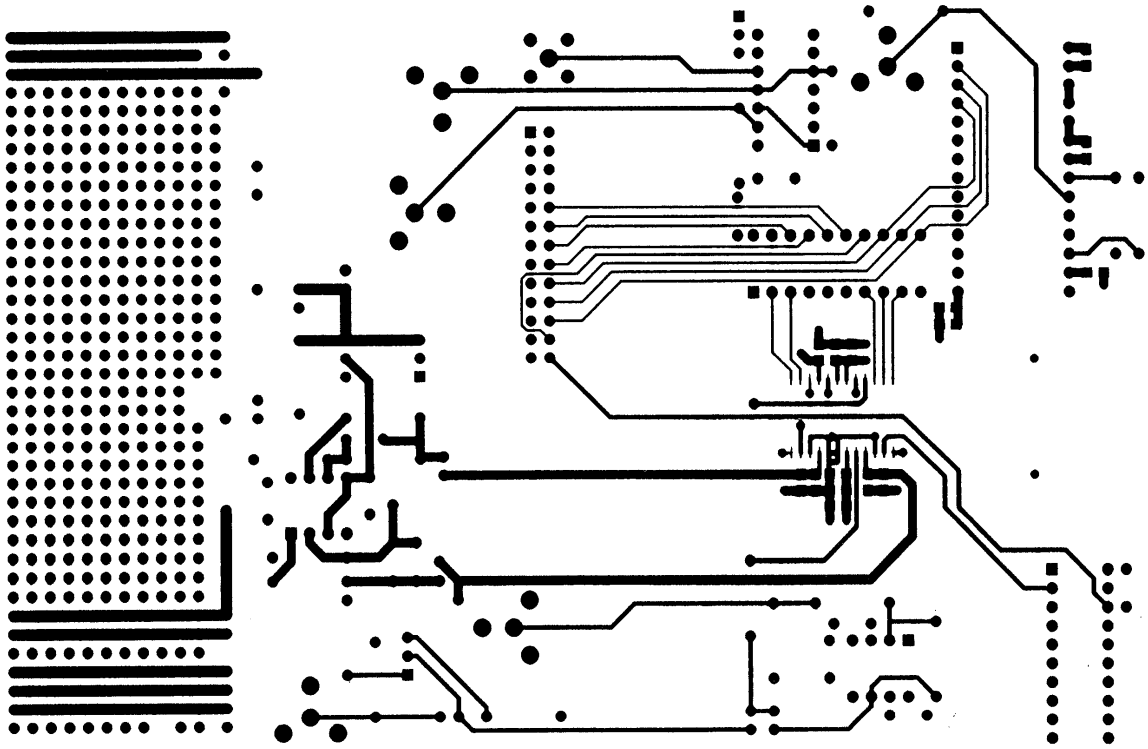

FIGURE 13. COMPONENT LAYER

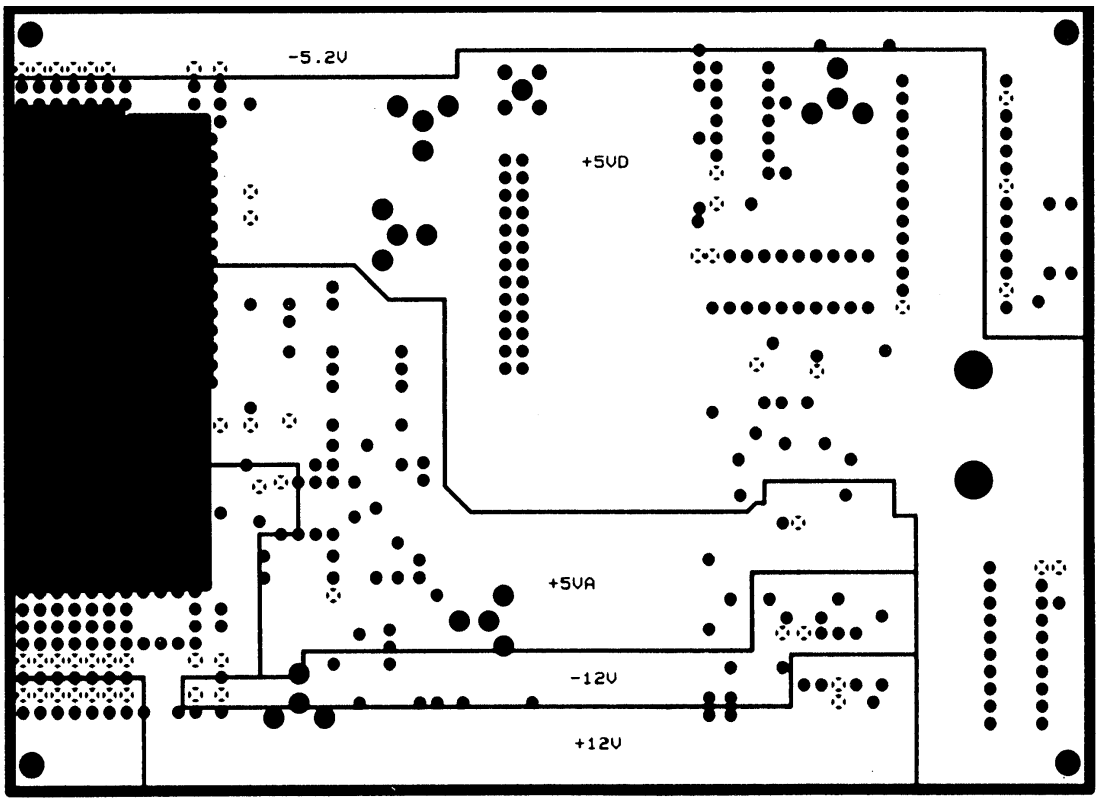

FIGURE 14. POWER LAYER

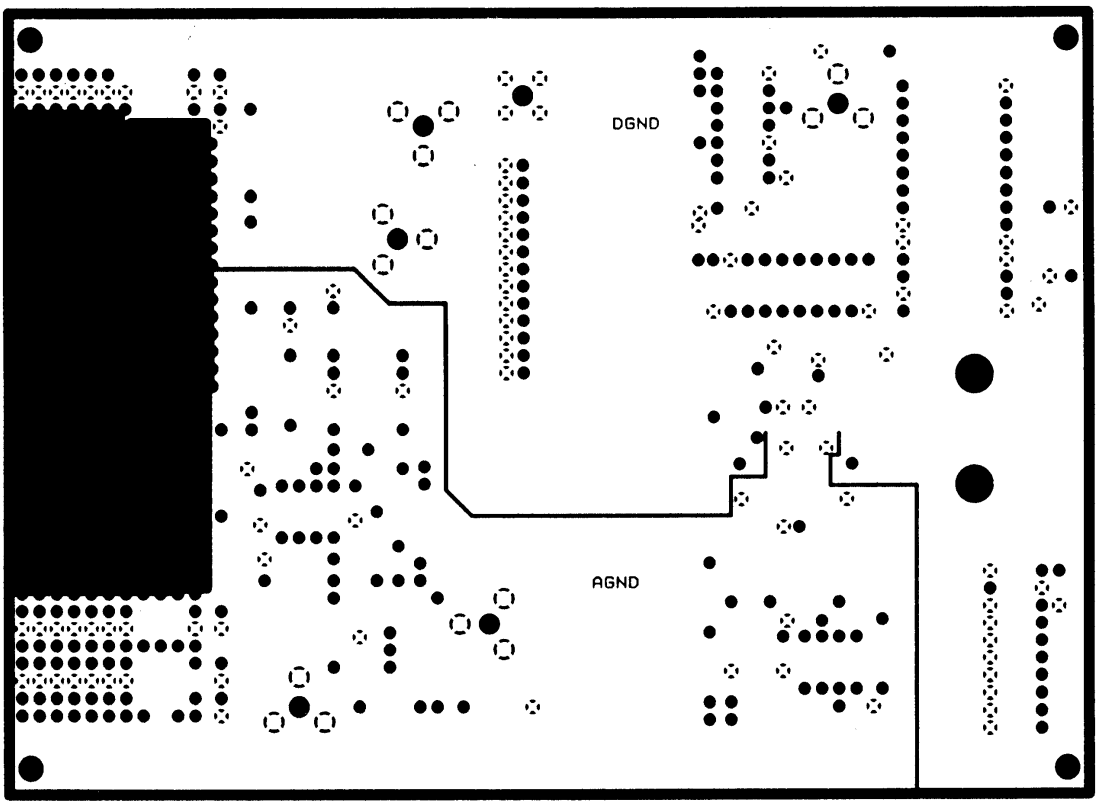

FIGURE 15. GROUND LAYER

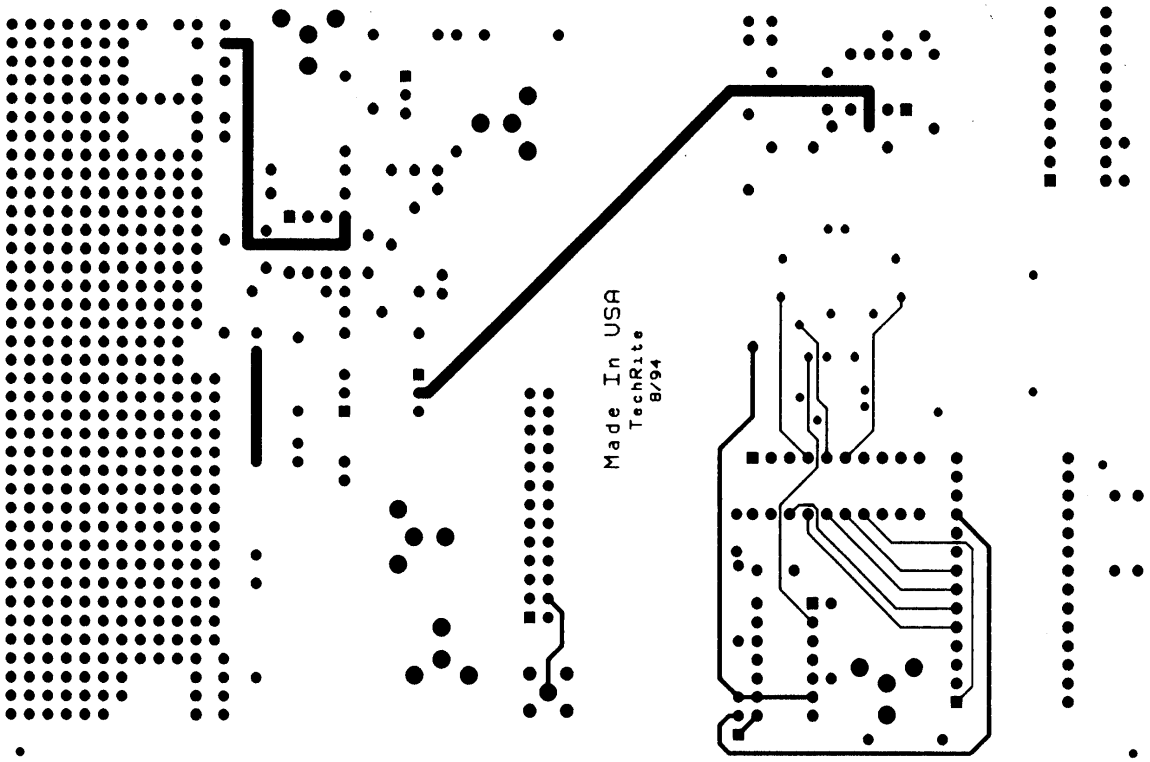

FIGURE 16. SOLDER LAYER

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