



# STB6N62K3 STD6N62K3

N-channel 620 V, 0.95  $\Omega$ , 5.5 A SuperMESH3™ Power MOSFET  
in D<sup>2</sup>PAK, DPAK

## Features

Order codes	V <sub>DSS</sub>	R <sub>DS(on) max.</sub>	I <sub>D</sub>	P <sub>w</sub>
STB6N62K3 STD6N62K3	620 V	< 1.2 $\Omega$	5.5 A	90 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

## Applications

- Switching applications

## Description

These SuperMESH3™ Power MOSFETs are the result of improvements applied to STMicroelectronics' SuperMESH™ technology, combined with a new optimized vertical structure. These devices boast an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering them suitable for the most demanding applications.

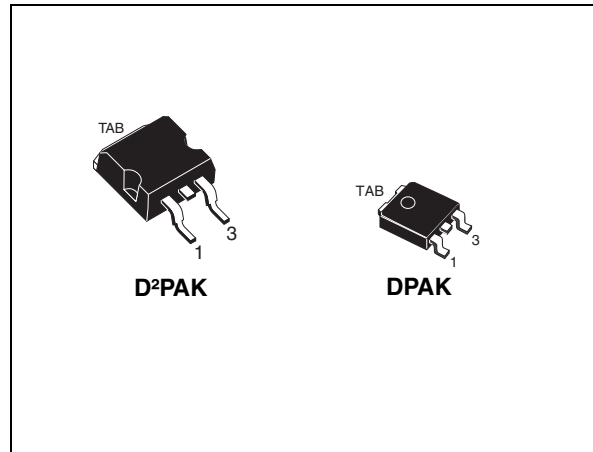


Figure 1. Internal schematic diagram

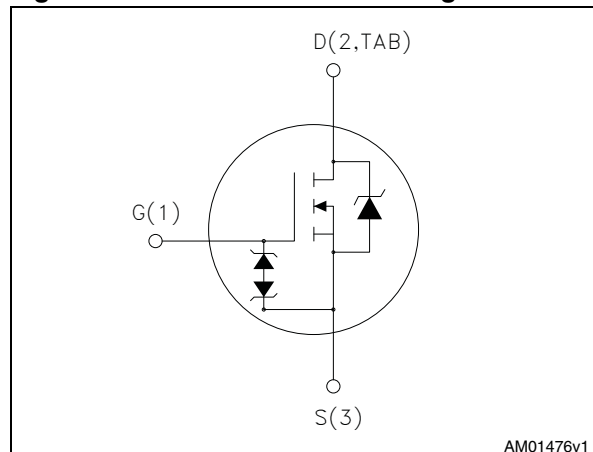


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB6N62K3 STD6N62K3	6N62K3	D <sup>2</sup> PAK DPAK	Tape and reel

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		D <sup>2</sup> PAK	DPAK	
$V_{DS}$	Drain-source voltage	620		V
$V_{GS}$	Gate- source voltage	± 30		V
$I_D$	Drain current (continuous) at $T_C = 25\text{ °C}$	5.5		A
$I_D$	Drain current (continuous) at $T_C = 100\text{ °C}$	3		A
$I_{DM}^{(1)}$	Drain current (pulsed)	22		A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ °C}$	90		W
$I_{AR}^{(2)}$	Avalanche current, repetitive or not-repetitive	5.5		A
$E_{AS}^{(3)}$	Single pulse avalanche energy	140		mJ
ESD	Gate-source human body model ( $R=1.5\text{ k}\Omega$ , $C=100\text{ pF}$ )	2.5		kV
$dv/dt^{(4)}$	Peak diode recovery voltage slope	12		V/ns
$T_{stg}$	Storage temperature	-55 to 150		°C
$T_j$	Max. operating junction temperature	150		°C

1. Pulse width limited by safe operating area.
2. Pulse width limited by  $T_j$  max.
3. Starting  $T_j = 25\text{ °C}$ ,  $I_D = I_{AR}$ ,  $V_{DD} = 50\text{ V}$ .
4.  $I_{SD} \leq 5.5\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ .

**Table 3. Thermal data**

Symbol	Parameter	D <sup>2</sup> PAK	DPAK	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	1.39		°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max.	30	50	°C/W

1. When mounted on 1inch<sup>2</sup> FR-4 board, 2 oz Cu.

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	620			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 620\text{ V}$ $V_{DS} = 620\text{ V}$ , $T_C = 125\text{ °C}$			0.8 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 9$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 2.8\text{ A}$		0.95	1.2	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	875	-	pF
$C_{oss}$	Output capacitance			100		pF
$C_{rss}$	Reverse transfer capacitance			17		pF
$C_{oss(er)}^{(1)}$	Equivalent output capacitance energy related	$V_{GS} = 0$ , $V_{DS} = 0\text{ to }480\text{ V}$	-	28	-	pF
$C_{oss(tr)}^{(2)}$	Equivalent output capacitance time related			63		pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	3.5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 496\text{ V}$ , $I_D = 5.5\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 18</a> )	-	34	-	nC
$Q_{gs}$	Gate-source charge			4		nC
$Q_{gd}$	Gate-drain charge			22		nC

1. Is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

2. Is defined as a constant equivalent capacitance giving the same storage energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 310\text{ V}$ , $I_D = 2.75\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 17</a> )		22		ns	
$t_r$	Rise time			12		ns	
$t_{d(off)}$	Turn-off-delay time				49		ns
$t_f$	Fall time				20		ns
				-		-	

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				5.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		27	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 5.5\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 5.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see <a href="#">Figure 22</a> )		290		ns
$Q_{rr}$	Reverse recovery charge			1900		nC
$I_{RRM}$	Reverse recovery current			13.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 5.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 22</a> )		335		ns
$Q_{rr}$	Reverse recovery charge			2400		nC
$I_{RRM}$	Reverse recovery current			14.5		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Table 8. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage ( $I_D = 0$ )	$I_{GS} = \pm 1\text{ mA}$	30		-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D<sup>2</sup>PAK

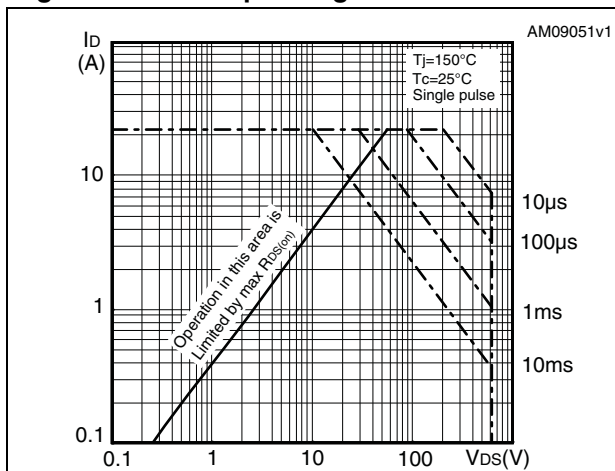


Figure 3. Thermal impedance for D<sup>2</sup>PAK

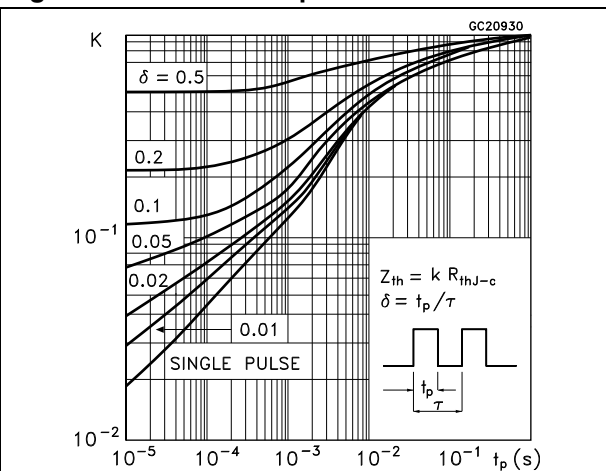


Figure 4. Safe operating area for DPAK

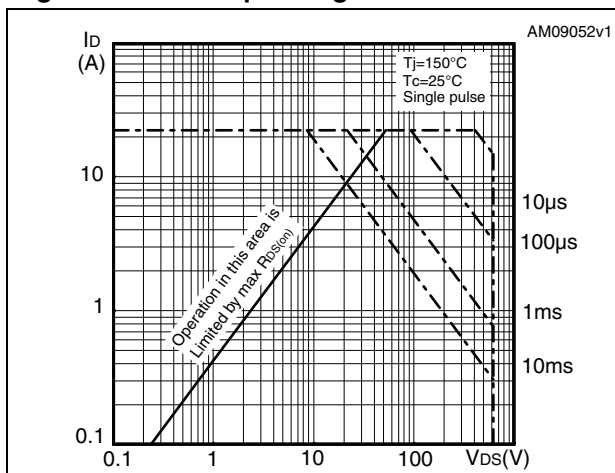


Figure 5. Thermal impedance for DPAK

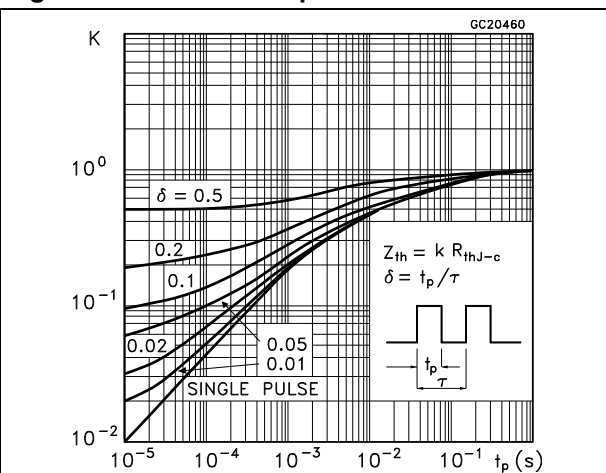


Figure 6. Output characteristics

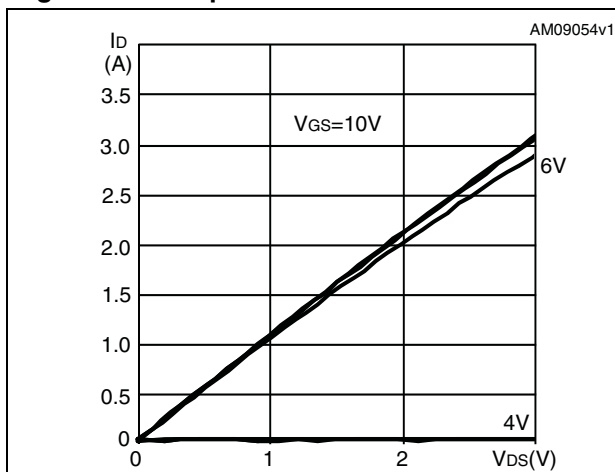
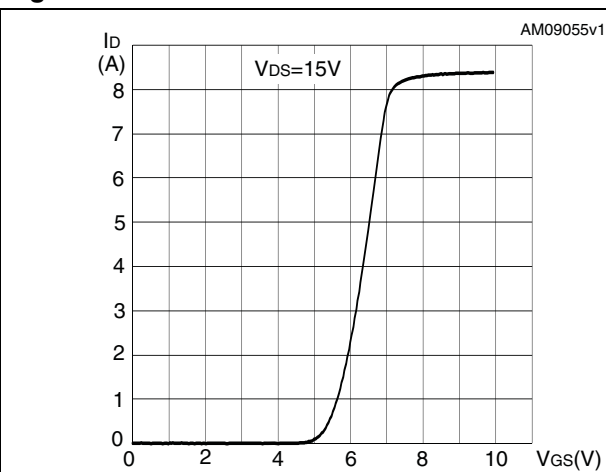
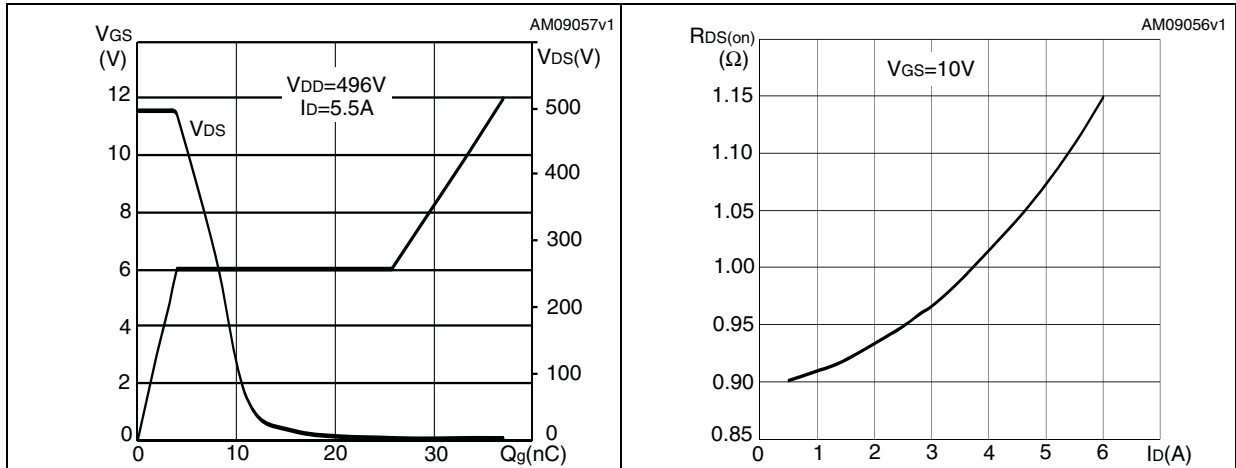


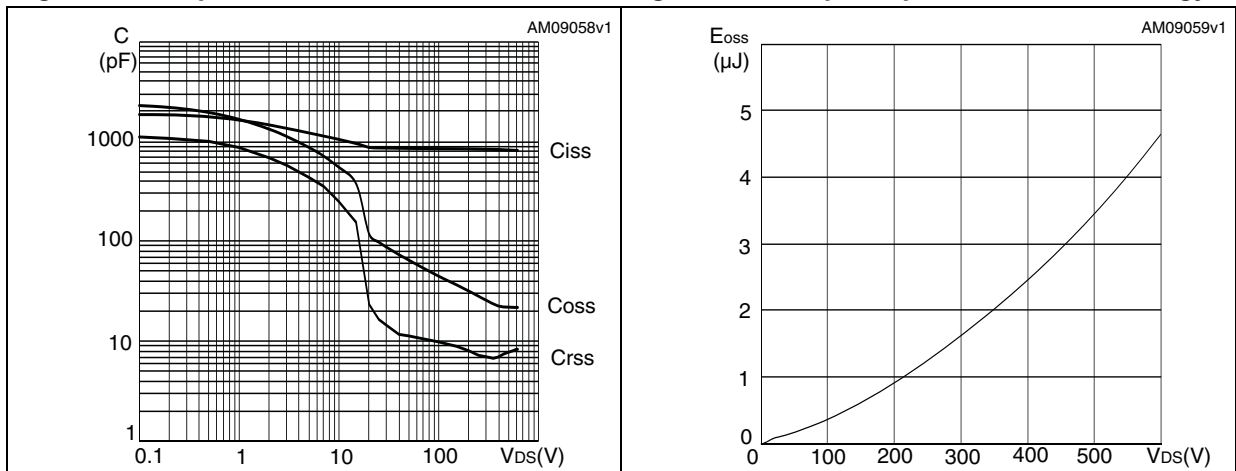
Figure 7. Transfer characteristics



**Figure 8. Gate charge vs gate-source voltage** **Figure 9. Static drain-source on resistance**



**Figure 10. Capacitance variations** **Figure 11. Output capacitance stored energy**



**Figure 12. Normalized gate threshold voltage vs temperature** **Figure 13. Normalized on resistance vs temperature**

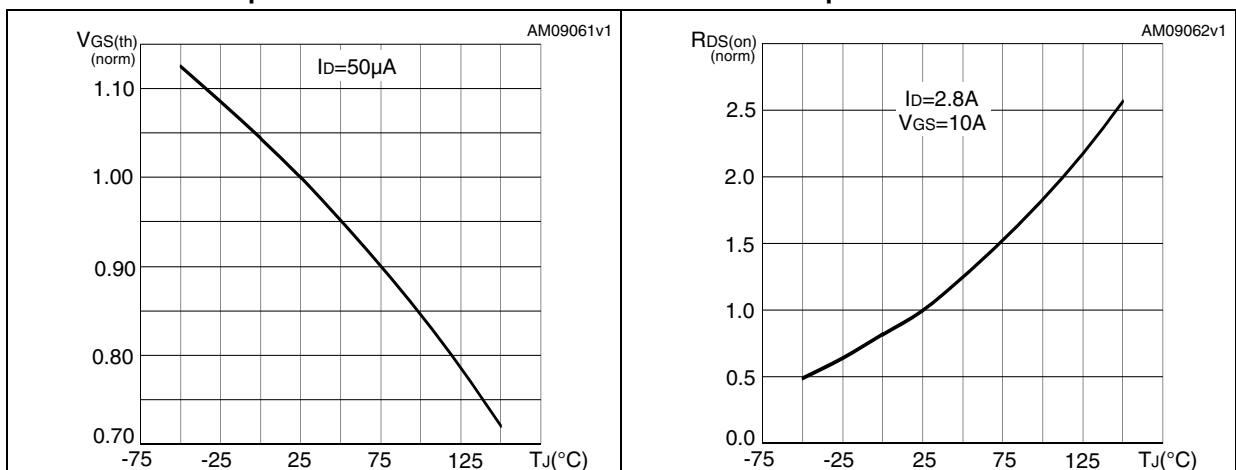


Figure 14. Normalized  $B_{VDSS}$  vs temperature

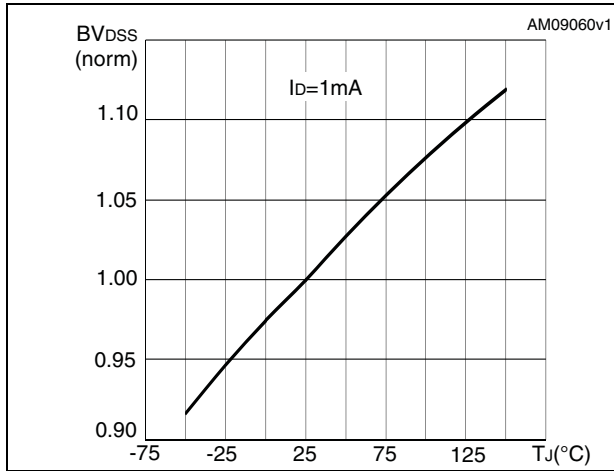


Figure 15. Source-drain diode forward characteristics

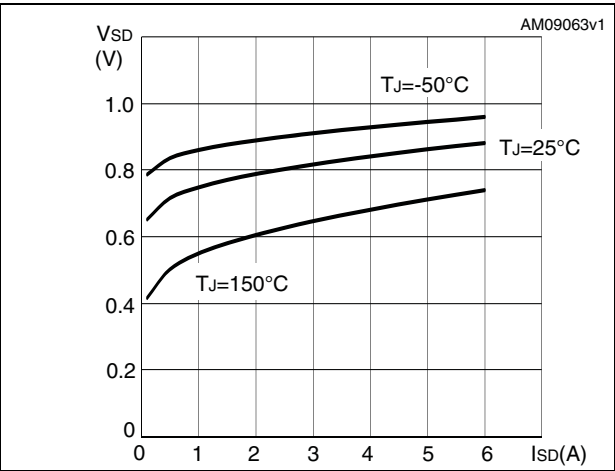
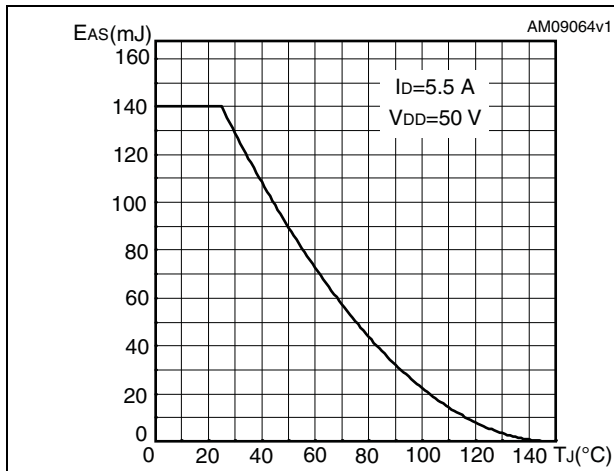
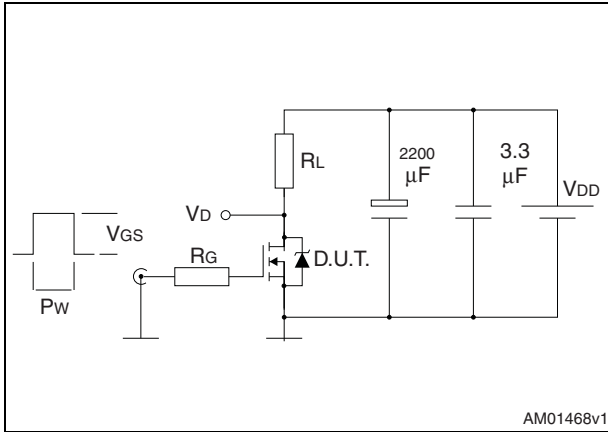


Figure 16. Maximum avalanche energy vs temperature



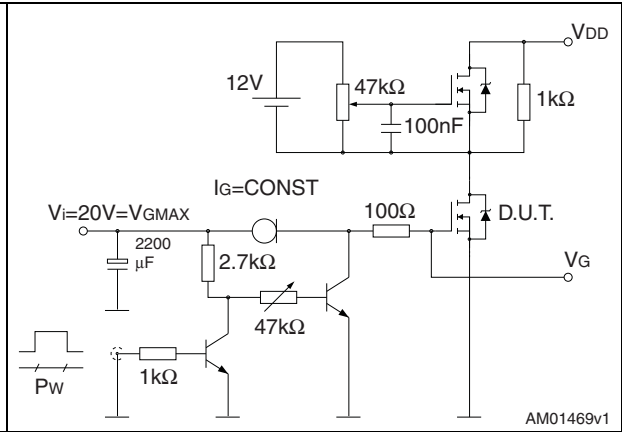
### 3 Test circuits

**Figure 17. Switching times test circuit for resistive load**



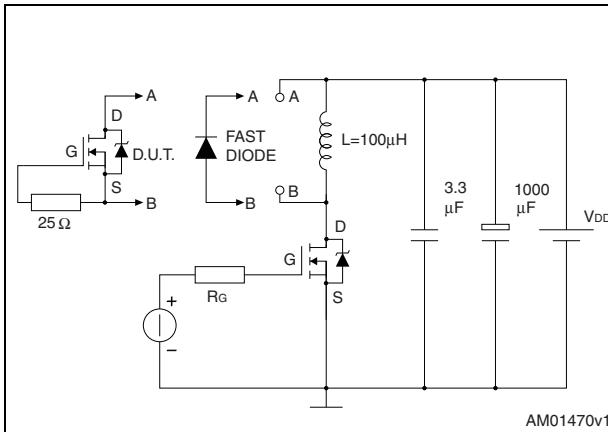
AM01468v1

**Figure 18. Gate charge test circuit**



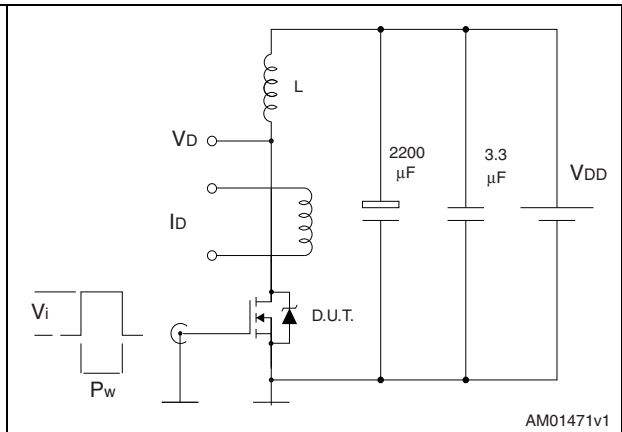
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**Figure 19. Test circuit for inductive load switching and diode recovery times**



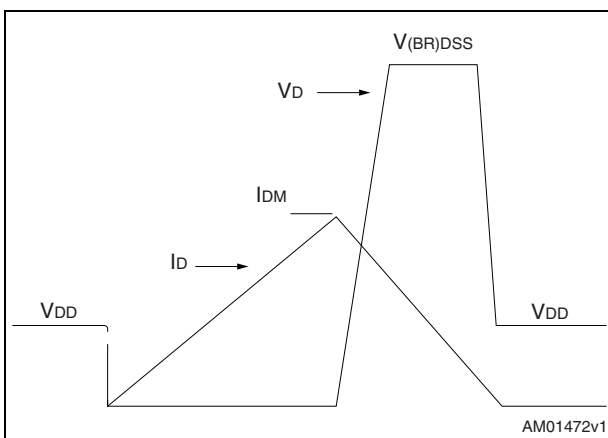
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**Figure 20. Unclamped Inductive load test circuit**



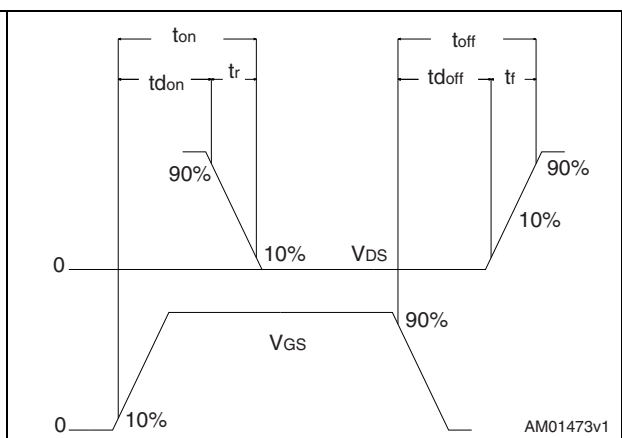
AM01471v1

**Figure 21. Unclamped inductive waveform**



AM01472v1

**Figure 22. Switching time waveform**



AM01473v1

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 9. D<sup>2</sup>PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 23. D<sup>2</sup>PAK (TO-263) drawing

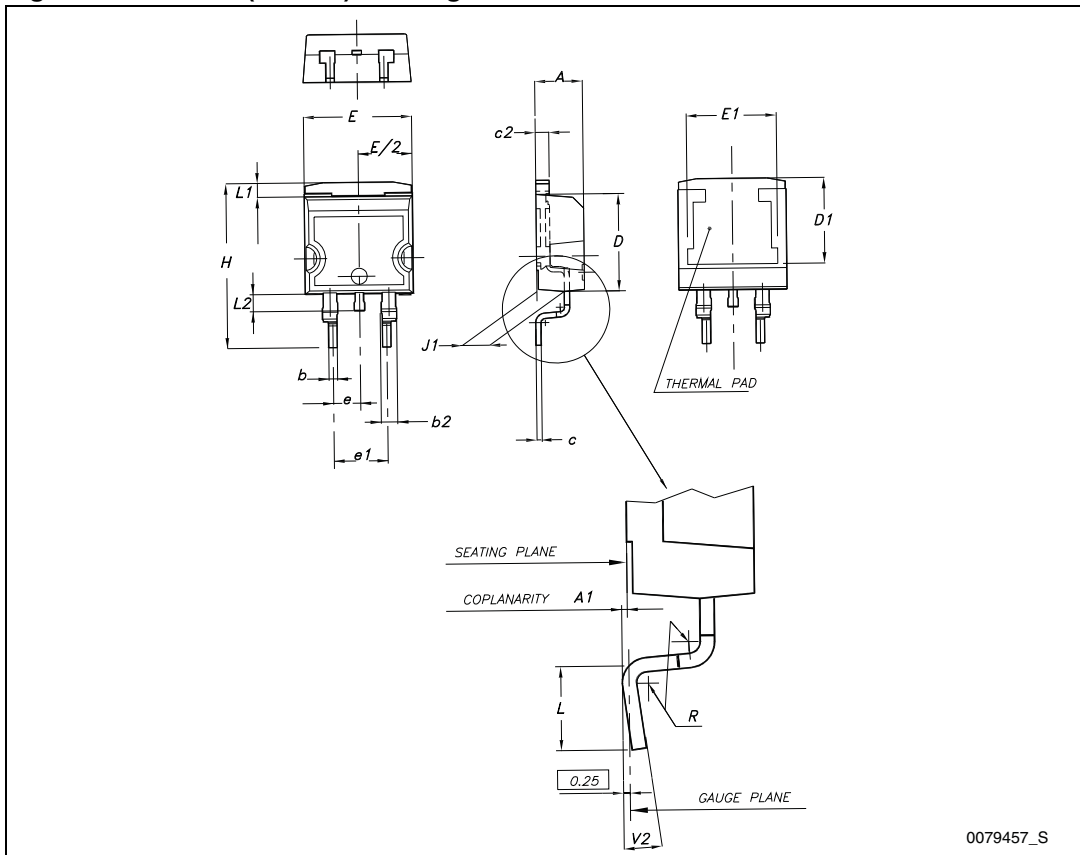
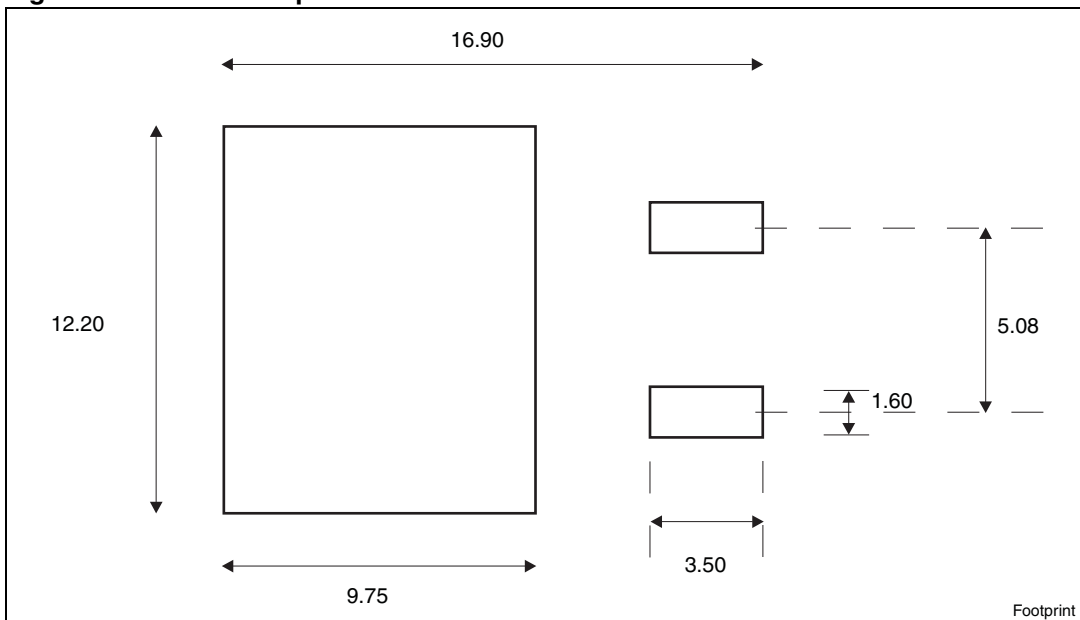


Figure 24. D<sup>2</sup>PAK footprint<sup>(a)</sup>



a. All dimensions are in millimeters

Table 10. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		1.50
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 25. DPAK (TO-252) drawing

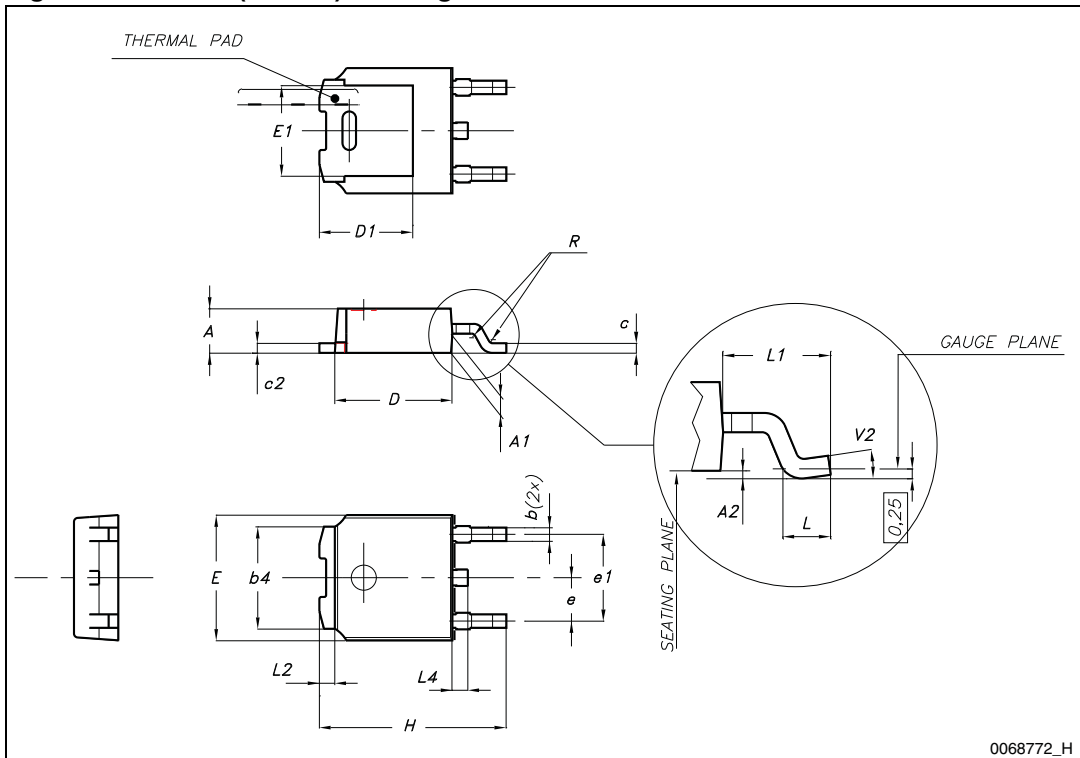
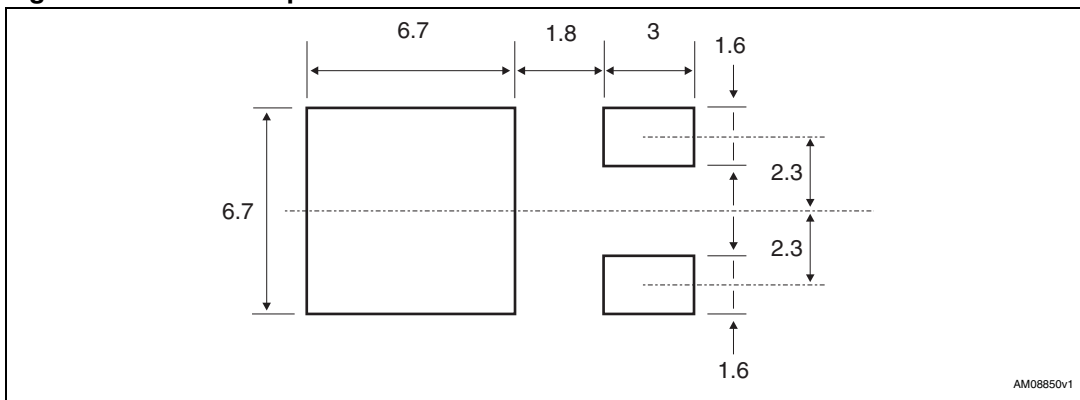


Figure 26. DPAK footprint<sup>(b)</sup>



b. All dimensions are in millimeters

## 5 Packaging mechanical data

Table 11. D<sup>2</sup>PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Table 12. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 27. Tape for DPAK (TO-252) and D<sup>2</sup>PAK (TO-263)

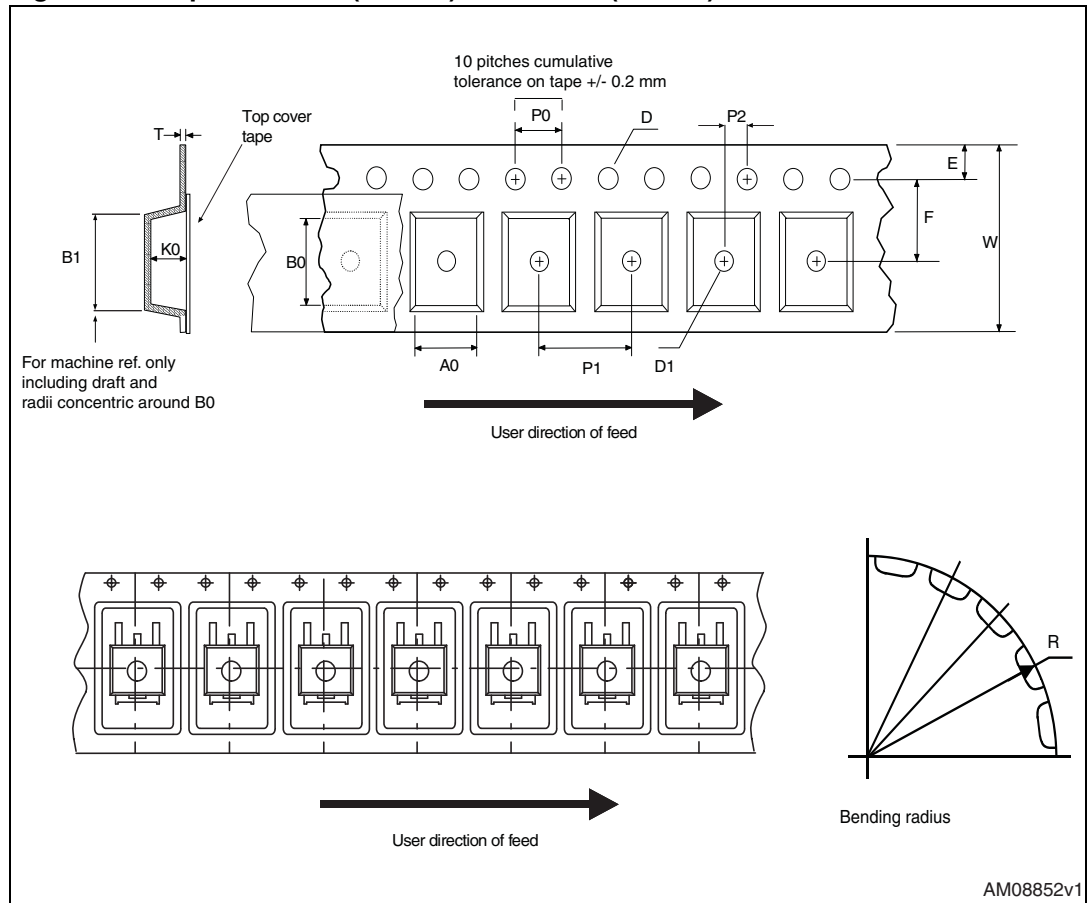
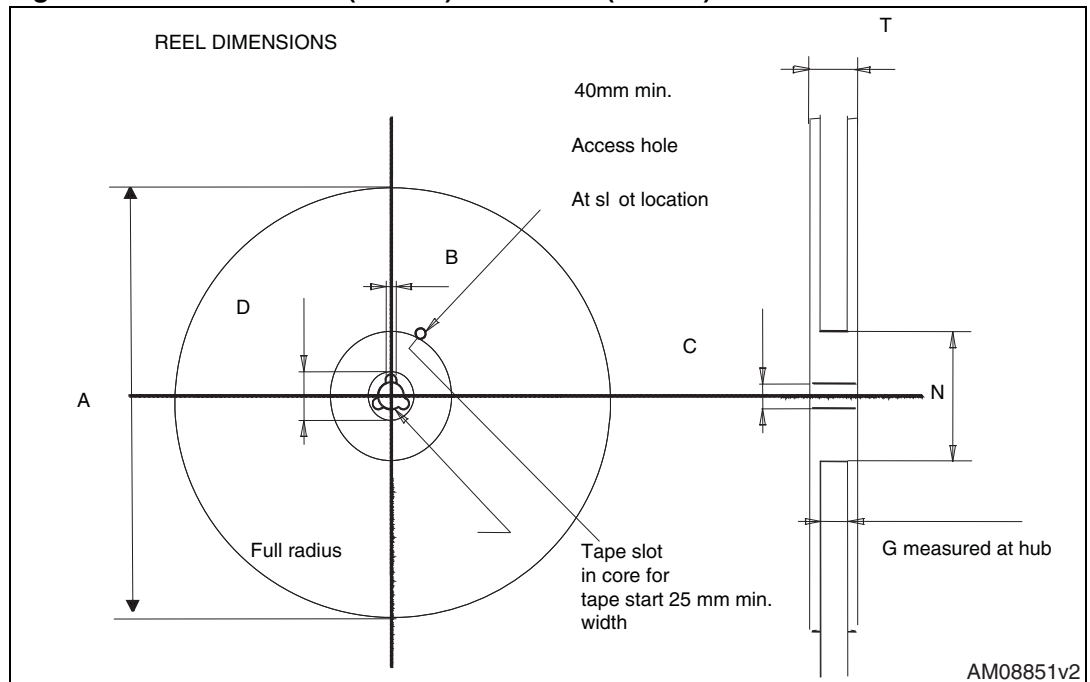


Figure 28. Reel for DPAK (TO-252) and D<sup>2</sup>PAK (TO-263)



## 6 Revision history

Table 13. Document revision history

Date	Revision	Changes
21-Dec-2011	1	First release.

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