



SN65LVDS049

SLLS575-AUGUST 2003

DUAL LVDS DIFFERENTIAL DRIVERS AND RECEIVERS

FEATURES

- DS90LV049 Compatible
- Up to 400 Mbps Signaling Rates
- Flow-Through Pin-out
- 50 ps Driver Channel-to-Channel Skew (Typ)
- 50 ps Receiver Channel-to-Channel Skew (Typ)
- 3.3-V Power Supply
- High-Impedance Disable for all Outputs
- Internal Failsafe Biasing of Receiver Inputs
- 1.4 ns Driver Propagation Delay (Typ)
- 1.9 ns Receiver Propagation Delay (Typ)
- High Impedance Bus Pins on Power Down
- ANSI TIA/EIA-644-A Compliant
- Receiver Input and Driver Output ESD Exceeds 10 kV
- 16-pin TSSOP Package

APPLICATIONS

- Full-duplex LVDS Communications of Clock and Data
- Printers

DESCRIPTION

The SN65LVDS049 is a dual flow-through differential line driver-receiver pair that uses low-voltage differential signaling (LVDS) to achieve signaling rates as high as 400 Mbps. The TIA/EIA-644-A standard compliant electrical interface provides a minimum differential output voltage magnitude of 250 mV into a 100- Ω load and receipt of signals with up to 1 V of ground potential difference between a transmitter and receiver. The LVDS receivers have internal failsafe biasing that places the outputs into a known high state for unconnected differential inputs.

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100- Ω characteristic impedance. The transmission media may be printed-circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics)

The SN65LVDS049 is characterized for operation from -40°C to 85°C



PW PACKAGE (Marked as LVDS049) (TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DRIVER TRUTH TABLE

INPUT	ENA	BLES	OUTPUTS (1)		
DIN	EN	EN	D _{OUT+}	D _{OUT-}	
L	Н	L or OPEN	L	Н	
Н			Н	L	
Х	All other	conditions	Z	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

RECEIVER TRUTH TABLE

DIFFERENTIAL INPUT	ENAI	BLES	OUTPUT (1)
R _{IN-} - R _{IN+}	EN	EN	R _{OUT}
$V_{ID} \ge 100 \text{ mV}$	Н	L or OPEN	Н
$V_{ID} \le -100 \text{ mV}$			L
Open/short or terminated			Н
X	All other of	conditions	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

ENABLE FUNCTION TABLE

ENA	BLES	OUTPUTS			
EN	EN	LVDS Out	LVCMOS Out		
L or Open	L or Open	DISABLED	DISABLED		
Н	L or Open	ENABLED	ENABLED		
L or Open	Н	DISABLED	DISABLED		
Н	Н	DISABLED	DISABLED		

POWER DISSIPATION RATING

PACKAGE	CIRCUIT BOARD	T _A ≤25°C	DERATING FACTOR (1)	T _A = 85°C
	MODEL	POWER RATING	ABOVE T _A = 25°C	POWER RATING
PW	Low-K (2)	774 mW	6.2 mW/°C	402 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

(2) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3.



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

			UNIT		
Supply voltage ra	ange (2), V _{CC}		-0.3 V to 4 V		
	D_{IN} , R_{OUT} , EN, or \overline{EN}		-0.3 V to (V _{CC} + 0.3 V)		
Voltage range	R _{IN+} or R _{IN-}	-0.3 V to 4 V			
	D _{OUT+} or D _{OUT-}		-0.3 V to 3.9 V		
	Lluman Dady Madal (3)	R_{IN+} , R_{IN-} , D_{OUT+} , and D_{OUT-}	±10 kV		
ESD		All pins	±2K V		
	Charged-Device Model (4)	Charged-Device Model (4) All pins			
LVDS output sho	ort circuit duration (DOUT+, DOUT-	-)	Continuous		
Continuous powe	er dissipation		See Dissipation Rating Table		
Storage tempera	ture range		-65°C to 150°C		
Lead temperature	e 1,6 mm (1/16 inch) from case for	10 seconds	260°C		

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.

(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}	3	3.3	3.6	V
Receiver input voltage	GND			V
Common-mode input voltage, V _{IC}	$\frac{ V_{ID} }{2}$		$2.4 - \frac{ V_{ D} }{2}$	V
			V _{CC} - 0.8	V
Operating free-air temperature, T _A	-40		85	°C

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DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
	DC SPECIFICATIONS (D _{IN} , EN, EN)					
VIH	Input high voltage		2.0		V _{CC}	V
V _{IL}	Input low voltage		GND		0.8	V
I _{IH}	Input high current	V _{IN} = V _{CC}	-10	3	10	μA
I _{IL}	Input low current	V _{IN} = GND	-10	1	10	μA
V _{CL}	Input clamp voltage	I _{CL} = -18 mA	-1.5	-0.8		V
LVDS O	utput DC Specifications (D _{OUT+} , D _{OUT-})					
V _{OD}	Differential output voltage		250	350	450	V
$\Delta V_{OD} $	Change in magnitude of V _{OD} for complimentary output states		-35	1	35	mV
V _{OS}	Offset voltage	$-R_L = 100 \Omega$, See Figure 1	1.125	1.2	1.375	V
ΔV_{OS}	Change in magnitude of V _{OS} for complimentary output states	_	-25	1	25	mV
I _{OS}	Output short circuit current	Enabled $D_{IN} = V_{CC}$ and $D_{OUT+} = 0 V$, or $D_{IN} = GND$ and $D_{OUT-} = 0 V$		-4.5	-9	mA
I _{OSD}	Differential output short circuit current (2)	Enabled, V _{OD} = 0 V		-3.6	-9	mA
I _{OFF}	Power-off leakage	V _{CC} = 0 V or Open; VO = 0 or 3.6 V	-20	0	20	μA
I _{OZ}	Output high-impedance current	EN = 0 V and \overline{EN} = V _{CC} , V _O = 0 or V _{CC}	-10	0	10	μA
LVDS In	put DC Specifications (R _{IN+} , R _{IN-})					
V _{IT+}	Differential input high threshold				100	mV
V _{IT-}	Differential input low threshold	V _{CM} - 1.2 V, 0.05 V, 2.35 V	-100			mV
V _{CMR}	Common-mode voltage range	$V_{ID} = \pm 100 \text{ mV}$	0.05		2.35	V
	Input current	V_{CC} = 3.6 V, V_{IN} = 0 V or 2.8 V	-20		20	μA
'IN	input current	V_{CC} = 0 V, V_{IN} = 0 V, 2.8 V, or 3.6 V	-20		20	μA
Outputs	DC Specifications (R _{OUT})					
V _{OH}	Output high voltage	I _{OH} = -0.4 mA, V _{ID} = 200 mV	2.7	3.3		V
V _{OL}	Output Low voltage	I _{OL} = 2 mA, V _{ID} = -200 mV		0.05	0.25	V
I _{OZ}	Output high-impedance current	Disabled, V_{OUT} = 0 V or V_{CC}	-10	0	10	μA
Device I	DC Specifications		1			
I _{CC}	Power supply current (LVDS loaded, enabled)	EN = 3.3 V, D_{IN} = V _{CC} or Gnd, 100 - Ω differential LVDS loads		17	35	mA
I _{ccz}	High impedance supply current (disabled)	No loads, EN = 0 V		1	25	mA

All typical values are at 25°C and with a 3.3 V supply.
Output short circuit current (IOS) is specified as magnitude only, the minus sign indicates direction only

TEXAS INSTRUMENTS

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SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAME	TER	TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
LVDS Ou	itputs (D _{OUT+} , D _{OUT-})		H		1	
t _{PLHD}	Differential propagation delay low to high	R _L = 100 Ω,		1.3	2.0	ns
t _{PHLD}	Differential propagation delay high to low	C_{L} = 15 pF distributed,		1.4	2.0	ns
t _{sk(p)}	Differential pulse skew (t _{PHL} - t _{PLH})		0	0.15	0.4	ns
t _{sk(o)}	Differential channel-to-channel skew (2)		0	0.05	0.5	ns
t _{sk(pp)}	Differential part-to-part skew (3)		0		1	ns
t _r	Differential rise time		0.2	0.5	1	ns
t _f	Differential fall time		0.2	0.5	1	ns
t _{PHZ}	Disable time, high level to high impedance	R _L = 100 Ω,		2.7	4	ns
t _{PLZ}	Disable time, low level to high impedance	C_L = 15 pF distributed, See Figure 3		2.7	4	ns
t _{PZH}	Enable time, high impedance to high level		1	5	8	ns
t _{PZL}	Enable time, high impedance to low level		1	5	8	ns
f _{MAX}	Maximum operating frequency (4)			250		MHz
LVCMOS	Outputs (R _{OUT})					
t _{PLH}	Propagation delay low to high	V _{ID} = 200 mV,	0.5	1.9	3.5	ns
t _{PHL}	Propagation delay high to low	C_{L} = 15 pF distributed, See Figure 4	0.5	1.7	3.5	ns
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})		0	0.2	0.4	ns
t _{sk(o)}	Channel-to-channel skew (5)		0	0.05	0.5	ns
t _{sk(pp)}	Part-to-part skew (6)		0		1	ns
t _r	Rise time		0.3	0.5	1.4	ns
t _f	Fall time		0.3	0.5	1.4	ns
t _{PHZ}	Disable time, high level to high impedance	$C_L = 15 \text{ pF}$ distributed,	3	7.2	9	ns
t _{PLZ}	Disable time, low level to high impedance	See Figure 5	2.5	4	8	ns
t _{PZH}	Enable time, high impedance to high level		2.5	4.2	7	ns
t _{PZL}	Enable time, high impedance to low level		2	3.3	7	ns
f _{MAX}	Maximum operating frequency (7)		200	250		MHz

(1) All typical values are at 25°C and with a 3.3 V supply.

(2) t_{sk(o)} is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all drivers of a single device with all of their inputs connected together.

(3) t_{sk(pp)} is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(4) $f_{(MAX)}$ generator input conditions: $t_r = t_f < 1$ ns (0% to 100%), 50% duty cycle, 0 V to 3 V. Output Criteria: duty cycle = 45% to 55%, $V_{OD} > 250$ mV, all channels switching.

(5) t_{sk(lim)} is the maximum delay time difference between drivers over temperature, V_{CC}, and process.

(6) tsk(pp) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate wf(MAX) generaith the same supply voltages, at the same temperature, and have identical packages and test circuits

(7) $f_{(MAX)}$ generator input conditions: $t_r = t_f < 1$ ns (0% to 100%), 50% duty cycle, $V_{ID} = 200$ mV, $V_{CM} = 1.2$ V. Output criteria: duty cycle = 45% to 55%, $V_{OH} > 2.7$ V, $V_{OL} < 0.25$ V, all channels switching.

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EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS





PARAMETER MEASUREMENT INFORMATION



Figure 1. Driver V_{OD} and V_{OS} Test Circuit



Figure 2. Driver Propagation Delay and Rise/Fall Time Test Circuit and Waveforms



Figure 3. Driver High-Impedance State Delay Test Circuit and Waveforms



Figure 4. Receiver Propagation Delay and Rise/Fall Test Circuit and Waveforms



Figure 5. Receiver High-Impedance State Delay Test Circuit and Waveforms (Note, V_{CC} = 3.3 V)



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TYPICAL CHARACTERISTICS



PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
	(1)		Drawing			(2)		(3)		(4)	
SN65LVDS049PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS049	Samples
SN65LVDS049PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS049	Samples
SN65LVDS049PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS049	Samples
SN65LVDS049PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS049	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Only one of markings shown within the brackets will appear on the physical device.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



All dimensions are nominal												
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS049PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

26-Jan-2013



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS049PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994. β . This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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